

DISPLACEMENT DAMAGE TEST REPORT AD585S

January 2023

Radiation Test Report	
Product:	AD585S
Die:	C585
Fluence:	1e12 n/cm ²
Test Method:	MIL-STD-883 TM1017
Facilities:	UMass Lowell
Tested:	January 5, 2023

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It is the responsibility of the Procuring Activity to screen products from Analog Devices, Inc. for compliance to Nuclear Hardness Critical Items (HCI) specifications.

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The Rout test was inoperable during the testing of these samples, thus was left out of this report.

Wafer#	SN	ISS+ (A)		ISS- (A)	
		Pre	1.E+12	Pre	1.E+12
CTRL	23	8.64E-03	8.60E-03	-8.62E-03	-8.58E-03
	4	8.72E-03	8.65E-03	-8.69E-03	-8.63E-03
	5	8.74E-03	8.72E-03	-8.71E-03	-8.70E-03
	7	8.64E-03	8.71E-03	-8.61E-03	-8.69E-03
	8	8.75E-03	8.75E-03	-8.73E-03	-8.72E-03
	9	8.71E-03	8.64E-03	-8.69E-03	-8.62E-03
	10	8.69E-03	8.76E-03	-8.66E-03	-8.73E-03
	11	8.72E-03	8.73E-03	-8.69E-03	-8.70E-03
	17	8.53E-03	8.71E-03	-8.51E-03	-8.68E-03
	19	8.50E-03	8.73E-03	-8.47E-03	-8.70E-03
	21	8.56E-03	8.55E-03	-8.53E-03	-8.52E-03
	22	8.60E-03	8.50E-03	-8.57E-03	-8.70E-03
min		8.50E-03	8.50E-03	-8.73E-03	-8.73E-03
max		8.75E-03	8.76E-03	-8.47E-03	-8.52E-03
mean		8.65E-03	8.68E-03	-8.63E-03	-8.67E-03
std. dev		9.00E-05	8.40E-05	8.98E-05	6.14E-05
- 3 Sigma		8.38E-03	8.43E-03	-8.89E-03	-8.86E-03
+3 Sigma		8.92E-03	8.93E-03	-8.36E-03	-8.49E-03

Wafer #	SN	VOS_RL=No_Load (V)		Ibias_VIN=0_Gain=1 (A)	
		Pre	1.E+12	Pre	1.E+12
CTRL	23	1.19E-03	2.08E-03	-4.53E-11	-5.08E-11
	4	1.49E-03	1.15E-03	-2.31E-11	-6.15E-11
	5	2.13E-03	1.45E-03	-4.38E-11	-5.83E-11
	7	6.25E-04	2.07E-03	-2.91E-11	-1.10E-10
	8	-1.45E-04	1.66E-03	-3.07E-11	-1.21E-10
	9	1.23E-03	3.33E-05	-2.95E-11	-1.08E-10
	10	-4.13E-04	2.05E-04	-3.18E-11	-1.07E-10
	11	3.00E-03	1.48E-03	-3.71E-11	-1.12E-10
	17	1.81E-03	-3.31E-04	-3.51E-11	-1.10E-10
	19	9.46E-04	3.34E-03	-3.67E-11	-1.11E-10
	21	-1.19E-03	1.57E-03	-2.84E-11	-1.12E-10
	22	2.11E-03	9.59E-04	-3.15E-11	-1.13E-10
min		-1.19E-03	-3.31E-04	-4.38E-11	-1.21E-10
max		3.00E-03	3.34E-03	-2.31E-11	-5.83E-11
mean		1.06E-03	1.23E-03	-3.24E-11	-1.02E-10
std. dev		1.25E-03	1.03E-03	5.51E-12	2.13E-11
- 3 Sigma		-2.70E-03	-1.85E-03	-4.90E-11	-1.66E-10
+3 Sigma		4.81E-03	4.32E-03	-1.59E-11	-3.85E-11

Wafer #	SN	VLREF @ 50UA LOAD		Resistor Mismatch (%)	
		Pre	1.E+12	Pre	1.E+12
CTRL	23	1.297	1.310	0.040	0.130
	4	1.303	1.306	-0.060	0.040
	5	1.307	1.310	0.004	0.076
	7	1.299	1.305	-0.028	-0.061
	8	1.299	1.308	-0.018	0.006
	9	1.300	1.306	-0.071	-0.028
	10	1.301	1.305	-0.037	-0.020
	11	1.304	1.307	-0.067	-0.072
	17	1.301	1.308	0.094	-0.037
	19	1.303	1.311	0.025	-0.066
	21	1.296	1.309	-0.011	0.093
	22	1.302	1.309	0.129	0.026
min		1.296	1.305	-0.071	-0.072
max		1.307	1.311	0.129	0.093
mean		1.301	1.308	-0.004	-0.004
std. dev		0.003	0.002	0.065	0.057
- 3 Sigma		1.293	1.302	-0.197	-0.175
+3 Sigma		1.310	1.314	0.190	0.167

Wafer #	SN	IIL HOLDB (A)		IIL HOLD (A)	
		Pre	1.E+12	Pre	1.E+12
CTRL	23	6.01E-06	5.73E-06	5.36E-06	5.68E-06
	4	6.81E-06	5.62E-06	5.94E-06	5.64E-06
	5	7.33E-06	5.84E-06	6.56E-06	6.01E-06
	7	6.81E-06	1.14E-05	6.02E-06	1.09E-05
	8	6.78E-06	1.24E-05	5.98E-06	1.15E-05
	9	6.78E-06	1.12E-05	6.02E-06	1.09E-05
	10	6.74E-06	1.11E-05	6.05E-06	1.07E-05
	11	7.73E-06	1.17E-05	7.08E-06	1.10E-05
	17	6.15E-06	1.18E-05	5.50E-06	1.12E-05
	19	6.23E-06	1.34E-05	5.65E-06	1.28E-05
	21	5.90E-06	1.11E-05	5.25E-06	1.07E-05
	22	6.12E-06	1.14E-05	5.50E-06	1.11E-05
min		5.90E-06	5.62E-06	5.25E-06	5.64E-06
max		7.73E-06	1.34E-05	7.08E-06	1.28E-05
mean		6.67E-06	1.06E-05	5.96E-06	1.02E-05
std. dev		5.48E-07	2.52E-06	5.14E-07	2.26E-06
- 3 Sigma		5.03E-06	3.09E-06	4.42E-06	3.46E-06
+3 Sigma		8.32E-06	1.82E-05	7.50E-06	1.70E-05

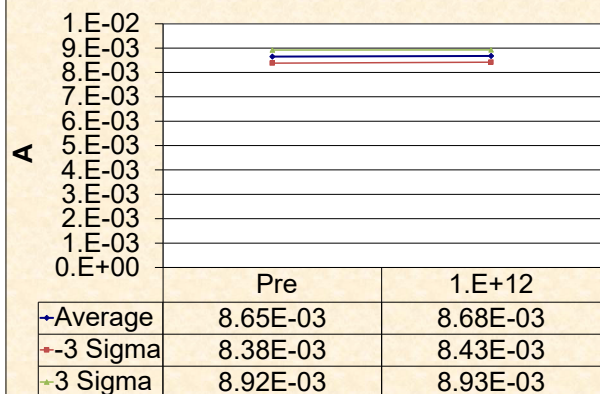
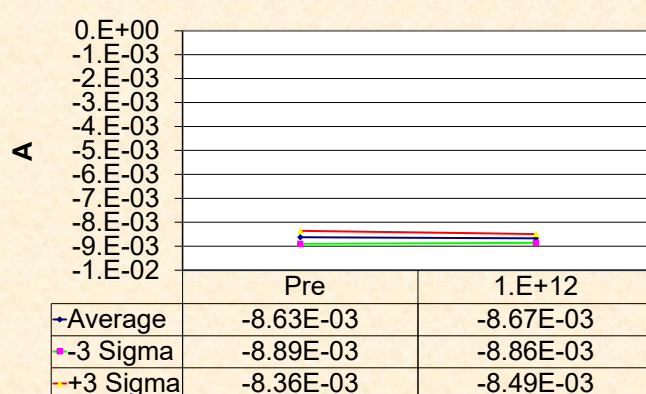
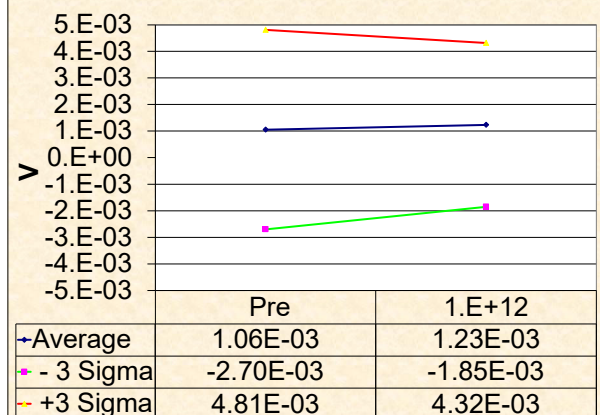
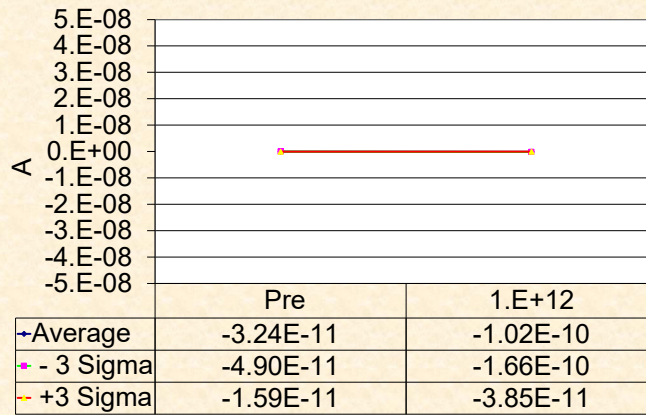
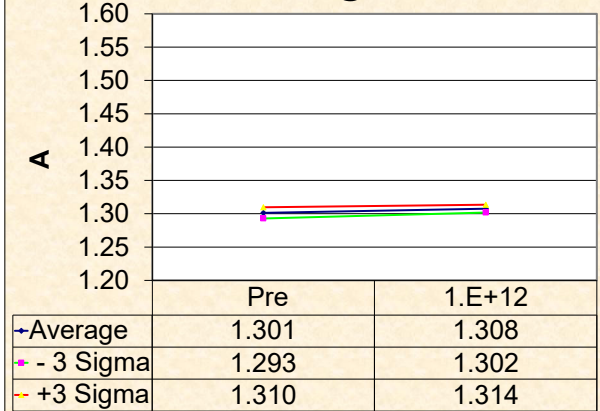
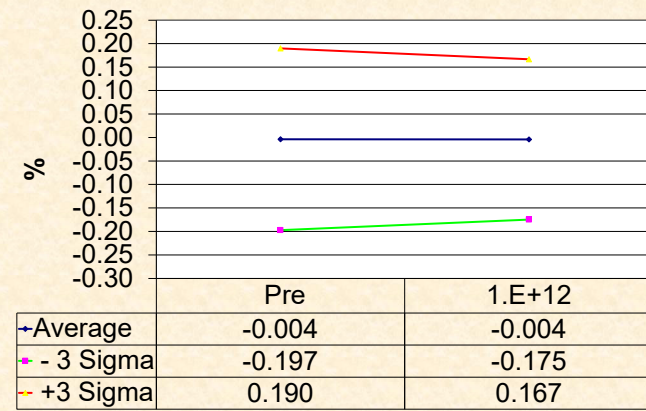
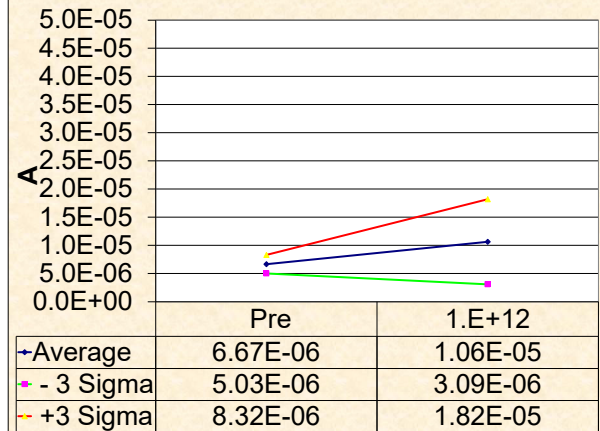
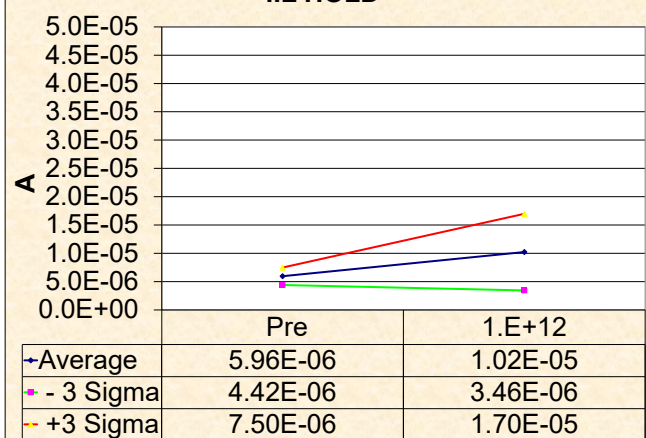
Wafer #	SN	VIH_VHOLDB=2V_VIN=0 V (V)		VIH_VHOLDB=2V_VIN=10 V (V)	
		Pre	1.E+12	Pre	1.E+12
CTRL	23	1.13E-03	2.08E-03	9.998	9.999
	4	1.42E-03	1.10E-03	9.998	9.998
	5	2.06E-03	1.34E-03	9.999	9.998
	7	5.45E-04	2.05E-03	9.997	9.998
	8	-2.08E-04	1.68E-03	9.997	9.999
	9	1.20E-03	-4.15E-05	9.998	9.997
	10	-3.85E-04	2.35E-04	9.996	9.997
	11	2.85E-03	1.54E-03	10.000	9.998
	17	1.84E-03	-2.91E-04	9.998	9.996
	19	9.75E-04	3.18E-03	9.998	10.000
	21	-1.33E-03	1.60E-03	9.995	9.998
	22	2.09E-03	9.82E-04	9.999	9.997
min		-1.33E-03	-2.91E-04	9.995	9.996
max		2.85E-03	3.18E-03	10.000	10.000
mean		1.01E-03	1.22E-03	9.998	9.998
std. dev		1.25E-03	9.95E-04	0.001	0.001
- 3 Sigma		-2.75E-03	-1.77E-03	9.994	9.995
+3 Sigma		4.76E-03	4.20E-03	10.002	10.001

Wafer #	SN	VIH_VHOLDB=0.8V_VIN=0V (V)		VIH_VHOLD=0.8V_VIN=0V (V)	
		Pre	1.E+12	Pre	1.E+12
CTRL	23	10.062	10.066	1.13E-03	2.07E-03
	4	10.068	10.058	1.41E-03	1.09E-03
	5	10.064	10.063	2.04E-03	1.33E-03
	7	10.063	10.401	5.21E-04	2.05E-03
	8	10.059	10.420	-2.14E-04	1.67E-03
	9	10.059	10.383	1.19E-03	-4.68E-05
	10	10.063	10.388	-3.92E-04	2.24E-04
	11	10.067	10.407	2.81E-03	1.53E-03
	17	10.065	10.396	1.83E-03	-2.85E-04
	19	10.064	10.422	9.74E-04	3.15E-03
	21	10.055	10.401	-1.36E-03	1.59E-03
	22	10.068	10.398	2.08E-03	9.45E-04
min		10.055	10.058	-1.36E-03	-2.85E-04
max		10.068	10.422	2.81E-03	3.15E-03
mean		10.063	10.340	9.90E-04	1.20E-03
std. dev		0.004	0.139	1.25E-03	9.90E-04
- 3 Sigma		10.051	9.924	-2.76E-03	-1.77E-03
+3 Sigma		10.075	10.756	4.74E-03	4.18E-03

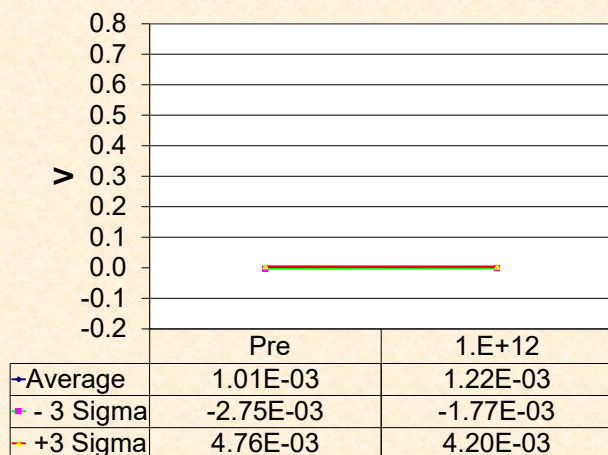
Wafer #	SN	VIH_VHOLD=0.8V_VIN=1 0V (V)		VIH_VHOLD=2V_VIN=0V (V)	
		Pre	1.E+12	Pre	1.E+12
CTRL	23	9.998	9.999	10.064	10.074
	4	9.998	9.998	10.066	10.064
	5	9.999	9.998	10.075	10.074
	7	9.997	9.998	10.066	10.440
	8	9.997	9.999	10.065	10.466
	9	9.998	9.997	10.066	10.435
	10	9.996	9.997	10.071	10.413
	11	10.000	9.998	10.072	10.444
	17	9.998	9.996	10.072	10.447
	19	9.998	10.000	10.074	10.459
	21	9.995	9.998	10.058	10.449
	22	9.999	9.997	10.076	10.437
min		9.995	9.996	10.058	10.064
max		10.000	10.000	10.076	10.466
mean		9.998	9.998	10.069	10.375
std. dev		0.001	0.001	0.005	0.152
- 3 Sigma		9.994	9.995	10.053	9.919
+3 Sigma		10.002	10.001	10.085	10.831

Wafer #	SN	IOUT_VIN=10V_RL=100 Ohms (A)		PSRR_+VS=+5V to +18V_- VS=-10.8V (dB)	
		Pre	1.E+12	Pre	1.E+12
CTRL	23	2.89E-02	2.96E-02	87.10	78.66
	4	2.95E-02	2.89E-02	80.62	86.55
	5	3.00E-02	3.01E-02	81.94	82.63
	7	2.99E-02	2.96E-02	79.62	79.20
	8	2.98E-02	3.01E-02	84.11	82.26
	9	2.99E-02	3.00E-02	84.60	79.76
	10	3.01E-02	2.98E-02	84.00	82.54
	11	2.93E-02	3.00E-02	84.83	84.10
	17	2.92E-02	3.02E-02	88.08	82.89
	19	2.92E-02	2.94E-02	84.66	82.67
	21	2.93E-02	2.93E-02	83.47	89.01
	22	2.97E-02	2.93E-02	78.65	84.08
min		2.92E-02	2.89E-02	78.65	79.20
max		3.01E-02	3.02E-02	88.08	89.01
mean		2.96E-02	2.97E-02	83.14	83.24
std. dev		3.34E-04	4.30E-04	2.72	2.76
- 3 Sigma		2.86E-02	2.84E-02	74.99	74.96
+3 Sigma		3.06E-02	3.10E-02	91.29	91.53

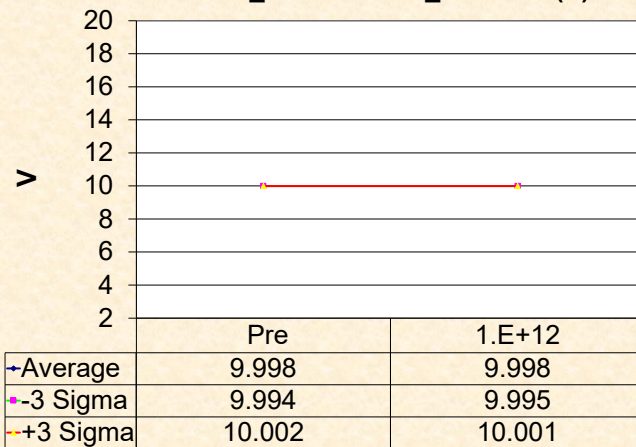
Wafer #	SN	PSRR_+VS=+15V_-VS=-12V to -18V (dB)		CMRR_Vsy15_Vcm+-10 (dB)	
		Pre	1.E+12	Pre	1.E+12
CTRL	23	91.18	84.73	89.82	87.30
	4	95.29	90.42	106.01	89.33
	5	83.00	86.15	85.77	93.76
	7	82.99	100.75	88.76	95.55
	8	85.00	82.91	91.42	85.22
	9	96.05	83.90	106.70	90.36
	10	90.12	86.37	106.26	98.54
	11	84.44	98.05	87.72	99.27
	17	85.66	91.60	89.01	101.67
	19	90.54	85.45	93.62	90.03
	21	84.57	87.30	91.59	90.46
	22	84.77	90.81	87.30	98.58
min		82.99	82.91	85.77	85.22
max		96.05	100.75	106.70	101.67
mean		87.50	89.43	94.02	93.89
std. dev		4.75	5.69	8.20	5.21
- 3 Sigma		73.25	72.36	69.41	78.27
+3 Sigma		101.74	106.50	118.62	109.51

+Iss**-Iss****VOS_RL=No_Load****Ibias_VIN=0_Gain=1****VLREF @ 50UA LOAD****Resistor Mismatch****IIL HOLDB****IIL HOLD**

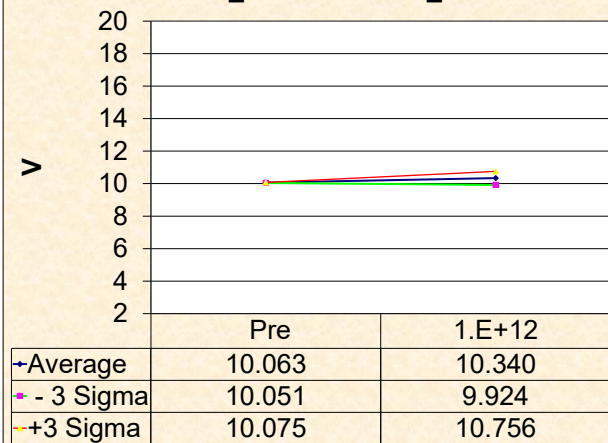
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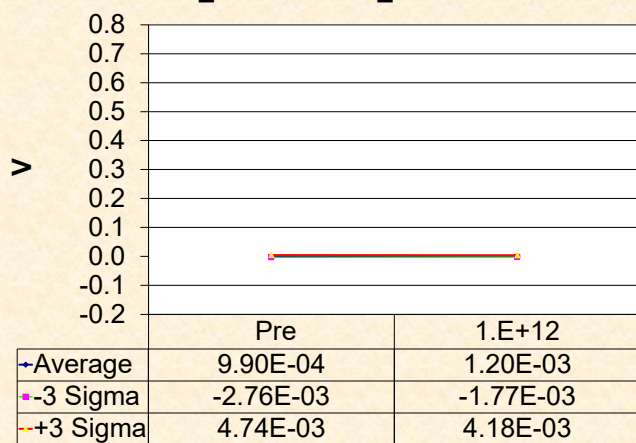
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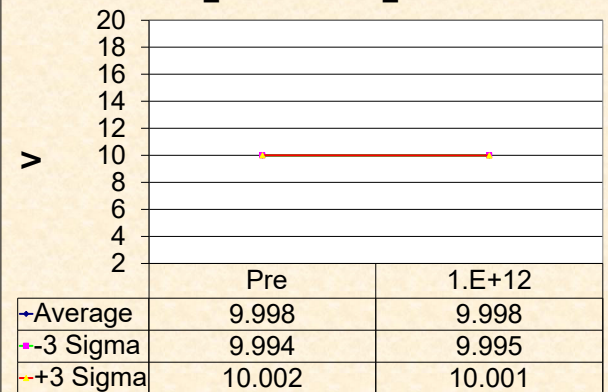
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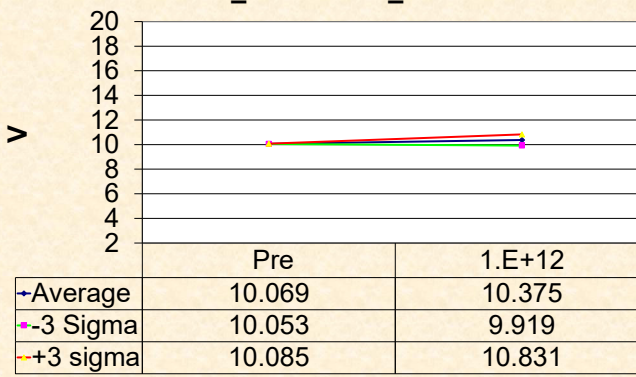
VIH_VHOLD=0.8V_VIN=0V



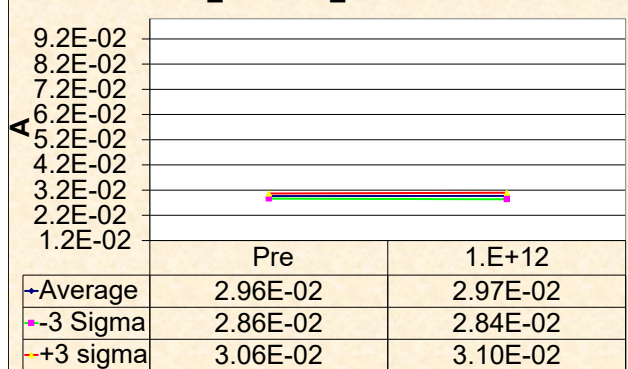
VIH_VHOLD=0.8V_VIN=10V



VIH_VHOLD=2V_VIN=0V



IOUT_VIN=10V_RL=100 Ohms



PSRR_+VS=+5V to +18V_-VS=-10.8V

