9510_quick_start.clk

Design Example Description

In this design the AD9510, 1.2GHz, 8-Channel Clock Distribution IC is used to provide clocks to analog-to-digital converters (ADCs), digital-to-analog converters (DACs) and digital application specific integrated circuits (ASICs).

The DACs and the ASIC1 connected to the DACs require fast clocks at 491.52MHz.
DAC1 and DAC2 need fast slewing, differential LVPECL clocks with broadband jitter < 400 femtoseconds rms.
ASIC1 also needs a 491.52MHz clock, but requires an LVDS level signal.

ADC1 and ADC2 send their output data to ASIC2. All three of these chips require clocks at 122.88MHz.
The ADCs require fast-slewing, differential LVPECL clocks with broadband jitter < 350 femtoseconds rms
The digital ASIC2 requires a CMOS clock at the same rate. However, the ASIC2 clock must be delayed in time relative to the ADC clocks to insure setup and hold times are met.

Finally, there is a need for a low jitter (<1 ps rms) CMOS copy of the reference clock.

The available reference in this example is 30.72 MHz. By using the phase locked loop synthesizer core on the AD9510 and an external VCO or VCXO, a 491.52MHz signal may be generated and locked to the reference. Each of the eight clock distribution channels of the AD9510 has an independent programmable divider which may be programmed to any integer 1 to 32. Each divider has a phase offset option which can be used for adding delays in integer multiples of the time period of the signal at CLK2 port. In this case that is a VCO at 491.52 MHz which corresponds to a period of ~2ns. Finally, by taking advantage of the multiple logic families available on the AD9510, the required combination of LVPECL, LVDS and CMOS output levels can be achieved.

Note that ADIsimCLK allows the user to create custom references and VCOs. By starting with custom oscillators specified with high performance, the user can determine the jitter limitation of the AD9510 on-chip PLL core and the clock distribution section. This serves as a good baseline for seeing what performance is possible. The user can then lower the phase noise performance of the reference and VCO to see the impact on output phase noise and jitter.

The notes and diagrams below describe how to configure the AD9510 for this application. For instructions on how to navigate the ADIsimCLK page tabs and windows, please check the tutorial and help files available from the Help pulldown menu.

NOTES

1) OUT0/OUT0B & OUT1/OUT1B differential LVPECL clocks set to DIV=1 or divider "bypass" mode, 780mV logic swing

2) OUT2/OUT2B & OUT3/OUT3B differential LVPECL clocks are set to DIV=4, 780mV logic swing

3) OUT4 LVDS/CMOS clock set to DIV=8, CMOS mode; OUT4B not connected

4) OUT5/OUT5B LVDS/CMOS clock set to DIV=1 or divider "bypass" mode, LVDS mode, 3.5mA current; optional fine delay bypassed

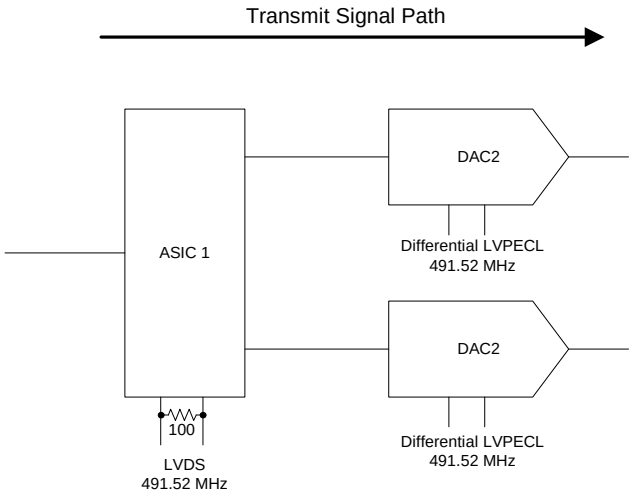
5) OUT6 LVDS/CMOS clock set to DIV=4, phase offset = 1 for ~2ns time delay; CMOS mode, optional fine delay bypassed; OUT6B not connected

6) OUT7 LVDS/CMOS clock set to DIV=16, CMOS mode; OUT7B not connected

7) Reference is custom 30.72 MHz with PN floor at -170dBc/Hz.

8) VCO is custom 491.52 MHz with PN floor at -160dBc/Hz

CIRCUITS REQUIRING CLOCKS



CIRCUIT