9515_quick_start.clk

Design Example Description

In this design the AD9515, 1.6 GHz, 2-Channel Clock Distribution IC is used to provide clocks to an analog-to-digital converter (ADC) and to a digital application specific integrated circuit (ASIC).

The ADC requires a fast-slewing, differential LVPECL 125MHz clock with broadband jitter < 350 femtoseconds rms. The digital ASIC also requires a 125MHz clock, but it must have LVDS levels and have adjustable phase delay. The system clock available for this example is a clean, low jitter 1.5GHz clock signal.

Because the AD9515 offers select integer divide ratios in the range of 1-32 on each clock channel, it is possible to derive the required frequencies by setting each of the dividers to DIV=12. To achieve the required delay on the ASIC clock for setup and hold time, a phase offset = 4 may be used. Note that the AD9515 does not require a serial port for programming. By consulting the product datasheet, the user can set divide ratios, phase, delay and logic settings using the 4-level logic input pins S0-S10.

Outputs OUT0/OUT0B are differential LVPECL. However, OUT1/OUT1B may be programmed to either LVDS or CMOS levels. This example calls for an LVDS clock. Although not used in this example, when OUT1 is set to CMOS levels, there is a complementary CMOS output available on pin OUT1B. This is available should a user need an additional CMOS clock 180 degrees out of phase with the clock on pin OUT1.

Note that ADIsimCLK allows the user to create custom input clocks. By starting with custom oscillators specified with high performance, the user can determine the jitter limitation of the AD9515 clock distribution section. This serves as a good baseline for seeing what performance is possible. The user can then change the phase noise performance of the input clock to see the impact on output clock phase noise and jitter.

The notes and diagrams below describe how to configure the AD9515 for this application. For instructions on how to navigate the ADIsimCLK page tabs and windows, please check the tutorial and help files available from the Help pulldown menu. For details on divide/phase/delay combinations available on the AD9515, please consult the product datasheet.

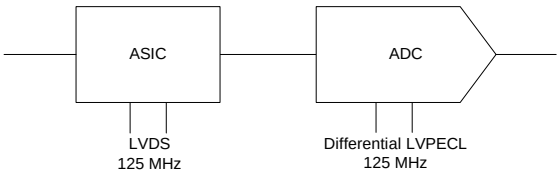
NOTES

1) OUT0/OUTB Differential LVPECL clock set to DIV=12, 780mV swing

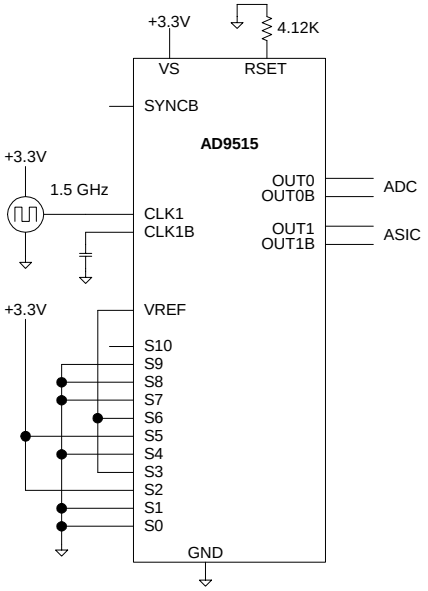
2) OUT1/OUTB LVDS/CMOS clock set to DIV=12, LVDS mode, phase offset = 4 for ~2.7ns delay; optional fine delay bypassed

3) Input Clock is custom 1.5 GHz with PN floor at -160dBc/Hz

CIRCUITS REQUIRING CLOCKS



CIRCUIT


+3.3V
4.12K
VS
RSET
SYNCB
AD9515
+3.3V
1.5 GHz
OUT0
OUT0B
ADC
CLK1
CLK1B
OUT1
OUT1B
ASIC
+3.3V
VREF
S10
S9
S8
S7
S6
S5
S4
S3
S2
S1
S0
GND