LINEAR TECHNOLOGY

DESIGN NOTES

1.25Msps 12-Bit A/D Converter Cuts Power Dissipation and Size

Design Note 104

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Introduction

Until now, high speed system designers had to compromise when selecting 1Msps 12-bit A/D converters. While hybrids typically had the best performance, they were big, power hungry (~1W) and costly (>$100). A few manufacturers offered monolithics, but they compromised either AC or DC performance.

That has now changed. The new LTC®1410 monolithic 1.25Msps 12-bit ADC performs better than hybrids with the power dissipation, size and cost of monolithics.

Some of the LTC1410's key benefits include:

- 1.25Msps throughput rate
- Fully differential inputs
- 60dB CMRR that remains constant to 1MHz
- Low power: 160mW (typ) from ±5V supplies
- "Instant on" NAP and µpower SLEEP shutdown modes
- Small package: 28-pin SO

The LTC1410's features can increase the performance and decrease the cost of current data acquisition systems and optimize new applications.

High Accuracy Conversions: AC or DC

In Figure 1 the LTC1410 combines a wide bandwidth differential sample-and-hold (S/H) with an extremely fast successive approximation register (SAR) ADC and an on-chip reference. Together they deliver a very high level of both AC and DC performance.

An ADC's S/H determines its overall dynamic performance. The LTC1410's S/H has a very wide bandwidth (20MHz) and generates very low total harmonic distortion (–84db) for the 625kHz Nyquist bandwidth.

Important DC specifications include excellent differential linearity error ≤0.8LSB, linearity error ≤0.5LSB and no missing codes over temperature. The on-chip 10ppm/°C curvature corrected 2.5V bandgap reference assures low drift over temperature.

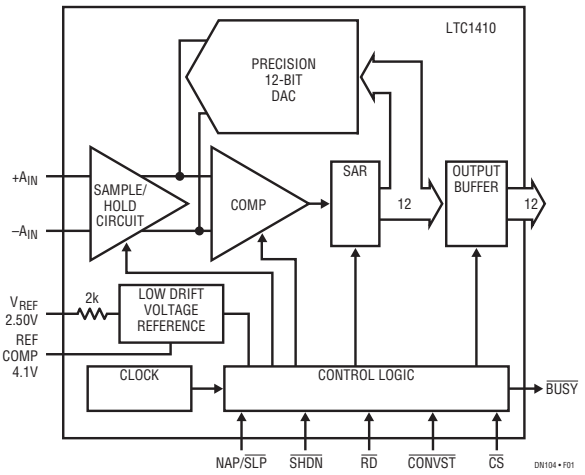

Figure 1. LTC1410 Features a True Differential S/H with Excellent Bandwidth and CMRR

If an application requires an external reference, it can easily overdrive the on-chip reference's 2kΩ output impedance.

Important Multiplexed Applications

The LTC1410's high conversion rate allows very high sample rate multiplexed systems. The S/H's high input impedance eliminates DC errors caused by a MUX's switch resistance. Also, the LTC1410's low input capacitance ensures fast 100ns acquisition times, even with high source impedance.

Ideal for Telecommunications

Telecommunications applications such as HDSL, ADSL and modems require high levels of dynamic performance. A key indicator of a sampling ADC's dynamic performance is its signal-to-noise plus distortion ratio (SINAD). The LTC1410's minimum SINAD is 72dB, or 11.67 Effective Number of Bits (ENOB), up to input frequencies of 100kHz. At the Nyquist frequency (625kHz) the SINAD is still a robust 70dB. Figure 2

shows that the LTC1410 can undersample signals well beyond the Nyquist rate.

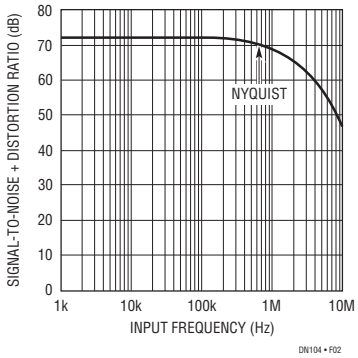

Figure 2. The Wideband S/H Captures Signals Well Beyond Nyquist

Differential Inputs Reject Noise

The LTC1410's differential inputs are ideal for applications whose desired signals must compete with EMI noise. The LTC1410's differential inputs provide a new way to fight noise.

Figure 3a shows a single-ended sampling system whose accuracy is limited by ground noise. When a single-ended signal is applied to the ADC's input, the ground noise adds directly to the applied signal. While a filter can reduce this noise, this does not work for in-band noise or common-mode noise at the same frequency as the input signal. However, Figure 3b shows how the LTC1410 provides relief. Because of its excellent CMRR,

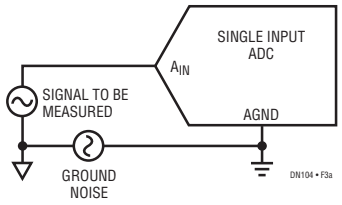

Figure 3a. An Input Signal is Contaminated by Ground Noise with a Single Input ADC

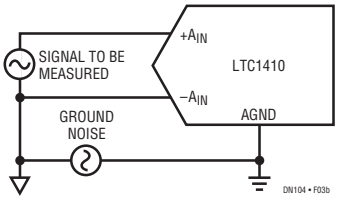

Figure 3b. The LTC1410's Differential Inputs Reject Common-Mode Noise and Preserve the Input Signal

the LTC1410's differential inputs reject the ground noise even if it is at the same frequency as the desired input frequency. Further, the LTC1410's wideband CMRR can eliminate extremely wideband noise, as shown in Figure 4.

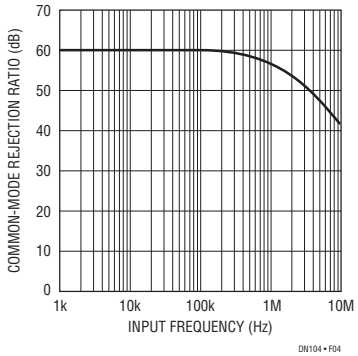

Figure 4. The LTC1410 Rejects Common-Mode Noise Out to 10MHz and Beyond

Low Power Applications

High speed applications with limited power budgets will greatly benefit from the LTC1410's low 160mW power dissipation. Power can be further reduced by using the power shutdown modes, NAP and SLEEP.

NAP reduces power consumption by 95% (to 7.5mW) leaving only the internal reference powered. The "wake-up" time is a very fast 200ns. The most recent conversion data is still accessible and $\overline{CS}$ and $\overline{RD}$ still control the output buffers. NAP is appropriate for those applications that require conversions instantly after periods of inactivity.

SLEEP reduces power consumption to less than 5µW. It is useful for applications that must maximize power savings. SLEEP mode shuts down all bias currents, including the reference. SLEEP mode wake-up time is dependent on the reference compensation capacitor's size. With the recommended 10µF, the wake-up time is 10ms. Typically, NAP mode is used for inactive periods shorter that 10ms and SLEEP is used for longer periods.

Conclusion

Available in 28-pin SO packages, the new LTC1410 is optimized for many high speed dynamic sampling applications including ADSL, compressed video and dynamic data acquisition.

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