Isolated Flyback Converter; Input +30-60V; Output 5V 100mA

Reference Design **PRD1139**

FEATURES

- Input - Output isolation
- Primary side control for low cost and improved efficiency

DESCRIPTION

This is an 30 - 60V input isolated flyback converter based on the ADP1613 boost regulator IC with a "cascode" MOSFET. It uses primary side regulation to avoid the power consumption of a feedback optocoupler.

Transistor Q2 and zener D2 form a linear regulator to provide startup bias current for the two primary side ICs; the ADCMP356 (Comparator + reference) and the ADP1613 (Boost switching regulator). The ADCMP356 implements input UVLO which shuts down the converter when the main input voltage is under ~27V. When the input gets above this threshold, theADCMP356 enables the ADP1613 which provides output from two transformer windings. One of these outputs is the power supply main output via D1. The other output is via D3 which provides IC bias current into C7. During operation, transistor Q4 takes over the bias supply current (away from Q2) so as to run the two ICs from the converter output power. This provides better efficiency than would be obtained by simply powering the ADP1613 directly from the 30V - 60V input.

At the "center" of the converter is the ADP1613 boost regulator. It operates in a cascode connection with Q1 which is a 100V SOT-23 MOSFET. The pcb was originally designed to implement either primary or secondary side regulation. While secondary side regulation provides better control of the output voltage, primary side regulation can deliver better efficiency in this low power application so was favored for that reason. It also allows lower cost. The optocoupler, secondary side reference, and associated components shown on the schematic diagram, which were intended for secondary side regulation, are neither used nor populated.

Primary side voltage regulation is best implemented with its own rectifier and filter, so the converter first filters spikes from the transformer bias winding via R10 and C14, then rectifies it with D5 and C13, and feeds back to the ADP1613 via R16 and R15.

D6, R11, C9, and R12 form an RCD clamp for limiting leakage inductance spikes on the drain of main cascode switch FET Q1.

Table 1. Target Specifications (0 to 55 degrees C)

Rail	Volts Min	Volts Nom	Volts Max	***Current***
+5V	4.9	5	5.1	10 - 100 mA DC
Vinput	30	45	60	----

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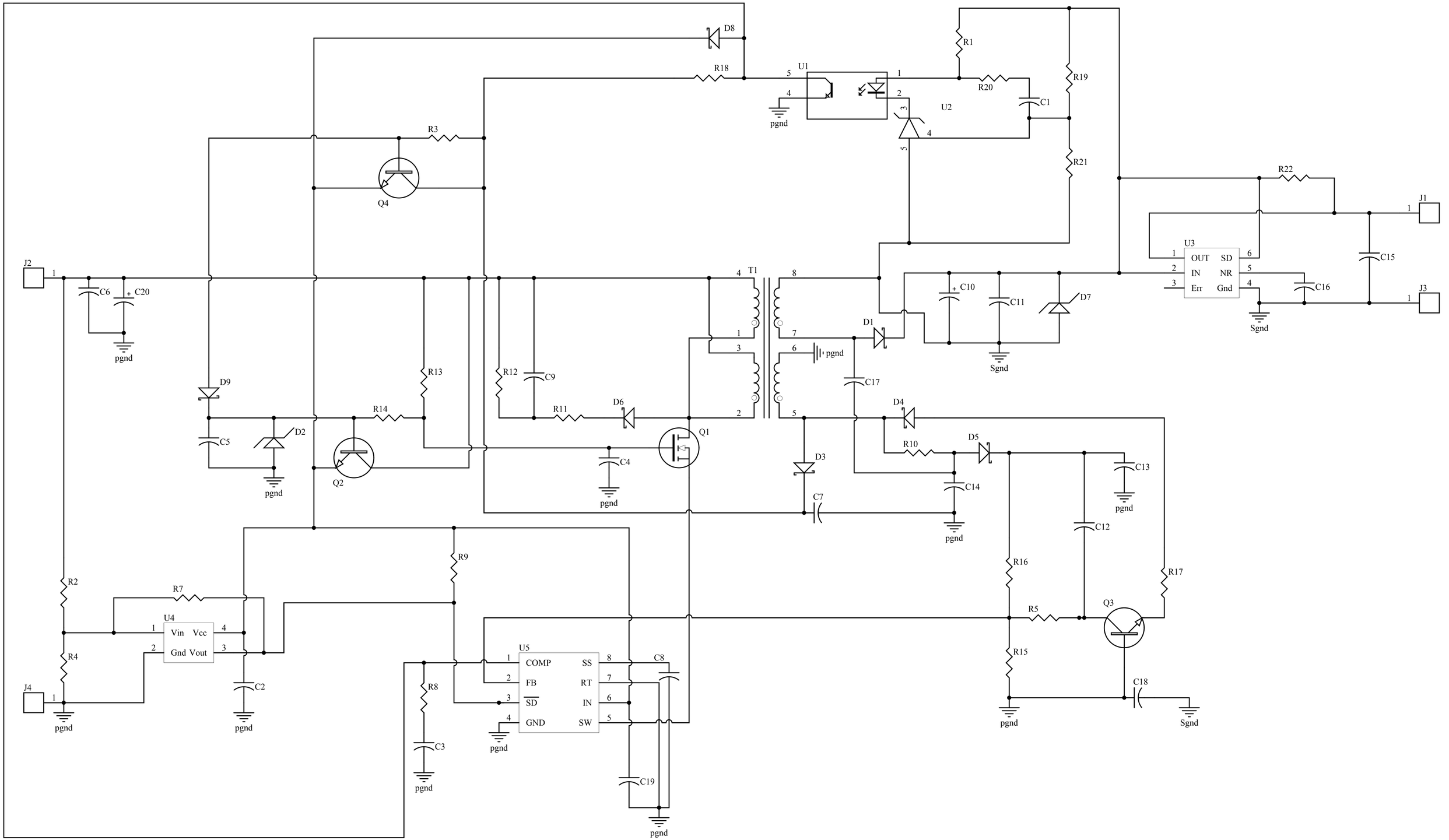
REVISION HISTORY

11/20/2009—Revision A: Tested Prototype



			Analog Devices Inc. Central Power Apps Fort Colins, Colorado USA
Size: B	Number: PRD1139	Revision: 11/6/09	Analog Devices

Table 2. Bill Of Materials

Sequence	*Ref Designation*	*Description*
1	C1	Open
2	C2	1 uF 16V X5R
3	C3	2.2 nF X7R
4	C4	100 nF 25V X7R
5	C5	1 uF 0805 25V X5R
6	C6	100V 1 uF 1210 X7R
7	C7	1 uF 16V X5R
8	C8	100 nF 100V X7R
9	C9	10 nF 50V X7R
10	C10	330 uF 16V low ESR Aluminum Electrolytic
11	C11	4.7 uF 10V 0805 X5R
12	C12	100 nF X7R
13	C13	2.2 uF 16V X5R
14	C14	100 pF NP0
15	C15	1 uF 16V X5R
16	C16	10 nF X7R
17	C17	Open
18	C18	100 nF 100V X7R
19	C19	1 uF 16V X5R
20	D1	MBR0540
21	D2	MMSZ5231B
22	D3	NSR0240
23	D4	NSR0240
24	D5	NSR0240
25	D6	BAV20
26	D7	BTZ52C6V8

Sequence	Ref Designation	Description
27	D8	Open
28	D9	NSR0240
29	Q1	Si2328DS
30	Q2	MMBTA06
31	Q3	Open
32	Q4	MMBT3904
33	R1	Open
34	R2	1.0M
35	R3	2.00K
36	R4	22.1K
37	R5	10K
38	R6	71.5K
39	R7	2.00 M
40	R8	20K
41	R9	Open
42	R10	100
43	R11	33
44	R12	100K 1206
45	R13	210K 1206
46	R14	40.2K
47	R15	15K
48	R16	46.4K
49	R17	Open
50	R18	Open
51	R19	Open
52	R20	Open
53	R21	Open

Sequence	Ref Designation	Description
54	R22	Open
55	U1	Open
56	U2	Open
57	U3	Open
58	U4	ADCMP356
59	**U5**	**ADP1613**

Note: For a first test and demo, the plan is to use a transformer Coilcraft type B0226-EL. This type should work reasonably well however it is not completely optimized for this application, and may not provide the needed isolation voltage. Based upon results with this transformer another one can be specified which will be more accurately tailored to the needs of this converter design. It is anticipated that the dimensions will remain similar.

Figure 2. Efficiency Test Data

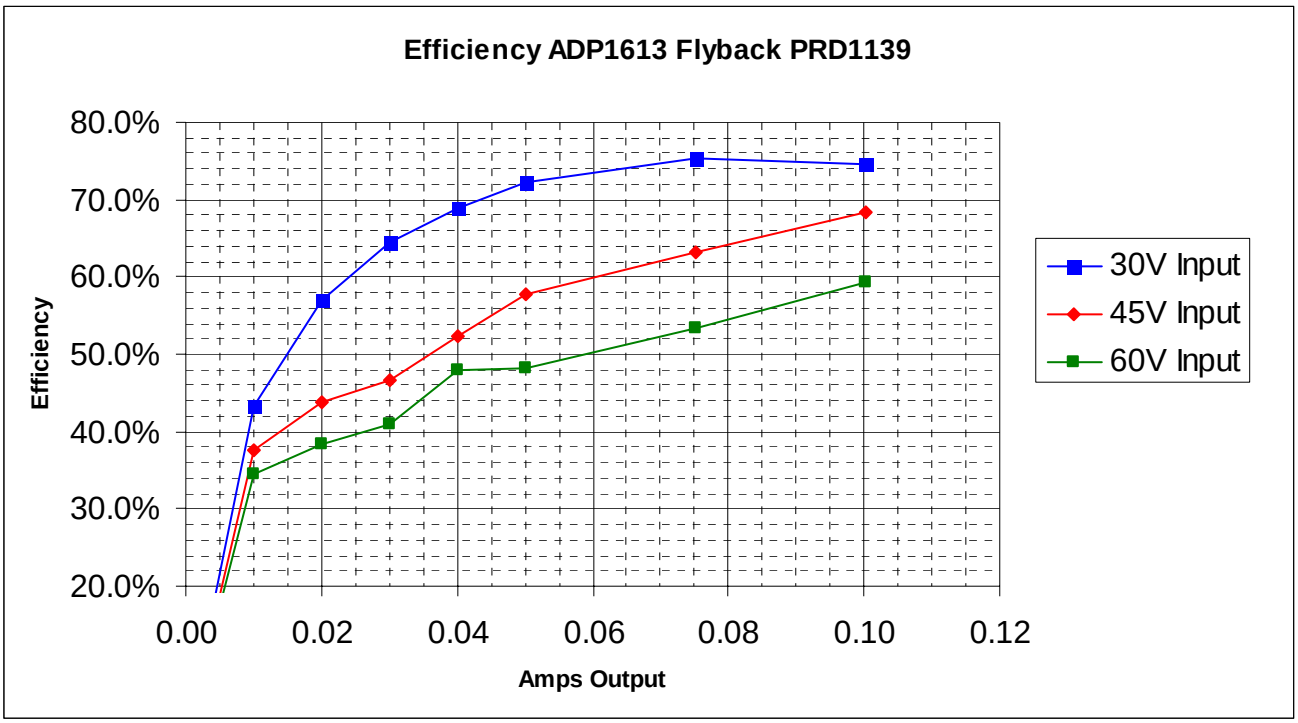


Figure 3. Voltage Regulation Test Data

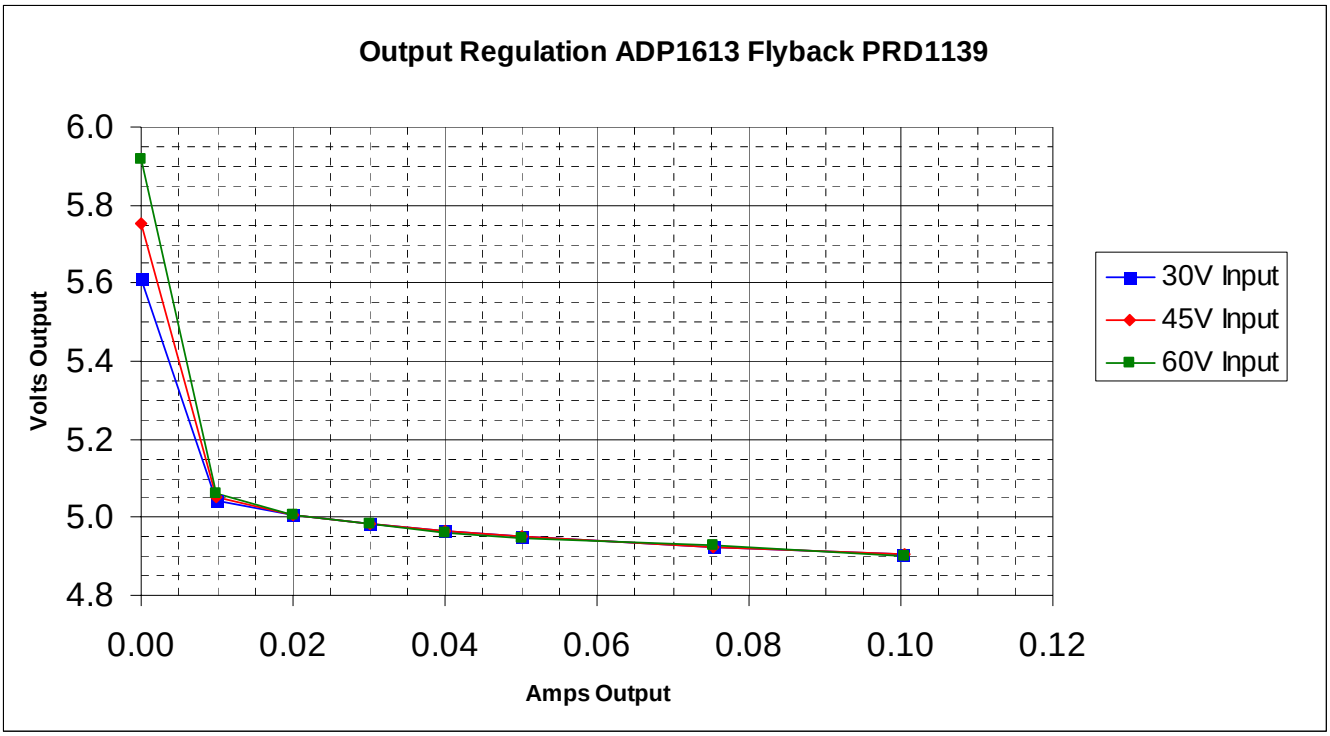
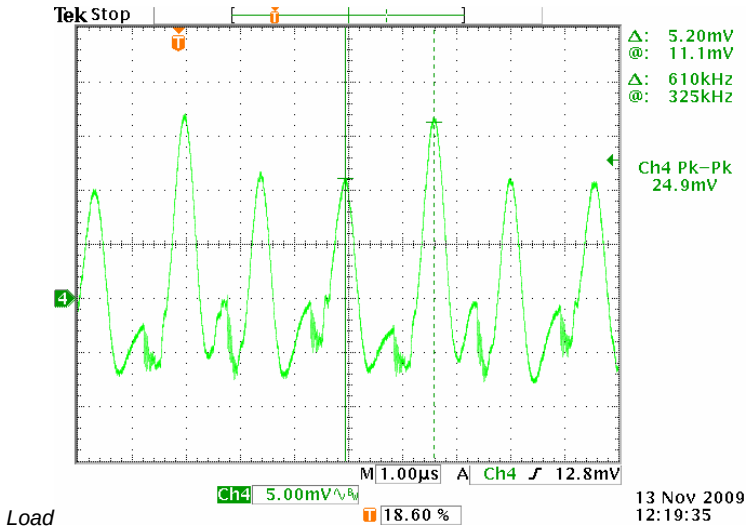


Figure 4. Output ripple with 60 VDC Input and 100 mA Load



Load

Figure 5. Output ripple with 60 VDC Input and 10 mA Load

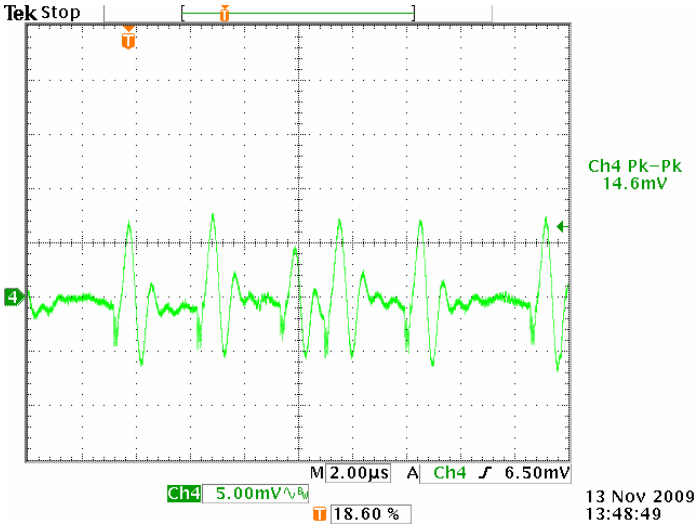


Figure 6. Output ripple with 30 VDC Input and 100 mA Load

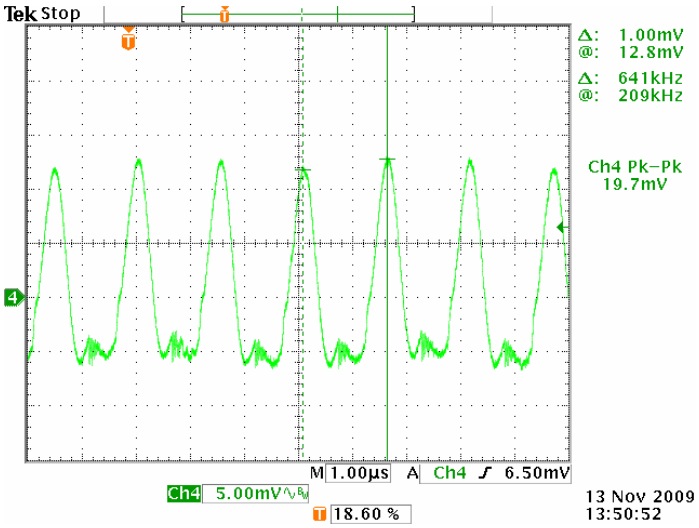
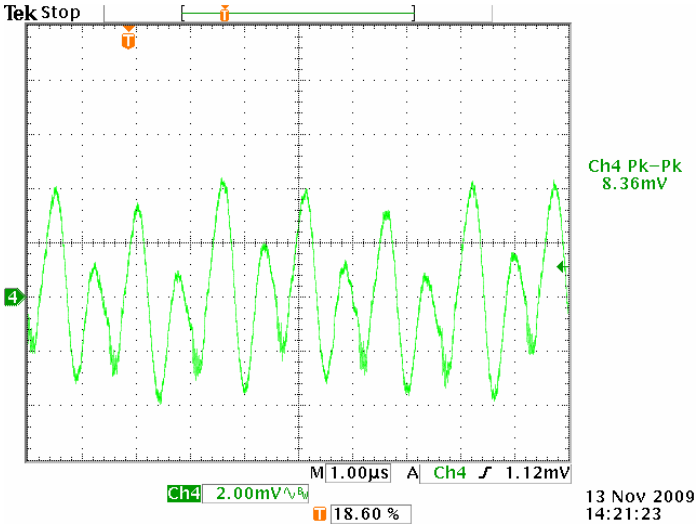


Figure 7. Output ripple with 30 VDC Input and 10 mA Load



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