ANALOG DEVICES

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APPLICATON NOTE

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# Component Processor Nonstandard Video Formats

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## INTRODUCTION

The purpose of this application note is to assist the user in configuring the component processor (CP) core to process the HD, PS, and graphics standards not covered by PRIM_MODE[3:0] and VID_STD[3:0]. For example, the CP can be programmed to support other SMPTE HD standards that are not supported using VID_STD[3:0], such as 720p/50 Hz and 1080i/50 Hz. Graphics standards such as MAC 13 and MAC 16 are examples of RGB nonstandard graphics formats that the CP can support if configured correctly.

In ADV7401/ADV7403 standard operation, the PRIM_MODE[3:0] and VID_STD[3:0] controls configure the CP to process the most common HD, PS, SD, and RGB graphics formats. (For more information on primary mode and video standard selection, refer to the ADV7401/ADV7403 hardware manuals, *Integrated Multiformat SDTV/HDTV Video Decoder and RGB Graphics Digitizer*, which list the supported modes.)

This application note describes how to configure the CP to process nonstandard video formats using the following steps:

1. Choose the appropriate PRIM_MODE[3:0]/VID_STD[3:0].
2. Program the latch clock.
3. Program PLL_DIV_RATIO[11:0].
4. Program FR_LL[10:0].

The PRIM_MODE[3:0]/VID_STD[3:0] Selection for Nonstandard Formats, Latch Clock, Pixel Clock Generation, and Free-Run Mode Configuration sections describe each of these steps, respectively. The Worked Examples section provides examples.

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# CP CORE CONFIGURATION

## PRIM_MODE[3:0]/VID_STD[3:0] SELECTION FOR NONSTANDARD FORMATS

The CP can be configured for nonstandard operation by setting PRIM_MODE[3:0] and VID_STD[3:0] to the nearest available standard. Table 2 gives examples of PRIM_MODE[3:0] and VID_STD[3:0] selections for nonstandard formats. A selection should be based on the best match for resolution and pixel clock frequency.

## LATCH CLOCK

The latch clock is an internal ADC parameter that controls sampling. The recommended latch clock settings can be set according to Table 1.

**Table 1. Latch Clock Settings**

| LATCH_CLK[3:0] | Pixel Clock (MHz) |
|---|---|
| 0001 | 13.5 to 54 |
| 0010 | 55 to 100 |
| 0101 | 108 |
| 0110 | 135 |

## PIXEL CLOCK GENERATION

The ADV7401/ADV7403 use a PLL to synthesize a pixel clock (TLLC) from the incoming Hsyncs. For nonstandard video formats, the PLL can be configured manually to derive a pixel clock of arbitrary frequency. This is achieved by programming the PLL feedback divider block (refer to Figure 1).

First, the user must set PLL_DIV_MAN_EN to 1 to enable manual programming of the PLL block. Then, for a nonstandard mode, PLL_DIV_RATIO[11:0] is set to give the required pixel clock.

Two methods are available to calculate this value of PLL_DIV_RATIO[11:0]. The user chooses one of these methods depending on the information available about the nonstandard format.

Method 1 is detailed in Equation 1 where the pixel clock frequency is divided by the incoming Hsync frequency. This equation describes the multiplying process of the PLL to generate a pixel clock from the incoming Hsyncs.

$$PLL\_DIV\_RATIO[11:0] = \frac{f_{PIXELCLOCK}}{f_{HSYNC}} \quad (1)$$

Method 2 follows the rule that PLL_DIV_RATIO[11:0] is always equal to the number of luma sample pixel periods per total line.

**Table 2. Examples of PRIM_MODE[3:0]/VID_STD[3:0] Selections for Nonstandard Formats**

| Nonstandard Video Format | | | ADV7401/ADV7403 CP Default Configurations | | | | |
|---|---|---|---|---|---|---|---|
| Format | Resolution | Pixel Clock (MHz) | PRIM_MODE[3:0] | VID_STD[3:0] | Format | Resolution | Pixel Clock (MHz) |
| VGA 70 | 640 × 480 | 28.561 | 0010 | 1001 | VGA 72 | 640 × 480 | 31.515 |
| WVGA60 | 852 × 480 | 34.000 | 0010 | 0000 | SVGA 56 | 800 × 600 | 36.00 |
| MAC 13 | 640 × 480 | 30.240 | 0010 | 1001 | VGA 72 | 640 × 480 | 31.515 |
| MAC 21 | 1152 × 870 | 100.00 | 0010 | 1111 | XGA 85 | 1024 × 768 | 94.5 |
| 1080i/50 Hz | 1920 × 1080 | 74.25 | 0001 | 1100 | HD 1080/60 | 1920 × 1080 | 74.25 |

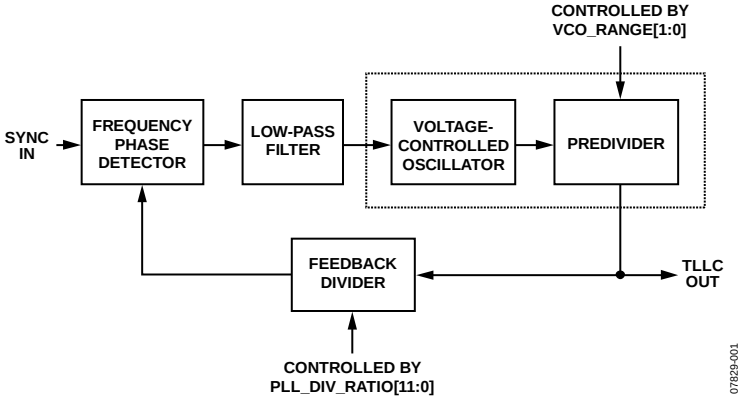


*Figure 1. PLL Architecture*

### *VCO_RANGE[1:0] and PLL_QPUMP[2:0] Manual Configuration*

VCO_RANGE[1:0] and PLL_QPUMP[2:0] must be set to configure the PLL to generate a stable TLLC. The recommended VCO range and PLL charge pump settings can be set according to Table 3 and Table 4.

**Table 3. Nonstandard Video Format VCO Range Settings**

| VCO_RANGE[1:0] | Pixel Clock (MHz) |
|---|---|
| 00 | 13.5 to 29 |
| 01 | 30 to 44 |
| 10 | 45 to 89 |
| 11 | 90 to 140 |

**Table 4. Nonstandard Video Format PLL Settings**

| Charge Pump Current, PLL_QPUMP[2:0] | Pixel Clock (MHz) |
|---|---|
| 001 | <22 |
| 011 | ≥22 |
| 100 | ≥31 |
| 101 | ≥42 |
| 011 | ≥45 |
| 100 | ≥48 |
| 101 | ≥58 |
| 100 | ≥90 |
| 101 | ≥95 |
| 110 | ≥136 |
| 111 | ≥205 |

The settings of VCO_RANGE[1:0] become active only if VCO_RANGE_MAN is set to 1. The appropriate VCO range is selected automatically for all standards supported by PRIM_MODE[3:0] and VID_STD[3:0].

### *Subsampling Input Video*

It is also possible to subsample the input video by adjusting the PLL divider ratio. This allows the CP to process a standard format at a lower horizontal resolution (luma samples per line) while keeping the same vertical resolution (lines per frame). Care should be taken to band limit the incoming video signal to prevent aliasing distortion.

Using subsampling, the CP can also process a video format with a resolution and pixel clock that are higher than the specifications of the ADV7401/ADV7403. For example, UXGA at 60 Hz (1600 × 1200) has a pixel clock at 162 MHz, which is above the maximum sample rate of the ADC. By using the PLL to generate a 108 MHz clock from the incoming Hsyncs, the 1200 line resolution can be processed by the CP. The lower pixel clock gives a lower horizontal resolution with just 1440 luma samples per total line (S/TL) instead of 1600 S/TL in the full bandwidth signal.

## FREE-RUN MODE CONFIGURATION

The free-run function in the ADV7401/ADV7403 enables a blue screen output to be displayed when the CP core enters the unlocked state. The CP uses the line length measurement to decide when to go into the free-run state. The CP uses VID_STD[3:0] to determine the expected line length. The CP must be manually programmed to expect a different line length for nonstandard formats.

The FR_LL (free-run line length) parameter is the number of crystal clock cycles in the ideal line length of the video format. CP uses this parameter to detect when the line length has changed, either when the input format changes or when there is no input present. This parameter is normally decoded from VID_STD[3:0] and PRIM_MODE[3:0].

When the measured line length differs from FR_LL[11:0] by 32 clock cycles (this threshold can be set in CP_F_RUN_TH[2:0]), the CP core goes into the unlocked state and enters into free-run mode. To configure the CP for nonstandard video, the FR_LL[11:0] must be set manually. This enables it to ignore the default line length associated with the corresponding VID_STD[3:0].

To calculate the FR_LL[11:0] manual parameter, the line period is divided by the 27 MHz clock period (for a 27 MHz crystal) or 28.6363 MHz clock period (for a 28.6363 MHz crystal); refer to Equation 2. The numerator in this equation can be calculated directly from the Hysnc period, or by using the total number of luma pixel periods per line, multiplied by the pixel clock period.

$$FR\_LL[11:0] = \frac{t_{LINE\ PERIOD}}{t_{XTAL\_MHZ}} \quad (2)$$

where $t_{XTAL\_MHZ} = t_{27\ MHZ}$ for a 27 MHz crystal or $t_{XTAL\_MHZ} = t_{28.6363MHZ}$ for a 28.6363 MHz crystal.

# WORKED EXAMPLES

## EXAMPLE 1: 720p AT 50 Hz

1. Set PRIM_MODE[3:0] and VID_STD[3:0] to the closest available standard.
   PRIM_MODE[3:0] = 0001b
   VID_STD[3:0] = 1010b
   This selection is based on the pixel clock frequency and resolution closest to the available nonstandard format.
2. Program the latch clock. Referring to Table 1 for 74.25 MHz, LATCH_CLK[3:0] = 0010b.
3. Program PLL_DIV_RATIO[11:0]. Equation 1 cannot be used because there is no information on the Hsync frequency for this standard. Because the number of luma sample periods per total line is equal to 1980, PLL_DIV_RATIO[11:0] is set to 1980 using Method 2 (as described in the Pixel Clock Generation section).
   PLL_DIV_MAN_EN = 1b
   PLL_DIV_RATIO[11:0] = $1980_{dec}$ = 0x7BC
   Program PLL_QPUMP[2:0] to 101b and VCO_RANGE[1:0] to 10b (refer to Table 3 and Table 4).
4. Use Equation 2 to calculate FR_LL[11:0].
   $t_{LINE\ PERIOD}$ = (1980 × 1/74.25 MHz) = 26.667 µs
   $t_{27\ MHz}$ = 37.037 ns
   FR_LL[11:0] = $720_{dec}$ = 0x2D0

As a result of combining these new register settings with the standard settings, the following I²C writes are obtained for the ADV7401/ADV7403 (Device Address 0x42) 720p/50 Hz.

```
##CP 720p YPrPb 1X1##
:720p/50 YPrPb In 1X1 30Bit 444 Out:
42 05 01 ; PRIM_MODE = 0001b COMP
42 06 0A ; VID_STD = 1010b for 720P 1x1
42 3A 20 ; set latch clock settings to 010b
42 3B 80 ; External Bias Enable
42 3C 5D ; PLL_QPUMP to 101b
42 6B C2 ; 30-bit 4:4:4 output
42 87 E7 ; Man set PLL_DIV_RATIO 1980
42 88 BC ; Man set PLL_DIV_RATIO 1980
42 8A D0 ; VCO Range to 10b
42 8F 02 ; Set FR_LL = 720
42 90 D0 ; Set FR_LL = 720
End
```

**Table 5. Video Signal Timing for 720p at 50 Hz**

| System Nomenclature | Luma Samples per Active Line | Active Lines per Frame | Frame Rate (Hz) | Sampling Frequency (MHz) | Luma Sample Periods per Total Line | Total Lines per Frame |
|---|---|---|---|---|---|---|
| 1280 × 720 | 1280 | 720 | 50 | 74.25 | 1980 | 750 |

## EXAMPLE 2: MAC 16

1. Set PRIM_MODE[3:0] and VID_STD[3:0] to the closest available standard.
   PRIM_MODE[3:0] = 0010b
   VID_STD[3:0] = 0100b
   This selection is based on the pixel clock frequency and resolution closest to the nonstandard format available.
2. Program the latch clock. Referring to Table 1 for 55.000 MHz:
   LATCH_CLK[3:0] = 0010
3. Program PLL_DIV_RATIO[11:0]. Using Equation 1, an Hsync frequency of 49.107 kHz and a pixel clock of 55.000 MHz give the following:
   PLL_DIV_MAN_EN = 1b
   PLL_DIV_RATIO[11:0] = $1120_{dec}$ = 0x460
   Program PLL_QPUMP[2:0] to 100b and VCO_RANGE[1:0] to 10b (refer to Table 3 and Table 4).
4. Use Equation 2 to calculate FR_LL[11:0].
   $t_{LINE\ PERIOD}$ = (1/49.107 kHz) = 20.36 µs
   $t_{27\ MHz}$ = 37.037 ns
   FR_LL[11:0] = $550_{dec}$ = 0x226

As a result of combining these new register settings with the standard settings, the following $I^2C$ writes are obtained for the ADV7401/ADV7403 (Device Address 0x42) MAC 16:

```
##CP RGB Graphics Special Modes##
:832 x 624 _@ 75.087Hz MAC 16 PIXEL CLOCK 55.00 MHz:
      42 04 75 ; enable max drive strength
      42 05 02 ; PRIM_MODE = 0010b for GR
      42 06 04 ; VID_STD = 0100b for 800x600 @ 85; closest available standard.
      42 0E 0F ; enable max drive strength Clock & Syncs
      42 3A 20 ; set latch clock settings to 010b
      42 3B 80 ; External Bias Enable
      42 3C 5C ; PLL_QPUMP to 100b
      42 6A 00 ; DLL Phase Adjust
      42 6B 82 ; Enable DE output, swap Pr& Pb
      42 73 90 ; Set man_gain
      42 7B 1C ; TURN OFF EAV & SAV CODES
      42 87 E4 ; PLL_Div_Ratio to 1120
      42 88 60 ; PLL_Div_Ratio to 1120
      42 8A D0 ; VCO Range to 10b
      42 8F 02 ; FR_LL = 550
      42 90 26 ; FR_LL = 550
      End
```

**Table 6. Video Signal Timing for MAC 16**

| System Nomenclature | Luma Samples per Active Line | Active Lines per Frame | Frame Rate (Hz) | Sampling Frequency (MHz) | Luma Sample Periods per Total Line | Total Lines per Frame |
|---|---|---|---|---|---|---|
| 832 × 624 | 832 | 624 | 75.087 | 55.000 | 1120 | 654 |

## EXAMPLE 3: SXGA AT 75 Hz (SUBSAMPLED PIXEL CLOCK = 108 MHz)

1. Set PRIM_MODE[3:0] and VID_STD[3:0] to the SXGA at 75 Hz standard.
   PRIM_MODE[3:0] = 0010b
   VID_STD[3:0] = 0101b
   This selection is based on the pixel clock frequency and resolution closest to the nonstandard format available.
2. Program the latch clock. Referring to Table 1 for 108 MHz (subsampling pixel clock),
   LATCH_CLK[3:0] = 0010b
   Note that in the standard format (135 MHz), the latch clock is LATCH_CLK[3:0] = 0110.
3. Program PLL_DIV_RATIO[11:0] to give the required subsampling pixel clock. Using Equation 1, an Hsync frequency of 79.976 kHz and a pixel clock of 108 MHz give the following:
   PLL_DIV_MAN_EN = 1b
   PLL_DIV_RATIO[11:0] = $1351_{dec}$ = 0x547
   Program PLL_QPUMP[2:0] to 101b and VCO_RANGE[1:0] to 11b (refer to Table 3 and Table 4).
   Note that there are 1350 S/TL for the subsampled video data and 1688 S/TL in the standard format.
4. Use Equation 2 to calculate FR_LL[11:0].
   $t_{LINE\ PERIOD}$ = (1/79.976 kHz) = 12.503 µs
   $t_{27\ MHz}$ = 37.037 ns
   FR_LL[11:0] = $338_{dec}$ = 0x152

As a result of combining these new register settings with the standard settings, the following I²C writes are obtained for the ADV7401/ADV7403 (Device Address 0x42) SXGA at 75 Hz:

```
##CP RGB Graphics MEI Special Modes##
:1280x1024 _@ 75.025Hz SubSamp. 108MHz Out through DAC:
      42 05 02 ; PRIM_MODE = 0010b for GR
      42 06 05 ; VID_STD = 0101b for 1280x1024 @ 75
      42 37 00 ; Invert PCLK
      42 3A 21 ; set latch clock settings to 010b, Power Down ADC3
      42 3B 80 ; Enable External Bias
      42 3C 5D ; PLL_QPUMP to 101b
      42 6A 00 ; DLL Phase Adjust
      42 6B C2 ; sets CPOP_SEL to 0010b 30 Bit Output Pr/Pb pins swapped.
      42 73 90 ; Set man_gain
      42 7B 1C ; TURN OFF EAV & SAV CODES
      42 87 E5 ; PLL_Div_Ratio to 1350
      42 88 47 ; PLL_Div_Ratio to 1350
      42 8A F0 ; VCO Range to 11b
      42 8F 01 ; FR_LL = 338
      42 90 52 ; FR_LL = 338
      42 B3 FE ; STDI Tweak
      42 F4 3F ; Max Drive Strength
      End
```

**Table 7. Video Signal Timing for SXGA at 75 Hz (Subsampled)**

| System Nomenclature | Luma Samples per Active Line | Active Lines per Frame | Frame Rate (Hz) | Sampling Frequency (MHz) | Luma Sample Periods per Total Line | Horizontal Frequency (kHz) |
|---|---|---|---|---|---|---|
| 1280 × 1024 | 1280 | 1024 | 75 | 135 (108[1]) | 1688 (1350[1]) | 79.976 |

[1] Subsampled video data format.

## EXAMPLE 4: VESA 1360 × 768 AT 60.015 Hz (PIXEL CLOCK = 85.5 MHz)

1. Set PRIM_MODE[3:0] and VID_STD[3:0] to the 1024 × 768 at 75 Hz standard.
   PRIM_MODE[3:0] = 0010b
   VID_STD[3:0] = 1110b
   This selection is based on the pixel clock frequency and resolution closest to the nonstandard format available.
2. Program the latch clock. Referring to Table 1 for 85.5 MHz gives
   LATCH_CLK[3:0] = 0010b
3. Program PLL_DIV_RATIO[11:0] to give the required sampling pixel clock. Using Equation 1, an Hsync frequency of 47.712 kHz and a pixel clock of 85.5 MHz give the following:
   PLL_DIV_MAN_EN = 1b
   PLL_DIV_RATIO[11:0] = $1792_{dec}$ = 0x700
   Program PLL_QPUMP[2:0] to 101b and VCO_RANGE[1:0] to 10b (refer to Table 3 and Table 4).
4. Use Equation 2 to calculate FR_LL[11:0].
   $t_{LINE\ PERIOD}$ = (1/47.712 kHz) = 20.959 µs
   $t_{27\ MHz}$ = 37.037 ns
   FR_LL[11:0] = $566_{dec}$ = 0x236

As a result of combining these new register settings with the standard settings, the following $I^2C$ writes are obtained for the ADV7401/ADV7403 (Device Address 0x42) 1360 × 768 at 60 Hz:

```
##CP RGB Graphics Special Modes##
:1360×768 _@ 60.015Hz, 85.500MHz Out through DAC:
      42 05 02 ; PRIM_MODE = 0010b for GR
      42 06 0E ; VID_STD = 1110b for 1024x768 @ 75
      42 3A 21 ; set latch clock settings to 010b, Power Down ADC3
      42 3B 80 ; Enable External Bias
      42 3C 5D ; PLL_QPUMP to 101b
      42 6A 00 ; DLL Phase Adjust
      42 6B 82 ; Enable DE output, swap Pr Pb
      42 73 90 ; Set man_gain
      42 7B 14 ; AV CODES DISABLE, TURN OFF EAV and SAV CODES
      42 87 E7 ; PLL_Div_Ratio to 1792
      42 88 00 ; PLL_Div_Ratio to 1792
      42 8A E0 ; VCO Range to 10b
      42 8F 02 ; FR_LL = 566
      42 90 36 ; FR_LL = 566
      42 F4 3F ; Max Drive Strength
      End
```

**Table 8. Video Signal Timing for 1360 × 768 at 50 Hz**

| System Nomenclature | Luma Samples per Active Line | Active Lines per Frame | Frame Rate (Hz) | Sampling Frequency (MHz) | Luma Sample Periods per Total Line | Horizontal Frequency (kHz) |
|---|---|---|---|---|---|---|
| 1360 × 768 | 1360 | 768 | 60.015 | 85.5 | 1792 | 47.712 |

# HINTS

Enabling AV_CODE_EN[1] while the DAC output is set can cause visible vertical line on the output. To avoid this, AV_CODE_EN[1] should be turned off when using DAC output.

AV_BLANK_EN[3] blanks the video according to where the VBI should be, as dictated by PRIM_MODE[3:0], and it may be incorrect for the new configuration. In this event, disable the AV_BLANK_EN bit.

Noise on the output can be caused by inappropriate polarization of PCLK between the decoder and the back end. (Refer to the ADV7401 and ADV7403 hardware manuals, *Integrated Multiformat SDTV/HDTV Video Decoder and RGB Graphics Digitizer*.) It is possible to inverse the PCLK signal and avoid noise using PCLK[0].

```
42 37 00 ; Invert PCLK
```

Changing the CP free-run threshold (CP_F_RUN_TH[2:0]) may cause invalid output. This value is set by default to 0x54.

Due to EMC and crosstalk, it may be advisable to strengthen or weaken the drive strength of the output drivers. DR_STR_S[1:0] set the drive strength of the synchronization signals, HS, VS, and FIELD. DR_STR_C[1:0] select the output strength of the clock signal output driver. DR_STR[1:0] set the drive strength of the data output drivers.

Suggested values are shown in Table 9.

**Table 9. Drive Strength Settings**

| DR_STR_S[1:0] | DR_STR_C[1:0] | DR_STR[1:0] | Pixel Clock (MHz) |
|---|---|---|---|
| 01 | 01 | 01 | <54 |
| 10 | 10 | 10 | <110 |
| 11 | 11 | 11 | >110 |

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