ADMV4801/ADMV4821 SPI Application Note

INTRODUCTION

This application note clarifies the features, implementations, and registers associated with the ADMV4801/ADMV4821 serial peripheral interfaces (SPI).

OVERVIEW

The ADMV4801 contains 16 independent channels and passes all 16-channel signals to or from one input/output port, RFC pin, with a combiner or a splitter. The ADMV4801 has a TRX pin to switch between transmit and receive mode, and a LOAD pin to transfer the content from holding registers to working registers.

The ADMV4821 also contains 16 independent channels, but unlike the ADMV4801, eight even channels are fed to the RFV pin and the other eight odd channels are fed to the RFH pin. Thus, the device supports horizontal and vertical polarized antennas simultaneously. The ADMV4821 also has individual control, via the TRXH and TRXV pins, for the horizontal and vertical channels to switch between transmit and receive mode. Similar to the ADMV4801, the ADMV4821 also has individual control for the load function, via the LOAD_V and LOAD_H pins, to transfer the content from the holding register to the working registers.

When referencing the load feature, function, or pins, LOAD represents the LOAD pin for the ADMV4801 and the LOAD_V and LOAD_H pins for the ADMV4821, unless otherwise noted. Similarly, when referencing the TRX pins, feature, or function, TRX represents the TRX pin for the ADMV4801 and the TRXV and TRXH pins for the ADMV4821, unless otherwise noted.

Details of how to use the LOAD pins are explained in the Hard Reset Pin, LOAD Pin, and TRX Pin section.

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REVISION HISTORY

1/2023—Revision D: Initial Version

DIGITAL PINS

SPI PINS

The SPI of the ADMV4801/ADMV4821 allow the user to configure the device for specific operation using one of two SPI configurations: a 3-wire SPI (SCLK, SDIO, and $\overline{CS}$) or a 4-wire SPI (SCLK, SDIO, SDO, and $\overline{CS}$). This interface provides users with added flexibility and customization. The SPI is 1.8 V dc logic. Along with the SPI pins, there are digital pins to control other digital functions within the ADMV4801/ADMV4821.

In 4-wire SPI mode, SDIO is an SPI serial data input only and SDO is a serial data output. In 3-wire SPI mode, SDIO is an SPI serial data input/output and SDO is not used.

Place series 22 Ω resistors on SPI wires for optimum performance. Place the resistors as close as possible to the controller device of the ADMV4801/ADMV4821.

HARD RESET PIN, LOAD PIN, AND TRX PIN

The $\overline{RST}$ pin is an SPI hard reset pin and is an active low interface. Connect $\overline{RST}$ to logic high (1.8 V CMOS logic) for normal operation. $\overline{RST}$ resets certain registers (see Standard SPI Registers and SRAM Registers section for details).

Certain registers feature a LOAD pin to toggle three times to load the values from the holding registers to the working registers, so that the change can take effect in the device. This load feature enables multiple ADMV4801/ADMV4821 devices on a single array to be synchronized and the data to take effect simultaneously when the load lines are toggled. Refer to the Register Information section for details on LOAD pin toggling requirements for each register.

A rising edge of an input signal transitions for channels from receive mode to transmit mode. A falling edge of an input signal transitions from transmit mode to receive mode.

SPI PROTOCOL

STANDARD SPI PROTOCOL

The ADMV4801/ADMV4821 protocol consist of a write or read bit, followed by 15 register address (A14 to A0) bits and eight data bits. The default for both the address and data fields is organized most significant bit (MSB) first and end with the least significant bit (LSB) when Register 0x000, Bit 6 is set to 0. For a write, set the first bit to 0, and for a read, set this bit to 1. Standard Analog Devices SPI data is set to eight bits wide. See the ADMV4801 and ADMV4821 data sheets for the standard Analog Devices SPI protocol register timing diagram and for the typical timing specifications.

In addition, the ADMV4801/ADMV4821 include various registers that require wider than eight bits of data to be able to set the register values correctly. Refer to Standard SPI Registers and SRAM Registers section for details.

STREAMING MODE

While operating in standard protocol, $\overline{CS}$ can be held low and multiple data bytes can be shifted during the data part, reducing the amount of overhead associated with data transfer. Sequential addresses are assumed in ascending or descending order based on how the configuration registers are set. Streaming mode can be used to quickly load gain and phase data for the SRAM for user defined beam positions. This technique allows one or more bytes to be written to or read from without providing an address for each. See the ADMV4801 and ADMV4821 data sheets for the streaming mode write timing diagram, which show a typical write to a device streaming three consecutive addresses.

SDO READ DELAY AT HIGH SPEED CLOCK

During an SPI read operation, data is available on the SDO pin 7 ns after the 16th falling SCLK edge arrives at the SCLK pin. This SDO delay remains constant, regardless of the SCLK speed. See the ADMV4801 and ADMV4821 data sheets for the SDO delay timing diagram and two workaround if high speed clock is needed.

MULTIPLE DEVICES HARDWARE CONFIGURATION

Configure multiple ADMV4801/ADMV4821 devices by connecting all four device hardware address bits to ground (ADD0 to ADD3). This configuration assigns Address 0 to all devices and the separate $\overline{CS}$ lines select which device is active for the SPI to control for write/read operation to individual beam formers (see Figure 1). Connecting address pins to nonground supplies may cause device operation issues. This configuration also allows broadcasting to all beam formers simultaneously, if desired. Set the SPI_MODE pin on the ADMV4801/ADMV4821 to logic low for operating in standard Analog Devices SPI mode.

If all the settings across multiple devices are to be loaded at the same time, bring all $\overline{CS}$ lines to logic low and write the same beam pointer to all devices on the same SPI transaction simultaneously. Next, toggle the LOAD pin to update all devices simultaneously. If the devices are written in sequence, the user must toggle the LOAD pin each time each chip is set up.

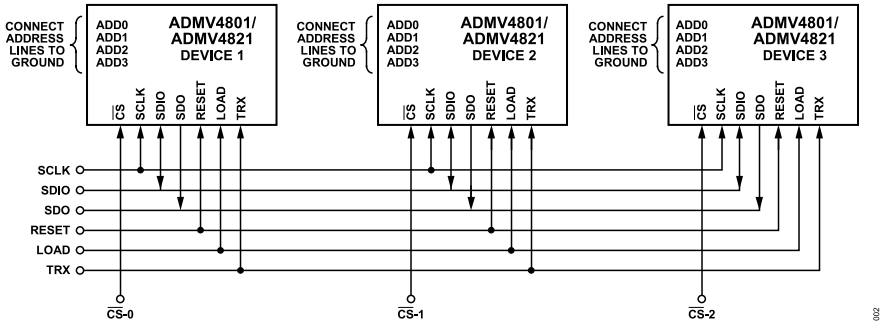

Figure 1. Multiple Chips Hardware Connection, SDIO Bidirectional

REGISTER DESCRIPTION

STANDARD SPI REGISTERS AND SRAM REGISTERS

The ADMV4801/ADMV4821 have two types of registers: SRAM registers and standard SPI registers.

The SRAM registers are divided into paged SRAM registers and global SRAM registers.

The paged (channel) SRAM registers retain their values after software reset using Register 0x000 or via a hardware reset by pulling the $\overline{RST}$ pin to a logic low. These values are cleared after a power recycle.

The values of the global SRAM register are cleared after a hardware reset or a power recycle.

Neither paged (channel) nor global SRAM registers have specific default values, which are required on startup for normal operation. To read back from the SRAM registers, the user must send the read command twice.

In addition to the SRAM registers, the ADMV4801 and ADMV4821 include standard SPI registers that provide configurability of the device, including but not limited to

- SPI configuration.
- Transmit mode power amplifier configuration.
- Receive mode LNA configuration.
- Transmit mode common gain offset for each channel, which adjusts the common gain applied to all channels.
- Power detector and temperature sensor readback.

The standard SPI registers are also divided into paged and global registers, and have specific default values. The values of the standard SPI registers are cleared to the default values after a software or hardware reset, or a power recycle.

Most standard SPI registers are eight bits wide. However, the ADMV4801/ADMV4821 include a group of registers that are 16 bits wide. In a single SPI transaction, there are only eight bits of data to write or read. Use Address Select Register 0x08 to select either the 8 LSBs or the 8 MSBs to write or read. Set Register 0x08 to 0x01 to select the 8 LSBs. Set Register 0x08 to 0x02 to select 8 MSBs.

Certain registers feature a LOAD pin that toggles three times to load the values to the device. The LOAD pin only needs to be toggled after all registers are updated so that the data across multiple registers and channels take effect simultaneously. Users can also toggle the LOAD pin anytime, if needed.

Refer to the Register Information section for details about global and page properties, as well as LOAD pin toggling requirements for each register.

PAGED REGISTERS AND GLOBAL REGISTERS

For efficient communication to the device, each channel has a counterpart memory page, totaling 16 memory pages. Each memory page contains paged registers for the corresponding channel settings. Use Register 0x013 and Register 0x014 to select the pages (channels). Paged registers are not written or read unless the corresponding memory page is selected.

For example, Register 0x200 is a paged register. To write to Register 0x200 in all channels, first set both Register 0x013 and Register 0x014 to 0xFF.

The global registers are always accessible, regardless of page selection.

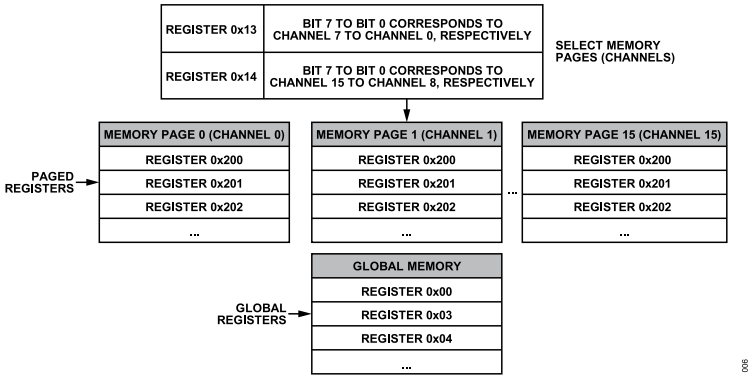

Figure 2. Global and Paged Registers

BEAM POINTER MODE AND BYPASS MODE

There are two methods to set the gain and phase for each channel in the ADMV4801 and ADMV4821: beam pointer mode and bypass mode.

In beam pointer mode, each channel memory page stores 256 user defined beam positions. For the ADMV4801, Register 0x081 is the beam pointer register that recalls (points to) the specific beam position to apply to the device. For the ADMV4821, Register 0x081 is the beam pointer register for eight vertical channels and Register 0x082 is for eight horizontal channels.

Each beam position contains phase and gain settings and can be loaded for either transmit or receive mode, regardless of the current operation mode. The LOAD pin is toggled three times to load the beam position settings to the selected channels simultaneously. The beam pointer method is recommended for the production environment due to its simplicity and the reduced amount of data transfer during beam position switching. The beam pointer can also be used for evaluation and characterization of the device.

The second method by which to set gain and phase for each channel is to bypass the beam pointer. In bypass mode, rather than using a predefined beam position and the beam pointer, directly program the settings for each channel. The bypass method is recommended only for evaluation to determine the phase and gain settings for each channel.

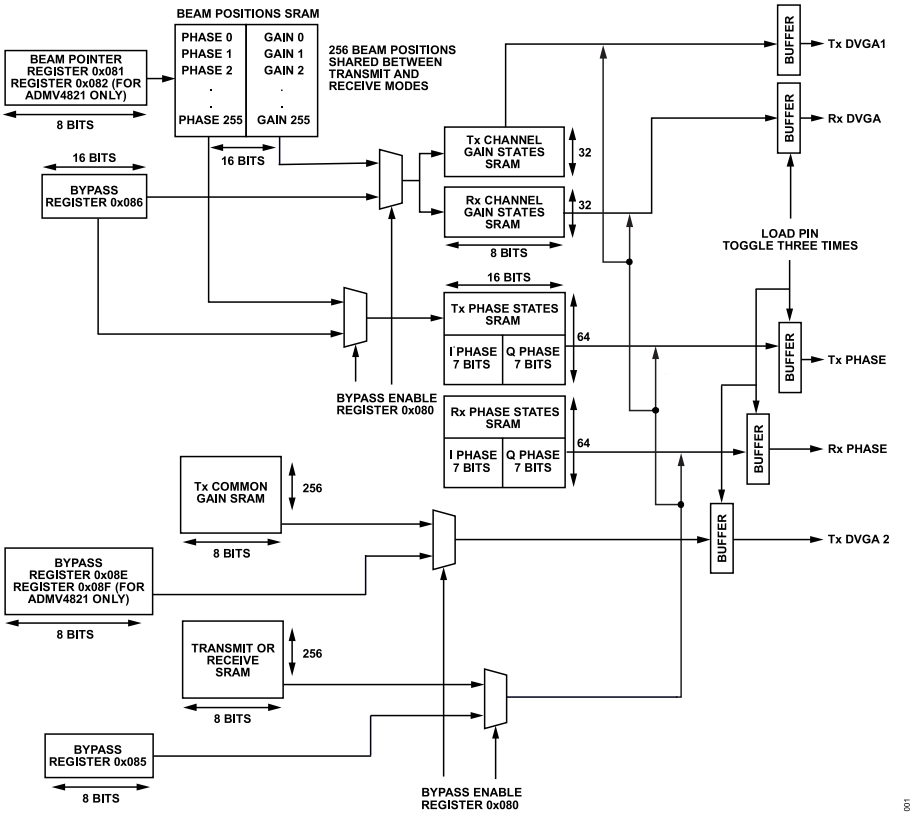

Figure 3. ADMV4801/ADMV4821 Beam Pointer Mode and Bypass Mode Block Diagram

PHASE AND GAIN STATES SRAM

Understanding SRAM space in the ADMV4801/ADMV4821 is critical before beginning beam pointer and bypass mode implementation, because these registers are used in both modes.

The user must write to certain registers to achieve phase and gain control for the device. For transmit mode, there are three settings regarding phase and gain control:

- Transmit channel gain settings. The registers are paged and applied to Digital Variable Gain Amplifier 1 (DVGA 1) in transmit path by default. Each channel has an independent setting.
- Transmit common gain settings. Registers are global and applied to Digital Variable Gain Amplifier 2 (DVGA 2) in the transmit path by default. All channels use one global setting.
- Phase settings. The registers are paged. Each channel has an independent setting.

In receiver mode, there is a single digital variable gain amplifier (DVGA) and two settings regarding phase and gain control:

- For each channel, there is only one receive gain setting. The registers are paged and applied to the receive DVGA. Each channel has an independent setting.
- For phase settings, the registers are paged. Each channel has an independent setting.

To understand the RF signal path details, refer to the ADMV4801 and ADMV4821 data sheets.

Transmit and Receive Phase States SRAM

The ADMV4801 or ADMV4821 SRAM assigns a group of 16-bit data registers to store the phase states for both transmit and receive modes. Each register stores a single phase state, consisting of 7-bit I phase data (Bits[13:7]) and 7-bit Q phase data (Bits[6:0]). The I and Q phase data must be the same for one phase state. The data corresponds to actual phase degree. Phase states are the basis for phase settings and are used in both beam pointer mode and bypass mode.

Table 1 describes the phase state registers. The index is important because the phase settings use this index to recall the phase states.

There are 64 registers for each transmit and receive mode, with a total of 128 registers. Register 0x180 to Register 0x1BF are for transmit mode and Register 0x100 to Register 0x13F are for receive mode. These registers are all paged registers. For optimum initial performance, set the phase states with an identical location index to the same values across all channels.

Table 2 is the truth table for the actual phase values from 0° to 354.75° in increments of 5.625° with unity gain. Users can select any 64 phase values for the transmit mode or receive mode to create customized phase states. Each phase state requires 16-bit data. As mentioned previously in the Standard SPI Registers and SRAM Registers section, to write to 16-bit data registers, use Register 0x08 to identify which eight bits of the 16 bits to write. For example, write 0x01 to Register 0x08 before writing 8 LSBs to the phase state registers and 0x02 to Register 0x08 for the 8 MSBs.

To write to phase states registers, use the following procedure (note that this procedure uses Register 0x180 as an example):

1. Write to Page Select Register 0x013 and Page Select Register 0x014 to target all channels (set Register 0x13 to 0xFF and set Register 0x014 to 0xFF).
2. Determine the hexadecimal value for the actual phase values. For example, to set phase value to 5.625°, the MSB is 0x3F and the LSB is 0xC6. See Table 2.
3. Write the LSB to the registers (set Register 0x08 to 0x01 and set Register 0x180 to 0xC6).
4. Write the MSB to the registers (set Register 0x08 to 0x02 and set Register 0x180 to 0x3F).
5. Toggle the LOAD pin three times. For the ADMV4821, toggle either the LOAD_V or the LOAD_H pin, as needed.

Table 1. Transmit and Receive Phase State Registers

Transmit Mode				Receive Mode			
Register Address	**Index**	**I Phase Data (Bits[13:7])**	**Q Phase Data (Bits[6:0])**	**Register Address**	**Index**	**I Phase Data (Bits[13:7])**	**Q Phase Data (Bits[6:0])**
0x180	0	User defined	User defined	0x100	0	User defined	User defined
0x181	1	User defined	User defined	0x101	1	User defined	User defined
…	…	…	…	…	…	…	…
0x1BF	63	User defined	User defined	0x13F	63	User defined	User defined

Table 2. Phase Value Truth Table

Phase Value in Degrees	MSB (8 Bits)	LSB (8 Bits)
0	3F	80
5.625	3F	C6
11.25	3F	4C
16.875	3E	52
22.5	3D	58
28.125	3C	5E
33.75	3A	63
39.375	38	E8
45	36	ED
50.625	34	71
56.25	31	F4
61.875	2F	78
67.5	2C	7A
73.125	29	7C
78.75	26	7E
84.375	23	7F
90	00	7F
95.625	03	7F
101.25	06	7E
106.875	09	7C
112.5	0C	7A
118.125	0F	78
123.75	11	F4
129.375	14	71
135	16	ED
140.625	18	E8
146.25	1A	63
151.875	1C	5E
157.5	1D	58
163.125	1E	52
168.75	1F	4C
174.375	1F	C6
180	1F	80
185.625	1F	86
191.25	1F	0C
196.875	1E	12
202.5	1D	18
208.125	1C	1E
213.75	1A	23
219.375	18	A8
225	16	AD
230.625	14	31
236.25	11	B4
241.875	0F	38
247.5	0C	3A
253.125	09	3C
258.75	06	3E
264.375	03	3F
270	00	3F
275.625	23	3F
281.25	26	3E
286.875	29	3C
292.5	2C	3A
298.125	2F	38
303.75	31	B4
309.375	34	31
315	36	AD
320.625	38	A8
326.25	3A	23
331.875	3C	1E
337.5	3D	18
343.125	3E	12
348.75	3F	0C
354.375	3F	86

Transmit and Receive Gain States SRAM

Similar to phase, the ADMV4801/ADMV4821 SRAM assigns another group of 8-bit data registers to store the gain states for both transmit mode and receive mode. Each register stores a single gain state. The gain data corresponds to actual gain levels. Gain states are the basis for gain settings and gain states are used in both beam pointer and bypass mode.

Table 4 describes the gain state registers. The index is important because the gain settings use this index to recall the gain states. Registers are eight bits wide but use only six bits.

There are 32 registers for each transmit mode and receive mode, for a total of 64 registers. Register 0x1C0 to Register 0x1DF are for transmit mode and Register 0x140 to Register 0x15F are for receive mode. These registers are paged registers. For optimum initial performance, set the gain states with an identical index to the same values across all channels.

Table 3 shows the truth table for the actual gain levels from 0 dB to 17.5 dB in increments of 0.5 dB. Users can choose any of the 32 gain levels (out of a total of 36 gain levels) for the transmit mode or receive mode to create customized gain states.

For transmit mode, only Register 0x1C0 to Register 0x1DF define the transmit channel gain states, which are applied to DVGA 1 by default. The transmit common gain is defined in other registers and discussed in the following sections.

To write to gain states registers, use the following procedure (note that this procedure uses Register 0x1C0 as an example):

1. Write to Page Select Register 0x013 and Page Select Register 0x014 to target all channels (set Register 0x13 and Register 0x14 to 0xFF).
2. Determine the hexadecimal value for the actual gain levels. For example, to set gain level to 17.5 dB, the data must be 0x23.
3. Write to the registers (set Register 0x1C0 to 0x23).
4. Toggle the LOAD pin three times. For the ADMV4821, toggle either the LOAD_V or LOAD_H pin, as needed.

Table 3. Gain Level Truth Table

Gain Level (dB)	Data (Hexadecimal)
0	00
0.5	01
1.0	02
1.5	03
2.0	04
2.5	05
3.0	06
3.5	07
4.0	08
4.5	09
5.0	0A
5.5	0B
6.0	0C
6.5	0D
7.0	0E

Table 3. Gain Level Truth Table (Continued)

Gain Level (dB)	Data (Hexadecimal)
7.5	0F
8.0	10
8.5	11
9.0	12
9.5	13
10.0	14
10.5	15
11.0	16
11.5	17
12.0	18
12.5	19
13.0	1A
13.5	1B
14.0	1C
14.5	1D
15.0	1E
15.5	1F
16.0	20
16.5	21
17.0	22
17.5	23

Table 4. Transmit Channel Gain State and Receive Gain State Registers

Transmit Mode			Receive Mode		
Register Address	Index	Channel Gain Data (Bits[5:0])	Register Address	Index	Gain Data (Bits[5:0])
0x1C0	0	User defined	0x140	0	User defined
0x1C1	1	User defined	0x141	1	User defined
…	…	…	…	…	…
0x1DF	31	User defined	0x15F	31	User defined

BEAM POINTER MODE

Beam pointer mode can be used for both the production environment and evaluation, given the advantages of simpler and fewer data transfers between beam position switching. Beam pointer mode acts like a double pointer. The beam pointer points to the beam settings that include three categories of SRAM registers: beam position SRAM, transmit or receive SRAM, and transmit common gain SRAM (see Figure 4). Then, the beam position SRAM points to the phase and gain SRAM described in the Phase and Gain States SRAM section.

The ADMV4801 and ADMV4821 SRAMs can store up to 256 user defined beam settings.

The beam pointer registers are eight bits wide, paged, standard SPI registers. For ADMV4801, there is only one beam pointer, Register 0x081. For ADMV4821, there are two beam pointers, Register 0x081 for eight vertical channels and Register 0x082 for eight horizontal channels. The registers recall the settings and load the settings to the device until LOAD toggling takes place. When transmit or receive SRAM is set to receive mode, the transmit common gain SRAM register data is irrelevant, although beam pointer registers are paged. For optimum performance, use identical values across all channels.

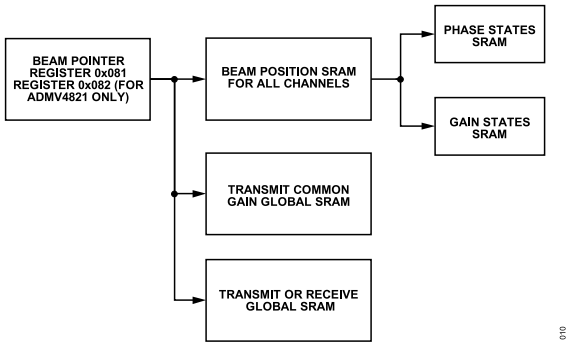

Figure 4. Beam Pointer Mode Simplified Diagram

BEAM POINTER VALUE	BEAM POSITION SRAM	TRANSMIT COMMON GAIN SRAM	TRANSMIT COMMON GAIN SRAM (FOR ADMV4821 ONLY)	TRANSMIT OR RECEIVE SRAM
0	REGISTER 0x200	REGISTER 0x400	REGISTER 0x500	REGISTER 0x600
1	REGISTER 0x201	REGISTER 0x401	REGISTER 0x501	REGISTER 0x601
...	...	...	...	...
255	REGISTER 0x2FF	REGISTER 0x4FF	REGISTER 0x5FF	REGISTER 0x6FF

011

Figure 5. Beam Pointer Value

Beam Position SRAM

Prior to writing to the beam pointer register, users must define the beam positions. Each channel memory page has 256 beam positions, stored in Register 0x200 to Register 0x2FF, indexed from 0 to 255. Each register is a 16-bit data paged register and stores the phase and gain states index, as shown in Figure 6. The beam positions with the same index can include different phase and gain settings for different channels.

To write the data into certain channel beam position registers, use the following procedure (note that this procedure uses Register 0x200 and Channel 0 as an example):

1. Write to Page Select Register 0x013 and Page Select Register 0x014 for targeted channels (set Register 0x13 to 0x01 and set Register 0x14 to 0x00).
2. Determine the index to recall the phase and gain states registers. For example, for Register 0x200, recall Register 0x183 as the phase setting and Register 0x1C1 as the gain setting. The phase state index is 0x03 and the gain state index is 0x01. Refer to Table 1 and Table 4.
3. Write to Register 0x008 and the 8-bit LSB of the beam position registers (set Register 0x08 to 0x01 and set Register 0x200 to 0x81).
4. Write to Register 0x008 and the 8-bit MSB of the beam position registers (set Register 0x08 to 0x02 and set Register 0x200 to 0x01).
5. Toggle the LOAD pin three times. For ADMV4821, toggle either the LOAD_V or the LOAD_H pin, as needed.

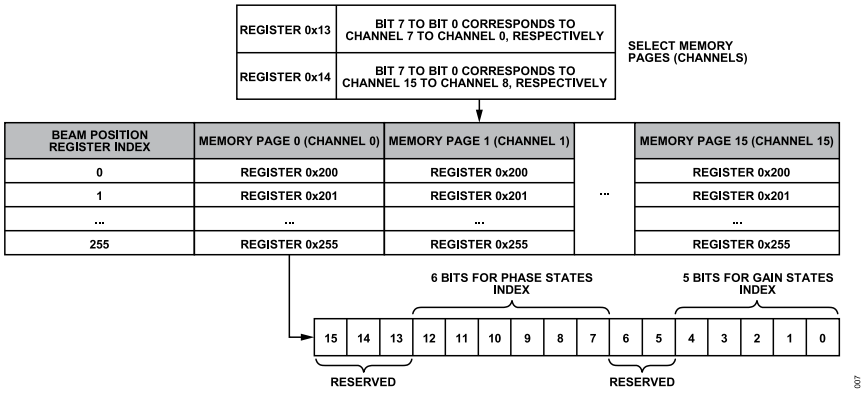

Figure 6. Beam Position Register and 16-Bit Data Map

Transmit Common Gain SRAM, and Transmit or Receive SRAM

In beam pointer mode, in addition to the beam position registers, users must also define the transmit common SRAM registers and transmit or receive SRAM registers.

For transmit mode, gain is determined by both the channel gain and the common gain. For the ADMV4801, Register 0x400 to Register 0x4FF are assigned to store the transmit common gain settings (see Table 7). The beam pointer uses the index to recall the common gain settings. The registers are eight bits wide but only five bits are used. Table 5 is the truth table for the actual gain levels from 0 dB to 17 dB in increments of 1 dB.

Similarly, for ADMV4821, transmit common gain settings, Register 0x400 to Register 0x4FF, are assigned to vertical channels, and Register 0x500 to Register 0x5FF are assigned to horizontal channels (see Table 7).

The transmit common gain SRAM registers are global registers, regardless of page selection.

To write to transmit common gain settings registers, use the following procedure (note that this procedure uses Register 0x400 as an example):

1. Determine the hexadecimal value for the actual gain levels. For example, to set transmit common gain to 17 dB, the data must be 0x11.
2. Write to the registers (set Register 0x400 to 0x11).
3. Toggle the LOAD line three times. For the ADMV4821, toggle either the LOAD_V or the LOAD_H pin, as needed.

The transmit or receive SRAM specifies the mode of the beam position. Register 0x600 to Register 0x6FF store the transmit or receive settings (see Table 6). These registers are global registers, regardless of page selection.

For the ADMV4801, when Bits[1:0] = 'b11, the beam position is assigned to transmit mode, and 'b00 is assigned to receive mode.

For the ADMV4821, Bit 0 determines the vertical channels statuses and Bit 1 determines the horizontal channels statuses. When the bit value is 1, the beam position is assigned to transmit mode, and when the bit value is 0, the beam position is assigned to receive mode.

Table 5. Transmit Common Gain Value Truth Table

Gain Level (dB)	Data (Hex.)
0	00
1	01
2	02
3	03
4	04
5	05
6	06
7	07
8	08
9	09
10	0A
11	0B
12	0C
13	0D
14	0E
15	0F
16	10
17	11

Table 6. Transmit or Receive SRAM Registers

Register Address	Index	Mode[1:0]
0x600	0	User defined
0x601	1	User defined
…	…	…
0x6FF	255	User defined

Table 7. Transmit Common Gain SRAM Registers

Register Address	Index	Transmit Common Gain Data (Bits[4:0])	Register Address (for ADMV4821 Only)	Index (ADMV4821 Only)	Transmit Common Gain Data (Bits[4:0])
0x400	0	User defined	0x500	0	User defined
0x401	1	User defined	0x501	1	User defined
…	…	…	…	…	…
0x4FF	255	User defined	0x5FF	255	User defined

Beam Pointer Mode Programming Flowchart

Figure 7 shows the flowchart and register writes for beam pointer mode initialization. Page Select Register 0x013 and Register 0x14 write transactions (Register 0x13 = 0xFF and Register 0x14 = 0xFF) can be combined when continuously writing to all channels. Refer to the Register Information section for register functions and settings.

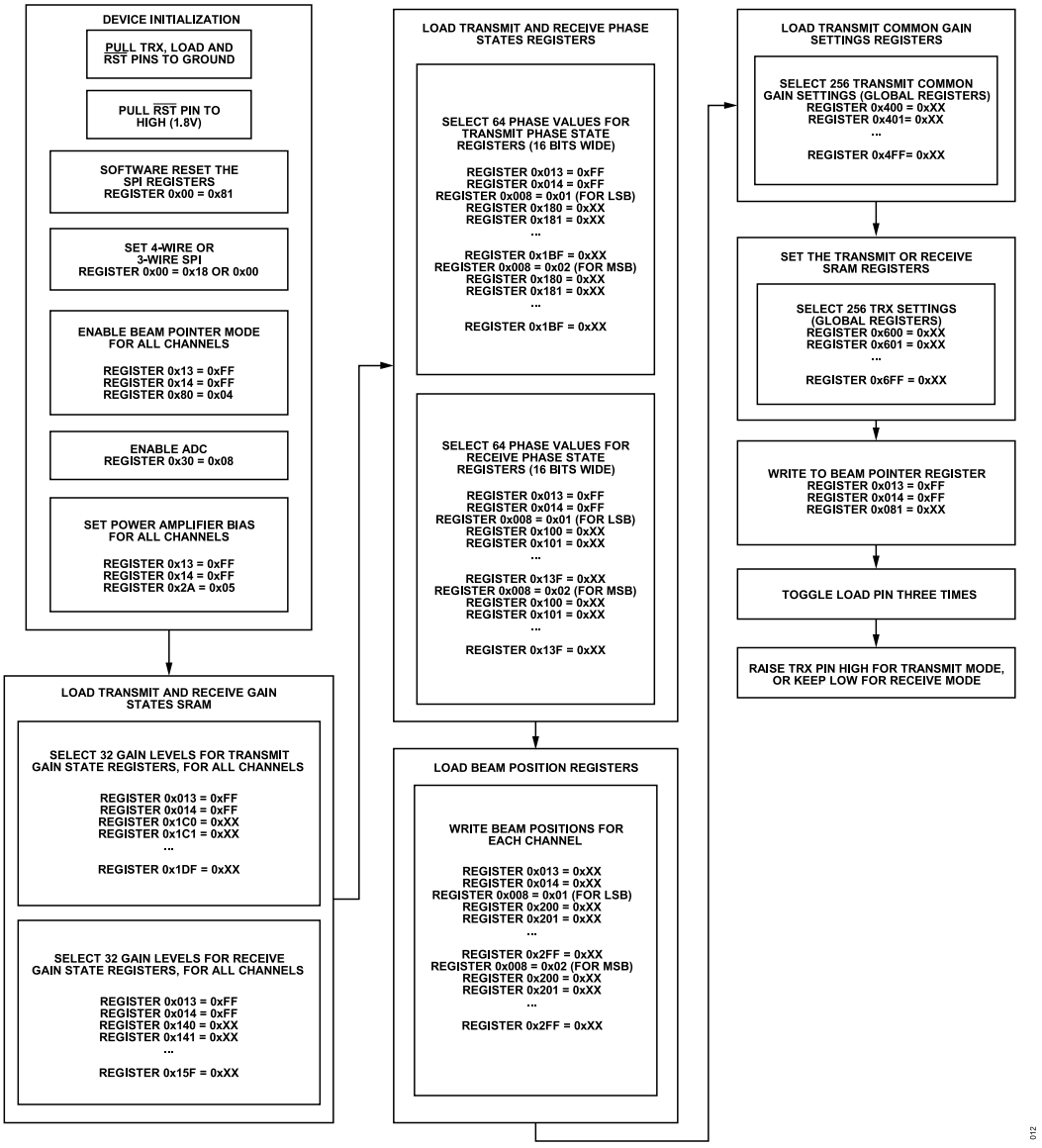

Figure 7. ADMV4801 Beam Pointer Mode Flowchart

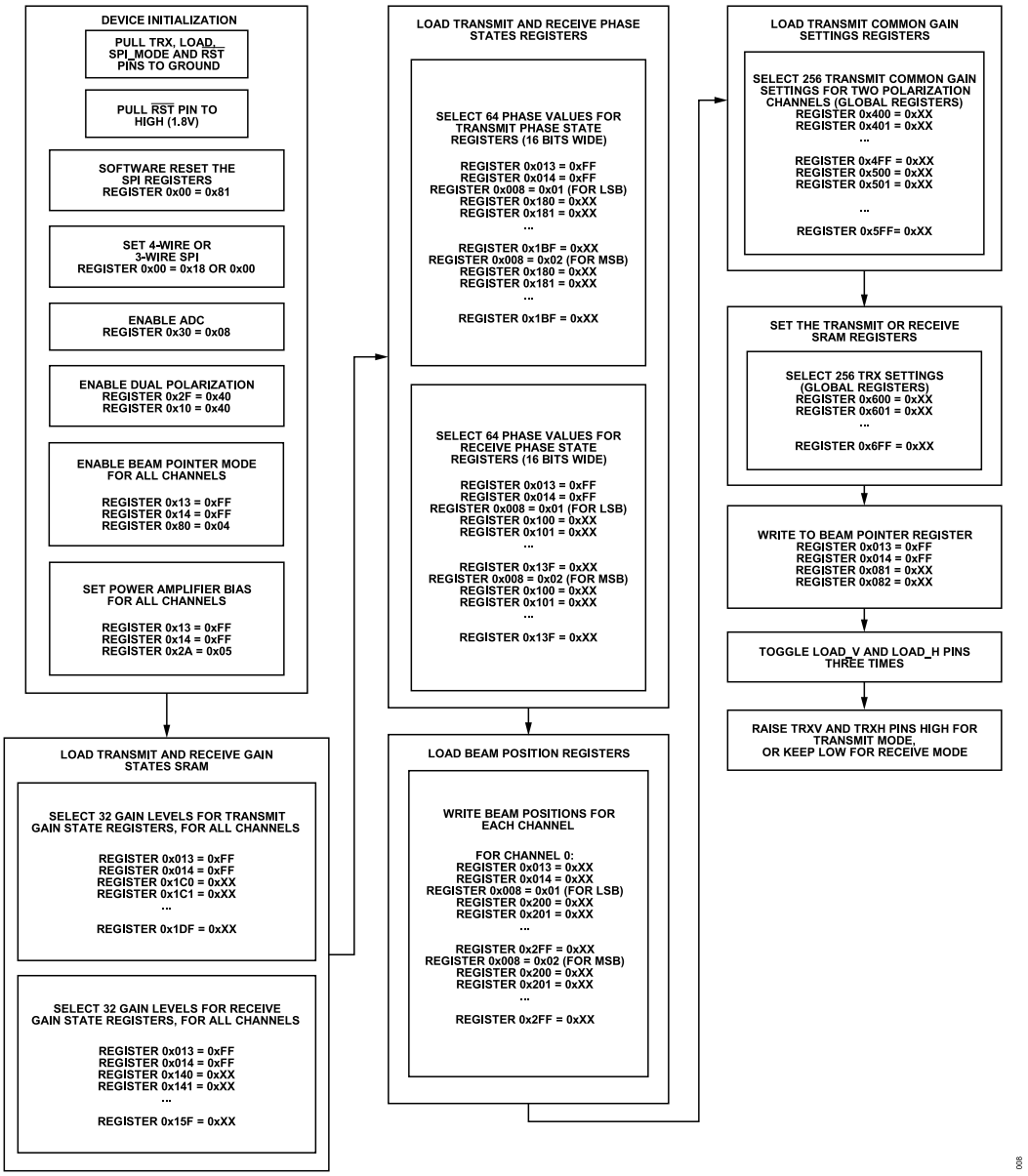

Figure 8. ADMV4821 Beam Pointer Mode Programming Flowchart

BYPASS MODE

Bypass mode (see Figure 3) bypasses the beam pointer, beam position SRAM, transmit common gain global SRAM, and transmit or receive global SRAM. Users directly program the settings for each channel. This method is straightforward and is recommended for evaluation to determine gain and phase settings for each channel. A group of registers enable bypass mode and send the settings to the device. Use the following procedure to use bypass mode:

1. Enable bypass mode by setting Paged Register 0x080 to 0x86.
2. Directly set the phase and gain settings using Register 0x86 for each channel. Register 0x86 is a 16-bit paged register. This register stores the phase and gain states index. Figure 9 shows the register bit map.
3. For the ADMV4801, directly set the transmit common gain settings by writing to Register 0x08E.

   For the ADMV4821, directly set the transmit common gain settings by writing to Register 0x08E (vertical channels) and Register 0x08F (horizontal channels). These registers are paged. The value is the hexadecimal representation of the common gain level shown in Table 5.
4. Directly set the transmit or receive mode by writing to Paged Register 0x85, Bits[6:5].

   For the ADMV4801, when Bits[6:5] = 'b11, the beam position is assigned to transmit mode, and 'b00 is assigned to receive mode.

   For the ADMV4821, Bit 5 determines the vertical channels statuses and Bit 6 determines the horizontal channels statuses.

When the bit value is 1, the beam position is assigned to transmit mode, and when the bit value is 0, the beam position is assigned to receive mode.

5. Set Register 0x081 to 0x00 for all channels. Register 0x081 must be written before toggling the LOAD pin and after changing any of the following registers: Register 0x085, Register 0x086, Register 0x08E, and Register 0x08F; otherwise, the bypass mode does not function.
6. Toggle the LOAD pin three times. For the ADMV4821, toggle either the LOAD_V or the LOAD_H pin, as needed.

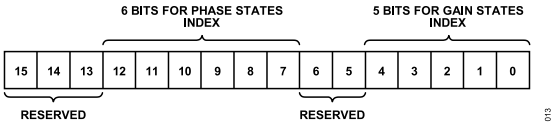

Figure 9. Register 0x86 Bit Map

Bypass Mode Programming Flowchart

Page Select Register 0x013 and Register 0x14 write transactions (Register 0x13 = 0xFF and Register 0x14 = 0xFF) can be combined when continuously writing to all channels. Refer to the Register Information section for register functions and settings.

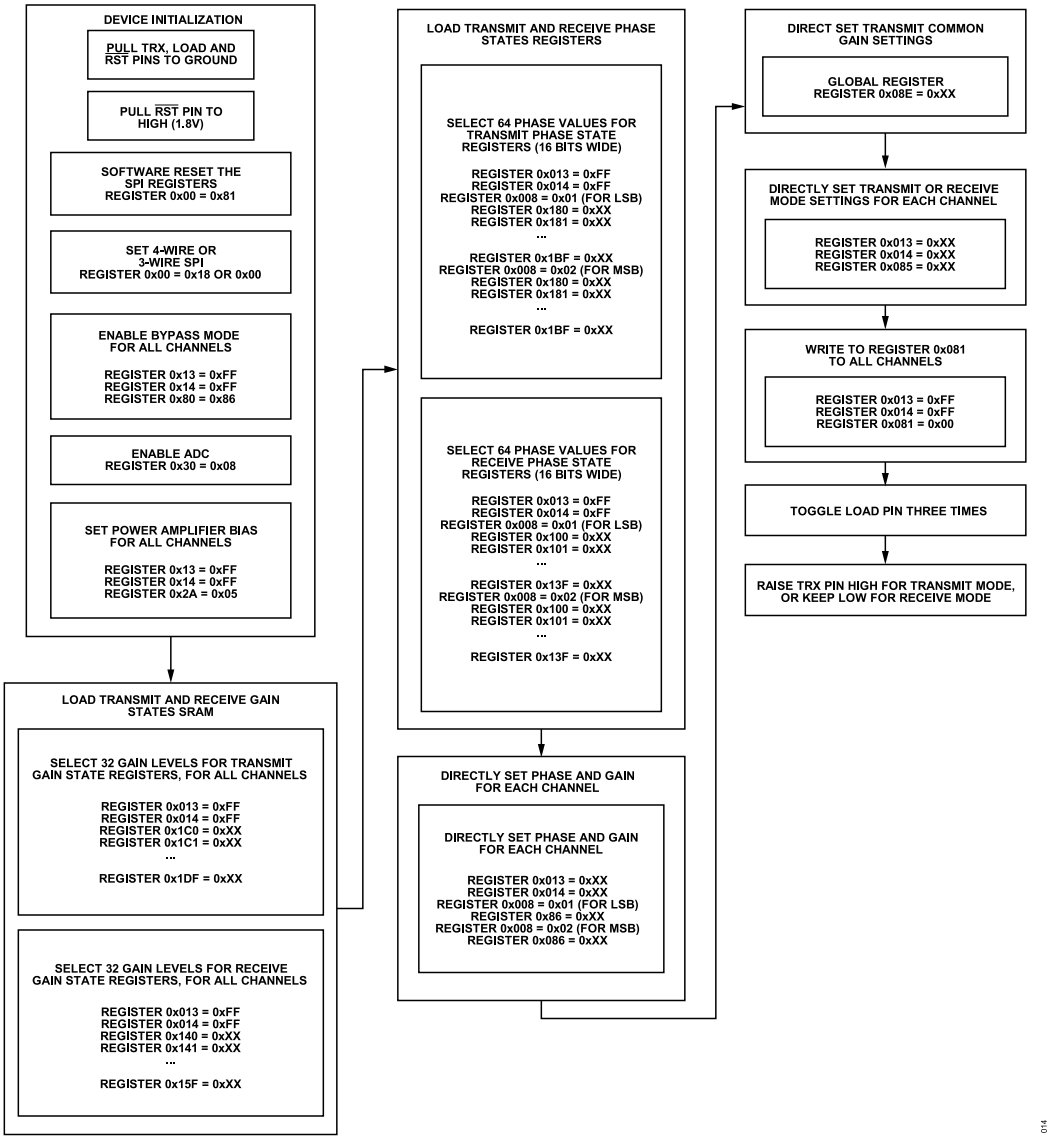

Figure 10. ADMV4801 Bypass Mode Flowchart

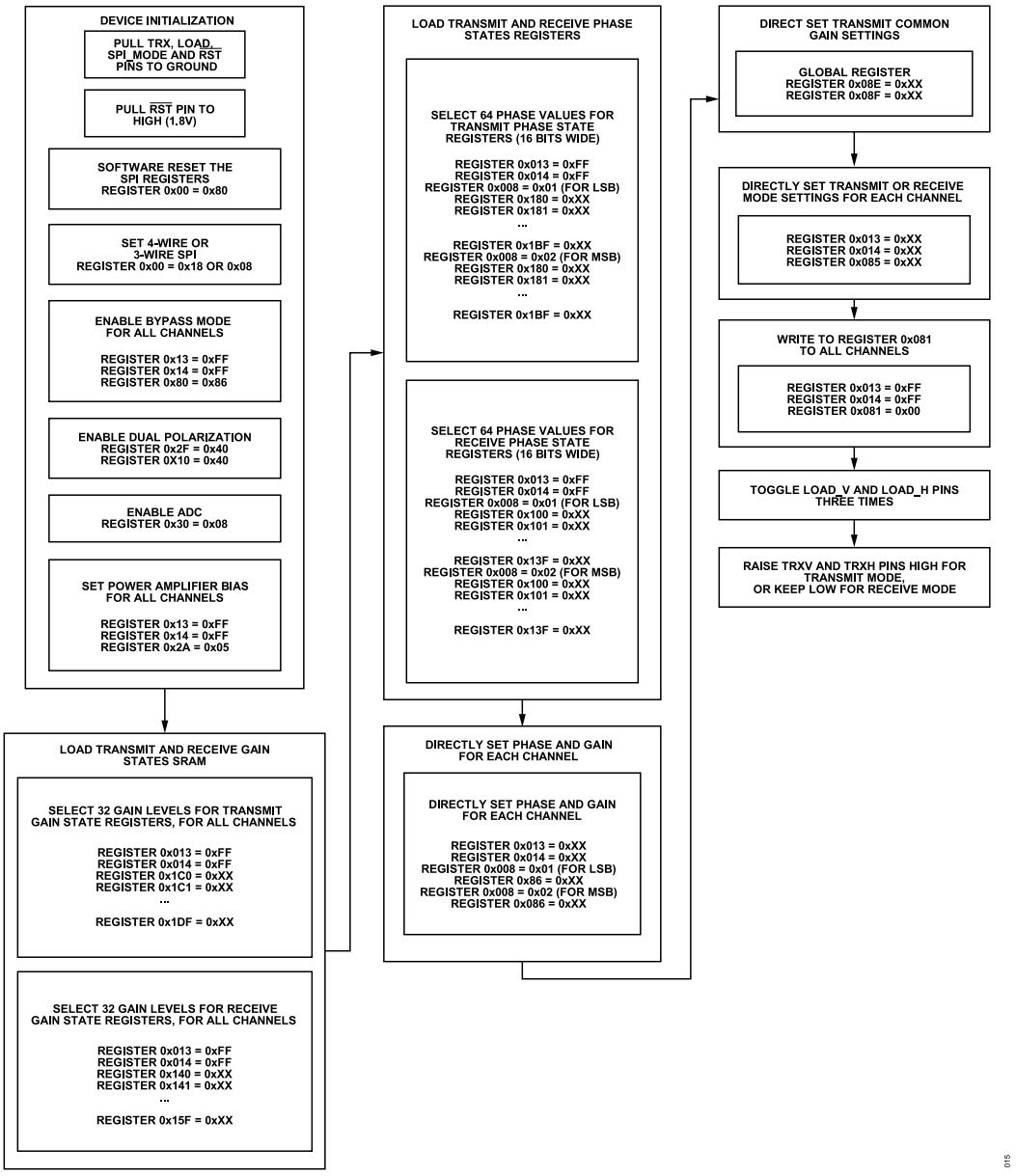

Figure 11. ADMV4821 Bypass Mode Flowchart

POWER-DOWN, POWER DETECTOR, AND TEMPERATURE SENSOR

The ADMV4801/ADMV4821 feature an on-chip temperature sensor and power detectors, which route to the on-chip ADC that provides SPI readback with eight bits of resolution. The ADC works in transmit mode only but can be read back in receive mode. Therefore, the temperature sensor and power detector data reflect the last transmit mode status only.

POWER DOWN

For transmit mode, use Page Select Register 0x013 and Register 0x014, together with Register 0x026, Bit 7, Register 0x027, Bit 7, and Register 0x028, Bit 7, to power down the corresponding channel. LOAD pin toggling is needed for the power-down function to take effect.

POWER DETECTOR

There are 16 power detectors (1 per transmitter channel) that sample the peak power coupled from the output of each power amplifier. These power detectors provide power monitoring and calibration for channel gain, as well as channel to channel gain mismatch. The power range of the power detector is programmable and can adjust the input power sense window from −15 dBm to +16 dBm. Register 0x40 to Register 0x4F are the readback registers for the power detectors from Channel 0 to Channel 15.

Refer to the ADMV4801 and ADMV4821 data sheets for power detector characteristic plots.

Use the following sequence to read back from the power detector:

1. Set Register 0x030 to 0x08 to enable the ADC clock.
2. Select the detector range for each channel by writing to Paged Register 0x027. Table 8 is the truth table for the register settings and power range. The information in this table is an approximate range division and may vary from device to device.
3. Read back the values in Register 0x40 to Register 0x4F.

Table 8. Register 0x027 Detector Range Truth Table

Range Index	Register 0x027, Bit 6 and Bits[2:0]	Power Range (dBm)
6	'b0110	−15 to −2
7	'b0111	−13 to 0
4	'b0100	−10 to +2
5	'b0101	−8 to +5
2	'b0010	−5 to +7
3	'b0011	−3 to +8
0	'b0000	0 to 11
8	'b1000	2 to 13
9	'b1001	5 to 16

TEMPERATURE SENSOR

The temperature sensor can sense from −40°C to +125°C. To convert the on-chip temperature sensor readback values to Celsius, use the following equation:

Case Temperature (°C) = 1.07 × (*Temperature Sensor Value in Decimal)* − 96

The temperature sensor value can be read back only when in transmit mode. Register 0x50 is used to read back the temperature sensor reading.

Use the following sequence to read back from the temperature sensor:

1. Set Register 0x030 to 0x08 to enable the ADC clock.
2. Read back from Register 0x50.

REGISTER INFORMATION

REGISTER SUMMARY

Table 9. ADMV4801/ADMV4821 Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset/ Startup	Values Cleared on Soft/ Hard Reset	Paging Required	LD Toggle Required	R/W
0x000	SPI_ CONFIG_1	[7:0]	SOFT_ RESET	LSB_ FIRST	ADDR_ ASCN	SDO_ ACTIVE	SDO_ ACTIVE_	ADDR_ ASCN_	LSB_ FIRST_	SOFT_ RESET_	0x00	Yes	No	No	R/W
0x003	CHIP_TYPE	[7:0]	Reserved				CHIP_TYPE				0x01	Yes	No	No	R
0x004	PRODUCT_ ID_LOWER	[7:0]	PRODUCT_ID[7:0]								0x44[1]	Yes	No	No	R
0x005	PRODUCT_ ID_UPPER	[7:0]	PRODUCT_ID[15:8]								0x00	Yes	No	No	R
0x008	MSB_LSB_ SELECT	[7:0]	Reserved						MSB_LSB_ SELECT		0x00	Yes	No	No	R/W
0x00A	SCRATCH_ PAD	[7:0]	SCRATCH_PAD								0x00	Yes	No	No	R/W
0x00C	VENDOR_ ID_LOWER	[7:0]	VENDOR_ID[7:0]								0x56	Yes	No	No	R
0x00D	VENDOR_ ID_UPPER	[7:0]	VENDOR_ID[15:8]								0x04	Yes	No	No	R
0x010	CMD_ TYPE (for ADMV4821 only)	[7:0]	Reserved	ADI_ DUAL_ POL	Reserved						0x00	Yes	No	No	R/W
0x012	Bandgap	[7:0]	Reserved							BGR_ ENABLE	0xBF	Yes	Yes	Yes	R/W
0x013	PAGE_ SELECT_ LOWER	[7:0]	CHS[7:0]								0xFF	Yes	No	No	R/W
0x014	PAGE_ SELECT_ UPPER	[7:0]	CHS[15:8]								0xFF	Yes	No	No	R/W
0x023	RX_ CHANNEL_ CONTROLS	[7:0]	Reserved	PD_ RX_ LNA2	PD_ RX_ LNA1	Reserved	LNA2_ ATTENUATION		Reserved		0x02	Yes	Yes	Yes	R/W
0x026	TX_ CHANNEL_ CONTROLS	[7:0]	PD_ PA[0]	Reserved							0x19	Yes	Yes	Yes	R/W
0x027	TX_ DETECTOR_ CHANNEL_ CONTROLS	[7:0]	PD_ PA[1]	TX_SQ_ DET_ SET TINGS [3]	Reserved			TX_SQ_DET_ SETTINGS[2:0]			0x40	Yes	Yes	Yes	R/W
0x028	TX_ CHANNEL_ CONTROLS_ 1	[7:0]	PD_ PA[2]	Reserved							0x31	Yes	Yes	Yes	R/W

Table 9. ADMV4801/ADMV4821 Register Summary (Continued)

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset/ Startup	Values Cleared on Soft/ Hard Reset	Paging Re-quired	LD Tog-gle Re-quired	R/W
0x029	TX_PA_ CHANNEL_ CONTROLS_ 1	[7:0]	Reserved			PA_BIAS_2			PA_BIAS_1		0x65	Yes	Yes	Yes	R/W
0x02A	TX_PA_ CHANNEL_ CONTROLS_ 2	[7:0]	Reserved			PA_ VCC_ SEL		PA_BIAS_3			0x0A	Yes	Yes	Yes	R/W
0x02B	TX_VGA_ COMMON_ GAIN_ CHANNEL_ CONTROLS	[7:0]	Reserved			COMMON_GAIN_OFFSET				COM-MON_ GAIN_ CTRL_ VGA_ SELECT	0x00	Yes	Yes	No	R/W
0x02F	COMMON_ GAIN_ POL (for ADMV4821 only)	[7:0]	Reserved	COM-MON_ GAIN_ POL_ SEL		Reserved					0x00	Yes	No	No	R/W
0x030	ADC_CLK	[7:0]	Reserved				ADC_ CLK_EN	Reserved			0x00	Yes	No	No	R/W
0x040	POWER_ CH0	[7:0]	POWER_CH0								0x00	Yes	No	No	R
0x041	POWER_ CH1	[7:0]	POWER_CH1								0x00	Yes	No	No	R
0x042	POWER_ CH2	[7:0]	POWER_CH2								0x00	Yes	No	No	R
0x043	POWER_ CH3	[7:0]	POWER_CH3								0x00	Yes	No	No	R
0x044	POWER_ CH4	[7:0]	POWER_CH4								0x00	Yes	No	No	R
0x045	POWER_ CH5	[7:0]	POWER_CH5								0x00	Yes	No	No	R
0x046	POWER_ CH6	[7:0]	POWER_CH6								0x00	Yes	No	No	R
0x047	POWER_ CH7	[7:0]	POWER_CH7								0x00	Yes	No	No	R
0x048	POWER_ CH8	[7:0]	POWER_CH8								0x00	Yes	No	No	R
0x049	POWER_ CH9	[7:0]	POWER_CH9								0x00	Yes	No	No	R
0x04A	POWER_ CH10	[7:0]	POWER_CH10								0x00	Yes	No	No	R
0x04B	POWER_ CH11	[7:0]	POWER_CH11								0x00	Yes	No	No	R

Table 9. ADMV4801/ADMV4821 Register Summary (Continued)

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset/ Startup	Values Cleared on Soft/ Hard Reset	Paging Re-quired	LD Tog-gle Re-quired	R/W
0x04C	POWER_ CH12	[7:0]	POWER_CH12								0x00	Yes	No	No	R
0x04D	POWER_ CH13	[7:0]	POWER_CH13								0x00	Yes	No	No	R
0x04E	POWER_ CH14	[7:0]	POWER_CH14								0x00	Yes	No	No	R
0x04F	POWER_ CH15	[7:0]	POWER_CH15								0x00	Yes	No	No	R
0x050	Temperature	[7:0]	TEMP								0x00	Yes	No	No	R
0x080	SRAM_ BYPASS	[7:0]	SRAM_ BY PASS_ REG_ 0X086	Reserved				AUTO-MATIC _BY-PASS_ MODE	SRAM_ BY-PASS_ COM-MON_ GAIN	Reserved	0x82	Yes	Yes	Yes	R/W
0x081	Beam pointer (V)	[7:0]	BEAM_POINTER (BEAM_POINTER_V for ADMV4821)								0x00	Yes	Yes	Yes	R/W
0x082	BEAM-POINTER_H	[7:0]	BEAM_POINTER_H (for ADMV4821 only)								0x00	Yes	Yes	Yes	R/W
0x085	BYPASS_ TRX_PRO-GRAM_ SRAM	[7:0]	Reserved	BYPASS_TRX_ PROGRAM_ SRAM_VALUE		Reserved					0x00	Yes	Yes	Yes	R/W
0x086	BYPASS_ BEAM-POSITION_ SRAM	[7:0]	GAIN_PHASE_BYPASS_BEAMPOSITION_SRAM_VALUES								0x00	Yes	Yes	Yes	R/W
0x08E	BYPASS_ COMMON_ GAIN_ SRAM(V)	[7:0]	COMMON_GAIN_BYPASS_VALUE (COMMON_GAIN_BYPASS_VALUE_V for ADMV4821)								0x11	Yes	No	Yes	R/W
0x08F	BYPASS_ COMMON_ GAIN_S RAM_H	[7:0]	COMMON_GAIN_BYPASS_VALUE_H (for ADMV4821 only)								0x11	Yes	No	Yes	R/W
0x100 to 0x13F	RX_ PHASE_ SRAM_x	[7:0]	RX_PHASE_SRAM_x								0x00	No	Yes	Yes	R/W
0x140 to 0x15F	RX_ GAIN_ SRAM_x	[7:0]	RX_GAIN_SRAM_x								0x00	No	Yes	Yes	R/W
0x180 to 0x1BF	TX_ PHASE_ SRAM_x	[7:0]	TX_PHASE_SRAM_x								0x00	No	Yes	Yes	R/W
0x1C0	TX_	[7:0]	TX_GAIN_SRAM_x								0x00	No	Yes	Yes	R/W

Table 9. ADMV4801/ADMV4821 Register Summary (Continued)

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset/ Startup	Values Cleared on Soft/ Hard Reset	Paging Re- quired	LD Tog- gle Re- quired	R/W
to 0x1DF	GAIN_ SRAM_x														
0x200 to 0x2FF	BEAM_ POSITION_ SRAM_x	[7:0]	BEAM_POSITION_SRAM_x								0x00	No	Yes	Yes	R/W
0x400 to 0x4FF	COMMON_ GAIN_ SRAM_ x(V)	[7:0]	COMMON_GAIN_SRAM_x (COMMON_GAIN_SRAM_x_V for ADMV4821)								0x00	Yes[2]	No	Yes	R/W
0x500 to 0x5FF	COMMON_ GAIN_ SRAM_x_H	[7:0]	COMMON_GAIN_SRAM_x_H (for ADMV4821 only)								0x00	Yes[2]	No	Yes	R/W
0x600 to 0x6FF	TRX_ PROGRAM_ SRAM_x	[7:0]	Reserved						TX_RX_ PROGRAM_ SRAM_x		0x00	Yes[2]	No	Yes	R/W

[1] Reset/startup value for Register 0x004 is 0x46 for the ADMV4821.

[2] Values cleared on hardware reset only.

REGISTER DETAILS

Address: 0x000, Reset: 0x00, Name: SPI_CONFIG_1

Table 10. Bit Descriptions for SPI_CONFIG_1

Bits	Bit Name	Settings	Description	Reset	Access
7	SOFT_RESET		Soft reset. Automatic clearing.	0x0	R/W
		0	Reset asserted.		
		1	Reset not asserted.		
6	LSB_FIRST		LSB first bit.	0x0	R/W
		0	LSB first.		
		1	MSB first.		
5	ADDR_ASCN		In streaming mode, set the sequential address order to ascending or descending.	0x0	R/W
		0	Descending.		
		1	Ascending.		
4	SDO_ACTIVE		4-wire SPI enable bit.	0x0	R/W
		0	3-wire SPI.		
		1	4-wire SPI.		
3	SDO_ACTIVE_		Mirror of Bit 4. Set to the same value as Bit 4.	0x0	R/W
2	ADDR_ASCN_		Mirror of Bit 5. Set to the same value as Bit 5.	0x0	R/W
1	LSB_FIRST_		Mirror of Bit 6. Set to the same value as Bit 6.	0x0	R/W
0	SOFT_RESET_		Mirror of Bit 7. Set to the same value as Bit 7.	0x0	R/W

Address: 0x003, Reset: 0x00, Name: CHIP_TYPE

Table 11. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	Reserved		Reserved.	0x0	R
[3:0]	CHIP_TYPE		Chip type bits. Read only.	0x0	R

Address: 0x004, Reset: 0x00, Name: PRODUCT_ID_LOWER

Table 12. Bit Descriptions for PRODUCT_ID_LOWER

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]		Product ID. Read only.	0x0	R

Address: 0x005, Reset: 0x00, Name: PRODUCT_ID_UPPER

Table 13. Bit Descriptions for PRODUCT_ID_UPPER

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]		Product ID. Read only.	0x0	R

Address: 0x008, Reset: 0x01, Name: MSB_LSB_SELECT

Table 14. Bit Descriptions for MSB_LSB_SELECT

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	Reserved		Reserved.	0x0	R
[1:0]	ADDRESS_SELECT		Identifies when addressing 8 MSBs or 8 LSBs for 16-bit wide registers.	0x1	R/W
		10	Access MSB.		
		01	Access LSB.		

Address: 0x00A, Reset: 0x00, Name: SCRATCH_PAD

Table 15. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SCRATCH_PAD		Scratch pad.	0x0	R/W

Address: 0x00C, Reset: 0x00, Name: VENDOR_ID_LOWER

Table 16. Bit Descriptions for VENDOR_ID_LOWER

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR_ID[7:0]		Vendor ID. Read only.	0x0	R

Address: 0x00D, Reset: 0x00, Name: VENDOR_ID_UPPER

Table 17. Bit Descriptions for VENDOR_ID_UPPER

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR_ID[15:8]		Vendor ID. Read only.	0x0	R

Address: 0x010, Reset: 0x00, Name: CMD_TYPE

Table 18. Bit Descriptions for CMD_TYPE

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved.	0x0	R
6	ADI_DUAL_POL	Enables dual polarization beam pointers. For ADMV4821 only.	0x0	R/W

Table 18. Bit Descriptions for CMD_TYPE (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Independent Beam Pointers Register 0x081, Register 0x082. 0: Register0x082 beam pointer follows Register 0x081.		

Address: 0x012, Reset: 0xBF, Name: Bandgap

Table 19. Bit Descriptions for Bandgap

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	Reserved		Reserved.	0x5F	R/W
0	BGR_ENABLE		BGR enable.	0x1	R/W

Address: 0x013, Reset: 0xFF, Name: PAGE_SELECT_LOWER

Table 20. Bit Descriptions for PAGE_SELECT_LOWER

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CHS[7:0]		Selects which channels to page. Channel 0 to Channel 15.	0xFF	R/W

Address: 0x014, Reset: 0xFF, Name: PAGE_SELECT_UPPER

Table 21. Bit Descriptions for PAGE_SELECT_UPPER

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CHS[15:8]		Selects which channels to page. Channel 0 to Channel 15.	0xFF	R/W

Address: 0x023, Reset: 0x02, Name: RX_CHANNEL_CONTROLS

Table 22. Bit Descriptions for RX_CHANNEL_CONTROLS

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		Reserved.	0x0	R/W
6	PD_RX_LNA2		Power down receive LNA2.	0x0	R/W
		1	Power down.		
		0	Power up.		
5	PD_RX_LNA1		Power down receive LNA1.	0x0	R/W
		1	Power down.		
		0	Power up.		
4	Reserved		Reserved	0x0	R/W
[3:2]	LNA2_ATTENUATION		LNA attenuation by 1 dB.	0x0	R/W
		11	2 dB attenuation.		
		00	0 dB attenuation.		
[1:0]	RESERVED[2:1]		Reserved.	0x2	R/W

Address: 0x026, Reset: 0x19, Name: TX_CHANNEL_CONTROLS

Table 23. Bit Descriptions for TX_CHANNEL_CONTROLS

Bits	Bit Name	Settings	Description	Reset	Access
7	PD_PA[0]	Register 0x28, Bit 7, Register 0x27, Bit 7, Register 0x26, Bit 7	Power-down of the power amplifier, works in conjunction with Register 0x27, Bit 7 and Register 0x28, Bit 7.	0x0	R/W
		111	Powers down the power amplifier.		
		000	Powers up the power amplifier.		
[6:0]	Reserved		Reserved.	0x65	R/W

Address: 0x027, Reset: 0x40, Name: TX_DETECTOR_CHANNEL_CONTROLS

Table 24. Bit Descriptions for TX_DETECTOR_CHANNEL_CONTROLS

Bits	Bit Name	Settings	Description	Reset	Access
7	PD_PA[1]	Register 0x28, Bit 7, Register 0x27, Bit 7, Register 0x26, Bit 7	Power-down of the power amplifier, works in conjunction with Register 0x26, Bit 7 and Register 0x28, Bit 7.	0x0	R/W
		111	Powers down the power amplifier.		
		000	Powers up the power amplifier.		
6	TX_SQ_DET_SETTINGS[3]	Bit 6, Bits[2:0]	Detector input range select, works in conjunction with Bits[2:0], MSB first.	0x1	R/W
		0110	−15 dBm to −2 dBm.		
		0111	−13 dBm to 0 dBm.		
		0100	−10 dBm to +2 dBm.		
		0101	−8 dBm to +5 dBm.		
		0010	−5 dBm to +7 dBm.		
		0011	−3 dBm to +8 dBm.		
		0000	0 dBm to 11 dBm.		
		1000	2 dBm to 13 dBm.		
		1001	5 dBm to 16 dBm.		
[5:3]	Reserved		Reserved.	0x0	R/W
[2:0]	TX_SQ_DET_SETTINGS[2:0]	Bit 6, Bits[2:0]	Detector input range select, works in conjunction with Bit 6.	0x0	R/W
		0110	−15 dBm to −2 dBm.		
		0111	−13 dBm to 0 dBm.		
		0100	−10 dBm to +2 dBm.		
		0101	−8 dBm to +5 dBm.		
		0010	−5 dBm to +7 dBm.		
		0011	−3 dBm to +8 dBm.		
		0000	0 dBm to 11 dBm.		
		1000	2 dBm to 13 dBm.		
		1001	5 dBm to 16 dBm.		

Address: 0x028, Reset: 0x31, Name: TX_CHANNEL_CONTROLS_1

Table 25. Bit Descriptions for TX_CHANNEL_CONTROLS_1

Bits	Bit Name	Settings	Description	Reset	Access
7	PD_PA[2]	Register 0x28, Bit 7, Register 0x27, Bit 7, Register 0x26, Bit 7	Power-down of the power amplifier, works in conjunction with Register 0x26, Bit 7 and Register 0x27, Bit 7.	0x0	R/W
		111	Powers down the power amplifier.		
		000	Powers up the power amplifier.		
[6:0]	Reserved		Reserved.	0x31	R/W

Address: 0x029, Reset: 0x65, Name: TX_PA_CHANNEL_CONTROLS_1

Table 26. Bit Descriptions for TX_PA_CHANNEL_CONTROLS_1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	Reserved		Reserved.	0x1	R/W
[5:3]	PA_BIAS_2		Transmit the power amplifier bias, value of 0x04 recommended.	0x4	R/W
[2:0]	PA_BIAS_1		Transmit the power amplifier bias, value of 0x05 recommended.	0x5	R/W

Address: 0x02A, Reset: 0x0A, Name: TX_PA_CHANNEL_CONTROLS_2

Table 27. Bit Descriptions for TX_PA_CHANNEL_CONTROLS_2

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	Reserved		Reserved.	0x0	R/W
4	PA_VCC_SEL		3.3 V vs. 2.5 V mode.	0x0	R/W
		0	3.3 V mode for chip.		
		1	2.5 V mode for chip.		
[3:0]	PA_BIAS_3		Transmit the power amplifier bias, value of 0x05 recommended.	0xA	R/W

Address: 0x02B, Reset: 0x00, Name: TX_VGA_COMMON_GAIN_CHANNEL_CONTROLS

Table 28. Bit Descriptions for TX_VGA_COMMON_GAIN_CHANNEL_CONTROLS

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	Reserved		Reserved.	0x0	R
[5:1]	COMMON_GAIN_OFFSET		Transmitter common gain offset. Step size = 1 dB. Minor tweak for transmit common gain settings.	0x0	R/W
0	COMMON_GAIN_CTRL_VGA_SELECT		Select DVGA 1 or DVGA 2 for transmit common gain.	0x0	R/W
		0	Select DVGA 2.		
		1	Select DVGA 1.		

Address: 0x02F, Reset: 0x00, Name: COMMON_GAIN_POL

Table 29. Bit Descriptions for COMMON_GAIN_POL

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved.	0x0	R
6	COMMON_GAIN_POL_SEL	Common gain polarization enable bit. For ADMV4821 only. 0: horizontal channel gain is ignored, and all channels use common gain vertical common gain values. 1: horizontal and vertical channels have separate common gain values	0x0	R/W
[5:0]	Reserved	Reserved.	0x0	R/W

Address: 0x030, Reset: 0x00, Name: ADC_CLK

Table 30. Bit Descriptions for ADC_CLK

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	Reserved		Reserved.	0x0	R
3	ADC_CLK_EN		Enable ADC clock.	0x0	R/W
		1	Enable ADC clock.		
		0	Disable ADC clock.		
[2:0]	Reserved		Reserved.	0x0	R/W

Address: 0x040, Reset: 0x00, Name: POWER_CH0

Table 31. Bit Descriptions for POWER_CH0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH0		Channel power detector readback for Channel 0.	0x0	R

Address: 0x041, Reset: 0x00, Name: POWER_CH1

Table 32. Bit Descriptions for POWER_CH1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH1		Channel power detector readback for Channel 1.	0x0	R

Address: 0x042, Reset: 0x00, Name: POWER_CH2

Table 33. Bit Descriptions for POWER_CH2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH2		Channel power detector readback for Channel 2.	0x0	R

Address: 0x043, Reset: 0x00, Name: POWER_CH3

Table 34. Bit Descriptions for POWER_CH3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH3		Channel power detector readback for Channel 3.	0x0	R

Address: 0x044, Reset: 0x00, Name: POWER_CH4

Table 35. Bit Descriptions for POWER_CH4

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH4		Channel power detector readback for Channel 4.	0x0	R

Address: 0x045, Reset: 0x00, Name: POWER_CH5

Table 36. Bit Descriptions for POWER_CH5

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH5		Channel power detector readback for Channel 5.	0x0	R

Address: 0x046, Reset: 0x00, Name: POWER_CH6

Table 37. Bit Descriptions for POWER_CH6

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH6		Channel power detector readback for Channel 6.	0x0	R

Address: 0x047, Reset: 0x00, Name: POWER_CH7

Table 38. Bit Descriptions for POWER_CH7

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH7		Channel power detector readback for Channel 7.	0x0	R

Address: 0x048, Reset: 0x00, Name: POWER_CH8

Table 39. Bit Descriptions for POWER_CH8

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH8		Channel power detector readback for Channel 8.	0x0	R

Address: 0x049, Reset: 0x00, Name: POWER_CH9

Table 40. Bit Descriptions for POWER_CH9

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH9		Channel power detector readback for Channel 9.	0x0	R

Address: 0x04A, Reset: 0x00, Name: POWER_CH10

Table 41. Bit Descriptions for POWER_CH10

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH10		Channel power detector readback for Channel 10.	0x0	R

Address: 0x04B, Reset: 0x00, Name: POWER_CH11

Table 42. Bit Descriptions for POWER_CH11

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH11		Channel power detector readback for Channel 11.	0x0	R

Address: 0x04C, Reset: 0x00, Name: POWER_CH12

Table 43. Bit Descriptions for POWER_CH12

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH12		Channel power detector readback for Channel 12.	0x0	R

Address: 0x04D, Reset: 0x00, Name: POWER_CH13

Table 44. Bit Descriptions for POWER_CH13

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH13		Channel power detector readback for Channel 13.	0x0	R

Address: 0x04E, Reset: 0x00, Name: POWER_CH14

Table 45. Bit Descriptions for POWER_CH14

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH14		Channel power detector readback for Channel 14.	0x0	R

Address: 0x04F, Reset: 0x00, Name: POWER_CH15

Table 46. Bit Descriptions for POWER_CH15

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	POWER_CH15		Channel power detector readback for Channel 15.	0x0	R

Address: 0x050, Reset: 0x00, Name: Temperature

Table 47. Bit Descriptions for Temperature

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	TEMP		Temperature readback.	0x0	R

Address: 0x080, Reset: 0x82, Name: SRAM_BYPASS

Table 48. Bit Descriptions for SRAM_BYPASS

Bits	Bit Name	Settings	Description	Reset	Access
7	SRAM_BYPASS_REG_0X086		Bypass beam pointer mode.	0x1	R/W
		1	Use bypass mode.		
		0	Use beam pointer mode.		
[6:3]	Reserved		Reserved.	0x0	R/W
2	AUTOMATIC_BYPASS_MODE		Set this bit to 1 for proper operation.	0x0	R/W

Table 48. Bit Descriptions for SRAM_BYPASS (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
1	SRAM_BYPASS_COMMON_GAIN		Select Bit 1 to bypass the transmit common gain SRAM.	0x1	R/W
		1	Bypass the transmit common gain SRAM for bypass mode.		
		0	Use transmit common gain SRAM for beam pointer mode.		
0	Reserved		Reserved.	0x0	R

Address: 0x081, Reset: 0x00, Name: Beam pointer (ADMV4801) or BEAMPOINTER_V (ADMV4821)

Table 49. Bit Descriptions for Beam Pointer

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	BEAM_POINTER[1]		Beam pointer. For ADMV4821, this bit is named BEAM_POINTER_V, for vertical channel beam pointer.	0x0	R/W

[1] For ADMV4821, the beam pointer register name is BEAMPOINTER_V and the bit name is BEAM_POINTER_V. For ADMV4801, there is a single beam pointer register (beam pointer) and bit (BEAM_POINTER).

Address: 0x082, Reset: 0x00, Name: BEAMPOINTER_H

Table 50. Bit Descriptions for BEAMPOINTER_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	BEAM_POINTER_H		Horizontal channel beam pointer. For ADMV4821 only.	0x0	R/W

Address: 0x085, Reset: 0x00, Name: BYPASS_TRX_PROGRAM_SRAM

Table 51. Bit Descriptions for BYPASS_TRX_PROGRAM_SRAM

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		Reserved.	0x0	R
[6:5]	BYPASS_TRX_PROGRAM_SRAM_VALUE		Transmit and receive settings in bypass mode. For ADMV4801, directly set the transmit and receive mode by writing to Paged Register 0x85, Bits[6:5]. When Bits[6:5] = 'b11, the beam position is assigned to transmit mode. When Bits[6:5] = 'b00, the beam position is assigned to receive mode. For ADMV4821, directly set the transmit and receive mode by writing to Register 0x85 Bit 5 for the vertical channels and to Bit 6 for the horizontal channels status. When the bit value is 1, the beam position is assigned to transmit mode, and when the bit value is 0, the beam position is assigned to receive mode.	0x0	R/W
[4:0]	Reserved		Reserved.	0x0	R

Address: 0x086, Reset: 0x00, Name: BYPASS_BEAMPOSITION_SRAM

Table 52. Bit Descriptions for BYPASS_BEAMPOSITION_SRAM

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	GAIN_PHASE_BYPASS_BEAMPOSITION_SRAM_VALUES		Phase and gain settings in bypass mode, 16 bits wide. Use Address Select Register 0x08 to access. Bits[15:13] are reserved, Bits[12:7] are phase states index, Bits[6:5] are reserved, and Bits[4:0] are gain states index.	0x0	R/W

Address: 0x08E, Reset: 0x11, Name: BYPASS_COMMON_GAIN_SRAM

Table 53. Bit Descriptions for BYPASS_COMMON_GAIN_SRAM

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	COMMON_GAIN_BYPASS_VALUE(V)		Transmit common gain settings in bypass mode. Sets vertical channels for ADMV4821.	0x11	R/W

Address: 0x08F, Reset: 0x11, Name: COMMON_GAIN_BYPASS_VALUE_H

Table 54. Bit Descriptions for COMMON_GAIN_BYPASS_VALUE_H

Bits	Bit Name	Description	Reset	Access
[7:0]	COMMON_GAIN_BYPASS_VALUE_H	Transmit common gain settings in bypass mode for horizontal channels. For ADMV4821 only.	0x11	R/W

Address: 0x100 to 0x13F, Reset: 0x00, Name: RX_PHASE_SRAM_x

Table 55. Bit Descriptions for RX_PHASE_SRAM_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	RX_PHASE_SRAM_x		Receive phase SRAM registers, 16 bits wide. Use Address Select Register 0x08. For read, the read command must be sent twice to read back.	0x0	R/W

Address: 0x140 to 0x15F, Reset: 0x00, Name: RX_GAIN_SRAM_x

Table 56. Bit Descriptions for RX_GAIN_SRAM_x

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	RX_GAIN_SRAM_x		Receive gain SRAM registers, eight bits wide. For read, the read command must be sent twice to read back.	0x0	R/W

Address: 0x180 to 0x1BF, Startup: 0x00, Name: TX_PHASE_SRAM_x

Table 57. Bit Descriptions for TX_PHASE_SRAM_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	TX_PHASE_SRAM_x		Transmit phase SRAM registers, 16 bits wide. Use Address Select Register 0x08. For read, the read command must be sent twice to read back.	0x0	R/W

Address: 0x1C0 to Address 0x1DF, Startup: 0x00, Name: TX_GAIN_SRAM_x

Table 58. Bit Descriptions for TX_GAIN_SRAM_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	TX_GAIN_SRAM_x		Transmit channel gain SRAM registers, eight bits wide. For read, the read command must be sent twice to read back.	0x0	R/W

Address: 0x200 to Address 0x2FF, Startup: 0x00, Name: BEAM_POSITION_SRAM_x

Table 59. Bit Descriptions for BEAM_POSITION_SRAM_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	BEAM_POSITION_SRAM_x		Beam position, 16 bits wide. Use Register 0x08 to access 8-bit MSB or 8-bit LSB. Bits[15:13] are reserved, Bits[12:7] are phase states index, Bits[6:5] are reserved, and Bits[4:0] are gain states index.	0x0	R/W

Address: 0x400 to Address 0x4FF, Startup: 0x00, Name: COMMON_GAIN_SRAM_x

Table 60. Bit Descriptions for COMMON_GAIN_SRAM_x

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	COMMON_GAIN_SRAM_x		Transmit common gain SRAM registers, eight bits wide. For ADMV4821, these are vertical channels transmit common gain SRAM.	0x0	R/W

Address: 0x500 to Address 0x5FF, Startup: 0x00, Name: COMMON_GAIN_SRAM_x_H

Table 61. Bit Descriptions for COMMON_GAIN_SRAM_x_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	COMMON_GAIN_SRAM_x_H		Transmit common gain SRAM registers for horizontal channels. For ADMV4821 only.	0x0	R/W

Address: 0x600 to Address 0x6FF, Startup: 0x00, Name: TRX_PROGRAM_SRAM_x

Table 62. Bit Descriptions for TRX_PROGRAM_SRAM_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	Reserved		Reserved.	0x0	R
[1:0]	TRX_PROGRAM_SRAM_x		Transmit or receive SRAM registers. For ADMV4801, directly set the transmit and receive mode by writing to Paged Register 0x85, Bits[6:5]. When Bits[1:0] = 'b11, the beam position is assigned to transmit mode. When Bits[1:0] = 'b00, the beam position is assigned to receive mode. For ADMV4821, directly set the transmit and receive mode by writing to Register 0x85 Bit 0 for the vertical channels and Bit 1 for the horizontal channels status. When the bit value is 1, the beam position is assigned to transmit mode, and when the bit value is 0, the beam position is assigned to receive mode.	0x0	R/W

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