ANALOG DEVICES

AN-132
APPLICATION NOTE

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OP-470 SPICE Macro-Model

by Joe Buxton

INTRODUCTION

This application note describes the SPICE macro-model for the OP-470 very low noise quad operational amplifier. This model was tested with and is compatible with PSpice* and HSpice**. The schematic and net-list are included here so that the model can easily be used. This model can accommodate multiple frequency poles and zeros, which is an advanced concept that results in more accurate AC and transient responses. For example, 6 poles and 2 zeros are required to accurately model the OP-470, which this model can easily accommodate.

This macro-model represents one of the four amplifiers on one chip. To use the quad amplifiers, the simulation circuit needs only to call up the model four separate times and specify the same power supplies each time. Throughout the OP-470 macro-model RC networks produce multiple poles which simulate the amplifiers AC behavior. The stages, which each contain a single pole or a pole- zero pair, are separated from each other by voltage-controlled current sources so that it is easy to set individual pole locations. The only nonlinear elements in the entire model are two NPN transistors which comprise the input stage, and diodes for voltage clamping. Limiting the model to almost entirely ideal, linear circuit elements significantly reduces simulation time and simplifies model development.

MODEL DESCRIPTION

The schematic (Figure 1) and net-list (Figure 2) describe the complete OP-470 model. This model breaks up the OP-470 into many distinct stages as described below:

INPUT STAGE

To correctly model the OP-470's input behavior, the model uses a differential pair of NPN transistors biased with a 1mA current source (Figure 1a). To keep this stage as simple as possible, only the forward beta, B_F, is specified in the NPN-BJT model. This is chosen to give the correct input bias current, I_B. The voltage limiting network of the OP-470 input is added with the diodes in series with the voltage source across the inputs. A voltage source is used instead of another diode to save computer time.

As for nonideal behaviors of the input stage, such as V_{OS}, I_{OS}, and C_{IN}, these are modelled with external circuit elements. For example, no junction capacitance is specified for the NPN model, therefore a capacitor, C_{IN}, is added across the inputs. Furthermore, since the input NPNs in this model are perfectly matched, V_{OS} and I_{OS} error sources are added using an external voltage source and current source, respectively. Lastly, the collector resistors R_3 and R_4 are chosen to be $1/g_m$ of the NPN transistors to give a gain of unity in the input stage. C_2 is added to create one of the secondary poles in the model.

GAIN STAGES

The open-loop gain of the OP-470 is acheived entirely in the gain stage (Figure 1b), and all other stages have unity-gain. The gain is taken in two steps due to a limit for only one step based on the combination of the slew rate, dominant pole, and open-loop gain. The voltage-controlled current sources, G_1 and G_2, have scaled transconductances that, when combined with R_7 and R_8, give the gain in the first step at node 12. The gain in the second step is produced the same way, and together the two steps give the open-loop gain of 1,000,000. The current sources G_1 and G_2 are controlled by the voltage drops across R_3 and R_4 in the input stage providing the differential to single ended voltage conversion. C_3 and C_4 create the dominant pole at 5.5Hz and model the amplifier's slew rate. Lastly, the diodes, D_5 and D_6 and voltage sources V_3 and V_4, are necessary to clamp the voltage of node 15 below the power supplies. Because the next stage (Figure 1c) has unity-gain and its voltage is controlled by the voltage at node 15, then it too is clamped, at node 18, below the power supplies. The same is true for subsequent stages, including the output, such that the output voltage is clamped to within the specified voltage range.

POLE STAGES

In addition to the poles in the input stage and the gain stage additional poles are easily added with separate stages. The pole and pole-zero stages (Figure 1c-e, g) have unity-gain, which is a result of the g_m of the voltage-controlled current sources being the reciprocal of the resistors. The pole and zero locations are determined by the resistor and capacitor or inductor values for each stage.

* PSpice is a registered trademark of MicroSim Corporation.
** HSpice is a tradename of Meta-Software, Inc.

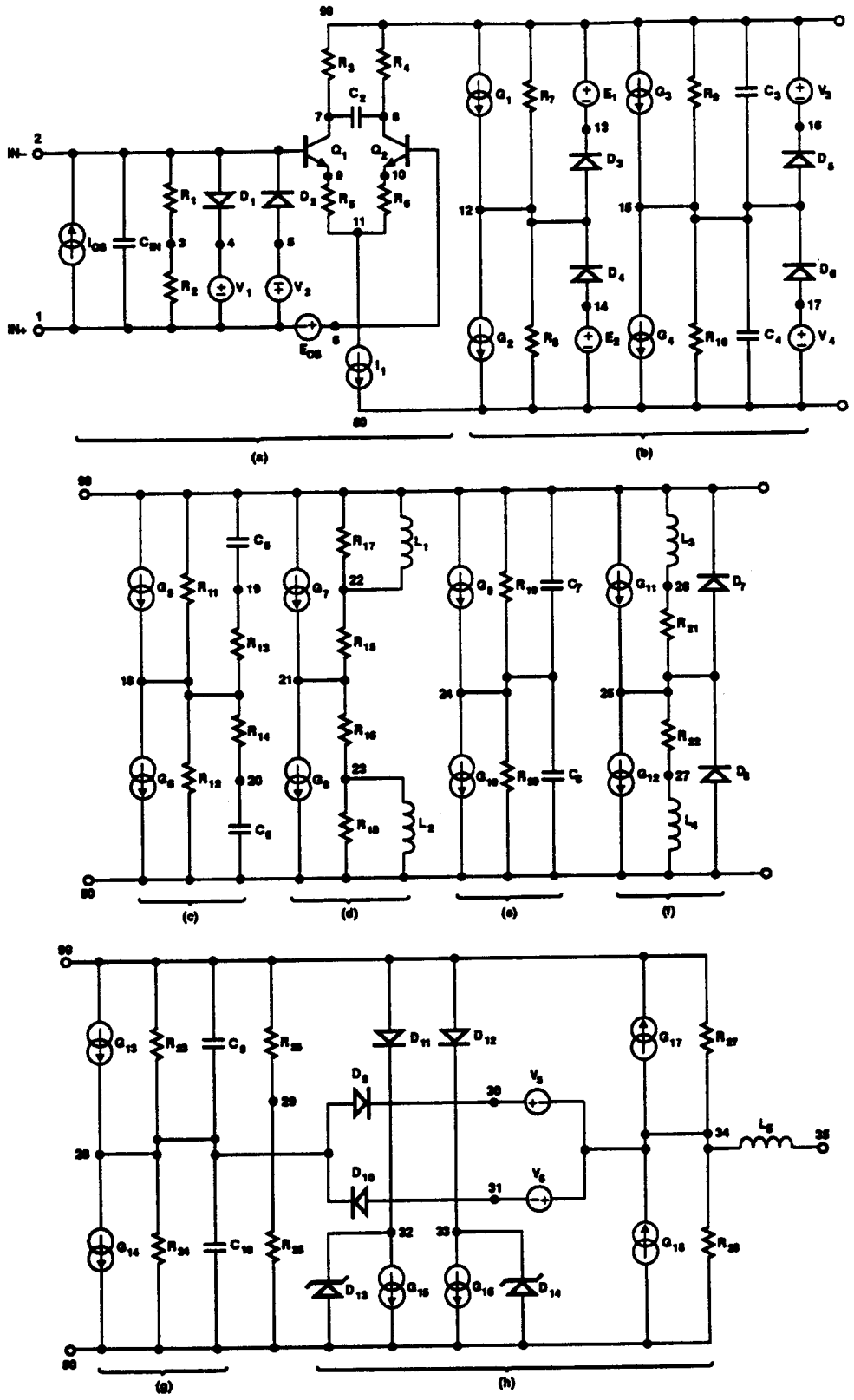

FIGURE 1: *OP-470 SPICE Macro-Model Schematic and Node List*

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OP-470 MACRO-MODEL © ADI 1990
*
.SUBCKT OP-470 1 2 35 99 50
*
* INPUT STAGE & POLE AT 60 MHZ
*
R1   2   3        2E5
R2   1   3        2E5
R3   7   99       101.6
R4   8   99       101.6
CIN  1   2        2E-12
C2   7   8        13.05E-12
I1   11  50       1E-3
IOS  1   2        3E-9
EOS  6   1        POLY(1) 25 29 1E-4 1
Q1   7   2   9    QX
Q2   8   6   10   QX
R5   9   11       50
R6   10  11       50
D1   2   4        DX
V1   4   1        0.7
V2   1   5        0.7
D2   5   2        DX
*
* FIRST GAIN STAGE
*
R7   12  99       1E6
R8   12  50       1E6
G1   99  12       7   8   64.1E-6
G2   12  50       8   7   64.1E-6
D3   12  13       DX
D4   14  12       DX
E1   99  13       POLY(1) 99 29 -2.6 1
E2   14  50       POLY(1) 29 50 -2.6 1
*
* FIRST GAIN STAGE & DOMINANT POLE AT 6.8 HZ
*
R9   15  99       46.8E6
R10  15  50       46.8E6
C3   15  99       500E-12
C4   15  50       500E-12
G3   99  15       POLY(1) 12 29 380E-6 333.3E-6
G4   15  50       POLY(1) 29 12 380E-6 333.3E-6
V3   99  16       1.9
V4   17  50       1.9
D5   15  16       DX
D6   17  15       DX
*
* POLE AT ZERO AT 1.9 MHZ/3.5 MHZ
*
R11  18  99       1E6
R12  18  50       1E6
R13  18  19       1.19E6
R14  18  20       1.19E6
C5   19  99       38.21E-15
C6   20  50       38.21E-15
G5   99  18       15 29 1E-6
G6   18  50       29 15 1E-6
*
* ZERO-POLE AT 5 MHZ/10 MHZ
*
R15  21  22       1E6
R16  21  23       1E6
R17  99  22       1E6
R18  50  23       1E6
L1   99  22       15.92E-3
L2   50  23       15.92E-3
G7   99  21       18 29 1E-6
G8   21  50       29 18 1E-6
*
* POLE AT 10 MHZ
*
R19  24  99       1E6
R20  24  50       1E6
C7   24  99       15.9E-15
C8   24  50       15.9E-15
G9   99  24       21 29 1E-6
G10  24  50       29 21 1E-6
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 100 HZ
*
R21  25  26       1E6
R22  25  27       1E6
L3   26  99       1.592E3
L4   27  50       1.592E3
G11  99  25       3   29  1E-12
G12  25  50       29  3   1E-12
D7   25  99       DX
D8   50  25       DX
*
* POLE AT 50 MHZ
*
R23  28  99       1E6
R24  28  50       1E6
C9   28  99       3.18E-15
C10  28  50       3.18E-15
G13  99  28       24 29 1E-6
G14  28  50       29 24 1E-6
*
* OUTPUT STAGE
*
R25  29  99       20E3
R26  29  50       20E3
R27  34  99       300
R28  34  50       300
L5   34  35       1E-6
G15  32  50       28 34 3.33E-3
G16  33  50       34 28 3.33E-3
G17  34  99       99 28 3.33E-3
G18  50  34       28 50 3.33E-3
V5   30  34       1.3
V6   34  31       1.3
D9   28  30       DX
D10  31  28       DX
D11  99  32       DX
D12  99  33       DX
D13  50  32       DX
D14  50  33       DX
*
* MODEL USED
*
.MODEL QX NPN (BF = 166667)
.MODEL DX D (IS = 1E-15)
.MODEL DY D (IS = 1E-15  BV = 50)
.ENDS OP-470
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FIGURE 2: *OP-470 SPICE Net-List*

COMMON-MODE STAGE

The common-mode error is based on the common-mode voltage of the input, which is created by the two input resistors, R_1 and R_2. This voltage is referenced by G_{11} and G_{12} in the common-mode stage (Figure 1f). The transconductances of these two sources are scaled such that, in combination with R_{21} and R_{22}, the V_{CM} is attenuated by the CMRR of 120dB. This error voltage is then inserted back into the input stage as part of the offset voltage, which is done by the voltage controlled voltage source E_{OS}. The inductors, L_3 and L_4, model the pole in the CMR versus frequency response of the OP-470.

OUTPUT STAGE

The output stage (Figure 1h) is modelled as an ideal output with an output resistance, R_{27} in parallel with R_{28}. An inductor, L_5, is added to model the rising output impedance of the emitter- follower output stage with frequency. The voltage sources V_5 and V_6, and diodes D_9 and D_{10}, combine to limit the voltage across the resistors, thus limiting the output current, I_{OUT} to 30mA.

PARAMETERS THAT ARE NOT MODELLED

To keep the OP-470 model as simple as possible and thus save computer and development time, not all features of the op amp were modelled as listed below:

- PSRR
- Crosstalk
- No Limits on Power Supply Voltages
- Maximum Input Voltage Range
- Temperature Effects (i.e., model parameters are assumed at 25°C)
- Input Noise Voltage and Current Sources
- Parameter Variations for Monte Carlo Analysis (i.e., all parameters are typical only)

These parameters are considered second-order effects and are not considered necessary for circuit simulation under normal operating conditions. However, users can easily add these functions as needed.

MODEL PERFORMANCE

The graphs on these next two pages compare the actual responses of the OP-470 to the SPICE analysis under various load and gain conditions. To show the accuracy of the model's frequency response, it was tested with different gains. Shown below are the gain-phase plots for an open-loop gain (Figures 3 and 4) and a closed-loop gain of −1 (Figures 5 and 6). The actual responses (part "a" of each figure), which were measured using a network analyzer, show very close agreement to the SPICE simulations (part "b" of each figure). This agreement holds true for both the gain and phase curves, which demonstrates the accuracy of the model's frequency response.

The model can also accurately simulate the OP-470's transient response. The comparisons to actual results were done with the amplifier in a a closed-loop gain of +1 with a 155pF capacitive load (260pF load for large signal) and a 2kΩ feedback resistor. The capacitive load was used to create the damped oscillations in the small and large-signal reponses. Because of the multiple poles and zeros, the model's small-signal transient response (Figure 7b) shows close resemblance to the actual reponse (Figure 7a). The large-signal reponse (Figure 8) again shows good accuracy. Notice in the large-signal reponse that the slew rate is accurately modelled, and that the "bump" before the amplifier starts slewing is also modelled. As can be seen from the figures, the model agrees closely with the actual device's performance. This accurate transient reponse, along with the accurate AC reponse, makes the OP-470 macro-model a powerful tool in analyzing circuit stability and AC behavior under various gains and load conditions.

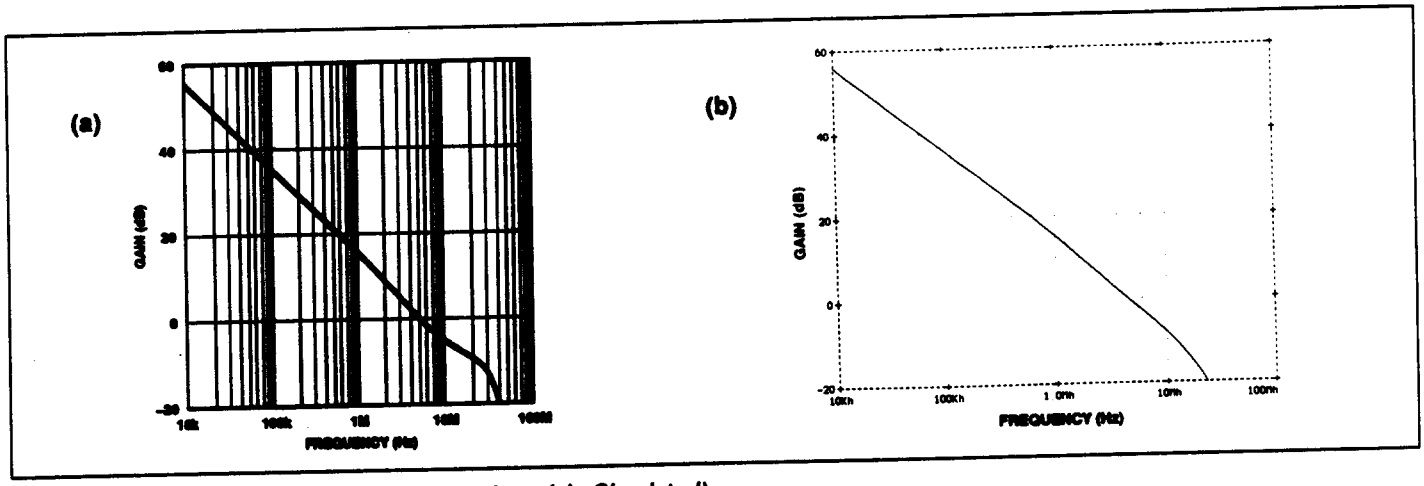

FIGURE 3: *Gain Plots, Open-Loop Gain (a. Actual, b. Simulated)*

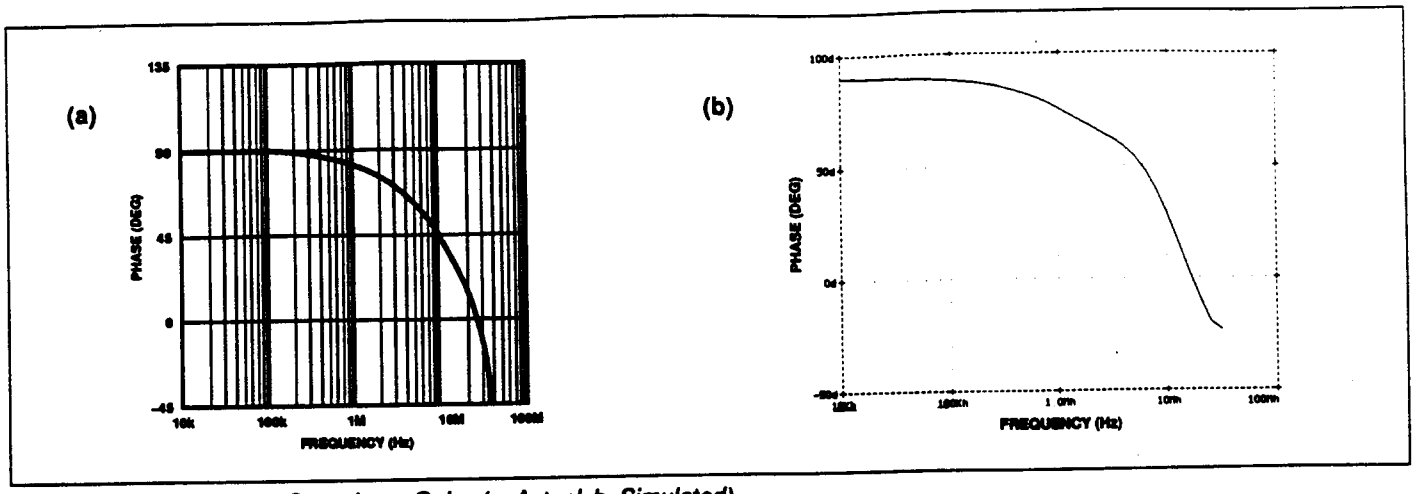

FIGURE 4: *Phase Plots, Open-Loop Gain (a. Actual, b. Simulated)*

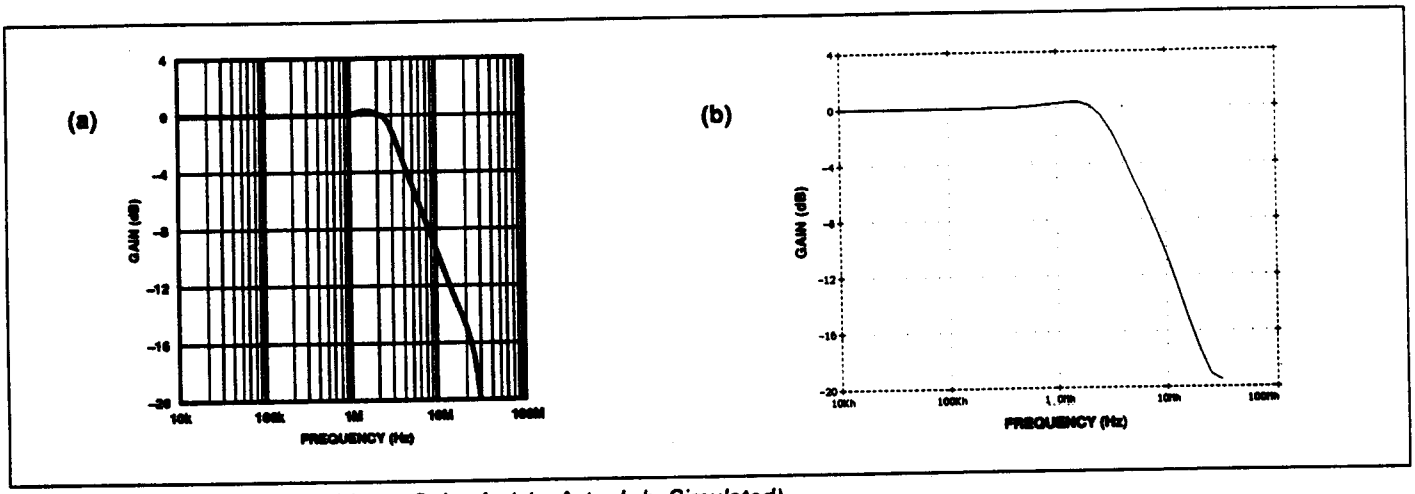

FIGURE 5: *Gain Plots, Closed-Loop Gain of –1 (a. Actual, b. Simulated)*

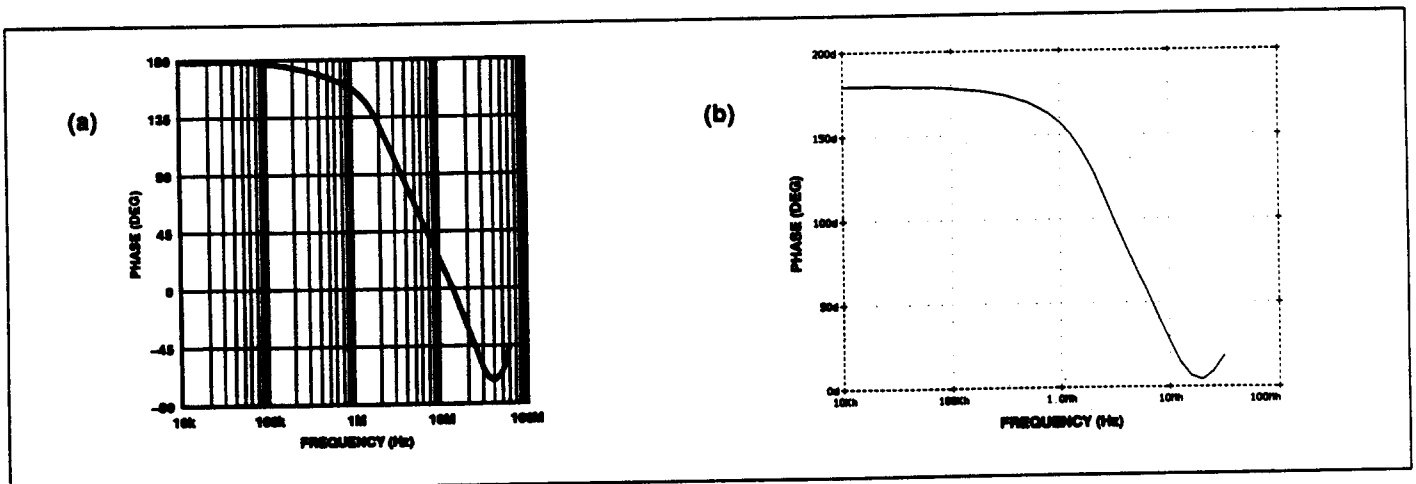

FIGURE 6: *Phase Plots, Closed-Loop Gain of –1 (a. Actual, b. Simulated)*

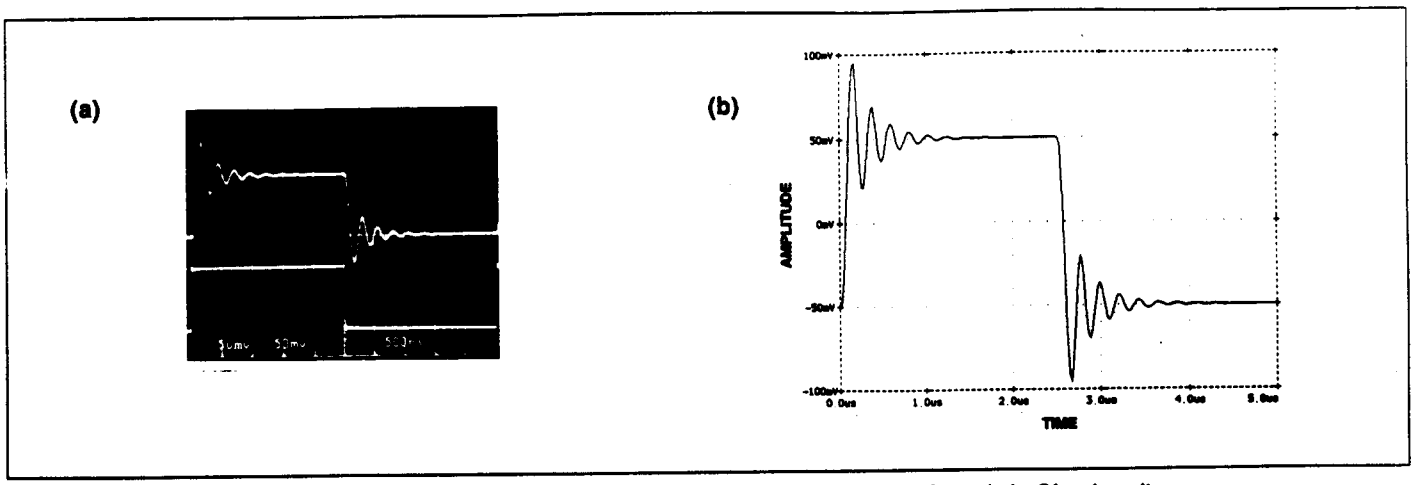

FIGURE 7: *Small-Signal Transient Response, Gain = +1, 155pF Capacitive Load (a. Actual, b. Simulated)*

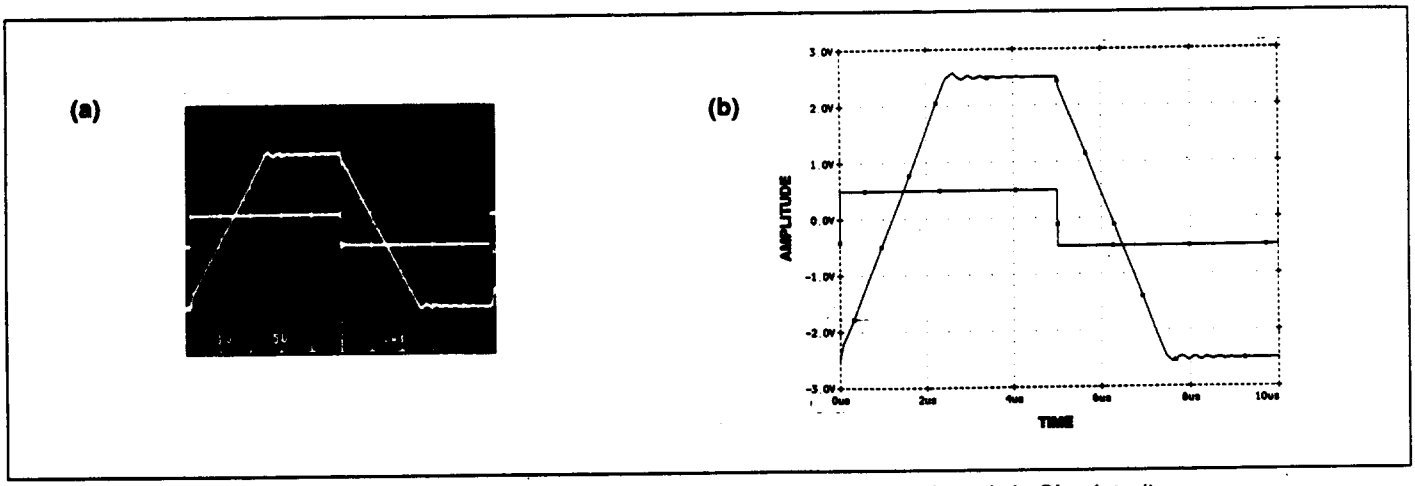

FIGURE 8: *Large-Signal Transient Response, Gain = +1, 260pF Capacitive Load (a. Actual, b. Simulated)*