

AN-1260 Application Note

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Crystal Design Considerations for Video Decoders, HDMI Receivers, and Transceivers

INTRODUCTION

To achieve frequency stability and accuracy, use this application note as a design guide for the external circuitry of the oscillator.

Additionally, it describes the oscillator circuits of video decoders. Most Analog Devices, Inc., video decoders typically require a crystal with a nominal frequency of 28.63636 MHz¹ and 50 ppm of frequency stability in fundamental mode. Table 1 details the specifications of the crystal used in the ADV7403 evaluation board. This application note is based on the ADV7401 and ADV7403; however, it also applies to the ADV740x, ADV718x, ADV728x, ADV7800, ADV7802, ADV7842, ADV7844 and ADV7850 video decoders.

The standalone High-Definition Multimedia Interface (HDMI*) receivers (the ADV7611, ADV7612, ADV7619, and ADV7604), as well as the HDMI video receivers built into video products not digitizing analog video (such as the ADV7622 and ADV7623), use a transition-minimized differential signaling (TMDS) clock for receiving pixels. These devices do not require a highly precise crystal clock source because the crystal accuracy does not affect the video quality. In this case, a clock derived from crystal circuitry is mainly used to measure the TMDS frequency clock, to generate the free-run video pattern, and to perform other, nonvideo-related operations such as extended display identification data (EDID) and high-bandwidth digital content protection (HDCP). Therefore, it has no impact on the quality of the processed video.

Table 1. Specifications of the Crystal Oscillator Used in theADV7403 Evaluation Board (See Reference 1)

Characteristics	Value
Holder Type	HC49
Nominal Frequency	28.63636 MHz
Mode of Oscillation	Fundamental
Frequency Calibration (at 25°C)	±0.0030%
Frequency Temperature Stability Tolerance	±0.0050%
Operating Temperature Range	-10°C to +60°C
Equivalent Resistance (Maximum)	30 Ω
Load Capacitance	30 pF
Drive Level	100 μW
Shunt Capacitance (Maximum)	7.0 pF
Aging for Year	±0.0003%

OSCILLATOR DESCRIPTION Circuitry

Figure 1 shows the block diagram of the oscillator used in the video decoders. The equivalent circuit of the quartz crystal is shown in Figure 2. C0 is the shunt or static capacitance of the crystal. R1 is the motional resistance, L1 is the motional inductance, and C1 is the motional capacitance. R1, L1, and C1 are determined by the mechanical properties of the crystal. They are in the motional arm of the crystal, and their effect only exists when the crystal is oscillating (see Reference 2). R is an external shunt resistance with a recommended value of 1 M Ω for the ADV740x family of products.

The additional external shunt resistance applies to most of the video decoders and HDMI receivers, except for the ADV7850 and the ADV7619. For the most up to date information, see the recommended schematic of the relevant video part on the Analog Devices, Inc., website (www.analog.com).



Figure 2. Crystal Representation

¹ In the case of the ADV7850, this is 27 MHz; for more details, see the recommended schematic of the relevant video part.

Series and Parallel Resonances

The effective reactance curve of the crystal is shown in Figure 3. The frequency range shown in Area 1 and Area 2 is fundamental mode.

There are two cases of resonance in fundamental mode: series and parallel.

Series resonance occurs when the L1 motional inductance resonates with the C1 motional capacitance. The series resonant frequency is given by (approximately)

$$f_{\rm S} = \frac{1}{2\pi\sqrt{L1C1}}$$

Parallel resonance occurs when a load capacitance, C_L, is connected between the crystal pins. The oscillating frequency of the crystal in parallel resonance is given by (approximately)

$$f_{XTAL} = f_s \left(\frac{C1}{2(C0 + C_L)} + 1 \right)$$

Note that the parallel resonance is shown in Area 2 of Figure 3, and can be calculated as follows:

$$f_A = \frac{1}{2\pi\sqrt{L1C1(C1C0)/(C1+C0)}}$$

The crystals used for the ADV740x decoders oscillate in parallel resonance mode, which is considered in the remainder of this application note. The operating frequency is the crystal frequency shown in the Area 2 range (see Figure 3).



Figure 3. Reactance of the Crystal Oscillator

1785-003

CRYSTAL SPECIFICATIONS

Frequency Tolerance

The frequency tolerance is the ability of the crystal to oscillate within a limited range of frequencies for proper tuning. The manufacturers typically give two specifications related to frequency tolerance which include the following:

- Frequency calibration tolerance corresponds to the maximum deviation from nominal frequency, usually at 25°C.
- Frequency temperature stability tolerance is the maximum deviation from nominal frequency when the temperature fluctuates within the operating temperature range.

The frequency calibration tolerance in Table 1 is $\pm 0.0030\%$; therefore, the maximum frequency deviation (Δf) is given by

 $\Delta f = 28.63636 \text{ MHz} \times 0.000030 \approx 859.09 \text{ Hz}$

Therefore, the following is true:

$$0.0030\% = \frac{0.0030}{10^2} = \frac{30}{10^6} = 30 \, ppm$$

Load Capacitance

The load capacitance given in a crystal data sheet specifies the parallel resonance frequency within the tolerance at 25°C. Therefore, it is important to design a circuit that matches the load capacitance to achieve the frequency stipulated by the manufacturer. Use the following equation to calculate the load:

$$C_{L} = \frac{(C_{PG1} + C1)(C_{PG2} + C2)}{C_{PG1} + C1 + C_{PG2} + C2} + C_{S}$$

where:

 C_{PGI} and C_{PG2} are the pin to ground capacitances. C_S is the printed circuit board (PCB) stray capacitance.

A good guideline is to approximate C_{PG1} and C_{PG2} to 5 pF to 10 pF and C_{s} to 2 pF to 3 pF.



Figure 4. Calculating Crystal Load Capacitance

For example, let $C_{PG1} = C_{PG2} = C_{PG} = 4$ pF and C1 = C2 = C. C_{PG} is the parasitic ground capacitance. To get a load capacitance of $C_L = 30$ pF, the C value must be known (see Table 1). The C value is derived from the previous equation.

$$C = 2(C_L - C_S) - C_{PG}$$

= 2(30 - 3) - 4
= 50 pF

Therefore, two 47 pF capacitors can be chosen for C1 and C2. The circuit can be optimized later by changing the starting values of C1 and C2.

Equivalent Series Resistance

The equivalent series resistance (ESR) is typically specified by the manufacturer. The ESR is the real value part of the crystal impedance, assuming that the oscillator matches the load capacitance (C_L).

$$ESR = Rl \left(1 + \frac{C0}{C_L}\right)^2$$

For example, ESR = 30 Ω for the crystal specified in Table 1, with a C_L equal to 30 pF. ESR \leq 30 Ω is recommended for the ADV740x decoders.

Drive Level

The drive level is the power dissipated in the crystal. It is important to limit the dissipated power to the value in the specifications to prevent the crystal from any damage. If the peak voltage across the crystal is approximated as its dc supply, the power dissipation can be approximated as

$$P = 2R1(\pi f_{XTAL}(C_L + C0)V_{CC})^2$$

Quality Factor

The quality factor (Q) is not typically specified in crystal data sheets. The Q factor is the ratio of stored energy in reactive form to the sum total of all energy losses. Therefore, the Q factor equals infinity in an ideal oscillator where there are no losses. The Q factor standard crystals fall between values of 20,000 and 200,000. A crystal with a very high Q factor contributes to the high frequency stability of the crystal oscillator.

REFERENCES

- ¹ Product Specification, HC49 Standard Crystal Series (Part Number MA01377), Golledge Electronics, Ltd. Please contact Golledge Electronics for further information about this part.
- ² Application Note AP-155, *Oscillator for Microcontrollers* (Intel Corporation, June 1983).

REVISION HISTORY

10/13—Revision 0: Initial Version

NOTES



www.analog.com

©2013 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners. AN11785-0-10/13(0)

Rev. 0 | Page 4 of 4