AN-1572
APPLICATION NOTE

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# IEC 61000-4-x and CISPR 11 Tested Analog Input Design with AD4111 for Industrial Automation

by Li Ke

## INTRODUCTION

The AD4111 integrates a low noise, fast settling, 24-bit, Σ-Δ analog-to-digital converter (ADC) with an analog front end for fully differential or single-ended, bipolar, ±10 V voltage inputs and single-ended, 20 mA inputs. The AD4111 is designed to work with programmable logic controller (PLC) and distributed control system (DCS) modules of industrial automation applications.

This application note details the functionality of the AD4111 electromagnetic compatibility (EMC) printed circuit board (PCB) that can be used with AD4111 for a typical ±10 V voltage and 0 mA to 20 mA current input. The board design demonstrates a proven EMC solution for industrial automation applications. The IEC 61000-4-x set of standards discusses the evaluation of immunity of electrical and electronic equipment at a system level.

The AD4111 EMC test board is characterized to ensure that the circuit performance is not affected by radiated radio frequency (RF) or conducted RF disturbances, and has sufficient immunity against electrostatic discharge (ESD), electrical fast transients (EFT), and surge. The board is also tested for CISPR 11, in which the radiated emissions of the board fall well below the Class A limits.

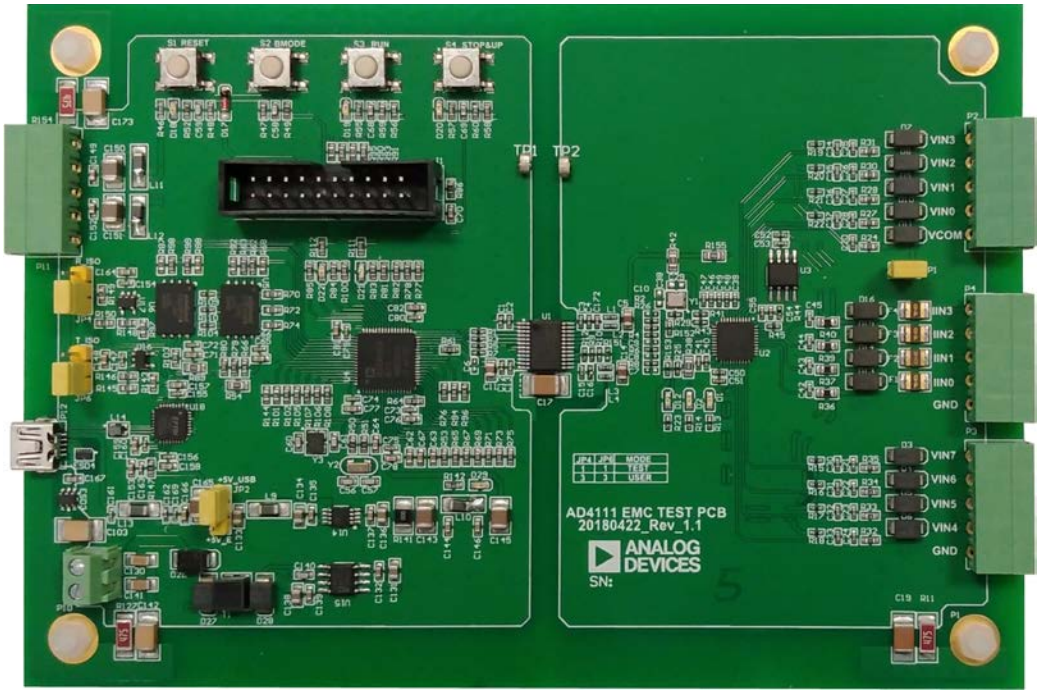


*Figure 1. AD4111 EMC Test Board Photograph*

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## REVISION HISTORY

**10/2018—Revision 0: Initial Version**

# SYSTEM DESIGN

## AD4111 ADC DESCRIPTION

The AD4111 is a low power, low noise, 24-bit, Σ-Δ ADC that integrates an analog front end (AFE) for fully differential or single-ended bipolar, ±10 V voltage inputs, and 0 mA to 20 mA current inputs. The AD4111 features a maximum channel scan rate of 6.2 kSPS (161 µs) for fully settled data.

The embedded 2.5 V, low drift (5 ppm/°C), band gap internal reference with output reference buffer reduces the external component count. The digital filter allows flexible settings, including simultaneous 50 Hz and 60 Hz rejection at a 27.27 SPS output data rate. The user can select between the different filter settings depending on the demands of each channel in the application. An automatic channel sequencer enables the ADC to switch through each enabled channel.

The precision performance of the AD4111 is achieved by integrating the proprietary *i*Passives™ technology from Analog Devices, Inc. The device is factory calibrated to achieve a high degree of specified accuracy. The AD4111 has the unique feature of open wire detection on the voltage inputs (patent pending) for system level diagnostics. The device operates with a single 3 V or 5 V power supply, making it easy to use in galvanically isolated applications.

For full details, refer to the AD4111 data sheet.

## CIRCUIT DESCRIPTION

The AD4111 is designed for PLC and DCS applications that are involved with harsh industrial environments. The AD4111 also satisfies the IEC 6100-4-x and CISPR 11 standards.

The circuit shown in Figure 2 demonstrates a typical multiple channel, group isolated, industrial voltage and current input module for harsh EMI and EMC conditions using the AD4111.

In the example circuit, the ADuCM3029 ultra low power Arm® Cortex-M3 microcontroller unit (MCU) handles local on-board control and data communication to the host computer. The ADuM5411 quad-channel isolator with integrated dc-to-dc converter enables a neat and robust solution of an isolated analog input design that operates off a single 3 V or 5 V supply. The AD4111 can simultaneously handle current input (single-ended or bipolar differential voltage input).

Two low dropout regulators (LDOs) substantially simplify the on-board power supply in the example circuit to provide the necessary voltages for board functionality. The ADP7142 steps down a 6 V to 40 V input to 5 V for powering the primary side of the ADuM5411. The ADP124 regulates the ADP7142 output to 3.3 V for the microprocessor and the digital isolator session of the ADuM5411.

The power supplies are not intended to match the robustness of the power supply module or the backplane supply in a typical industrial automation control system. Only basic protections are implemented for the supply circuit. This AD4111 EMC test board has an option to fully function off the 5 V universal serial bus (USB) supply from the host computer while communicating with the host through a nonisolated universal asynchronous receiver transmitter (UART) to USB port. When undergoing the EMI and EMC testing, the AD4111 EMC test board is alternatively powered by a separate 12 V dc supply while data is sent to the host computer through the off board isolated data link.

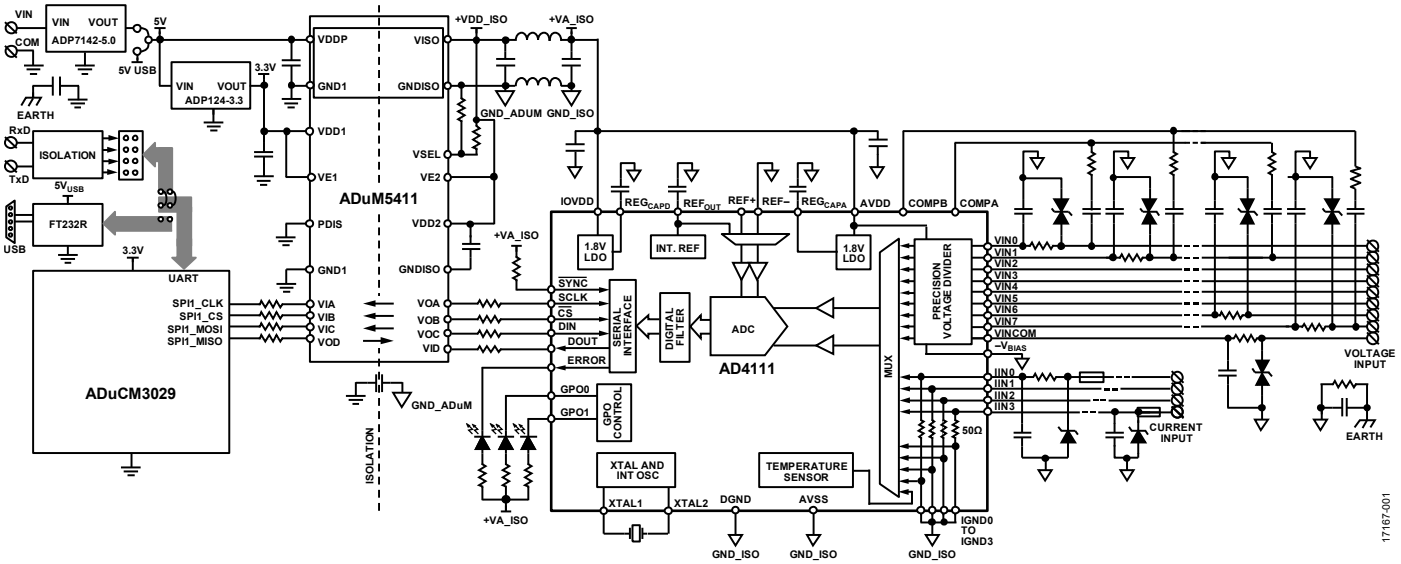


*Figure 2. AD4111 EMC Test Board in Circuit*

## CIRCUIT EVALUATION AND TEST

The AD4111 EMC test board can be run by being connected to a host computer or in standalone mode. The operational parameters are programmed in the on-board flash memory. During emission tests, the board is disconnected from the host computer while the firmware runs, and the hardware is kept operational. In the immunity tests, the board is connected to the host computer through the isolated data link. The serial port data capture program on the host computer receives ADC conversion samples from the AD4111.

The AD4111 on the EMC test board has only gone through the standard factory calibration at the component level. No further board level calibration was conducted.

With an output data rate set to 1007 SPS, the AD4111 is configured to continuously sequence sample the voltage and current input channels VIN0 to VIN1, VIN6, VIN2 to VIN3, VIN7, VIN4 to VIN5, IIN3, IIN2, IIN1, and IIN0. When evaluating performance in EMC testing, VIN2 to VIN3 represent the differential voltage input channels, VIN7 represents the single-ended voltage input channels, and IIN3 represents the current input channels. Further connections in EMC testing are detailed in Table 1.

**Table 1. AD4111 Pin Connection in EMC Testing**

| AD4111 Pin | Connection in the EMC Tests |
|---|---|
| AVDD | 5 V |
| IOVDD | 5 V |
| AVSS | GND_ISO |
| DGND | GND_ISO |
| REF+ | Internally enabled |
| VIN0 to VIN1 | GND_ISO |
| VIN6 | GND_ISO |
| VIN2 to VIN3 | 2.5 V |
| VIN7 | 2.5 V |
| VIN4 to VIN5 | GND_ISO |
| IIN3 | 2.5 V |
| IIN2 | GND_ISO |
| IIN1 | GND_ISO |
| IIN0 | GND_ISO |

Before and after each possibly destructive EMC test, the board samples the 2.5 V external signal source together with an independent precision bench digital multimeter (DMM). After being translated into voltage or current, the AD4111 samples from the representative channels are compared with the measurement from the DMM in the same period to quantify the error. The deviation between the two measurements must stay within the predefined range to meet the performance criterion. The maximum allowable error is 0.1% of full scale, which aligns with the common requirements of the industrial automation applications.

During the nondestructive EMC tests, the board samples the 2.5 V external signal source together with the bench DMM. The voltage or current measurements are compared to that of the DMM for judging the performance criterion.

During emissions testing, the analog input channels of the board are shorted to the isolated ground. The board is disconnected from the host computer while AD4111 keeps sampling at 1007 SPS in each channel. The only auxiliary device in this setup is a 12 V battery to power the EMC test board and which is assumed not to contribute EMI. The general setup for EMC testing is shown in Figure 3.

A pair of twisted leads followed by a low pass filter probe the output of the precision signal source. The filtered output is wired to the DMM with a pair of twisted leads. The DMM is connected to the PC via the USB cable. The RealTerm software on the host computer logs AD4111 samples via the electrically isolated data link. For each EMC test item, the EMC test board was tested in its voltage input mode and the current input mode.

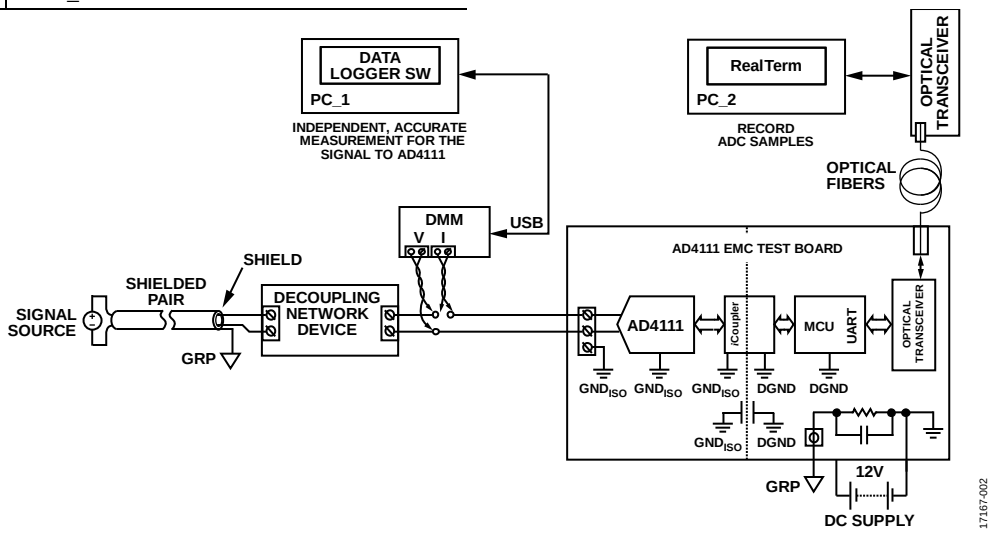


*Figure 3. General EMC Test Setup*

## SOFTWARE NEEDED

To perform EMC testing on the AD4111, the following software is required:

- Firmware revision E0-01 on AD4111 EMC board
- RealTerm: Serial/TCP Terminal 2.0.0.70
- Keysight Technologies BenchVue software V 2.6

## EQUIPMENT NEEDED

To perform EMC testing on the AD4111, the following equipment is required:

- Optical USB transceiver board
- Industrial fiber optic cable
- PC running Windows® 7, 64-bit version, image V3.0.2011.10.14
- DC power supply: Agilent 3630A or YUASA NP7-12
- Digital multimeter: Keysight 33470A
- Precision signal source: ADR421
- Shielded two-conductor cable, foil/braid
- Schaffner FN353Z-30-33

## STANDARDS AND PERFORMANCE CRITERIA

The EMC and electromagnetic interference (EMI) test items, limits, and performance criteria for which this board was designed are defined according to IEC 61131-2. According to this standard, the following six applicable tests were selected:

- IEC 61000-4-2
- IEC 61000-4-3
- IEC 61000-4-4
- IEC 61000-4-5
- IEC 61000-4-6
- CISPR 11

According to these standards, the performance criteria are classified as described in Table 4.

The AD4111 EMC test board was tested and has met the CISPR 11 and IEC 61000-4-x standards detailed in Table 2 and Table 3.

**Table 2. Emission Performance Summary**

| Test | Basic Standard | Frequency Range | Limits | Measured Minimum Margin | Result |
|---|---|---|---|---|---|
| Radiated Emissions | CISPR 11 Class A | 30 MHz to 1000 MHz | See Table 11 and Table 12 | 7.5 dBµV | Pass |

**Table 3. Immunity Performance Summary**

| Test | Basic Standard | Test Levels | Performance Criterion | Measured Minimum Margin | Result |
|---|---|---|---|---|---|
| Conducted Immunity | IEC 61000-4-6 | 10 V/m | A | See Table 5 | Pass |
| Radiated Immunity | IEC 61000-4-3 | 10 V/m | A | See Table 9 | Pass |
| ESD | IEC 61000-4-2 | ±6 kV | B | See Table 6 | Pass |
| EFT | IEC 61000-4-4 | ±2 kV | B | See Table 7 | Pass |
| Surge | IEC 61000-4-5 | ±2 kV | B | See Table 8 | Pass |

**Table 4. Performance Criteria**

| Performance Criterion | Description |
|---|---|
| A | Normal performance within an error band specified by the manufacturer. |
| B | Temporary loss of function or degradation of performance, which ceases after the disturbance is removed. The equipment under test recovers its normal performance without operator intervention. |
| C | Temporary loss of function or degradation of performance, and correction of performance requires operator intervention such as manual restart, power off, or power on. |
| D | Loss of function or degradation of performance, which is not recoverable. Permanent damage to hardware or software, or loss of data. |

# PRINTED CIRCUIT BOARD

The AD4111 EMC test board is a separate design from the standard AD4111 evaluation board, EVAL-AD4111SDZ, which is designed to give optimum ADC performance but is not optimized for EMC and EMI testing.

The AD4111 EMC test board is built on a FR4 four layer PCB. The PCB stack up is shown in Figure 4. Both the primary side and the secondary side have 0.5 oz copper foil. The system side of the board (consisting of the LDOs, the microprocessor, the primary side of ADuM5411, and the UART to USB transceiver) sits on the four-layer structure. The internal layers are on 1 oz copper. These layers are designed to provide the optimum EMC and EMI performance on the portion of the board that does not directly host the AD4111.

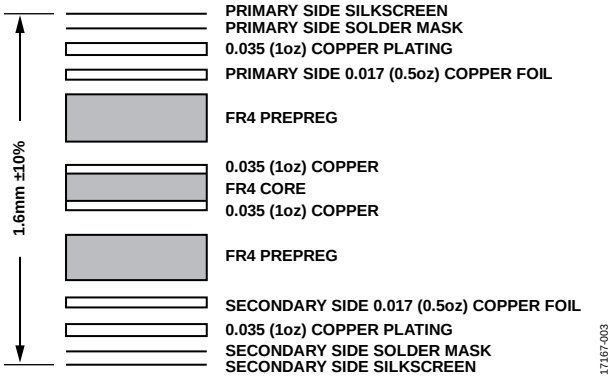


*Figure 4. PCB Stack Up*

The field side of the EMC board, including the AD4111 and its entire periphery, sit on a pseudo two layer structure where the inner layers for the ground plane and the power plane are completely etched out. These layers are designed to demonstrate the feasibility for AD4111 to achieve its specified functional performance, as well as EMC and EMI performance on a low cost two layer PCB.

## COMPONENT PLACEMENT AND LAYOUT CONSIDERATIONS

Because the resolution of the high resolution of and the low noise levels from the AD4111, take care with regard to decoupling, grounding, and layout. The analog and digital sections are separated on the EMC board and confined to certain areas of the board. The AD4111 is placed on one solid ground plane, to which both the AVSS and DGND pins are soldered when a more than 2-layer printed circuit board is used. The digital interface side of AD4111 is located close to the isolators, and the analog side faces the voltage and current input terminal blocks. The power supplies are decoupled with a 0.1 µF capacitor in parallel with a 10 nF capacitor. Both are low equivalent series resistance (ESR) ceramic capacitors in a surface mount footprint and located as close as possible to the AD4111 power supply pins.

The damping resistors attenuate the electrical transients from tens of ohms to hundreds of ohms on the digital lines due to the complementary metal-oxide semiconductor (CMOS) switching on and off, helping to reduce EMI. The resistors can also reduce the ringing caused by adding ferrite beads in the serial peripheral interface (SPI).

Take care to follow the recommendations in the ADuM5411 data sheet to achieve improved radiated emissions performance. A parallel combination of at least two capacitors between the $V_{DD1}$ pin and $GND_1$ pin, between the $V_{DDP}$ pin and $GND_1$ pin, between the $V_{ISO}$ pin and $GND_{ISO}$ pin, and between the $VDD_2$ pin and $GND_{ISO}$ pin is used to suppress noise and reduce ripple. The 0.1 µF and 10 nF low ESR ceramic capacitors provide low inductance in high frequencies. The 10 µF capacitor is used for ripple suppression and proper regulation at $V_{DDP}$ and $V_{ISO}$. Both these capacitors are placed as close as possible to the ADuM5411 power pins, with PCB traces of minimum length.

A surface-mount ferrite bead (BLM15HD182SN1D) is placed in series with the $V_{ISO}$ and $GND_{ISO}$ pins to increase the impedance to high frequency currents. The ferrite bead typically has 2 kΩ impedance from 100 MHz to 1 GHz, which can reduce the emissions at the 125 MHz primary switching frequency and the 250 MHz secondary side rectifying frequency and harmonics. $V_{ISO}$ directly powers $VDD_2$ via a short trace. $GND_{ISO}$ (Pin 23) is connected to other $GND_{ISO}$ pins internally. Pin 23 is wired only to the bypassing capacitors as shown in Figure 5.

A high voltage surface-mount technology (SMT) capacitor is connected directly between $GND_1$ (Pin 12) and $GND_{ISO}$ (Pin 13) for optimal performance. For additional reduction in emissions, PCB stitching capacitance can be implemented, as detailed in the AN-0971 Application Note.

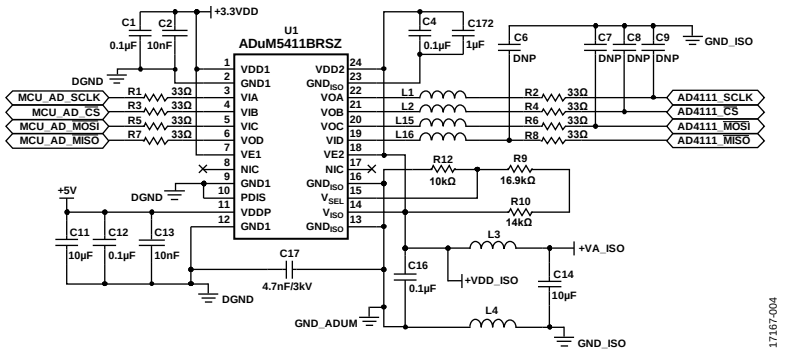


*Figure 5. ADuM5411 Bypass and Peripheral*

## OTHER COMPONENT CONSIDERATIONS

The AD4111 EMC test board uses 0.1 µF, 50 V/X5R, 10%, low ESR ceramic capacitors in a C0402 footprint for the decoupling capacitors on the field side of the board. Use of ESR capacitors is a trade-off among considerations for performance, derating, cost, and space saving. The decoupling capacitors on the system microprocessor side use 0.1 µF, 50 V/X7R, 10%, low ESR ceramic capacitors in a C0603 footprint.

## VOLTAGE SUPPLY PROTECTION

The scope of EMC and EMI evaluation and demonstration is focused on the AD4111 and its companion devices. The power supply circuits on the AD4111 EMC test board provide the necessary voltages for board functionality. The supply circuits are not intended to match the robustness of the power supply module or the backplane supply in an industrial automation control system. As such, only basic protections are implemented for these supply circuits. A 1 nF capacitor is placed next to each pin of the power input terminal to the protected ground, where transient energy can be discharged to the earth ground through a 3.3 nF/3 kV capacitor. The 4.7 MΩ resistor bleeds the energy to the earth that may be accumulated on the protected ground. A diode is inserted to protect from miswiring to the power supply input. The SMBJ26CA transient voltage suppression (TVS) diode clamps the transient voltage from going higher than 24 V (nominal). A common-mode inductor blocks the emissions escaping from the downstream circuits. A second SMBJ26CA TVS diode after the inductor provides further clamping for the transient.

## ESD PROTECTION

Appropriate ESD protection circuitry must exist on the EMC test board. The protection consists of a current limiting resistor, a transient voltage clamp, and a transient energy diverting capacitor.

There are three minimum mandatory components for AD4111 EMC and EMI in the voltage input channels: a 180 Ω resistor, a 4.7 nF capacitor, and a TVS device. The 180 Ω resistor on the trace between the AD4111 VINx pin and the terminal block in conjunction with the 4.7 nF/50 V C0G GRT155R71H472KE01D capacitor provides antialias filtering for the ADC. The RC filter can attenuate the RF interferences during the EMC testing. Because the AD4111 VINx pins are internally connected to approximately 1 MΩ resistors, the 180 Ω serial resistor provides some additional isolation between the AD4111 and the high voltages that the TVS clamps. The TVS device is crucial to clamp the electrical transient on the board during the EMC events. An SMAJ33CA-TR is inserted between the AD4111 and the input terminal block. The TVS pins are routed to the VINx terminal pins with short and heavy traces.

There are four minimum mandatory components for AD4111 EMC and EMI in the current input channels: a PTC resettable fuse, a 180 Ω resistor, a TVS device, and a GRM1555C1H471JA01D capacitor. The fuse trips when the current flowing through it exceeds 150 mA. A 180 Ω resistor on the trace between the AD4111 IINx pin and the terminal block helps to limit the transient current to and from the device because the input resistance of the IINx is approximately 60 Ω. The TVS device is crucial to clamp the electrical transient on the board during the EMC events. An SMA6J10A-TR is inserted after the input terminal block and before the current limiting resistor. The TVS pins are routed to the VINx terminals with short and heavy traces. A 470 pF/50 V C0G GRM1555C1H471JA01D capacitor located after the current limiting resistor diverts the small amount of high frequency transient to the isolated ground.

# EMC AND EMI MEASUREMENT RESULTS OF THE AD4111 EMC TEST BOARD

## CONDUCTED IMMUNITY

As per IEC 61000-4-6, the equipment under test (EUT) is placed on an insulating support of 0.1 meter height above a ground reference plane. All cables exiting the EUT are supported at a height of at least 30 mm above the ground reference plane. The interference is injected with a coupling/decoupling network (CDN), KEMA 801A. The cable is decoupled by an attenuation clamp, KEMA 801A. The frequency range is swept from 150 kHz to 80 MHz (10 V/m) with the disturbance signal of 80% amplitude modulated with a 1 kHz sine wave. The step size is 1% of the start and thereafter 1% of the preceding frequency value where the frequency is swept incrementally. The dwell time of the amplitude modulated carrier at each frequency is 1 sec.

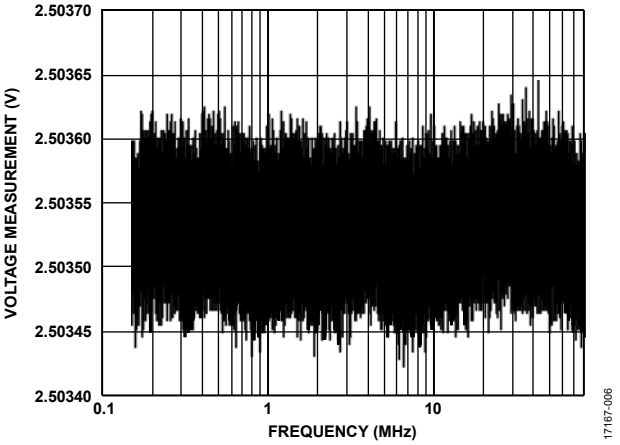


*Figure 7. Voltage Measurement vs. Frequency, VIN7 Under 10 V/m*

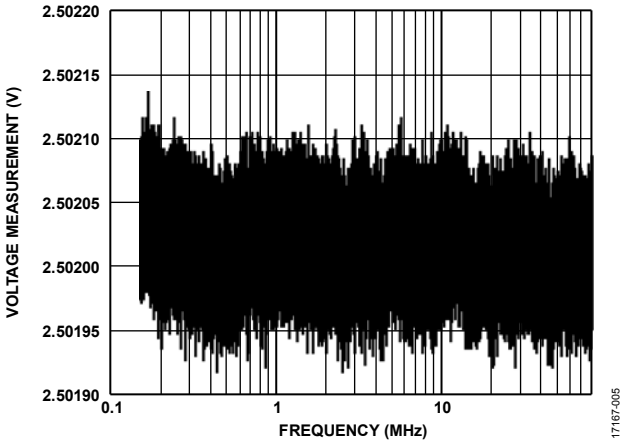


*Figure 6. Voltage Measurement vs. Frequency, VIN2 to VIN3 Under 10 V/m*

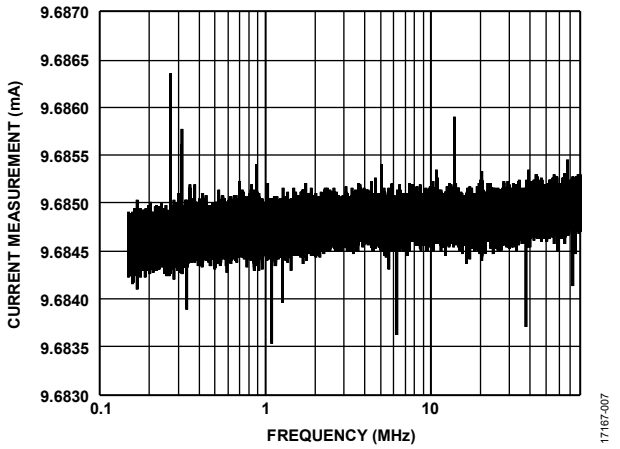


*Figure 8. Current Measurement vs. Frequency, IIN3 Under 10 V/m*

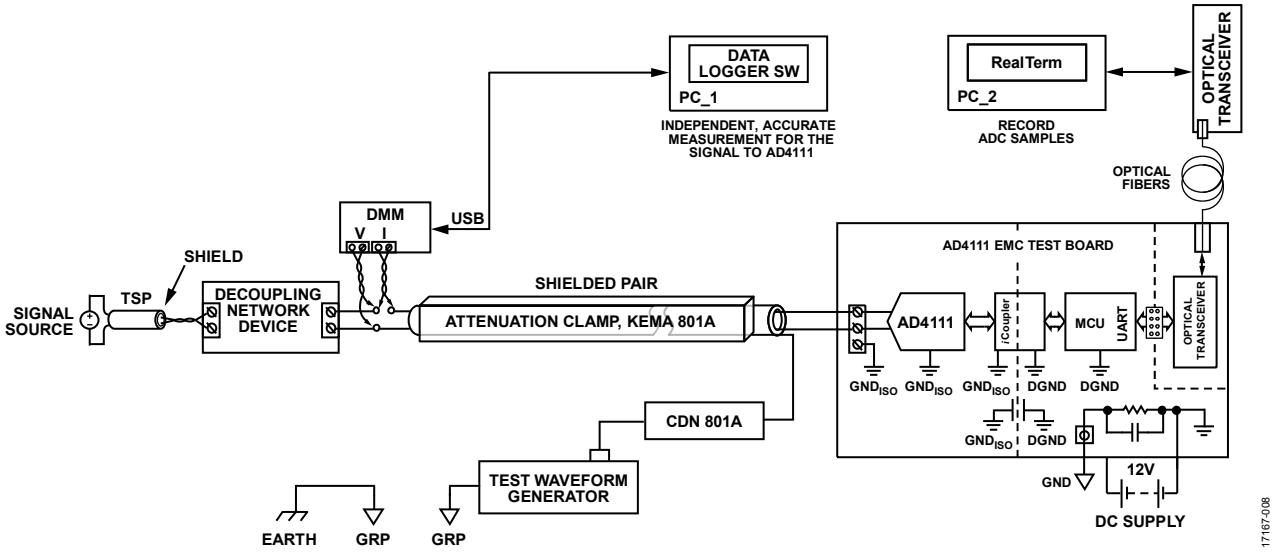


*Figure 9. IEC 61000-4-6 Test Setup Connection Diagram*


*Figure 10. IEC 61000-4-6 Test Setup Photograph*

**Table 5. 61000-4-6 Test Levels and Results**

| | | During Zap | | | |
|---|---|---|---|---|---|
| **Input Mode** | **Average** | **Min** | **Max** | **Deviation** | **Pass or Fail** |
| VIN2 to VIN3 | 2.502017 | 2.501917 | 2.502137 | −10 ppm, 12 ppm × full scale (FS) | Pass, Criterion A |
| VIN7 | 2.503531 | 2.503422 | 2.503645 | −4 ppm, 5 ppm × FS | Pass, Criterion A |
| IIN3 | 9.684782 | 9.681976 | 9.688193 | −14 ppm, 18 ppm × full scale range (FSR) | Pass, Criterion A |

## IMMUNITY TO ESD

As per IEC 61000-4-2, the test setup consists of a nonconductive table, 0.8 m high, standing on the ground reference plane. A horizontal coupling plane (HCP) of 1.6 m × 0.8 m is placed on the table. The EUT and its cable are isolated from the coupling plane by an insulating mat 0.5 mm in thickness. The contact discharges are applied to the VINx and IINx screws of the AD4111 input terminal block. The EUT is exposed to at least 20 discharges at each rating, 10 each at negative and positive polarity. The discharges are repeated at a rate of 1 per sec.

Because the precision signal as the auxiliary equipment is essentially a voltage source, the measurements in the AD4111 current mode can vary due to the parameter drift of the components in the measurement loop during the immunity tests. For the current input channel, the 2.5 V reference voltage forces a 10 mA dc current (approximately). The performance is judged with the difference between the AD4111 reading and the multimeter reading, rather than the absolute measurements. The same applies for the EFT and surge test.

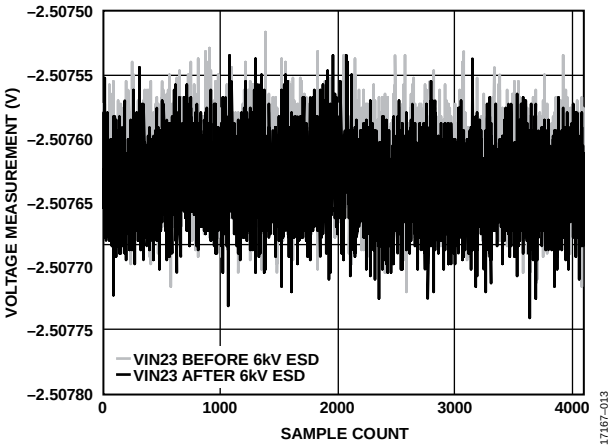


*Figure 11. Voltage Measurement vs. Sample Count, VIN2 to VIN3 Under 6 kV ESD*

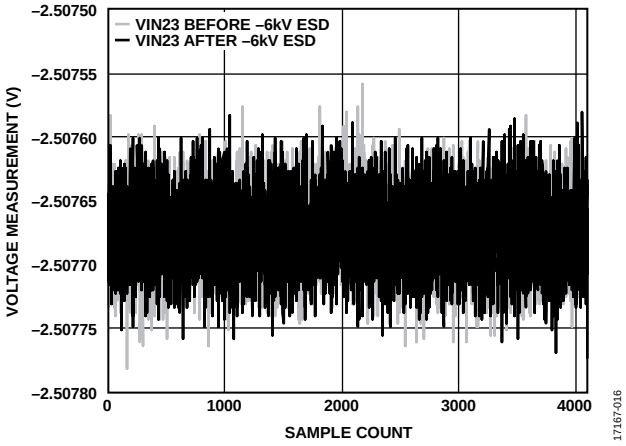


*Figure 12. Voltage Measurement vs. Sample Count, VIN2 to VIN3 Under –6 kV ESD*

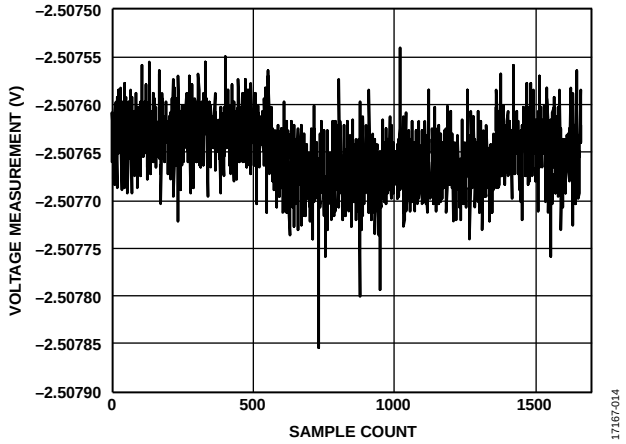


*Figure 13. Voltage Measurement vs. Sample Count, VIN2 to VIN3 During 6 kV ESD*

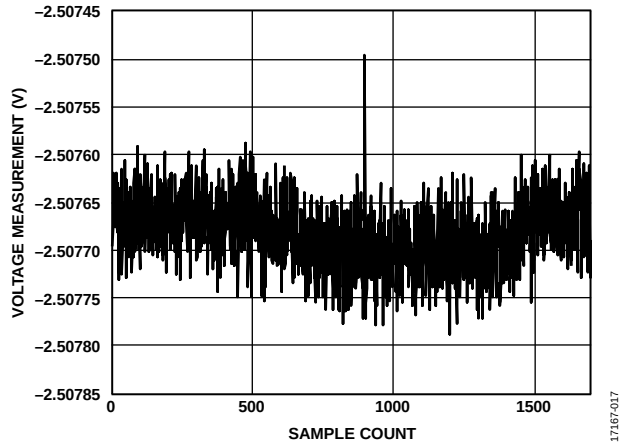


*Figure 14. Voltage Measurement vs. Sample Count, VIN2 to VIN3 During –6 kV ESD*

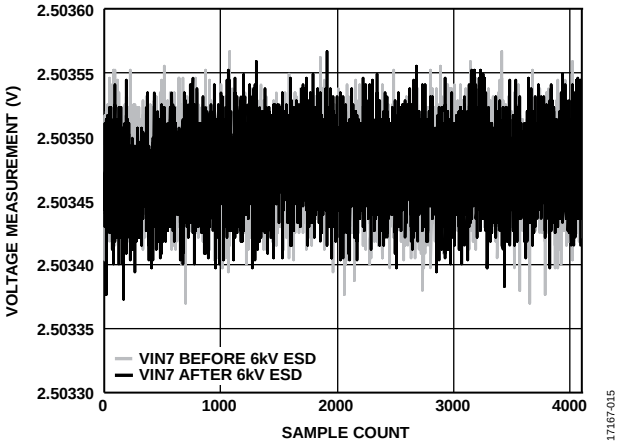


*Figure 15. Voltage Measurement vs. Sample Count, VIN7 Under 6 kV ESD*

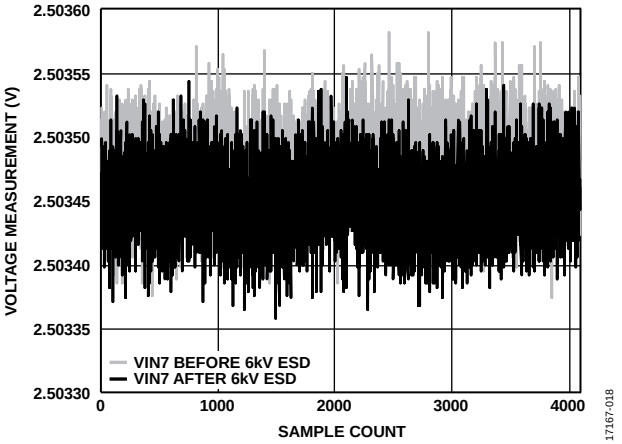


*Figure 16. Voltage Measurement vs. Sample Count, VIN7 Under –6 kV ESD*

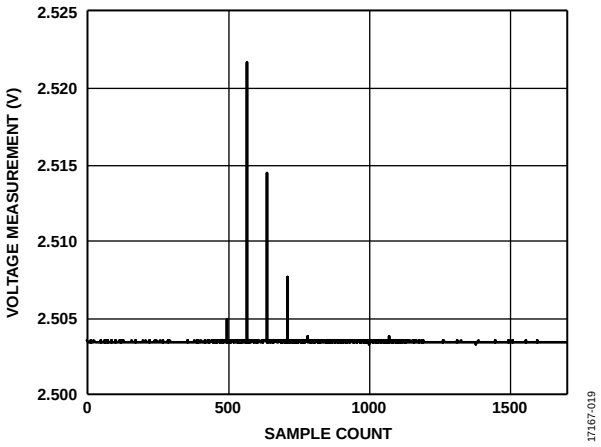


*Figure 17. Voltage Measurement vs. Sample Count, VIN7 During 6 kV ESD*

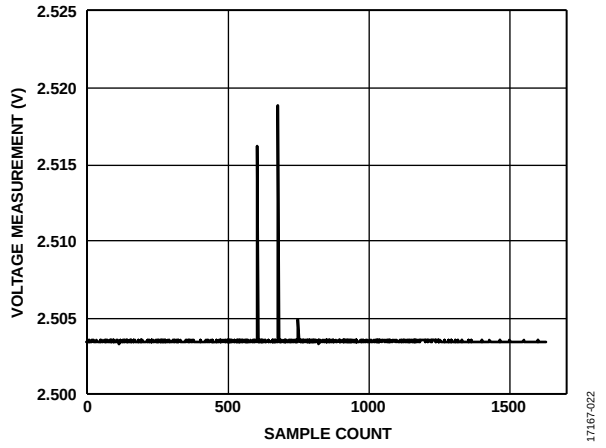


Figure 18. Voltage Measurement vs. Sample Count, VIN7 During –6 kV ESD

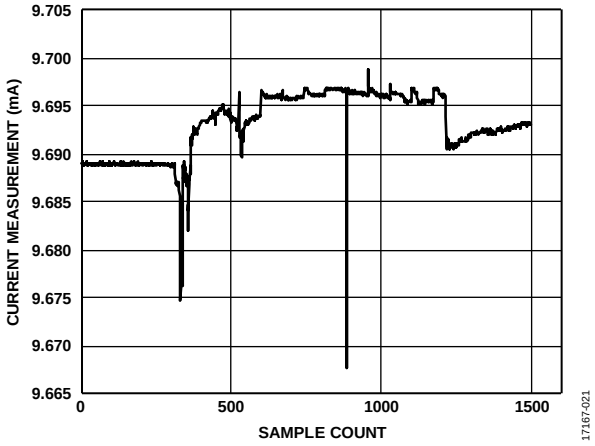


Figure 21. Current Measurement vs. Sample Count, IIN3 During 6 kV ESD

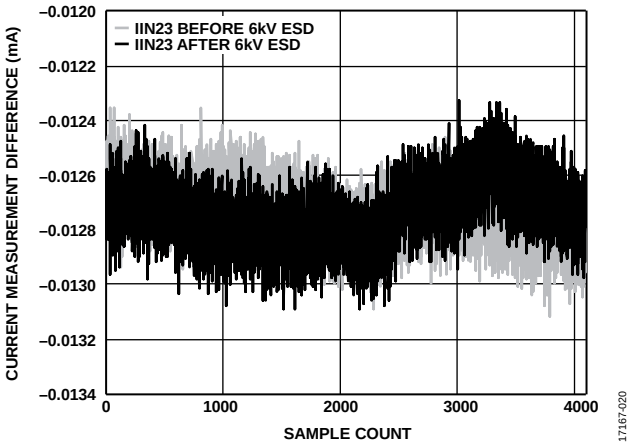


Figure 19. Current Measurement Difference vs. Sample Count, ΔIIN3 Under 6 kV ESD

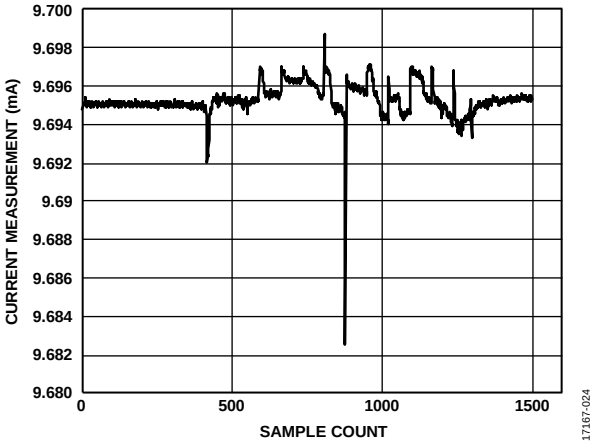


Figure 22. Current Measurement vs. Sample Count, IIN3 During –6 kV ESD

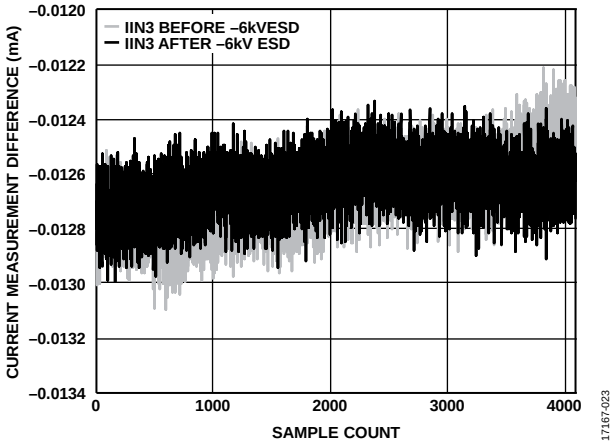


Figure 20. Current Measurement Difference vs. Sample Count, ΔIIN3 Under –6 kV ESD

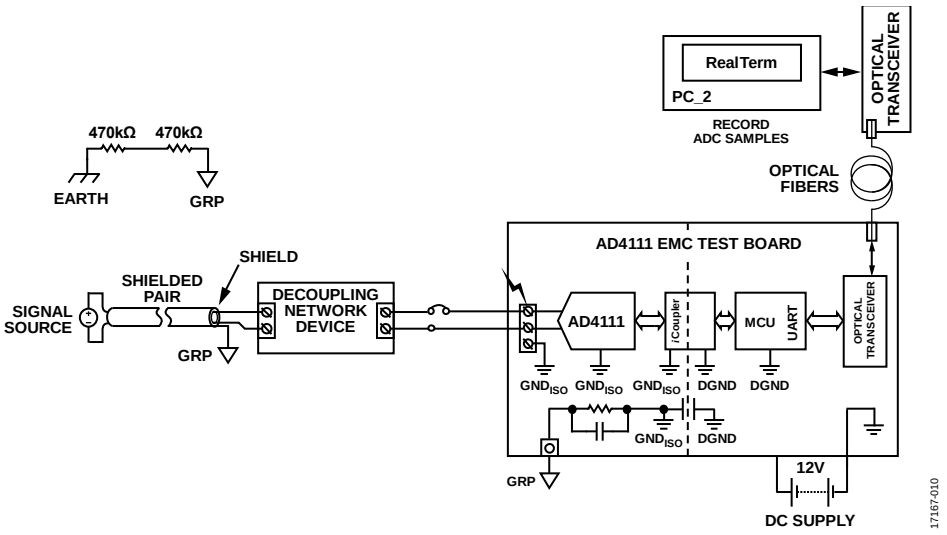


*Figure 23. IEC 61000-4-2 Test Setup Connection Diagram*

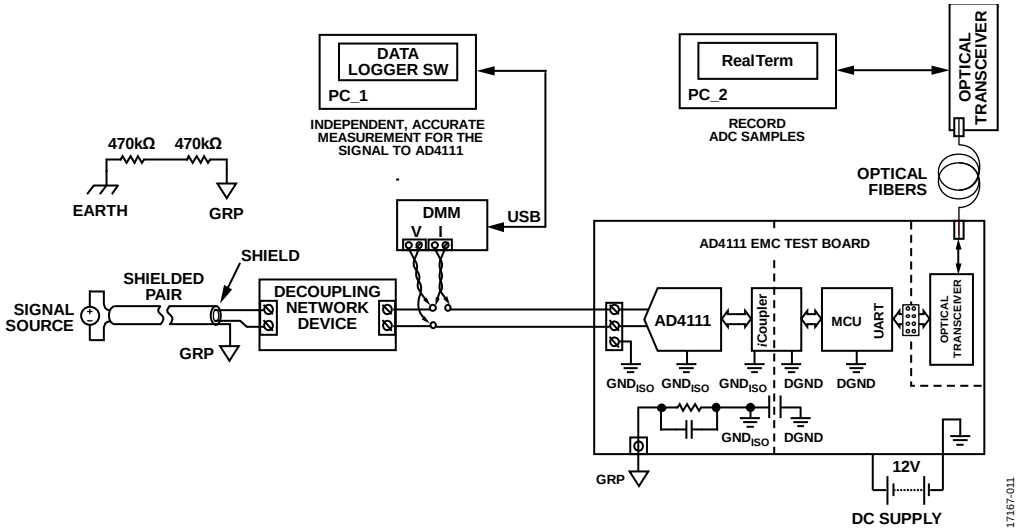


*Figure 24. IEC 61000-4-2 Test Setup, Measurements Before and After Disturbances*

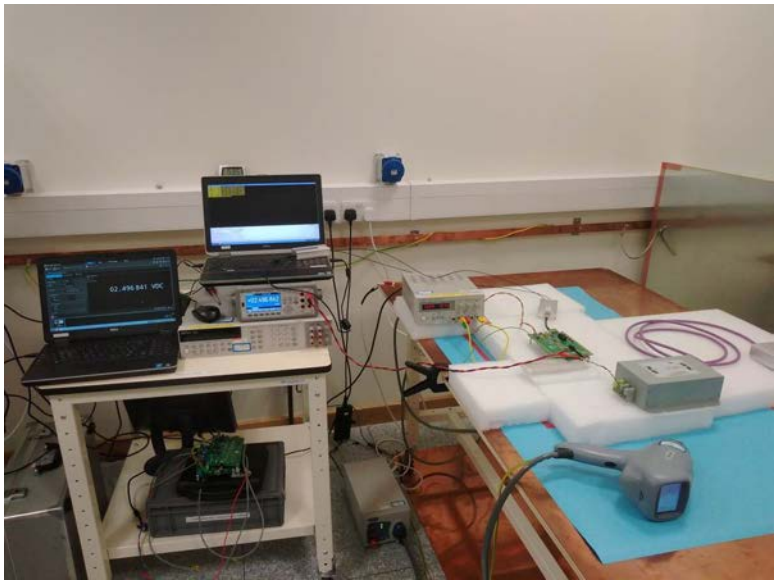


*Figure 25. IEC 61000-4-2 Test Setup Photograph*

**Table 6. IEC 61000-4-2 Test Levels and Results of ±6 kV Contact ESD**

| Input Mode | Zap Point | Test Level (kV) | Before Zap | After Zap | Deviation (ppm) | Pass or Fail |
|---|---|---|---|---|---|---|
| Differential Voltage | VIN2 to VIN3 | 6 | −2.507621 V | −2.507634 V | −5 | Pass, Criterion A |
| | | −6 | −2.507673 V | −2.507674 V | −0.4 | Pass, Criterion A |
| Single-Ended Voltage | VIN7 | 6 | 2.503477 V | 2.503476 V | −0.5 | Pass, Criterion B |
| | | −6 | 2.503480 V | 2.503452 V | −11 | Pass, Criterion B |
| Current | ΔIIN3 | 6 | −12.731 µA | −12.734 µA | −0.4 | Pass, Criterion B |
| | | −6 | −12.669 µA | −12.641 µA | 3 | Pass, Criterion B |

**Table 7. IEC 61000-4-2 Test Results During ±6 kV Contact ESD**

| | | | | During Zap (V) | | |
|---|---|---|---|---|---|---|
| Input Mode | Zap Point | Test Level (kV) | Before Zap (V) | Min | Max | Deviation |
| Differential Voltage | VIN2 to VIN3 | 6 | −2.507621 | −2.507854 | −2.507541 | −32 ppm, 93 ppm |
| | | −6 | −2.507673 | −2.507788 | −2.507496 | −11 ppm, 18 ppm |
| Single-Ended Voltage | VIN7 | 6 | 2.503477 | 2.503362 | 2.521655 | −46 ppm, 0.73% |
| | | −6 | 2.503480 | 2.503291 | 2.518806 | −75 ppm, 0.61% |
| Current | ΔIIN3 | 6 | 9.597673 | 9.667706 | 9.698868 | 0.73%, 1.05% |
| | | −6 | 9.597954 | 9.682500 | 9.698671 | 0.88%, 1.05% |

## IMMUNITY TO ELECTRICAL FAST TRANSIENTS

As per IEC 61000-4-4, the EUT is tested with 2000 V discharges on the analog input cable. Both positive and negative polarity discharges are applied. The length of the hot wire from the coaxial output of the EFT generator to the terminals on the EUT must not exceed 1 m. The duration time of each test sequential is 1 min. The transient and burst waveform is in accordance with IEC 61000-4-4, 5 ns or 50 ns.

The configuration consists of a wooden table 0.8 m high covered with a sheet of copper at least 0.25 mm thick connected to the protective grounding system. The EUT is placed on a 0.1 m thick isolating support. A minimum distance of 0.5 m is provided between the EUT and the walls of the laboratory.

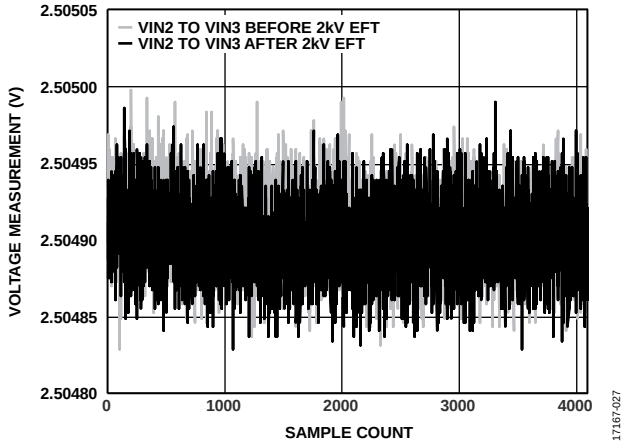


*Figure 26. Voltage Measurement vs. Sample Count, VIN2 to VIN3 Under 2 kV EFT*

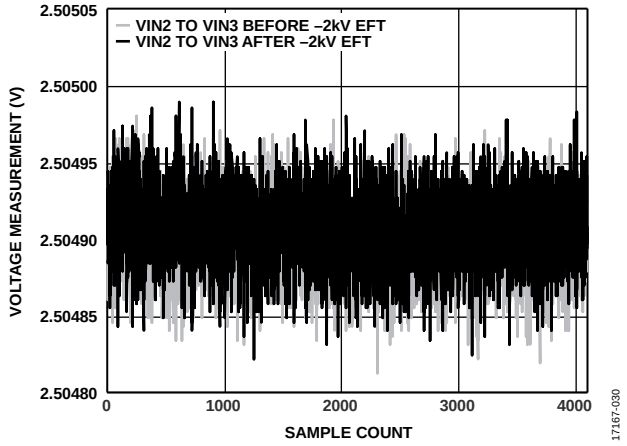


*Figure 27. Voltage Measurement vs. Sample Count, VIN2 to VIN3 Under –2 kV EFT*

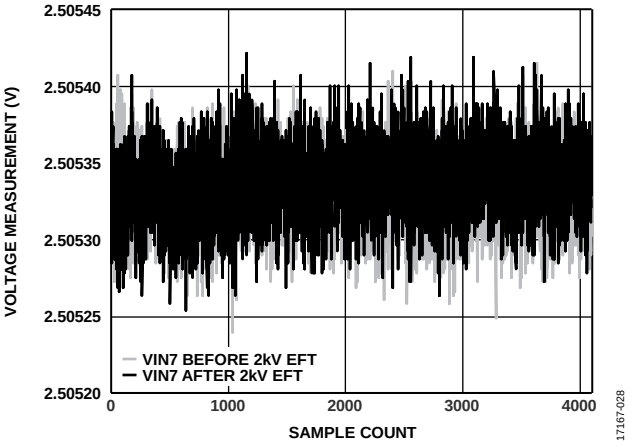


*Figure 28. Voltage Measurement vs. Sample Count, VIN7 Under 2 kV EFT*

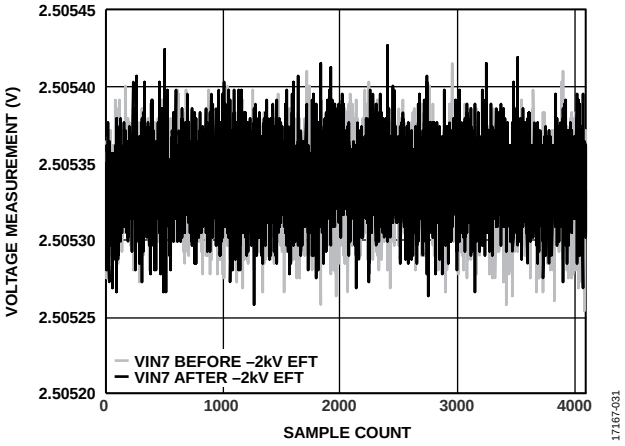


*Figure 29. Voltage Measurement vs. Sample Count, VIN7 Under –2 kV EFT*

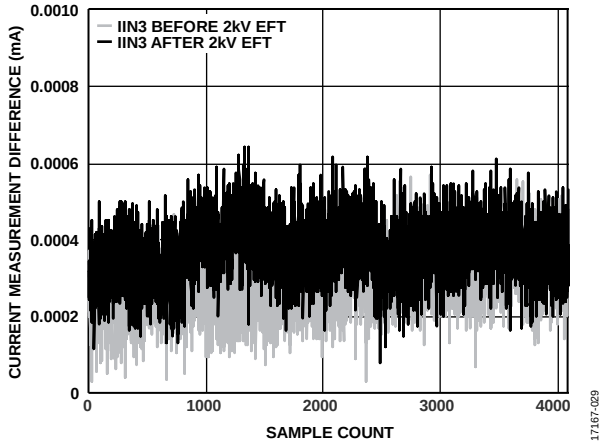


*Figure 30. Current Measurement Difference vs. Sample Count, ΔIIN3 vs. DMM Under 2 kV EFT*

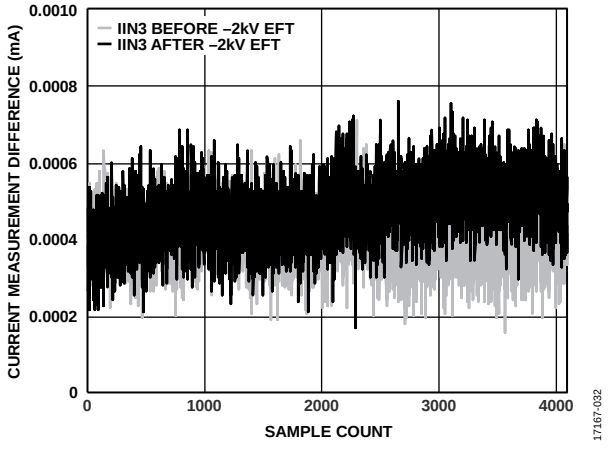


*Figure 31. Current Measurement Difference vs. Sample Count, ΔIIN3 vs. DMM Under –2 kV EFT*

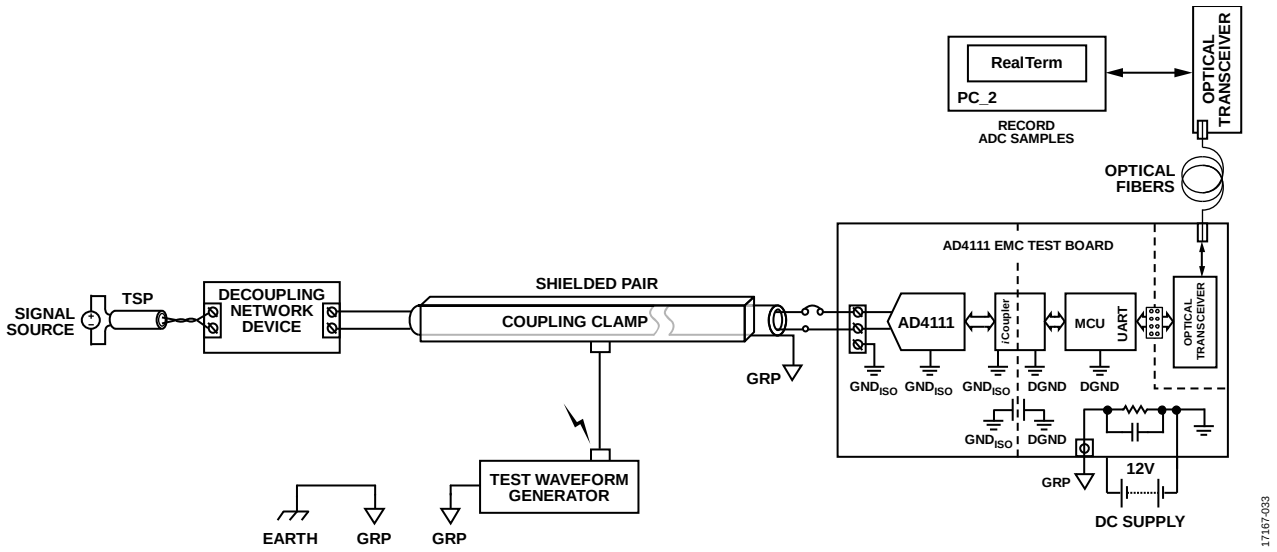


*Figure 32. IEC 61000-4-4 Test Setup Connection Diagram*

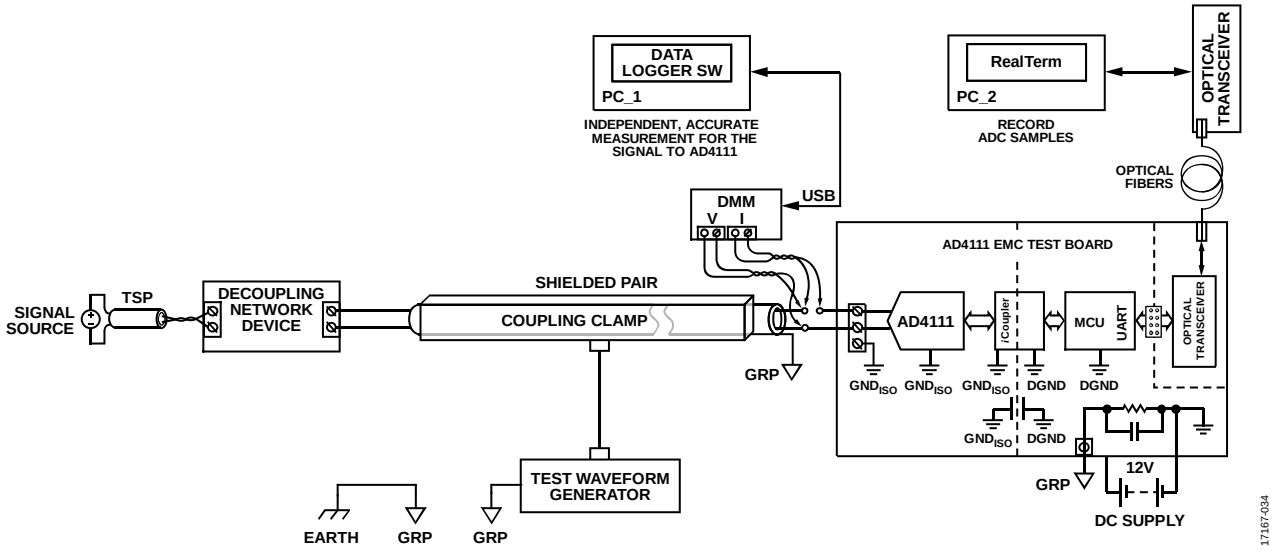


*Figure 33. IEC 61000-4-4 Test Setup, Measurement Before and After Disturbances*

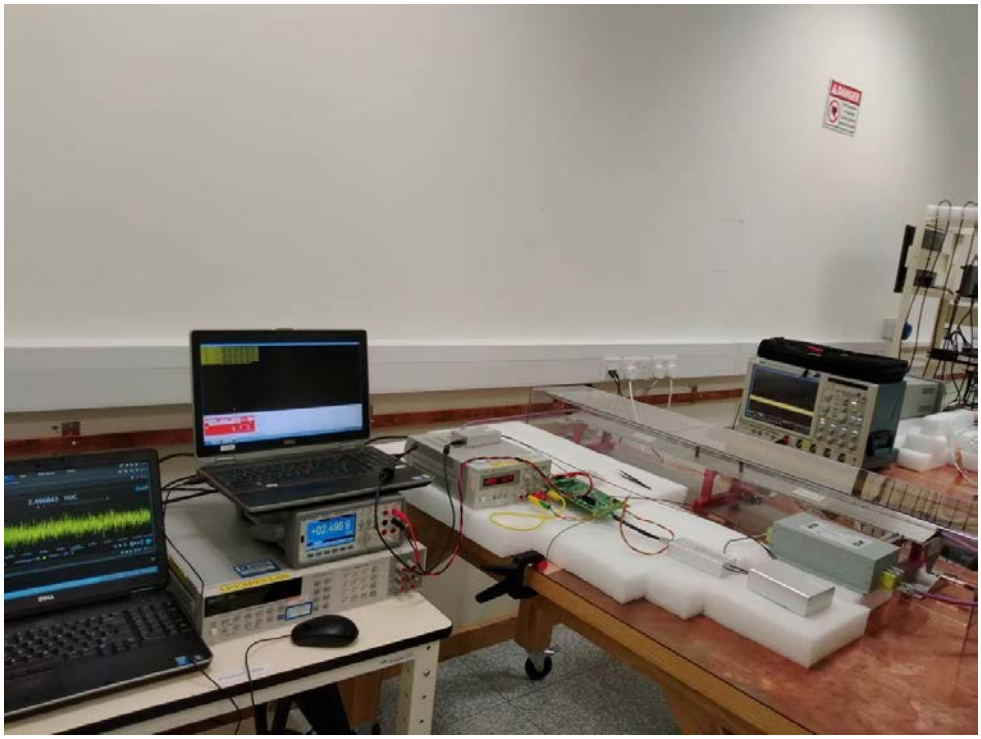


*Figure 34. IEC 610004-4 Test Setup Photograph*

**Table 8. Test Levels and Results of ±2 kV EFT**

| Input Mode | Zap Point | Test Level (kV) | Before Zap | After Zap | Deviation (ppm) | Pass or Fail |
|---|---|---|---|---|---|---|
| Differential Voltage | VIN2 to VIN3 | 2 | 2.504909 V | 2.504802 V | −0.1 | Pass, Criterion B |
| | | −2 | 2.504900 V | 2.504908 V | −0.5 | Pass, Criterion B |
| Single-Ended Voltage | VIN7 | 2 | 2.505330 V | 2.505337 V | −0.2 | Pass, Criterion B |
| | | −2 | 2.505335 V | 2.505339 V | 0.2 | Pass, Criterion B |
| Current | IIN3 | 2 | 0.292 µA | 0.373 µA | 9 | Pass, Criterion B |
| | | −2 | 0.404 µA | 0.474 µA | 8 | Pass, Criterion B |

## IMMUNITY TO SURGE

As per IEC 61000-4-5, the surge is a combination wave of 1.2 µS and 50 µS open circuit voltage, 8 µS and 20 µS short circuit current. The EUT is subject to five positive and five negative surges at each rating. The interval between each surge is 1 min. The surge is tested to the AD4111 input cable, which is treated as unshielded asymmetrically operated interconnection lines of the EUT. The surge is applied to the lines via the capacitive coupling. The coupling and decoupling networks cannot influence the specified functional conditions of the EUT. The interconnection line between the EUT and the coupling and decoupling networks is 2 m in length (or shorter).

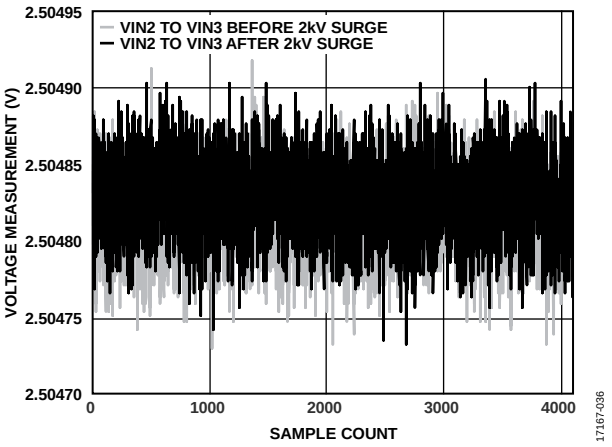


*Figure 35. Voltage Measurement vs. Sample Count, VIN2 to VIN3 Under 2 kV Surge*

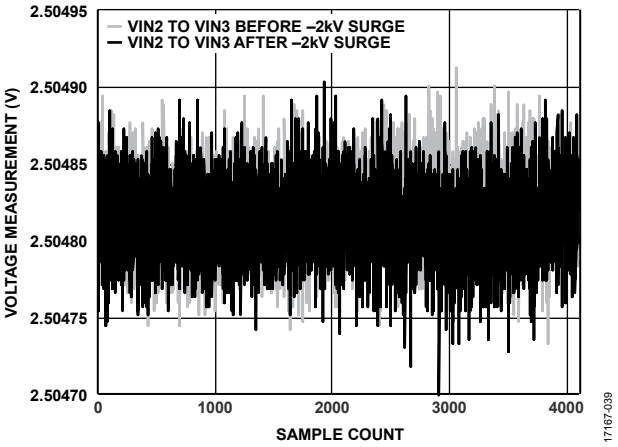


*Figure 36. Voltage Measurement vs. Sample Count, VIN2 to VIN3 Under –2 kV Surge*

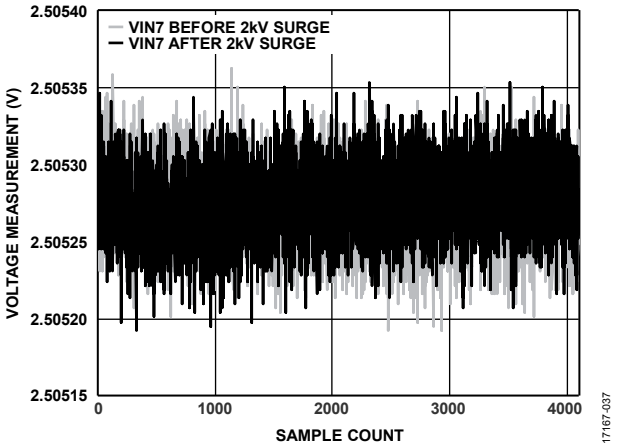


*Figure 37. Voltage Measurement vs. Sample Count, VIN7 Under 2 kV Surge*

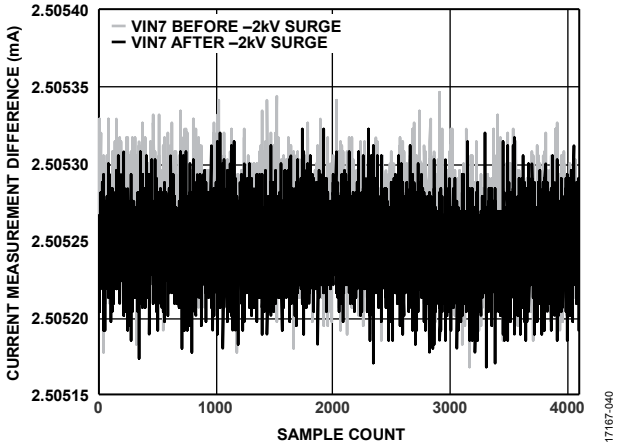


*Figure 38. Current Measurement Difference vs. Sample Count, VIN7 Under –2 kV Surge*

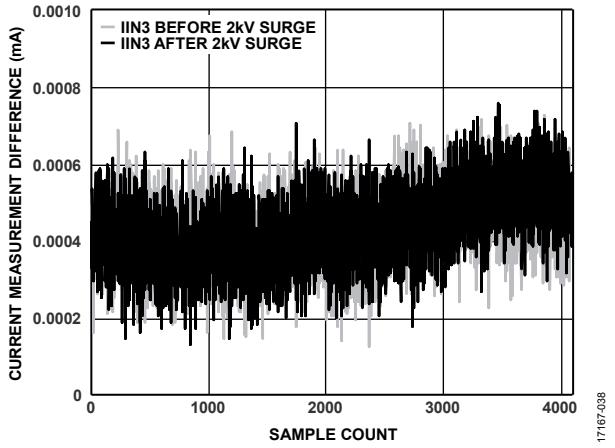


*Figure 39. Current Measurement Difference vs. Sample Count, ΔIIN3 vs. DMM Under 2 kV Surge*

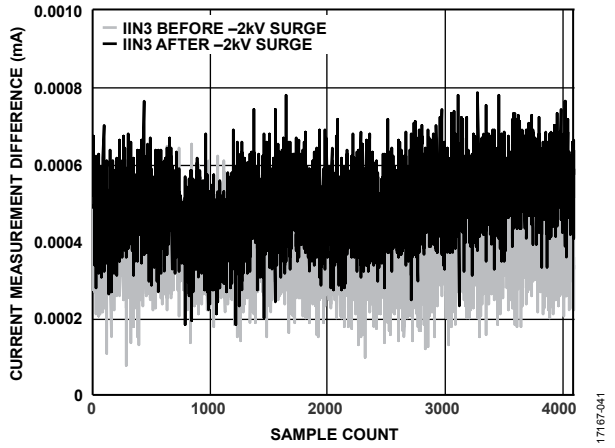


*Figure 40. Current Measurement Difference vs. Sample Count, ΔIIN3 vs. DMM Under –2 kV Surge*

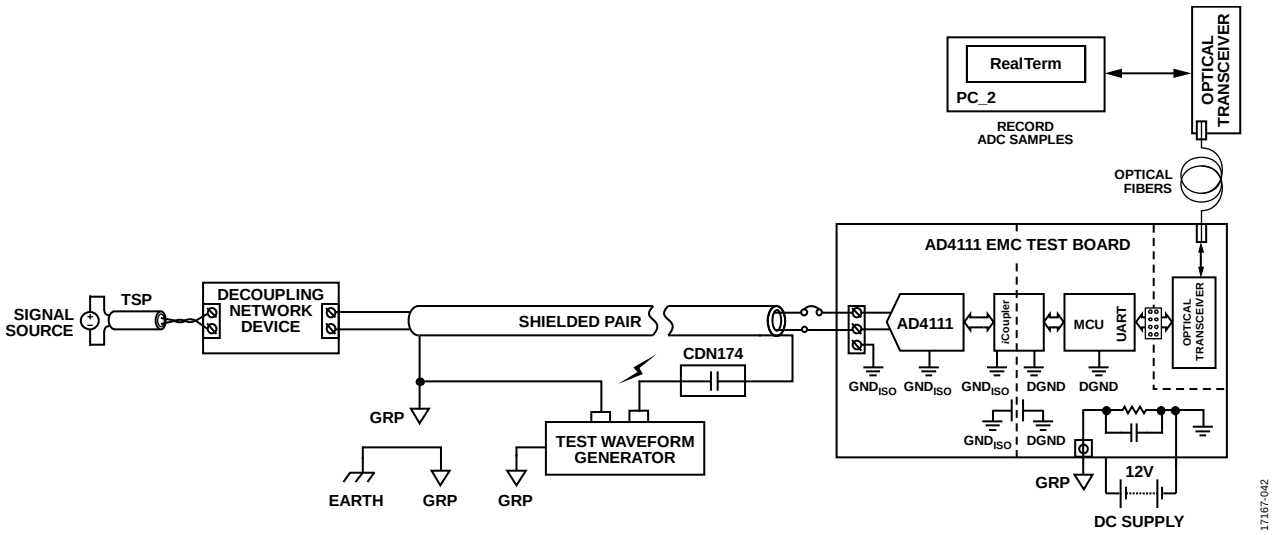


*Figure 41. IEC 61000-4-5 Test Setup Connection Diagram*

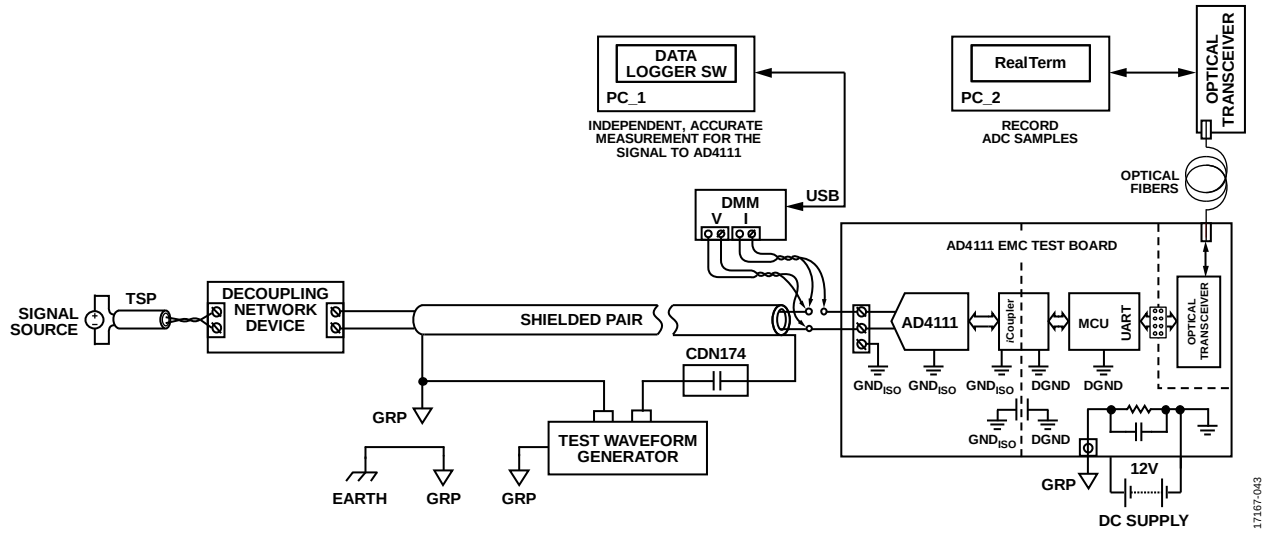


*Figure 42. IEC 61000-4-5 Test Setup Connection Diagram, Measurements Before and After Disturbances*

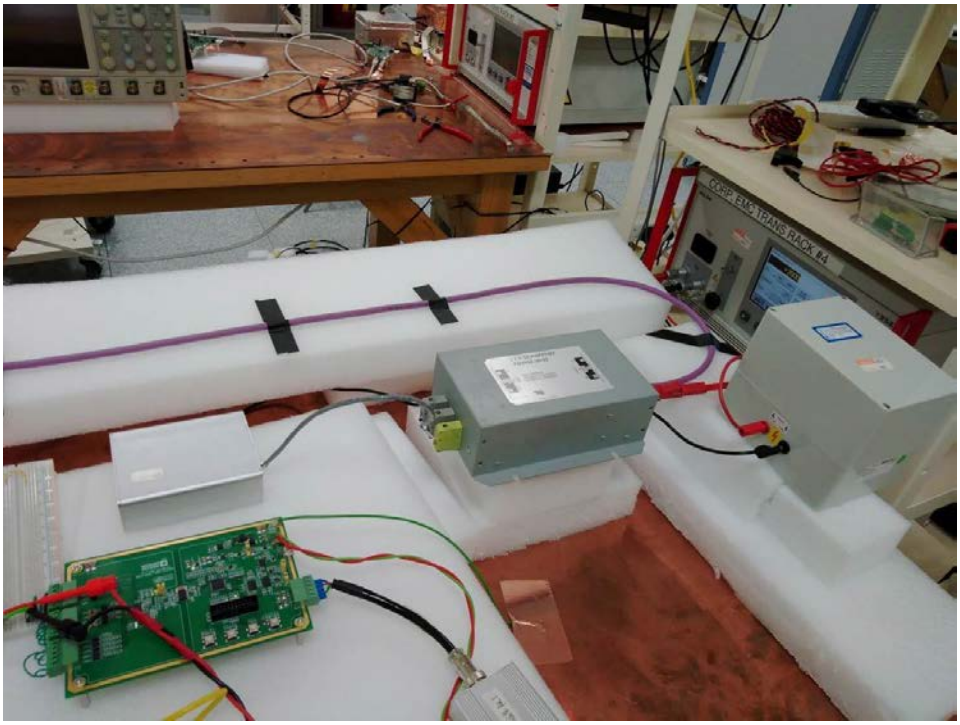


*Figure 43. IEC 61000-4-5 Test Setup Photograph*

**Table 9. IEC 61000-4-5 Test Levels and Results**

| Input Mode | Zap Point | Test Level (kV) | Before Zap | After Zap | Deviation (ppm) | Pass or Fail |
|---|---|---|---|---|---|---|
| Differential Voltage | VIN2 to VIN3 | 2 | 2.504817 V | 2.504828 V | 5 | Pass, Criterion B |
| | | −2 | 2.504820 V | 2.504813 V | −3 | Pass, Criterion B |
| Single-Ended Voltage | VIN7 | 2 | 2.505272 V | 2.505276 V | 2 | Pass, Criterion B |
| | | −2 | 2.505263 V | 2.505248 V | −6 | Pass, Criterion B |
| Current | IIN3 | 2 | 0.435 µA | 0.440 µA | 0.5 | Pass, Criterion B |
| | | −2 | 0.375 µA | 0.496 µA | 13 | Pass, Criterion B |

## RADIATED IMMUNITY

As per IEC 61000-4-3, the test is performed in a fully anechoic chamber. The EUT is placed on a nonconductive table 0.8 m in height. The AD4111 inputs are shorted to its isolated ground. The transmit antenna is located at a distance of 3 m from the EUT. The frequency range is swept from 80 MHz to 1000 MHz with the signal 80% amplitude modulated with a 1 kHz sinewave. The frequency range is swept incrementally, and the step size is 1% of the preceding frequency value. The dwell time at each frequency is 1 sec, and cannot be less than the time necessary for the EUT to respond. The field strength is 10 V/m. The test is performed with the EUT exposed to both a vertically and horizontally polarized field. The AD4111 samples are sent to the host PC that is outside of the chamber through optically isolated data link.

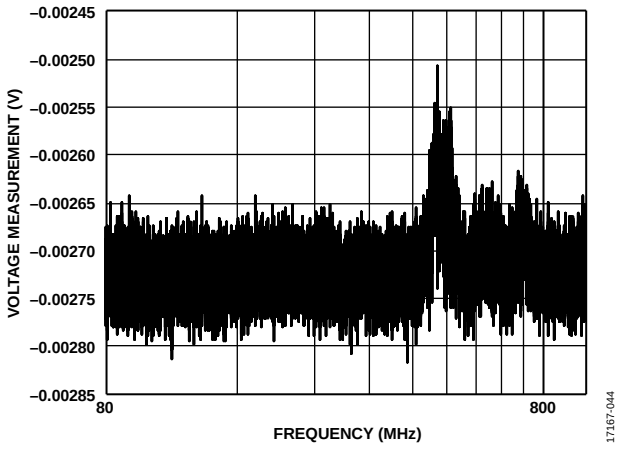


*Figure 44. Voltage Measurement vs. Frequency, VIN2 to VIN3 Under 10 V/m, Horizontal Antenna*

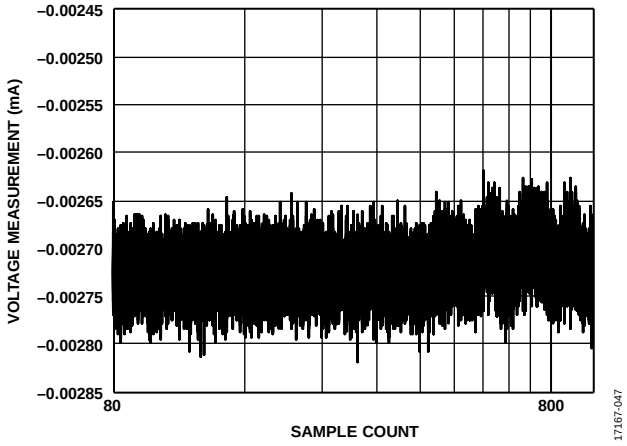


*Figure 45. Voltage Measurement vs. Frequency, VIN2 to VIN3 Under 10 V/m, Vertical Antenna*

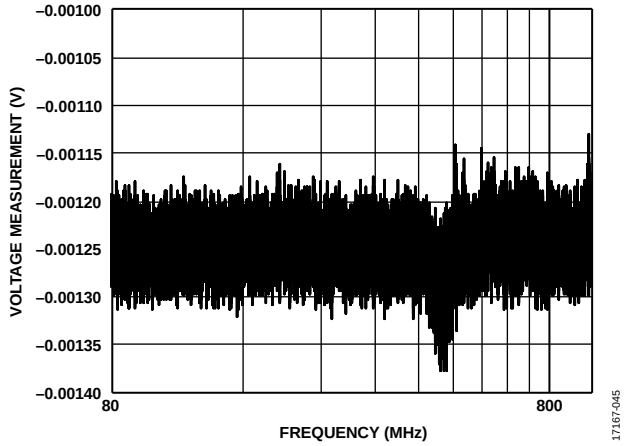


*Figure 46. Voltage Measurement vs. Frequency, VIN7 Under 10 V/m, Horizontal Antenna*

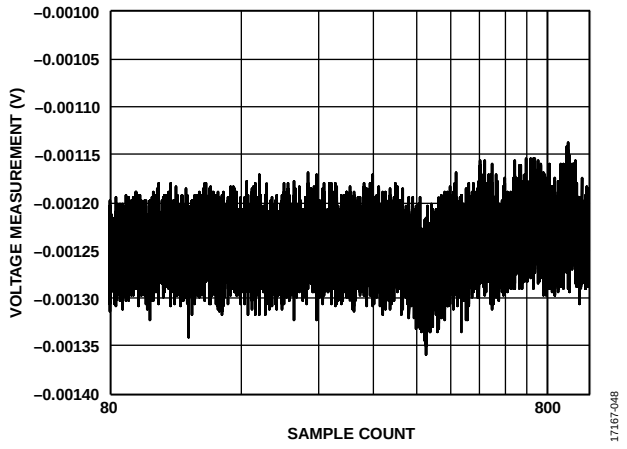


*Figure 47. Voltage Measurement vs. Frequency, VIN7 Under 10 V/m, Vertical Antenna*

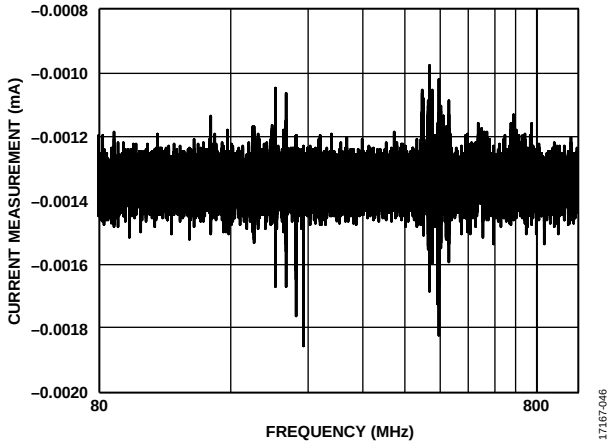


*Figure 48. Current Measurement vs. Frequency, IIN3 Under 10 V/m, Horizontal Antenna*

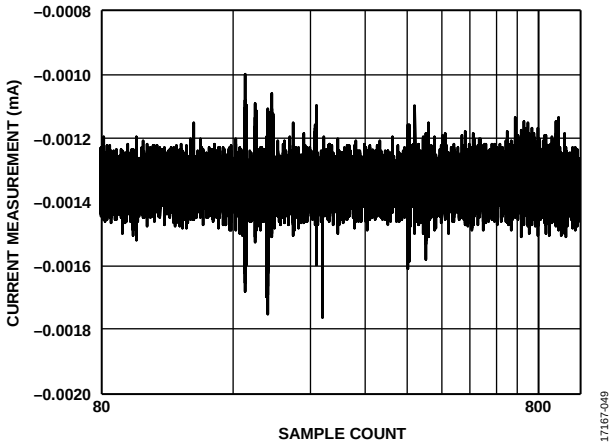


*Figure 49. Current Measurement vs. Frequency, IIN3 Under 10 V/m, Vertical Antenna*

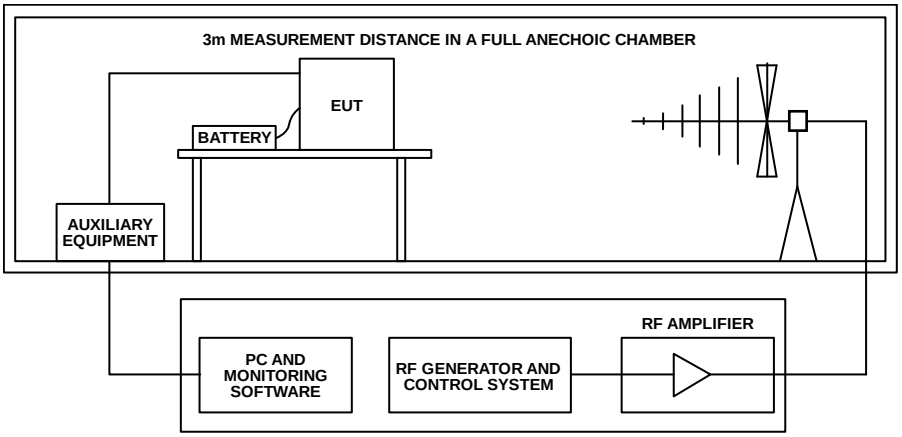


*Figure 50. IEC 61000-4-3 Test Setup Configuration Diagram*


*Figure 51. IEC 61000-4-3 Test Setup Photograph*

**Table 10. IEC 61000-4-3 Test Levels and Results, 10 V/m Radiated RF Immunity**

| | | | During Zap | | | | |
|---|---|---|---|---|---|---|---|
| **Input Mode** | **Input Channel** | **Average** | **Min** | **Max** | **Deviation (ppm)** | **Antenna** | **Pass or Fail** |
| Differential Voltage | VIN2 to VIN3 | −2.729 mV | −2.816 mV | −2.506 mV | 22 × FS | Horizontal | Pass, Criterion A |
| | | −2.728 mV | −2.819 mV | −2.620 mV | 11 × FS | Vertical | Pass, Criterion A |
| Single-Ended Voltage | VIN7 | −1.249 mV | −1.377 mV | −1.130 mV | −13 × FS | Horizontal | Pass, Criterion A |
| | | −1.248 mV | −1.359 mV | −1.138 mV | 11 × FS | Vertical | Pass, Criterion A |
| Current | IIN3 | −1.345 µA | −1.854 µA | −0.978 µA | −25 × FSR | Horizontal | Pass, Criterion A |
| | | −1.343 µA | −1.764 µA | −1.001 µA | −21 × FSR | Vertical | Pass, Criterion A |

## RADIATED EMISSIONS

As per CISPR 11, the EUT is placed on the top of a rotating table 0.8 m above the ground in a 10 m semianechoic chamber. The table is rotated 360° to identify the position of the highest radiation. The EUT is set 10 m away from the interference receiving antenna, which can be set to horizontal or vertical polarization position. The antennas are mounted on the top of a variable height antenna tower. The heights of the antennas vary from 1 m to 4 m above the ground to identify the maximum value of the field strength. The EUT is configured to its worst case, the antenna is tuned to a height from 1 m to 4 m, and the table is turned from 0 degrees to 360° to find the maximum reading. The test receiver system is set to quasi peak detection mode. The EUT is powered by a 12 V dc battery pack. As such, any radiated emission from the auxiliary supply can be excluded.

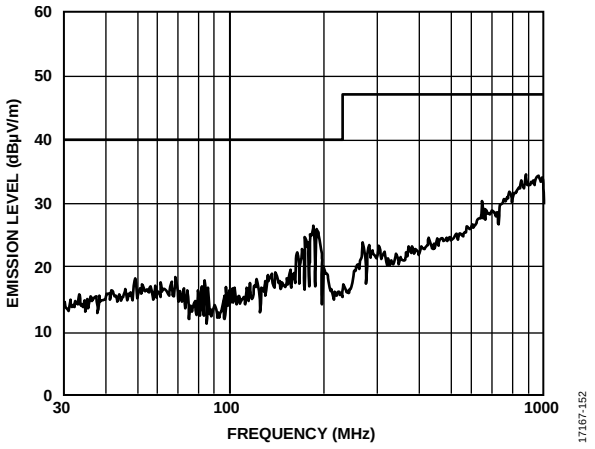


*Figure 52. Emission Level vs. Frequency, Radiated Emissions, Vertical Antenna Polarization*

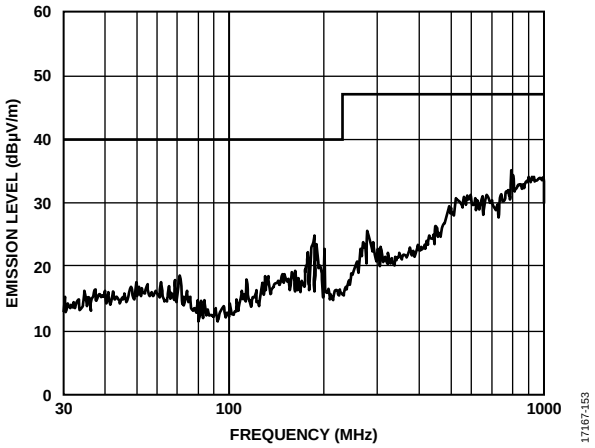


*Figure 53. Emission Level vs. Frequency, Radiated Emissions, Horizontal Antenna Polarization*

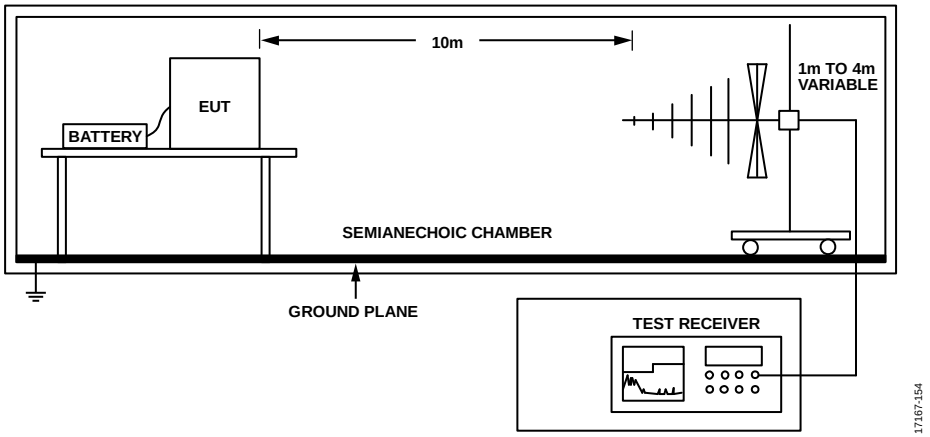


*Figure 54. CISPR 11 Test Setup Configuration Diagram*

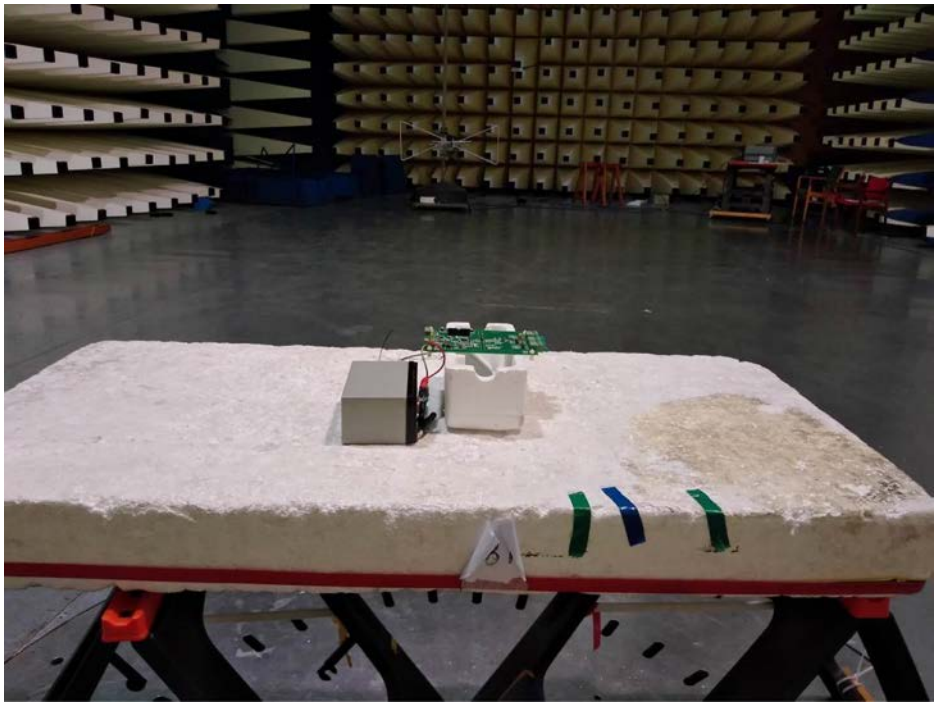


*Figure 55. CISPR 11 Test Setup Photograph*

**Table 11. CISPR 11 Radiated Emissions, Vertical Antenna Polarization at Critical Frequencies**

| Frequency (MHz) | Result (dBµV) | Limit (dBµV) | Margin (dB) | Height (cm) | Antenna Polarity | Conditions |
|---|---|---|---|---|---|---|
| 140.004 | 14.8 | 40 | −25.2 | 1 | Vertical | Quasi peak |
| 890.712 | 28.9 | 47 | −18.1 | 1 | Vertical | Quasi peak |

**Table 12. CISPR 11 Radiated Emissions, Horizontal Antenna Polarization at Critical Frequencies**

| Frequency (MHz) | Result (dBµV) | Limit (dBµV) | Margin (dB) | Height (cm) | Antenna Polarity | Conditions |
|---|---|---|---|---|---|---|
| 187.216 | 32.5 | 40 | −7.5 | 4 | Horizontal | Quasi peak |
| 201.360 | 25.6 | 40 | −14.4 | 2.5 | Horizontal | Quasi peak |
| 276.256 | 29.2 | 47 | −17.8 | 4 | Horizontal | Quasi peak |
| 567.672 | 29.7 | 47 | −17.3 | 1 | Horizontal | Quasi peak |
| 788.512 | 36.9 | 47 | −10.1 | 3 | Horizontal | Quasi peak |

# EMC BOARD SCHEMATICS AND ARTWORK

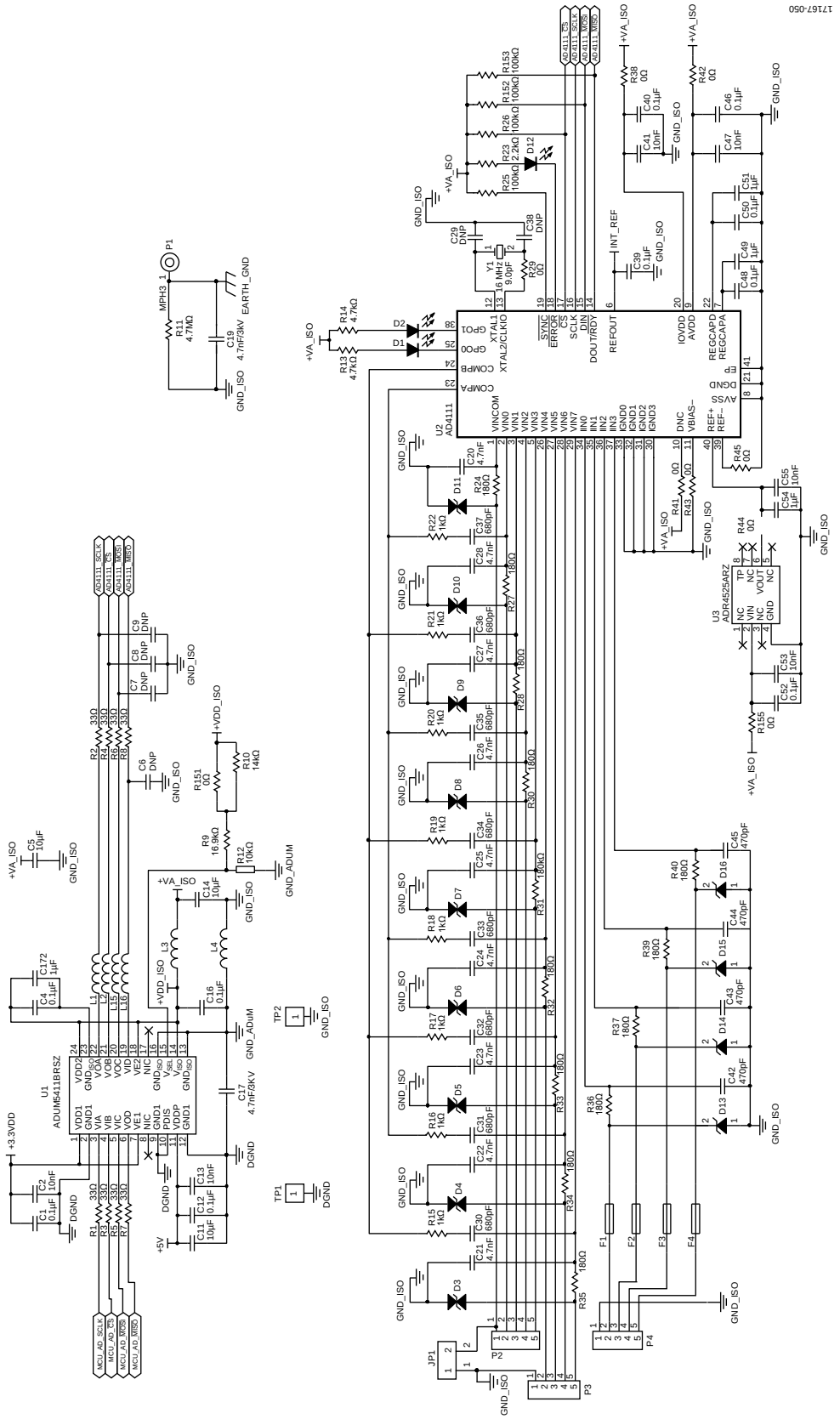

*Figure 56. EMC Board Schematics, AD4111 and ADuM5411*

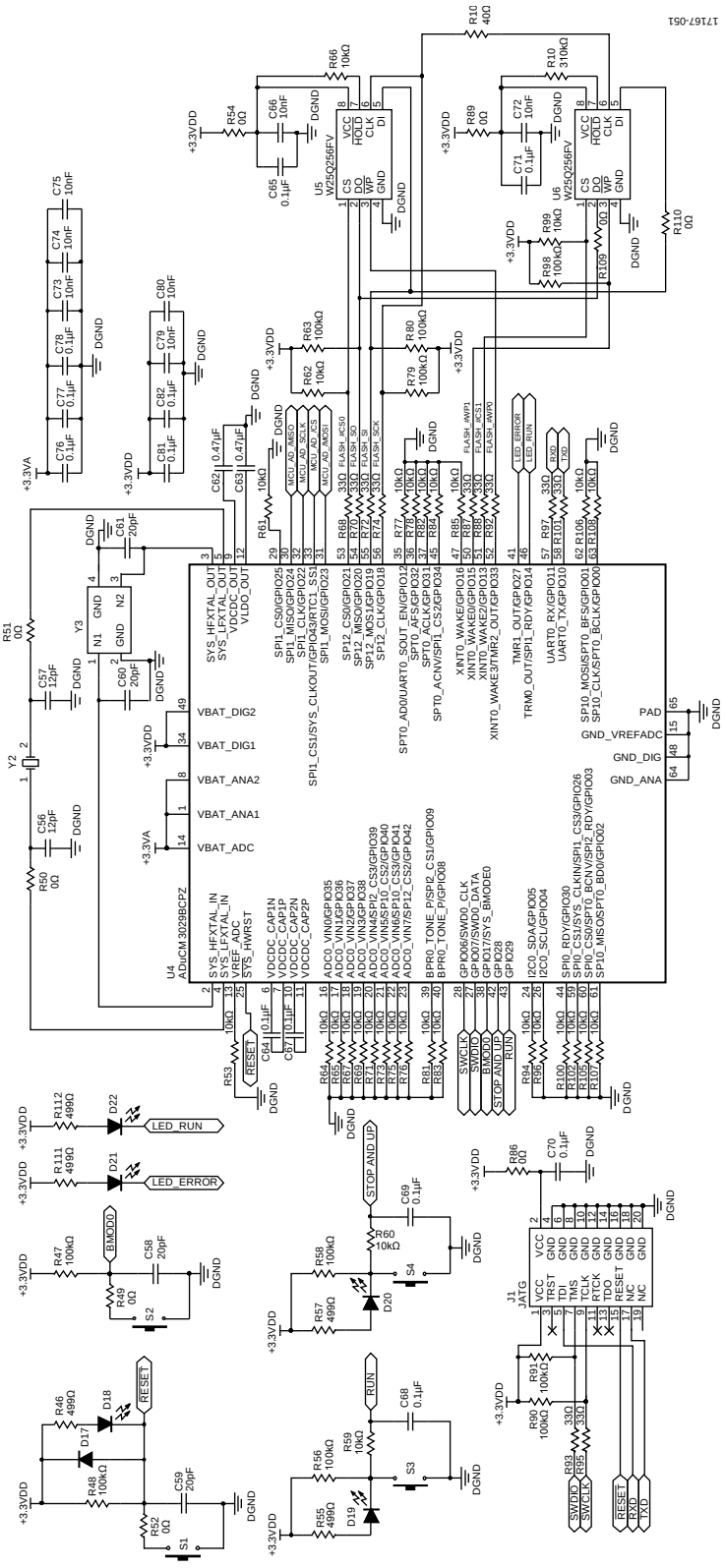

*Figure 57. EMC Board Schematics, MCU and Periphery*

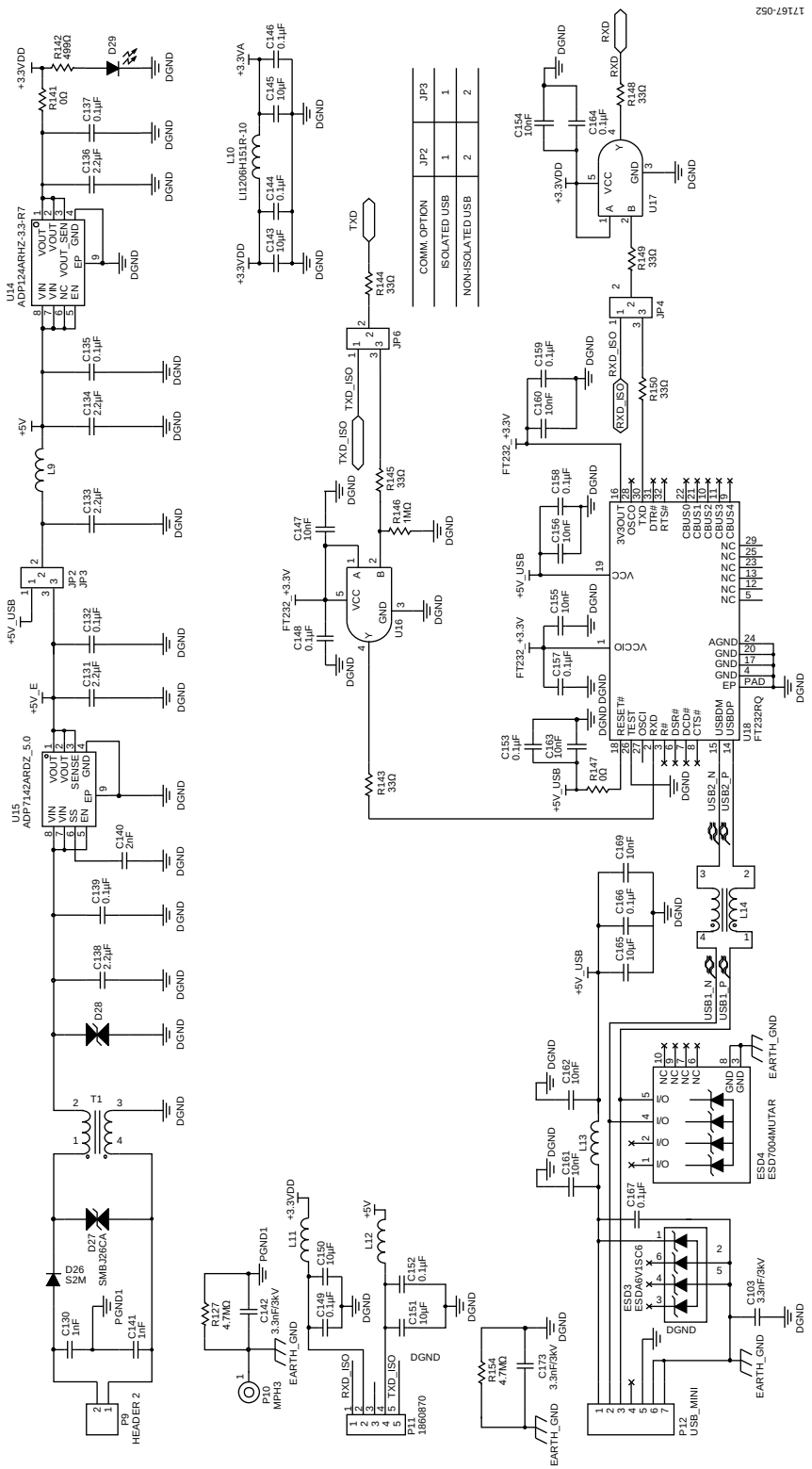


*Figure 58. EMC Board Schematics, Power Supply and Communication Interface*

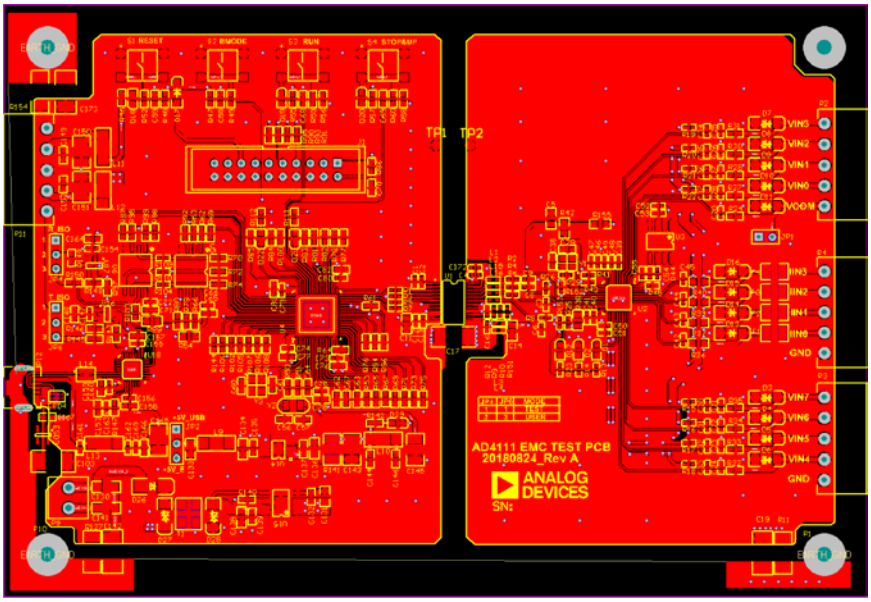


*Figure 59. Layer 1, Top Side*

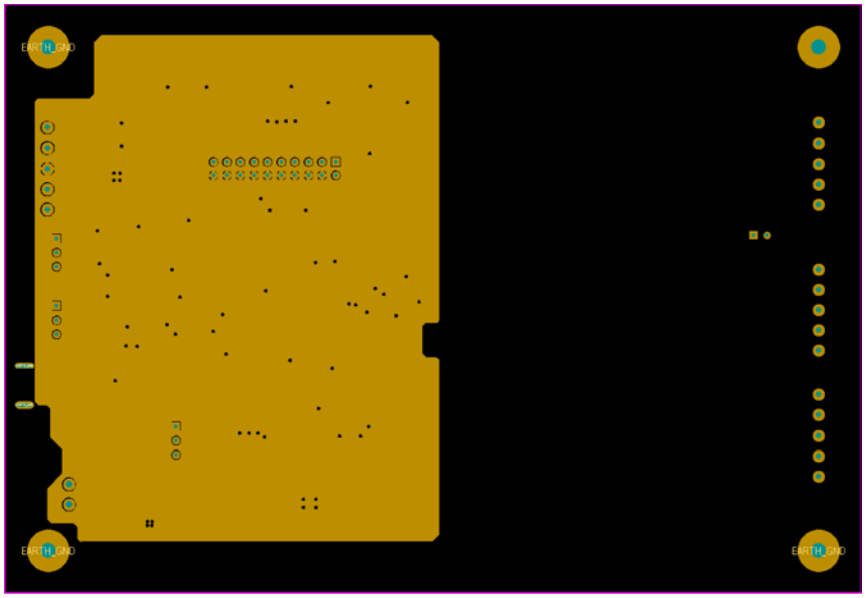


*Figure 60. Layer 2, Inner Ground Plane*

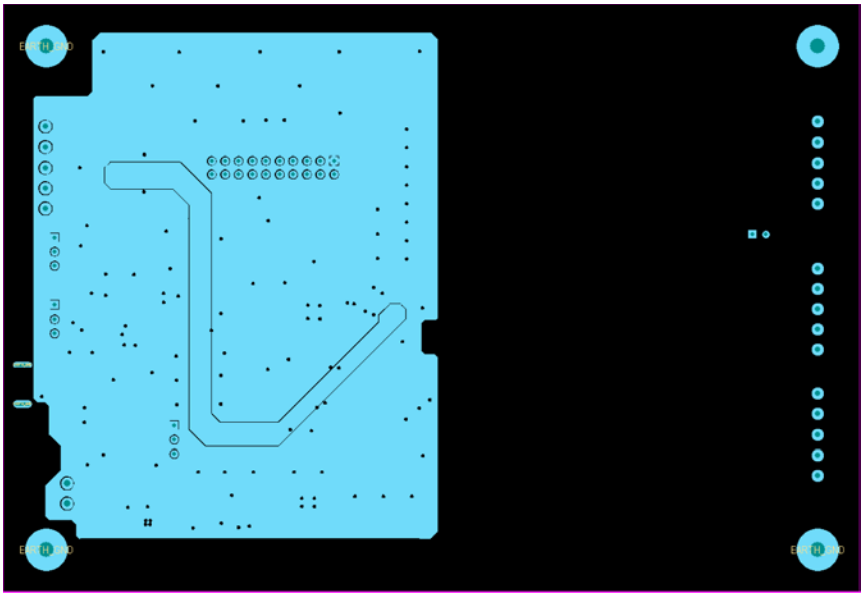


*Figure 61. Layer 3, Inner Power Plane*

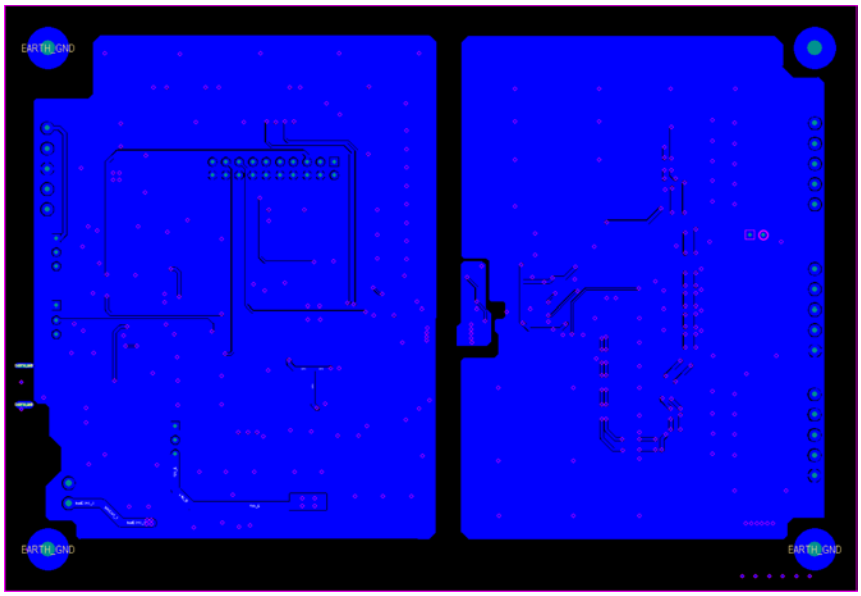


*Figure 62. Layer 4, Bottom Side*

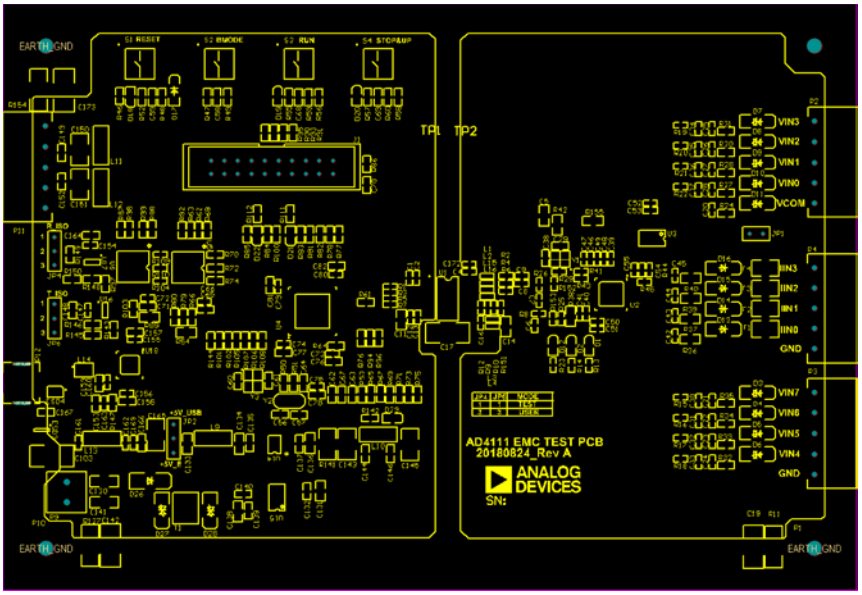


*Figure 63. Silkscreen Top*

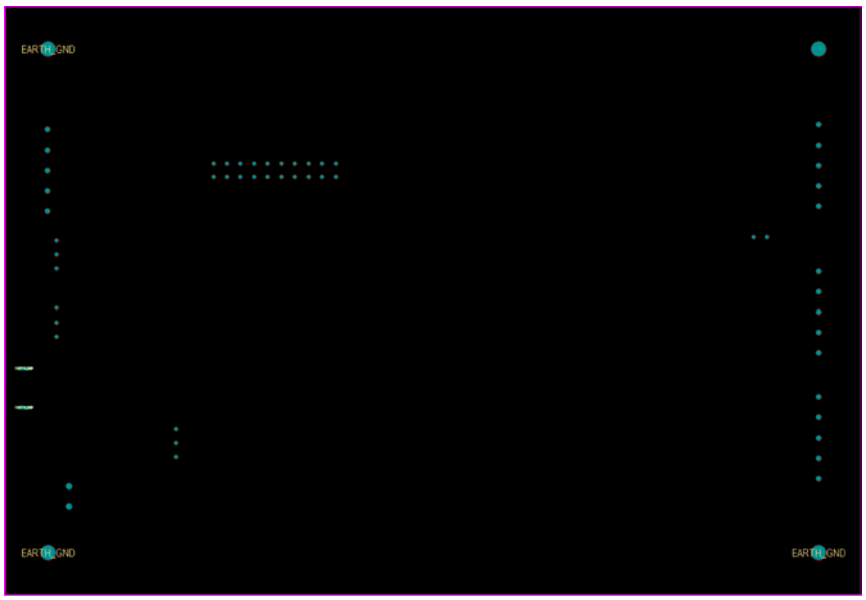


*Figure 64. Silkscreen Bottom*

# ORDERING INFORMATION

## BILL OF MATERIALS

**Table 13.**

| Reference Designator | Part Description | Value | Part Number | Farnell Order Code | Manufacturer |
|---|---|---|---|---|---|
| C1, C4, C12, C16, C39, C40, C46, C48, C50, C52 | Capacitor, ceramic, 0.1 µF, 50 V, X5R, 0402 | 0.1 µF | GRM155R61H104KE19D | FEC-2218856 | Murata |
| C2, C3, C13, C41, C47, C53, C55, C66, C72, C73, C74, C75, C79, C80, C147, C154, C155, C156, C160, C161, C162, C163, C169 | Capacitor, ceramic, 0.01 µF, 50 V, X5R, 0402 | 0.01 µF | GRM155R71H102JA01D | FEC-2470474 | Murata |
| C5, C11, C14 | Capacitor, ceramic, 10 µF, 10 V, X7R, 0805 | 10 µF | C2012X7R1A106K125AC | FEC-2346934 | TDK |
| C6, C7, C8, C9 | Capacitor, ceramic, 0402 | Do not populate (DNP) | Not applicable | Not applicable | Not applicable |
| C17, C19 | Capacitor, ceramic, 4.7 nF, 2000 V, X7R, 1812 | 4.7 nF | CC1812KKX7RDBB472 | FEC-1284179 | Yageo |
| C20, C21, C22, C23, C24, C25, C26, C27, C28 | Capacitor, ceramic, 4.7 nF, 50 V, C0G, 0402 | 4.7 nF | GRT155R71H472KE01D | FEC-2672129 | Murata |
| C29, C38 | Capacitor, ceramic, 0603 | DNP | Not applicable | Not applicable | Not applicable |
| C30, C31, C32, C33, C34, C35, C36, C37 | Capacitor, ceramic, 680 pF, 50 V, X7R, 0402 | 680 pF | GRT155R71H681KE01D | FEC-2672130 | Murata |
| C42, C43, C44, C45 | Capacitor, ceramic, 470 pF, 50 V, C0G, 0402 | 470 pF | GRM1555C1H471JA01D | FEC-8819688 | Murata |
| C49, C51, C54, C172 | Capacitor, ceramic, 1 µF, 16 V, X5R, 0402 | 1 µF | GRM155R61C105KA12D | FEC-2362093 | Murata |
| C56, C57 | Capacitor, ceramic, 12 pF, 50 V, C0G, 0603 | 12 pF | GRM1885C1H120JA01D | FEC-1828907 | Murata |
| C58, C59, C60, C61 | Capacitor, ceramic, 20 pF, 50 V, C0G, 0402 | 20 pF | MC0402N200J500CT | FEC-2627461 | Multicomp |
| C62, C63 | Capacitor, ceramic, 0.47 µF, 50 V, X7R, 0603 | 0.47 µF | UMK107B7474KA-TR | FEC-2779057 | Taiyo Yuden |
| C64, C65, C67, C68, C69, C70, C71, C76, C77, C78, C81, C82, C132, C135, C137, C139, C144, C146, C148, C149, C152, C153, C157, C158, C159, C164, C166, C167 | Capacitor, ceramic, 0.1 µF, 50 V, X7R, 0603 | 0.1 µF | MCSH18B104K500CT | FEC-1856385 | Multicomp |
| C103, C142 | Capacitor, ceramic, 3300 pF, 3 kV, X7R, 1812 | 3.3 nF | HV1812Y332KXHATHV | FEC-2611555 | Vishay |
| C130, C141 | Capacitor, ceramic, 1000 pF, 50 V, X7R, 1206 | 1 nF | C1206C102M5RACTU | FEC-2678368 | KEMET |
| C131, C133, C134, C136, C138 | Capacitor, ceramic, 2.2 µF, 50 V, X7R, 0805 | 2.2 µF | UMK212BB7225KG-T | FEC-2779058 | Taiyo Yuden |
| C140 | Capacitor, ceramic, 2000 pF, 50 V, C0G, 0603 | 2 nF | GRM1885C1H202JA01D | FEC-2470480 | Murata |
| C143, C145, C150, C151, C165 | Capacitor, ceramic, 10 µF, 25 V, X7R, 1210 | 10 µF | C1210C106K3RACAUTO | FEC-2665759 | KEMET |
| C173 | Capacitor, ceramic, 1812 | Not applicable | Not applicable | Not applicable | Not Applicable |

| Reference Designator | Part Description | Value | Part Number | Farnell Order Code | Manufacturer |
|---|---|---|---|---|---|
| D1, D2 | Light emitting diode (LED), yellow, 0603, surface mount device (SMD) | LED | TLMY1000-GS08 | FEC-1328310 | Vishay |
| D12, D21 | LED, red, 0603, SMD | LED | TLMS1000-GS08 | FEC-1328308 | Vishay |
| D18, D19, D20, D22, D29 | LED, green, 0603, SMD | LED | KPT-1608LVZGCK | FEC-2610409 | Kingbright |
| D13, D14, D15, D16 | TVS diode, 10 V, 19.6 V, Subminiature Version A (SMA) | TVS | SMA6J10A-TR | Digi-Key 497-5915-1-ND | STMicroelectronics |
| D17 | Diode, general-purpose, 75 V, 150 mA, SOD123 | 1N4148 | 1N4148W-E3-08 | FEC-2433353 | Vishay |
| D26 | Diode, general-purpose, 1 kV, 2 A, DO214AA | S2M | S2M | FEC-2677413 | Taiwan Semiconductor |
| D3, D4, D5, D6, D7, D8, D9, D10, D11 | TVS diode, 33 V, 69.7 V, SMA | TVS | SMAJ33CA-TR | FEC-9802843 | STMicroelectronics |
| D27, D28 | TVS diode, 26 V, 42.1 V, DO214AA | TVS | SMBJ26CA | FEC-1749366 | STMicroelectronics |
| D13, D14, D15, D16 | TVS diode, 10 V, 19.6 V, SMA | TVS | SMA6J10A-TR | Digi-Key 497-5915-1-ND | STMicroelectronics |
| ESD3 | TVS diode, 5.25 V, SOT23-6 | ESD | ESDA6V1SC6 | FEC-9802274 | STMicroelectronics |
| ESD4 | TVS diode, 5 V, 10 V, 10UDFN | ESD | ESD7004MUTAG | FEC-1961708 | ON Semiconductor |
| F1, F2, F3, F4 | Positive temperature coefficient (PTC), reset fuse, 30 V, 50 mA, 1210 | Fuse | MF-USMF005-2 | FEC-2309134 | Bourns |
| J1 | Connected header, 20 position, gold | Joint Action Test Group (JATG) | 5103308-5 | FEC-2452432 | TE Connectivity |
| JP1 | 2 Pin (2x1), 0.1", header | JP2 | M20-9990245 | FEC-1022245 | Harwin |
| JP2, JP4, JP6 | 3 Pin (3x1), 0.1", header | JP3 | M20-9990345 | FEC-1022248 | Harwin |
| INSERTED TO JP1, JP2, JP4, JP6 | 2 Pin (2x1), 0.1", shorting block | Not applicable | M7566-05 | FEC-150411 | Harwin |
| L1, L2, L3, L4, L15, L16 | Ferrite bead, 1.8 kΩ, 0402 1 line | 1.8 kΩ | BLM15HD182SN1D | FEC-1515786 | Murata |
| L9, L10, L11, L12, L13 | Ferrite bead, 150 Ω, 1206, 1 line | 150 Ω | LI1206H151R-10 | FEC-2292444 | Laird Technologies |
| L14 | USB, common-mode filter, 0805 | Filter | 0805USB-502MLB | FEC-2458105 | Coilcraft |
| P1, P10 | Mounting hole, 3 mm diameter | Not applicable | Not applicable | Not applicable | Not applicable |
| P2, P3, P4, P11 | Terminal block header, 5 position, 90°, 3.81 mm | CON5 | 1860870 | Digi-Key 277-11004-ND | Phoenix Contact |
| P9 | Terminal block, 2 position, 3.81 mm, PCB, green | CON2 | 1727010 | FEC-3704579 | Phoenix Contact |
| P12 | Connected receipt, mini USB 2.0, 5 position | CON5 | UX60SC-MB-5S8 | FEC-2300433 | Hirose (HRS) |
| R1, R2, R3, R4, R5, R6, R7, R8 | Resistor, SMD, 33 Ω, 1%, 1/16 W, 50 V, 0402 | 33 Ω | MCWR04X33R0FTL | FEC-2447161 | Multicomp |

| Reference Designator | Part Description | Value | Part Number | Farnell Order Code | Manufacturer |
|---|---|---|---|---|---|
| R9 | Resistor, SMD, 16.9 kΩ, 1%, 1/16 W, 50 V, 0402 | 16.9 kΩ | CRCW040216K9FKED | FEC-1652757 | Vishay |
| R10 | Resistor, SMD, 14 kΩ, 1%, 1/16 W, 50 V, 0402 | 14 kΩ | MCWR04X1402FTL | FEC-2447109 | Multicomp |
| R11, R127 | Resistor, SMD, 4.7 MΩ, 5%, 1/2 W, 2 kV, 2010 | 4.7 MΩ | CHV2010-JW-475ELF | FEC-2470939 | Bourns |
| R12 | Resistor, SMD, 10 kΩ, 1%, 1/16 W, 50 V, 0402 | 10 kΩ | RC0402FR-0710KL | FEC-2144755 | Yageo |
| R13, R14 | Resistor, SMD, 4.7 kΩ, 1%, 1/10 W, 50 V, 0402 | 4.7 kΩ | ERJ2GEJ472X | FEC-2059234 | Panasonic |
| R15, R16, R17, R18, R19, R20, R21, R22 | Resistor, SMD, 1 kΩ, 1%, 1/16 W, 50 V, 0402 | 1 kΩ | CRG0402F1K0 | FEC-2331474 | TE Connectivity |
| R23 | Resistor, SMD, 2.2 kΩ, 1%, 1/10 W, 50 V, 0402 | 2.2 kΩ | ERJ2RKF2201X | FEC-2302673 | Panasonic |
| R24, R27, R28, R30, R31, R32, R33, R34, R35 | Resistor, SMD, 180 Ω, 1%, 1/10 W, 50 V, 0603 | 180 Ω | MCWR06X1800FTL | FEC-2447267 | Multicomp |
| R25, R26, R152, R153 | Resistor, SMD, 100 kΩ, 1%, 1/16 W, 50 V, 0402 | 100 kΩ | MCWR04X1003FTL | FEC-2447094 | Multicomp |
| R29, R41, R43, R44, R45, R104, R109, R110, R151 | Resistor, SMD, 0 Ω, 1%, 1/16 W, 50 V, 0402 | 0 Ω | CRG0402ZR | FEC-1174140 | TE Connectivity |
| R36, R37, R39, R40 | Resistor, SMD, 180 Ω, 5%, 1/2 W, 0805 | 180 Ω | ERJ-P6WJ181V | Digi-Key P16945CT-ND | Panasonic |
| R38, R42, R54, R89, R155 | Resistor, SMD, 0 Ω, 1%, 1/8 W, 150 V, 0805 | 0 Ω | WR08X000 PTL | FEC-2502664 | Walsin |
| R46, R55, R57, R111, R112, R142 | Resistor, SMD, 499 Ω, 1%, 1/16 W, 50 V, 0603 | 499 Ω | MC0603SAF4990T5E | FEC-1632442 | Multicomp |
| R47, R48, R56, R58, R63, R79, R80, R90, R91, R98 | Resistor, SMD, 100 kΩ, 1%, 1/16 W, 50 V, 0603 | 100 kΩ | RC0603FR-13100KL | FEC-1799369 | Yageo |
| R49, R50, R51, R52, R86, R147 | Resistor, SMD, 0 Ω, 1%, 1/16 W, 50 V, 0603 | 0 Ω | MC0603SAF0000T5E | FEC-2309111 | Multicomp |
| R53, R59, R60, R61, R62, R64, R65, R66, R67, R69, R71, R73, R75, R76, R77, R78, R81, R82, R83, R84, R85, R94, R96, R99, R100, R102, R103, R105, R106, R107, R108 | Resistor, SMD, 10 kΩ, 1%, 1/16 W, 50 V, 0603 | 10 kΩ | RC0603FR-0710KL | FEC-9238603 | Yageo |
| R68, R70, R72, R74, R87, R88, R92, R93, R95, R97, R101, R143, R144, R145, R148, R149, R150 | Resistor, SMD, 33 Ω, 1%, 1/16 W, 50 V, 0603 | 33 Ω | MCWR06X33R0FTL | FEC-2447344 | Multicomp |
| R141 | Resistor, SMD, 0 Ω, 1%, 1/2 W, 200 V, 1210 | 0 Ω | CRCW12100000ZSTA | FEC-1653183 | Vishay |
| R146 | Resistor, SMD, 1 MΩ, 1%, 1/16 W, 50 V, 0603 | 1 MΩ | MCWR06X1004FTL | FEC-2447285 | Multicomp |
| R154 | Resistor, SMD, 2010 | DNP | Not applicable | Not applicable | Not applicable |
| S1, S2, S3, S4 | Switch, tactile, single pole single throw (SPST), number, 0.05 A, 24 V | Switch | B3S-1000 | FEC-177807 | Omron |
| T1 | 2 line, common-mode choke, surface-mount, 190 Ω at 100 MHz, 5 A dc resistance, 20 mΩ | DLW5BS | DLW5BSN191SQ2L | FEC-1515607 | Murata |
| TP1, TP2 | Test point, tin, SMD | CON1 | S1751-46R | FEC-2293786 | Harwin |
| U1 | IC digital iso, 2.5 kV, 4 channel, 24 SSOP | ADuM5411 | ADUM5411BRSZ | FEC-2667947 | Analog Devices |

| Reference Designator | Part Description | Value | Part Number | Farnell Order Code | Manufacturer |
|---|---|---|---|---|---|
| U2 | IC, ADC, 24-bit, SPI, serial, 40 LFSCP | AD4111 | AD4111BCPZ | Not applicable | Analog Devices |
| U3 | IC, VREF, series, 2.5 V, 8 SOIC | ADR4525 | ADR4525ARZ | FEC-2112685 | Analog Devices |
| U4 | IC, MCU, 32-bit, 256 KB, flash, 64 LFCSP | ADuCM3029 | ADUCM3029BCPZ | FEC-2747646 | Analog Devices |
| U14 | IC, regulator, linear, 3.3 V, 500 mA, 8 MSOP | ADP124 | ADP124ARHZ-3.3-R7 | FEC-1827296 | Analog Devices |
| U15 | IC, regulator, linear, 5.0 V, 200 mA, 8 MSOP | ADP7142 | ADP7142ARDZ-5.0-R7 | FEC-2727495 | Analog Devices |
| U5, U6 | IC, flash, 256-mbit, 80 MHz, 8 WSON | W25Q256FV | W25Q256FV | Digi-Key W25Q256FVEIG-ND | Winbond Electronics |
| U16, U17 | IC, gate, 1 channel, 2-INP SOT23-5 | 74LVC1G08 | SN74LVC1G08DBV | FEC-1287593 | Texas Instruments |
| U18 | IC, USB, FS, serial, UART, 32-QFN | FT232R | FT232RQ | FEC-1146033 | FTDI |
| Y1 | Crystal, 16.00 MHz, 9.0 pF, SMD | 16 MHz | Q24FA20H00044 FA-20H 16 MHz 9.0 pF | FEC-1712814 | Epson |
| Y2 | Crystal, 32.7680 KHz, 12.5 pF, SMD | 32.768 KHz | ABS07-32.768KHZ-T | FEC-2101347 | Abracon |
| Y3 | Crystal, 26.0000 MHz, 10 pF, SMD | 26 MHz | ABM8G-26.000MHZ-B4Y-T | FEC-2101340 | Abracon |