DS21552/DS21Q552
5V, Enhanced, T1 Single-Chip Transceivers

REVISION B1 ERRATA

The errata listed below describe situations where DS21552/DS21Q552 revision B1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS21552/DS21Q552 revision B1 components. Revision B1 components are branded on the top side of the package with a six-digit code in the form yywwB1, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS21552/DS21Q552 die revision, visit our website at www.maxim-ic.com/errata.

1. SLC-96 MESS5 MESSAGE CORRUPTION IN T1 D4 FRAMING

Description:
When the DS21552 tries to process the following SLC-96 message, the information reported becomes corrupted. The MESS5 message is covered in BellCore TR-TSY-000008 page 4-5 and Telcordia GR-8 page 4-7. This message is sent from the RT to the COT every 1.15 seconds.

The first six bits of this message are ‘000111,’ an exact match for the SLC-96 synchronization bits, which are '000111000111.' A normal SLC-96 data stream in the Fs bits of D4 framing would be formatted as follows:

'000111000111ccccccccccc010mmmaassss1'

With the MESS5 message, the stream becomes:

'000111000111000111111111010mmmaassss1'

The c bits at the start of the message look exactly like the synchronization part of the message. The end result is that the SLC-96 message is reported incorrectly by the DS21552.

Work Around:
None.

2. FAILURE TO DETECT J1 LFA (YELLOW ALARM) IN ESF MODE

Description:
The DS21552 does not correctly identify the J1 LFA (also called Yellow or RAI) alarms correctly. In J1 ESF mode, the DS21552 does not report the LFA alarm when the Japanese JT-G704 LFA pattern of '11111111 11111111' is present in the facilities data link. The DS21552 only responds to the normal G.704 LFA pattern of '11111111 00000000.'

Work Around:
To transmit the Japanese ESF LFA alarm, which is 0xFFFF in the FDL, the following can be done. Set the TFDL register to 0xFF and set the TFDLS bit to 0. The TFDLS bit is located in the TCR1 register.

To receive the Japanese ESF LFA alarm, which is 0xFFFF, the software must monitor the RFDL register. The RFDL register is updated regularly and an update is indicated by the RFDLF status bit. The RFDL status bit is located in the SR2 register. Since the Japanese ESF LFA alarm pattern is 2 bytes long, the RFDL register must be read on two consecutive updates for a complete pattern. When 16 consecutive patterns of 0xFFFF appear in the FDL, the alarm is set. If 14 or fewer patterns of 0xFFFF out of 16 possible appear in the FDL, the alarm is cleared.