DS2155
T1/E1/J1 Single-Chip Transceiver

REVISION C2 ERRATA

The errata listed below describe situations where DS2155 revision C2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS2155 revision C2 components. Revision C2 components are branded on the topside of the package with a six-digit code in the form yywwC2, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. The die revision can also be determined through the lower four bits of the IDR register at location 0Fh. These four bits contain "0100" on C2 revision devices.

To obtain an errata sheet on another DS2155 die revision, visit our website at www.maxim-ic.com/errata, or contact technical support at telecom.support@dalsemi.com.

1) PULSE SHAPE OPTIMIZATION

Description:
Output pulse shapes are not ideally centered within the applicable template windows when using the Automatic Gain Control (AGC) mode of operation (TLBC.6 = 0). Testing to verify template compliance for the AGC mode is performed with the supplemental register settings provided in the following table. Writing the indicated values in register F1h adjusts the target amplitude of the output waveform. When internal transmit impedance matching is disabled (LIC4.2 = 0 and LIC4.3 = 0), writing 08h in register F2h improves the output rise time for E1 line build-out 0. Register F2h should contain 00h if internal transmit impedance matching is enabled.

Work Around:
When in these conditions, also set the appropriate values to F1h and F2h:

LIC2.7	LIC1.7	LIC1.6	LIC1.5	TLBC.6	TO OPTIMIZE WAVESHAPE:
0	0	0	1	0	Write F1h = 0Ah
0	0	1	0	0	Write F1h = 0Ah
0	0	1	1	0	Write F1h = 0Ah
0	1	0	0	0	Write F1h = 0Ah
1	0	0	0	0	Write F1h = 20h, F2h = 08*
1	0	0	0	1	Write F1h = 20h, F2h = 08*
1	0	0	1	0	Write F1h = 20h
1	1	0	1	0	Write F1h = 20h

**Only set F2h to 08 if transmit impedance matching is off (LIC4.2 = 0 and LIC4.3 = 0).*

For all other conditions, write F1h = 00h and F2h = 00h.

2) FAILURE TO DETECT J1 LFA (YELLOW ALARM) IN ESF MODE

Description:
The DS2155 does not correctly identify the J1 LFA (also called Yellow or RAI) alarms correctly. In J1 ESF mode, the DS2155 will not report the LFA alarm when the Japanese JT-G704 LFA pattern of "11111111 11111111" is present in the facilities data link. The DS2155 will only respond to the normal G.704 LFA pattern of "11111111 00000000."

Work Around:
To transmit the Japanese ESF LFA alarm, which is 0xFFFF in the FDL, the following can be done. Set the TFDL register to 0xFF and set the TFDLS bit to a 0. The TFDLS bit is located in the T1TCR1 register.

To receive the Japanese ESF LFA alarm, which is 0xFFFF, the software must monitor the RFDL register. The RFDL register is updated regularly and an update is indicted by the RFDLF status bit. The RFDLF status bit is located in the SR8 register. Since the Japanese ESF LFA alarm pattern is 2 bytes long, the RFDL register has to be read on two consecutive updates for a complete pattern. When 16 consecutive patterns of 0xFFFF appear in the FDL, the alarm will be set. If 14 or fewer patterns of 0xFFFF out of 16 possible appear in the FDL, the alarm will be cleared.

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