DS21Q55
T1/E1/J1 Quad Transceiver

REVISION B1 ERRATA

The errata listed below describe situations where DS21Q55 revision B1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS21Q55 revision B1 components. Revision B1 components are branded on the top side of the package with a six-digit code in the form yywwB1, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. The die revision can also be determined through the lower four bits of the IDR register at location 0Fh. These four bits contain "0011" on B1 revision devices. To obtain an errata sheet on another DS21Q55 die revision, visit the website at www.maxim-ic.com/errata or email technical support at telecom.support@dalsemi.com.

1. BERT DALY PATTERN SYNCHRONIZATION

Description:
If a BRLOS occurs while switching from the Daly pattern to any other BERT pattern after being synchronized to the Daly pattern, the DS21Q55 BERT may not resynchronize to the new pattern.

Work Around:
Before switching out of the Daly pattern, place the device in framer loopback by setting FLB = 1. After switching to the new pattern, remove the loopback by setting FLB = 0.

2. BERT BIT ERRORS IN UNFRAMED MODE

Description:
The BERT gives false indication of received bit errors when operating in the unframed mode. This mode is enabled when the RFUS bit in the BIC register contains a 1.

Work Around:
Use framed modes of operation only.

3. RECEIVER GAIN BOOST

Description:
Production testing of the receiver is performed with a 2dB gain-boost test mode enabled to compensate for a portion of the device population in which the receiver has slightly lower gain than required. Possible results of not enabling this test mode include the equalizer reducing the gain limit by up to 2dB when using the EGL bit and a negative offset in the receive level indication of up to 2dB.

Work Around:
Program a value of C0h to address location F5h to enable 2dB of additional receiver gain.

4. CSU FILTERS

Description:
A small amount of switching noise is present on the TTIP and TRING outputs of the device when using the CSU line build-out values in register LIC1:

L2	L1	L0	Application
1	0	1	-7.5dB CSU
1	1	0	-15dB CSU
1	1	1	-22.5dB CSU

The frequency of the noise is equal to the transmit system clock, and the magnitude is approximately 100mV. Devices are tested to the applicable amplitude specifications, but no template testing is performed for the CSU line build-outs.

5. PULSE SHAPE OPTIMIZATION

Description:
Output pulse shapes are not ideally centered within the applicable template windows when using the automatic gain control (AGC) operation mode (TLBC.6 = 0). Testing to verify template compliance for the AGC mode is performed with the supplemental register settings provided in the following table. Writing the indicated values in register F1h adjusts the target amplitude of the output waveform. When internal transmit impedance matching is disabled (LIC4.2 = 0 and LIC4.3 = 0), writing 08h in register F2h improves the output rise time for E1 line build-out 0. Register F2h should contain 00h if internal transmit impedance matching is enabled.

Work Around:
When in these conditions, also set the appropriate values to F1h and F2h:

LIC2.7	LIC1.7	LIC1.6	LIC1.5	TLBC.6	TO OPTIMIZE WAVESHAPE:
0	0	0	1	0	Write F1h = 0Ah
0	0	1	0	0	Write F1h = 0Ah
0	0	1	1	0	Write F1h = 0Ah
0	1	0	0	0	Write F1h = 0Ah
1	0	0	0	0	Write F1h = 20h, F2h = 08*
1	0	0	0	1	Write F1h = 20h, F2h = 08*
1	0	0	1	0	Write F1h = 20h
1	1	0	1	0	Write F1h = 20h

*Only set F2h to 08 if transmit impedance matching is off (LIC4.2 = 0 and LIC4.3 = 0).

All other conditions, write F1h = 00h and F2h = 00h.

6. PAYLOAD LOOPBACK OPERATION

Description:
When operating in payload loopback, the device does not automatically map TCLKO to equal the recovered clock.

Work Around:
When operating in payload loopback, set CCR1.1 = 1 and CCR1.2 = 1 to force TCLKO equal to RCLK.

7. INSERT BIPOLAR VIOLATION FUNCTION

Description:
When manually inserting a bipolar violation using the IBPV bit (LIC2.5), while operating in E1 mode with HDB3 line coding enabled, the potential exists for the transmit LIU to insert up to three bipolar violations rather than a single bipolar violation.

Work Around:
There is no known work around for this erratum.

8. HDLC CONTROLLER FIFO

Description:
The potential exists to introduce bit errors into the receive HDLC data stream when the device is actively receiving a packet and the last byte of data in the receive FIFO is accessed with a read operation.

Work Around:
When receiving a packet, allow one byte to remain in the receive FIFO until the end-of-packet is detected. The following example algorithm implements the work around:

1) Reset receive HDLC controller.
2) Set HDLC mode, mapping, and high watermark.
3) Start new message buffer.
4) Enable RPE and RHWM interrupts.
5) Wait for interrupt.
6) Disable RPE and RHWM interrupts.
7) Read HxRPBA register. N = HxRPBA (lower 7 bits are byte count, MSB is status).
8) Perform a logical “and” with 7fh to mask the MSB of HxRPBA.
9) Subtract 1.
10) Read [(N and 7Fh) –1] bytes from receive FIFO and store in message buffer.
11) Check the status of RPE for a receive packet-end event.
12) If RPE = 1
    a) Read one more byte from the receive FIFO and store in message buffer.
    b) Read INFO5 register.
    c) If PS2, PS1, PS0 = 000, then go to Step 4.
    d) If PS2, PS1, PS0 = 001, then packet terminated OK, save present message buffer.
    e) If PS2, PS1, PS0 = 010, then packet terminated with CRC error.
    f) If PS2, PS1, PS0 = 011, then packet aborted.
    g) If PS2, PS1, PS0 = 100, then FIFO overflowed.
13) Go to Step 3.

9. HDLC CONTROLLER TRANSMIT CRC

Description:
When the transmitted CRC on an HDLC packet ends in five 1s, the calculated CRC on the following packet will be incorrect.

Work Around:
When the receiving node detects a mismatch between the data and CRC in the corrupted packet, it should request a retransmission of that packet. The packet’s CRC will be correctly calculated on retransmission, and normal transmission should resume. For each packet in which a calculated CRC ends in five 1s, one “bad” packet will need to be retransmitted.

10. SLC-96 MESS5 MESSAGE CORRUPTION IN T1 D4 FRAMING

Description:
When the DS21Q55 tries to process the following SLC-96 message, the information reported becomes corrupted. The MESS5 message is covered in BellCore TR-TSY-000008 page 4-5 and Telcordia GR-8 page 4-7. This message is sent from the RT to the COT every 1.15 seconds.

The first six bits of this message are '000111,' an exact match for the SLC-96 synchronization bits, which are '000111000111'. A normal SLC-96 data stream in the Fs bits of D4 framing would be formatted as follows:

'000111000111ccccccccccc010mmmaassss1'

With the MESS5 message, the stream becomes:

'000111000111000111111111010mmmaassss1'

The 'c' bits at the start of the message look exactly like the synchronization part of the message. The end result is that the SLC-96 message is reported incorrectly by the DS21Q55.

Work Around:
None.

11. TEST MODE

Description:
When using the TEST0 and TEST1 bits in the MSTRREG to force output pins to a known state, the parallel port pins are also affected. This prevents further communication with the device until the user toggles the TSTRST pin.

Work Around:
Use the TSTRST pin to clear internal registers and reset the TEST0 and TEST1 bits to zero.

12. FAILURE TO DETECT J1 LFA (YELLOW ALARM) IN ESF MODE

Description:
The DS21Q55 does not correctly identify the J1 LFA (also called Yellow or RAI) alarms correctly. In J1 ESF mode, the DS21Q55 will not report the LFA alarm when the Japanese JT-G704 LFA pattern of '11111111 11111111' is present in the facilities data link. The DS21Q55 will only respond to the normal G.704 LFA pattern of '11111111 00000000'.

Work Around:
To transmit the Japanese ESF LFA alarm, which is 0xFFFF in the FDL, the following can be done. Set the TFDL register to 0xFF and set the TFDLS bit to a 0. The TFDLS bit is located in the T1TCR1 register.

To receive the Japanese ESF LFA alarm, which is 0xFFFF, the software must monitor the RFDL register. The RFDL register is updated regularly and an update is indicted by the RFDLF status bit. The RFDLF status bit is located in the SR8 register. Since the Japanese ESF LFA alarm pattern is 2 bytes long, the RFDL register has to be read on two consecutive updates for a complete pattern. When 16 consecutive patterns of 0xFFFF appear in the FDL, the alarm is will be set. If 14 or fewer patterns of 0xFFFF out of 16 possible appear in the FDL, the alarm will be cleared.

13. FAST ONE-SECOND TIMER PERIOD RESULTS IN LOW ERROR COUNT

Description:
The period of the on-chip one-second timer is 125μs fast, resulting in an actual period of 0.999875 seconds. This may result in the error count registers reporting a lower error count than what actually occurs during a one-second period. The device detects and counts errors correctly, but because the error count registers are updated slightly more often than once per second, the error count reported could be less than the actual error count recorded against a reference one-second timer.

Work Around:
None.