DS26334
3.3V, 16-Channel, E1/T1/J1 Short-/Long-Haul Line Interface Unit

REVISION A1 ERRATA

The errata listed below describe situations where DS26334 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26334 revision A1 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS26334 die revision, visit our website at **www.maxim-ic.com/errata**.

NOTE: THE FOLLOWING ARE FEATURE ENHANCEMENTS IMPLEMENTED IN REVISION A2 THAT WILL NOT WORK FOR REVISION A1:

1) Programmable corner frequency for the jitter attenuator in E1 mode.
2) Fully internal impedance matching option for RTIP/RRING.
3) Option for system-side deployment of BERT.
4) RESREF pin for receive termination calibration.

1. SHORT-CIRCUIT AND OPEN-CIRCUIT DETECTION DO NOT OPERATE RELIABLY

Description:
When the part is operating in either T1/J1 or E1 mode and impedance matching is on, short-circuit detection and open-circuit detection do not operate reliably. This issue affects all line build-outs with impedance matching on.

Work Around:
None.

2. RPOS, RNEG, AND RCLK PINS DO NOT TRI-STATE

Description:
The RPOS, RNEG, and RCLK pins for all the 16 LIUs do not tri-state as specified in the data sheet.

Work Around:
None.

3. TEMPLATE COMPLIANCE OF OUTPUT WAVEFORMS

Description:
Output waveforms may not be centered in their respective templates leading to possible template violations or less than ideal template compliance.

Work Around:
Table 1 below specifies the address to the ADDP registers and the addresses of the registers within the test bank that needs to be set in order to center the output waveform within the template. The setting depends on whether impedance matching is on or off. Impedance matching can be set or unset using the TIMPOFF bit in Template Select Register (Register Address = 11h).

With impedance matching on, short-circuit protection should be disabled to avoid a false detection and thereby shutting down of the device (see Errata #1 on short-circuit and open-circuit detection).

Table 1. Addresses and Register Settings for Output Waveform Template Compliance

ADDRESS TO THE ADDP REGISTER	HEX VALUE TO ENTER IN ADDRESS	WILL ACCESS THE FOLLOWING LIU	WRITE TO THE FOLLOWING ADDRESS WITHIN THE TEST BANK	HEX VALUE TO WRITE IN ADDRESS WITH IMPEDANCE MATCHING:	
				OFF (TIMPOFF BIT = 1)	ON (TIMPOFF BIT = 0)
1Fh	04h	LIU1	04h	**Contact factory for register settings**	**Contact factory for register settings**
1Fh	05h	LIU2	04h		
1Fh	06h	LIU3	04h		
1Fh	07h	LIU4	04h		
1Fh	08h	LIU5	04h		
1Fh	09h	LIU6	04h		
1Fh	0Ah	LIU7	04h		
1Fh	0Bh	LIU8	04h		
3Fh	04h	LIU9	24h		
3Fh	05h	LIU10	24h		
3Fh	06h	LIU11	24h		
3Fh	07h	LIU12	24h		
3Fh	08h	LIU13	24h		
3Fh	09h	LIU14	24h		
3Fh	0Ah	LIU15	24h		
3Fh	0Bh	LIU16	24h		

4. ALL-ONES INSERTION IN DIGITAL LOOPBACK

Description:
The transmit all-ones logic is inside the digital loopback path. The data looped back to RPOS/RNEG will be overwritten by any transmit all-ones condition.

Work Around:
TPOS/TNEG can be looped back to RPOS/RNEG while simultaneously sending all ones on TTIP/TRING. However all-ones will be sent on groups of 1–8 and 9–16 TTIP/TRING outputs. Use the settings in Table 2 to enable this feature. Use these settings instead of the TAOE register.

Table 2. Addresses and Register Settings to Transmit All Ones in Digital Loopback

ADDRESS TO THE ADDP REGISTER	HEX VALUE TO ENTER IN ADDRESS	WILL ACCESS THE FOLLOWING LIUs	WRITE TO THE FOLLOWING ADDRESS WITHIN THE TEST BANK	HEX VALUE TO WRITE IN ADDRESS TO TRANSMIT ALL ONES IN DIGITAL LOOPBACK
1Fh	03h	LIU 1–8	07h	07h
3Fh	03h	LIU 9–16	27h	07h

5. OUTPUT ENABLE (OE*n*) BIT

Description:
OE*n* bit in the output-enable register (register address for LIUs 1–8:12h and for LIUs 9–16:32h) is inverted. When OE*n* bit is high, the transmitter is disabled. When it is low, the transmitter is enabled.

Work Around:
None.

6. RECEIVE IMPEDANCE ON (RIMPON) BIT

Description:
When RIMPON bit (in register TS) is set to 0, receive impedance matching is ON. When RIMPON bit is set to 1, receiver is in high-Z. In default mode, RIMPON = 0 and receive impedance matching is ON.

Work Around:
None.

7. RECEIVE TERMINATION CONTROL (RTCTL) BIT

Description:
RTCTL bit (in GC register) does not work.

Work Around:
None.