Rev: 031408

ERRATA SHEET
DS26504

Revision A1 Errata

The errata listed below describe situations where DS26504 revision A1 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26504 revision A1 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another DS26504 die revision, visit our website at ***www.maxim-ic.com/errata****.*

1) COMPOSITE CLOCK RECEIVE AMPLITUDE TOLERANCE DOES NOT MEET THE GR378 OR G.703 OPTION B SPECIFICATIONS

Description:
When the receive path is configured for GR378 or G.703 Option B composite clock mode, the receive amplitude tolerance level does not meet the required specifications. The receive tolerance level is approximately 3V. There is a software work around for this that will allow the part to meet the required amplitude tolerance.

Workaround:
To make the DS26504 meet the required receive amplitude tolerance when operating in GR378 or G.703 Option B composite clock modes, write the value 60h to address F5. This is a factory test register that is not specified in the data sheet. Note that doing this will increase the RLOS threshold to around 600mV, so it should only be used in GR378 or G.703 Option B composite clock operating modes. This workaround is not available in hardware mode.

2) GR378 AND G.703 OPTION B COMPOSITE CLOCK TRANSMIT WAVEFORMS MAY SHOW A 20MHz, 500mV PEAK-TO-PEAK OSCILLATION

Description:
When the transmit path is configured for GR378 or G.703 Option B composite clock modes, the transmit waveforms may show a 20MHz oscillation with a 500 mV peak-to-peak amplitude.

Workaround:
This oscillation can be eliminated by setting several factory test registers as shown below. These registers should only be set if the transmit path is set to GR378 or G.703 Option B composite clock operating modes and the oscillation is present. This workaround is not available in hardware mode.

REGISTER ADDRESS (hex)	VALUE (hex)
F2	40
F4	C0
F7	80

3) TS_8K_4 PIN JTAG FUNCTIONALITY DOES NOT WORK PROPERLY IN TRANSMIT 6312kHz HARDWARE MODE

Description:
When the part is configured for transmit 6312kHz hardware mode, the TS_8K_4 pin will always sample a logic 1 in JTAG mode. This pin is not used in the transmit 6312kHz operating mode.

Workaround:
None.

4) T1 AND E1 TRANSMIT WAVEFORMS MAY NOT BE CENTERED IN THEIR RESPECTIVE TEMPLATES AND MAY FAIL TEMPLATE COMPLIANCE IN CERTAIN LINE BUILD-OUTS

Description:
When the transmit path is configured in certain T1 or E1 line build-outs (LBOs), the transmit waveform may fail template compliance, or the transmit waveform may not be centered in the corresponding template. To center the waveforms, several factory test registers should be set as shown below. The setting is also dependent on the use of the automatic gain controller (AGC) and the use of the impedance matching (IM) feature.

Workaround:
To center the transmit waveforms, set the factory test registers as shown. This workaround is not available in hardware mode.

MODE	AGC	IM	ADDRESS	VALUE
T1 LBO1	On	On or Off	F1h	0Ah
T1 LBO2	On	On or Off	F1h	0Ah
T1 LBO3	On	On or Off	F1h	0Ah
T1 LBO4	On	On or Off	F1h	0Ah
E1 LBO0	On or Off	Off	F1h F2h	20h 08h
E1 LBO0	On or Off	On	F1h	20h
E1 LBO1	On	On or Off	F1h	20h
E1 LBO5	On	On or Off	F1h	20h

5) THE RECEIVE 6312kHz SENSITIVITY LEVEL MAY NOT MEET THE G.703 SPECIFICATION

Description:
When the receive path is configured for the 6312kHz operating mode, the receive sensitivity may not meet the -16dB requirement defined in the G.703 standard. The actual receive sensitivity may be closer to -14dB.

Workaround:
To ensure that the receive sensitivity meets the G.703 standard of -16dB when operating in 6312kHz mode, set the factory test register at address F4h = 60h. This workaround is not available in hardware mode.

6) THE TRANSMIT GR378 AMPLITUDE MAY NOT MEET THE G.703 LOWER LIMIT SPECIFICATION

Description:
When the transmit path is configured for the GR378 operating mode, the transmit amplitude may not meet the 2.7V lower limit specified in the G.703 standard.

Workaround:
To ensure that the GR378 minimum transmit amplitude meets the G.703 standard of 2.7V, set bit 3 of the transmit line build-out control register (TLBC) at address 34h to a logic 1 (TLBC.3 = 1). This workaround is not available in hardware mode.

7) THE RECEIVE COMPOSITE CLOCK INTERFACE MAY NOT PROPERLY RECOVER A COMPOSITE CLOCK SIGNAL

Description:
When the Composite Clock Interface is used, the receiver may not be able to properly recover a Composite Clock Signal. In some applications, the recovered output clock may have glitches or other impairments and may not be a valid clock signal.

Workaround:
None.