DS80C390
Dual CAN High-Speed Microprocessor

REVISION A1 ERRATA

The errata listed below describe situations where DS80C390 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS80C390 revision A1 components. Revision A1 components are branded on the top side of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS80C390 die revision, visit our website at www.maxim-ic.com/errata.

1. DEVICE EXHIBITS A SENSITIVITY TO LATCHUP WHEN OVERSHOOT CURRENTS EXCEED 10mA

Description:
The DS80C390 exhibits a sensitivity to latchup when the overshoot currents exceed 10mA.

Work Around:
Do not allow overshoot currents to exceed 10mA.

2. DEVICE WILL NOT OPERATE FROM AN EXTERNAL CRYSTAL

Description:
The DS80C390 will not operate from an external crystal.

Work Around:
Use an external clock oscillator to provide a time base for the device.

3. SYSTEM CLOCK IS NOT OUTPUT ON XTAL2

Description:
The system clock is not output on XTAL2, instead XTAL2 presents an inverted XTAL1 in enhanced hooks mode. This prevents high-speed and PLL emulation.

Work Around:
None, but the initial emulation requirement of 16MHz should be possible.

4. RST INPUT HAS AN INTERNAL PULLUP

Description:
The RST input pin has an internal pullup.

Work Around:
The pin must be overdriven or tied low.

5. $\overline{\text{RSTOL}}$ OUTPUT IS INVERTED

Description:
The $\overline{\text{RSTOL}}$ output in inverted.

Work Around:
Use an external hardware to adjust the logic level as needed.

6. R0, R1 WORKING REGISTERS CAN ONLY BE MODIFIED FROM THE CURRENT BANK

Description:
R0, R1 working registers can only be modified from the current bank. For example, if the RS0 = RS1 = 0 (working bank 0 selected), do not modify scratchpad RAM locations 08h, 09h (R0, R1 working bank 1), 10h, 11h (R0, R1 working bank 2), or 18h, 19h (R0, R1 working bank 3).

Work Around:
None.

7. RING OSCILLATOR AND ASSOCIATED FEATURES DO NOT FUNCTION

Description:
The ring oscillator and its associated features do not function.

Work Around:
None.

8. REGISTER ASSOCIATED WITH SERIAL PORTS (SCON0, SCON1, SBUF1, SBUF0.2) CANNOT BE MODIFIED FOR AT LEAST ONE SERIAL PORT CLOCK PERIOD AFTER TI OR RI BITS ARE SET BY INTERNAL HARDWARE

Description:
The registers associated with the serial ports (SCON0, SCON1, SBUF1, SBUF0.2) cannot be modified for at least one serial port clock period after the TI or RI bits are set by internal hardware. The documentation implies that these bits can be modified at any time.

Work Around:
The incorporation of a software delay can ensure a successful modification of the above-mentioned registers. After reading the RI or TI bits in a logic 1 state, wait the following delay period, based on the serial port baud rate, before modifying the register:

$$\text{Delay} = \left[\frac{1}{\text{baud\_rate} \bullet 16} \right] \text{ seconds}$$

9. SETTING ANY OF THE PDCE3–PDCE0 BITS WILL CAUSE THE DEVICE TO MALFUNCTION

Description:
Setting any of the PDCE3–PDCE0 bits causes the device to malfunction.

Work Around:
None.

10. USING THE CAN BUS IN CONJUNCTION WITH PMM, STOP, OR IDLE MODES WILL RESULT IN UNEXPECTED OPERATION AND SHOULD BE AVOIDED

Description:
Using the CAN Bus in conjunction with PMM, Stop, or Idle modes will result in unexpected operation and should be avoided.

Work Around:
None.

11. CJNE INSTRUCTIONS INVOLVING ANY REGISTER ASSOCIATED WITH THE DATA POINTERS WILL NOTE WORK CORRECTLY

Description:
CJNE instructions involving any register associated with the data pointers will not work correctly.

Work Around:
Avoid using these instructions.

12. INTERRUPTS DURING MOVX INSTRUCTIONS WILL PUSH INCORRECT DATA ONTO THE STACK

Description:
Interrupts during MOVX instructions will push incorrect data onto the stack.

Work Around:
Disable interrupts prior to MOVX instructions, and enable afterwards.

13. SIMULTANEOUS INTERRUPTS AT DIFFERENT PRIORITY LEVELS WILL VECTOR TO INCORRECT LOCATIONS

Description:
Simultaneous interrupts at different priority levels will vector to incorrect locations.

Work Around:
Do not enable the high priority or PFI interrupts.

14. THE JMP @A+DPTR DOES NOT CALCULATE THE CORRECT JUMP ADDRESS IN 24-BIT PAGED MODE

Description:
The JMP @A+DPTR does not calculate the correct jump address in 24-bit paged mode.

Work Around:
None. Do not use this instruction in 24-bit paged mode.

15. USE OF THE WATCHDOG RESET FUNCTION WHILE THE CTM BIT IS SET WILL CAUSE UNPREDICTABLE DEVICE OPERATION

Description:
Use of the watchdog reset function while the CTM bit is set will cause unpredictable device operation.

Work Around:
Do not use the watchdog reset function in conjunction with the crystal clock multiplier. This erratum will be corrected in the next revision of the device.

16. SERIAL PORT 0 WILL NOT OPERATE CORRECTLY UNDER CERTAIN CONDITIONS

Description:
Serial Port 0 will not operate correctly under the following conditions:
1) Timer 2 is used as the time base (RCLK = TCLK = 1), and
2) The SMOD bit for serial port 0 is cleared, and
3) Timer 1 is running (TR1 = 1).

Work Around:
Ensure that these conditions never occur simultaneously while using Serial Port 0. The easiest way is to use the serial port with the serial port doubler bit set (SMOD = 1).

17. EXTERNAL INTERRUPTS 2–5 CANNOT BE USED TO CAUSE THE DEVICE TO EXIT STOP MODE

Description:
External interrupts 2–5 cannot be used to cause the device to exit Stop mode.

Work Around:
Use external interrupts 0 and 1 if an external interrupt must be used to exit Stop Mode. It may also be possible to use the Idle mode of operation in place of Stop mode. This erratum does not affect DS80C390 revision C devices.

18. CAN AUTOBAUD MODE RXS BIT FUNCTION CLARIFIED

Description:
When either CAN is operating in autobaud mode, the RXS bit in the CxS SFR will only be set upon reception of a valid (i.e., no bus errors) identifier that matches one or more of the message IDs programmed into the CAN module. The documentation implies that the RXS bit should be set if a valid identifier is received, even if the identifier did not match any of the message IDs programmed into the CAN module.

Work Around:
If it is desired to use the autobaud mode to monitor bus activity and set RXS when any message is successfully received, the user should enable a message center to receive messages with any ID. Upon exit from autobaud mode, this message center can be reconfigured for other uses.

SPECIFICATION MODIFICATIONS

The t_{RLAZ} maximum AC timing specification will be replaced with a note stating, “Address is held in a weak latch until overdriven by external memory.”