ANALOG DEVICES

Key Sheet
AD7176-2

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Highlights of the AD7176-2—24-Bit, 250 kSPS Sigma-Delta ADC with 20 µs Settling

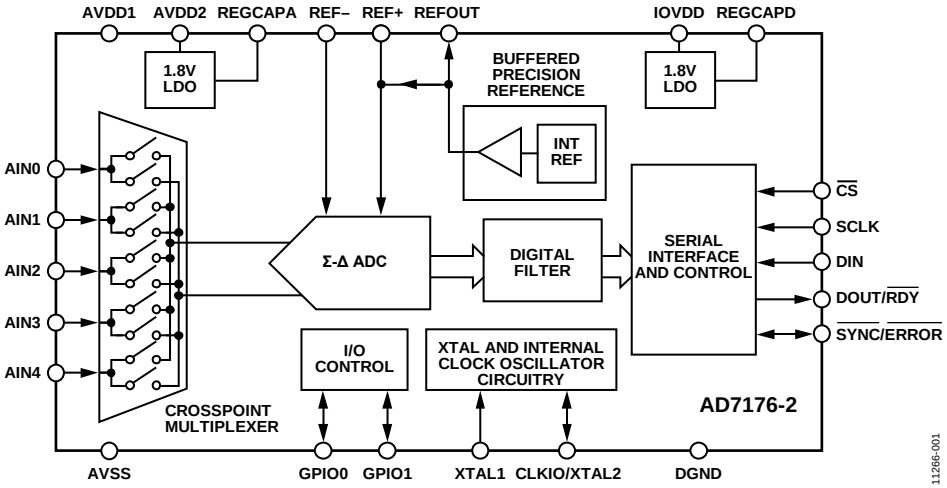

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

This key sheet[1] provides users with an overview of the AD7176-2. Key attributes of the part include the following:

- Designed for process control: PLC/DCS modules, temperature and pressure measurement, medical and scientific multi-channel instrumentation, and chromatography.
- Fast settling, highly accurate, high resolution, multiplexed, 24-bit Sigma-Delta (Σ-Δ) ADC for low bandwidth input signals with a fully flexible output data rate (ODR) between 5 SPS and 250 kSPS.
- Combines two fully differential or four pseudo differential input channels, selected via the integrated crosspoint multiplexer.
- With an ODR of 250 kSPS, the AD7176-2 boasts an rms noise of 9.7 µV when operating with the default Sinc5 + Sinc1 filter.
- User friendly, with the part being fully configurable over a 4-wire serial interface.
- Available in a small 24-lead TSSOP package, allowing a reduced board size.

FEATURES AND BENEFITS

The AD7176-2 offers the following features and benefits:

- Simultaneous 50 Hz and 60 Hz rejection at 27 SPS ODR
- Internal oscillator adds functionality and reduces external component count
- Optional split supply operation of ±2.5 V with AVDD1 referenced to AVSS
- System offset and gain errors can be corrected on a per channel basis
- Low noise performance across the ODR range
- Fully compatible with SPI, QSPI™, MICROWIRE®, and DSP
- Sinc5 + Sinc1, Sinc3, and enhanced 50 Hz and 60 Hz rejection digital filter options (see the Frequently Asked Questions section for more information)
- SPI configuration control
- 3- or 4-wire serial digital interface (Schmitt trigger on SCLK)

[1] This document provides users with an overview of the AD7176-2; it is not a notice of performance or intent. Refer to the AD7176-2 data sheet for performance and more specific information about this product.

Rev. 0

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KEY CHARACTERISTICS

FUNDAMENTAL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
ADC Type		Σ- Δ ADC		
Number of Input Channels		Two fully differential or four pseudo differential input channels		
Resolution	24		24	Bits
Output Data Rate (ODR)	5		250,000	SPS
Differential Input Voltage Range		$\pm V_{REF}$		V
Power Supply Voltage				
AVDD1 with Respect to AVSS	4.5		5.5	V
AVDD2 with Respect to AVSS	2		5.5	V
IOVDD with Respect to DGND	2		5.5	V
Offset Error		±40		µV
Gain Error		±10	±50	ppm/FSR
Integral Nonlinearity (INL)				
With 2.5 V Reference		±2.5	±7	ppm of FSR
With 5 V Reference		±7		ppm of FSR
Power Dissipation (AVDD1 = 5 V, AVDD2 = 2 V, IOVDD = 2 V)				
With External Clock and Reference		20.1	23.15	mW
With Internal Clock and Reference		22.25	25.9	mW
Operating Temperature Range	−40		+105	°C

NOISE

Table 2. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate[1]

	Sinc5 + Sinc1 Filter (Default)		Sinc3 Filter	
Output Data Rate (SPS)	Noise (µV rms)	Peak-to-Peak Resolution (Bits)	Noise (µV rms)	Peak-to-Peak Resolution (Bits)
250,000	9.7	17.2	220	12.8
62,500	5.4	18.2	5.1	18.3
10,000	2.5	19	1.8	19.8
1000	0.82	20.8	0.62	21
60	0.46	21.4	0.32	22
50	0.42	21.7	0.31	22
16.7	0.42	21.7	0.29	22.4
5	0.32	22.2	0.29	22.4

[1] Selected rates only; 1000 samples.

OPERATING THE AD7176-2

DATA INTERFACE

The data interface for the AD7176-2 is

- Performed using a 4- or 3-wire SPI
- Compatible with SPI, QSPI, MICROWIRE, and DSP
- Allows a user to both write to and read from the AD7176-2 on the same data bus
- Indicates when transferred data is available by bringing the DOUT/$\overline{RDY}$ signal and the $\overline{RDY}$ bit in the status register low

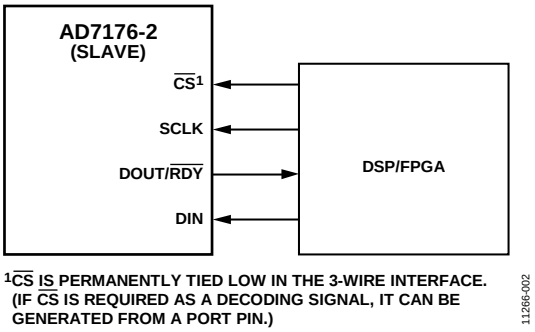


Figure 2. AD7176-2 Data Interface, 4-Wire

Table 3. 4-Wire Serial Interface Pin Functions

Pin	Function
$\overline{CS}$[1]	Selects the ADC (also applicable in systems with multiple devices on the serial bus).
SCLK	Determines when data transfers (either on DIN or DOUT/$\overline{RDY}$) occur.
DOUT/$\overline{RDY}$	Accesses data from the on-chip registers. Indicates when the transferred data is available.
DIN	Transfers data into the on-chip registers.

[1] $\overline{CS}$ is permanently tied low in the 3-wire interface. (If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin.)

ACCESSING THE ADC REGISTER MAP

The communications register controls access to the full register map of the ADC. This register is an 8-bit write only register. All communication begins by writing to the communications register. Figure 3 provides an overview of the configuration flow, which is divided into three blocks.

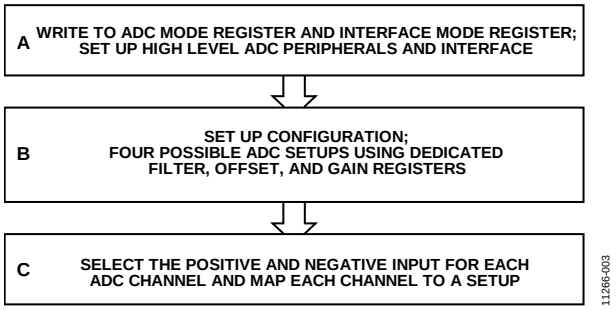


Figure 3. Configuration Flow

As Figure 3 shows, three configuration stages are required to set up the part.

ADC and Interface Mode Configuration

The ADC mode register and the interface mode register (see Block A in Figure 3) configure the core peripherals to be used by the AD7176-2 and the mode for the digital interface.

ADC Mode Register

The ADC mode register is used primarily to set the conversion mode of the ADC to either continuous or single conversion. The user can also select the standby and power-down modes as well as any of the calibration modes. In addition, this register contains the clock source select bits and the internal reference enable bits.

Interface Mode Register

The interface mode register is used to configure the digital interface operation. This register allows the user to control data-word length, CRC enable, and continuous read mode, as well as whether status bits are appended to the data that is read.

DATA MODES

There are three data modes available: continuous conversion mode, continuous read mode, and single conversion mode.

Continuous Conversion Mode (Default)

Continuous conversion is the default power-up mode. In this mode, the AD7176-2 converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user writes to the communications register, indicating that the next operation is a read of the data register. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The user can read this register additional times, if required.

When several channels are enabled, the ADC automatically sequences through the enabled channels, performing one conversion on each channel. When all channels have been converted, the sequence starts again with the first channel.

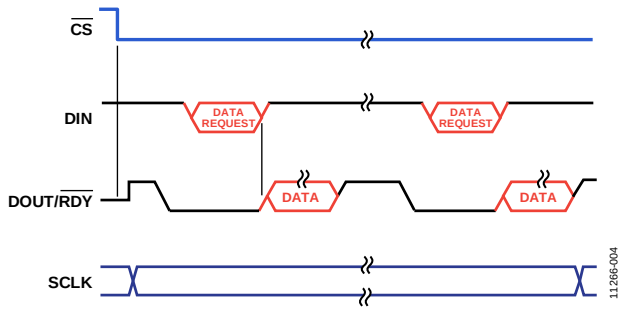


Figure 4. Continuous Conversion Mode

Continuous Read Mode

In continuous read mode, it is not required to write to the communications register before reading ADC data; just apply the required number of SCLKs after DOUT/$\overline{RDY}$ goes low to indicate the end of a conversion. When the conversion is read,

DOUT/$\overline{RDY}$ returns high until the next conversion is available. In this mode, the data can be read only once. If multiple ADC channels are enabled, each channel is output in turn, with the status bits being appended to the data if DATA_STAT is set in the interface mode register. The status register indicates the channel to which the conversion corresponds.

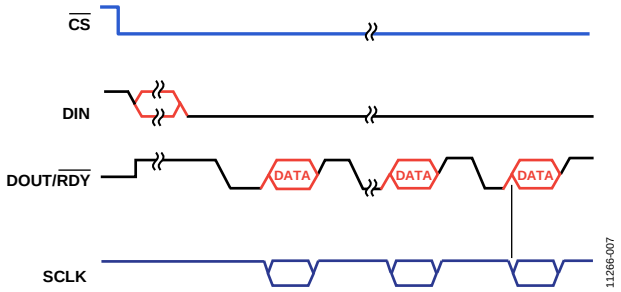


Figure 5. Continuous Read Mode

Single Conversion Mode

In single conversion mode, the AD7176-2 performs a single conversion and is placed in standby mode after the conversion is complete. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The data register can be read several times, if required, even when DOUT/$\overline{RDY}$ has gone high.

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. When a conversion is started, DOUT/$\overline{RDY}$ goes high and remains high until a valid conversion is available and $\overline{CS}$ is low. As soon as a conversion is available, DOUT/$\overline{RDY}$ goes low. The ADC then selects the next channel and begins another conversion. The user can read the present conversion while the next conversion is being performed. The two LSBs of the status register indicate the channel to which the conversion corresponds.

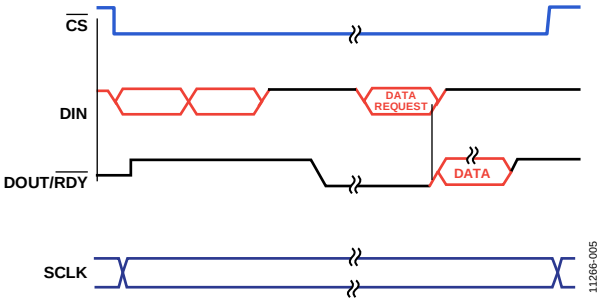


Figure 6. Single Conversion Mode

TYPICAL APPLICATION DIAGRAM

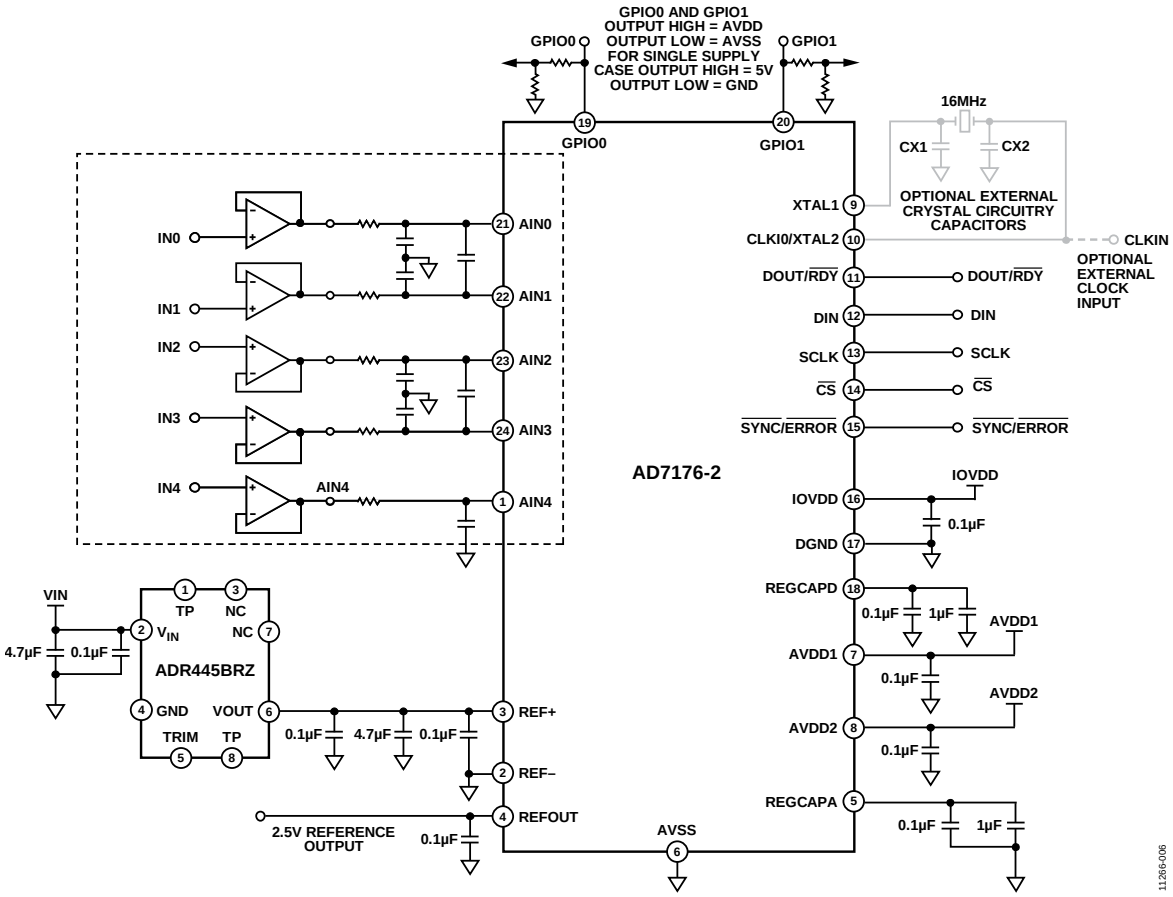


Figure 7. Typical Application Diagram

FREQUENTLY ASKED QUESTIONS

How fast can the AD7176-2 output data?
The maximum ODR is 250 kSPS, but the AD7176-2 can be configured to output data at an ODR from 5 SPS to 250 kSPS.

The AD7176-2 has a maximum ODR of 250 kSPS but a channel scan rate of 50 kSPS/channel. What does this mean?
When operating the AD7176-2 with a single channel enabled, the device can output data at an ODR of up to 250 kSPS. However, when more than one channel is enabled, the full filter settling time must be allowed for each channel. The data rate for fully settled data is 50 kSPS. Therefore, if two channels are enabled, the output data rate for each channel is 50 kSPS/2, or 25 kSPS.

What digital filtering options are available?
The AD7176-2 has three filter options: Sinc5 + Sinc1, Sinc3, and enhanced 50 Hz and 60 Hz filters. The Sinc5 + Sinc1 filter is most suitable for multichannel applications in which fast multiplexing is required. The Sinc3 filter is best for single-channel applications running at lower output data rates. In applications in which rejection of 50 Hz and 60 Hz is important, the enhanced 50 Hz and 60 Hz rejection filters should be used because they provide better performance than the Sinc5 + Sinc1 or Sinc3 filter and allow the user to trade off settling time or rejection to meet the needs of a given application. For more on digital filters, read Section 6: Digital Filters in *Mixed-Signal and DSP Design Techniques* (Analog Devices, 2000).

How do I interface with the part?
The part can be configured by using a 4-wire SPI interface; this interface is also used as the data interface. After the AD7176-2 is configured on the board, the SPI interface allows the user to read the status of the part and to change the setup to optimize performance.

Are there any ESD protection schemes that should be considered for the AD7176-2?
This converter is manufactured on a standard CMOS process; therefore, all standard practices and protection schemes that apply to other CMOS devices also apply to this device. There are ESD protection diodes on all the inputs that protect the device from possible ESD damage due to handling and production. To determine the appropriate ESD precautions, refer to the AD7176-2 data sheet for information about the absolute maximum ratings.

What information is provided in the noise tables of the AD7176-2 data sheet, and what are the sources of this noise?
The noise tables in the AD7176-2 data sheet show the output rms noise for different combinations of ODRs and filters. The values given are for bipolar input ranges with an external 5 V reference. The noise values indicated are typical and are generated at an analog input voltage of 0 V based on 1000 conversion results at the specified ODR. It is important to note that the peak-to-peak resolution is calculated based on the peak-to-peak noise.

What per channel configurability is available on the AD7176-2?
Each channel of the AD7176-2 can be configured with different

- Gain and offset correction
- Filter type
- Output data rate
- Reference source selection (internal or external)

LEARN MORE AND START DESIGNING

To learn more about the AD7176-2 and compatible products or to sample and buy the AD7176-2 device, click on the links provided or contact an Analog Devices, Inc., sales representative.

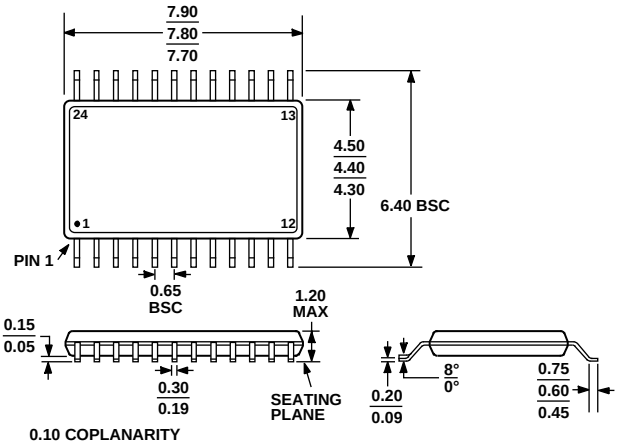
COMPATIBLE DEVICES

Table 4. Recommended Compatible Devices[1]

Linear Regulators	Precision References	ADC Driver Amplifiers	Circuits from the Lab™	Evaluation Board
ADP3309 family ADP7104 family	ADR44x family	AD8606 family AD8475 family ADA4940-2/ADA4941 family	CN-0310: *Precision 24-Bit, 250 kSPS Single-Supply Sigma-Delta ADC System for Industrial Signal Levels*	AD7176-2 evaluation board

[1] Information about additional companion products is provided on the AD7176-2 product page.

PACKAGE DIAGRAM



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 8. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

GETTING STARTED

AD7176-2
DATA SHEET

SAMPLE AND BUY
THE AD7176-2

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