Data Sheet

AD4080

20-Bit, 40 MSPS, Differential SAR ADC

FEATURES

- High performance
  - Throughput: 40 MSPS, 46.25 ns conversion latency
  - INL: ±4 ppm (typical), ±8 ppm (maximum)
  - SNR/THD
    - 93.6 dB (typical)/−110 dB (typical) at f_{IN} = 1 kHz
    - 93.5 dB (typical)/−104 dB (typical) at f_{IN} = 1 MHz
  - Noise spectral density: −167.6 dBFS/Hz
  - 20-bit resolution, no missing codes
- Low power
  - 79.3 mW typical at 40 MSPS with −0.5 dBFS sine-wave input
- Easy Drive, fully differential Input
  - 6 V p-p differential input range
  - Continuous signal acquisition
  - Linearized, 5 µA/MSPS input current
- Integrated, low-drift reference buffer and decoupling
- Integrated V_{CM} generation
- Digital features and data interface
  - Conversion result FIFO, 16K sample depth
  - Digital averaging filter with up to 2^{10} decimation
- SPI configuration
- Configurable data interface
  - Single lane, DDR, serial LVDS, 800 MBPS per lane
  - Dual lane, DDR, serial LVDS, 400 MBPS per lane
  - Single/quad lane SPI data interface
- Package
  - 49-ball, 5 mm x 5 mm CSP_BGA, 0.65 mm pitch
  - Integrated supply decoupling capacitors
- Operating temperature range: −40°C to +85°C

APPLICATIONS

- Digital imaging
- Cell analysis
- Spectroscopy
- Automated test equipment
- High speed data acquisition
- Digital control loops, hardware in the loop
- Power quality analysis
- Source measurement units
- Electron and x-ray microscopy
- Radar level measurement
- Nondestructive test
- Predictive maintenance and structural health

FUNCTIONAL BLOCK DIAGRAM

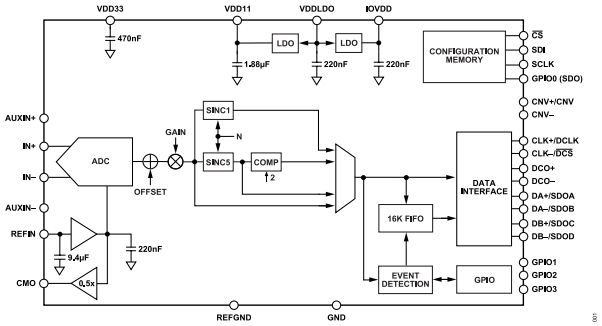

Figure 1. AD4080 Functional Block Diagram

GENERAL DESCRIPTION

The AD4080 is a high-speed, low noise, low distortion, 20-bit, Easy Drive, successive approximation register (SAR) analog-to-digital converter (ADC). Maintaining high performance (signal-to-noise and distortion (SINAD) ratio > 90 dBFS) at signal frequencies in excess of 1 MHz enables the AD4080 to service a wide variety of precision, wide bandwidth data acquisition applications. Simplification of the input anti-alias filter design can be accomplished by applying over-sampling along with the integrated digital filtering and decimation to reduce noise and lower the output data rate for applications that do not require the lowest latency of the AD4080.

The AD4080 Easy Drive features reduce both signal chain complexity and power consumption while enabling greater channel density and flexibility in companion component selection. The product input structure was designed to minimize any input dependent signal currents; therefore, reducing any converter induced settling artifacts. The continuous acquisition architecture allows settling across the entire conversion cycle, easing ADC driver settling and bandwidth requirements as compared to other high-speed data converters.

The AD4080 includes several elements that simplify data converter integration: a low drift reference buffer, low dropout (LDO) regulators to generate ADC core and digital interface supply rails, and a 16K result data first-in first out (FIFO) that can greatly reduce the load on the digital host. Additionally, critical supply and reference decoupling capacitors are integrated in the package to ensure optimum performance, simplify printed circuit board (PCB) layout, and reduce the overall solution footprint.

Rev. 0

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REVISION HISTORY

3/2024—Revision 0: Initial Version

SPECIFICATIONS

VDD33 = 3.3 V ± 5%, VDDLDO = 1.5 V to 2.7 V, VDD11 = 1.1 V ± 5%, IOVDD = 1.1 V − 5% to 1.2 V + 5%, voltage reference input (V_{REFIN}) = 3.0 V, sampling frequency (f_S) = 40 MHz, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		20			Bits
ANALOG INPUT					
Absolute Operating Input Voltage	Voltage at input, referred to GND	−0.1		VDD33 + 0.1	V
Differential Input Voltage Range	IN+ voltage − IN− voltage	$-V_{REFIN}$		$+V_{REFIN}$	V
Common-Mode Input Range		$V_{REFIN}/2 - 0.05$	$V_{REFIN}/2$	$V_{REFIN}/2 + 0.05$	V
DC PERFORMANCE					
No Missing Codes		20			Bits
Differential Nonlinearity (DNL)			±0.5	±0.99	LSB
Integral Nonlinearity (INL)			±4	±8	ppm
Transition Noise			6.9		LSB RMS
Gain Error	T_A = 25°C		0.01	±0.025	%FS
Gain Error Drift			0.095		ppm/°C
Zero Error	T_A = 25°C		15		µV
Zero Error Drift	T_A = −40°C to +85°C		0.05		ppm/°C
Power Supply Rejection	VDD33 = 3.3 V ± 5%		−89		dB
	VDD11 = 1.1 V ± 5%		−68		dB
Low Frequency Noise	Bandwidth = 0.1 Hz to 10 Hz		174		nV RMS
AC PERFORMANCE					
Dynamic Range			94.6		dB
Noise Spectral Density (NSD)			167.6		dBFS/Hz
Total RMS Noise	Bandwidth = 20 MHz		39.4		µV RMS
Signal-to-Noise Ratio (SNR)	Voltage magnitude (V_{MAG}) = −0.5 dBFS, input frequency (f_{IN}) = 1 kHz	92.7	93.6		dB
	V_{MAG} = −1 dBFS, f_{IN} = 1 MHz		93.5		dB
	Sinc5 + compensation filter, decimate by 8, V_{MAG} = −0.5 dBFS, f_{IN} = 1 kHz,	101.7	102.5		dB
Total Harmonic Distortion (THD)	V_{MAG} = −0.5 dBFS, f_{IN} = 1 kHz		−110	−101.7	dB
	V_{MAG} = −1 dBFS, f_{IN} = 1 MHz		−104		dB
Signal-to-Noise-and-Distortion (SINAD)	V_{MAG} = −0.5 dBFS, f_{IN} = 1 kHz		93.3		dB
	V_{MAG} = −0.5 dBFS, f_{IN} = 1 MHz		93		dB
Spurious-Free Dynamic Range			−112		dB
−3 dB Bandwidth	Input at IN+ and IN−, no external filter		272		MHz
Intermodulation Distortion (IMD)	Frequency A (f_A) = 1.0 MHz, Frequency B (f_B) = 800 kHz				
Second-Order IMD (IMD2)			−96.2		dB
Third-Order IMD (IMD3)			−97.2		dB
Power Supply Rejection	Ripple voltage = 50 mV p-p, f = 1 kHz				
VDD33			−92.5		dB
VDD11			−81.2		dB
REFERENCE INPUT					
V_{REFIN} Range		2.995	3.0	3.005	V
V_{REFIN} Current		−0.3		+1	µA/MSPS
	T_A = 25°C	−6.3		+26.9	µA
V_{REFIN} Leakage Current	Converter Idle	−2		+2	µA

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE OUTPUT (CMO)					
Absolute Output Voltage	V_{REFIN} = 3.0 V	1.48		1.51	V
Noise	Bandwidth = 7.4 MHz		71		µV RMS
Noise Spectral Density			26.1		nV/√Hz
LOW DROPOUT REGULATORS (VDD11, VIO11)					
Input Voltage Range		1.4		2.7	V
Output Voltage	T_A = 25°C, VDDLDO = 1.8 V		1.1		V
Start-Up Time			10		µs
LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) INPUT AND OUTPUT (EIA-644)					
Data Format	Serial LVDS data output		Twos complement		
LVDS Inputs (CLK± and CNV±)	IOVDD supply domain inputs.				
Common-Mode Input Voltage, V_{ICM}	Default setting	700		1400	mV
Differential Input Voltage, V_{IDIFF}	Default setting	100		600	mV
LVDS Outputs (DCO±, DA±, and DB±)	IOVDD supply domain outputs, differential termination, load resistance (R_L) = 100 Ω				
Common-Mode Output Voltage, V_{OCM}	LVDS_VOD = 001b	915	927	935	mV
	LVDS_VOD = 010b (default)	840	851	860	mV
	LVDS_VOD = 100b	695	706	715	mV
Differential Output Voltage, V_{ODIFF}	LVDS_VOD = 000b	370	395	420	mV
	LVDS_VOD = 010b (default)	500	530	560	mV
	LVDS_VOD = 100b	740	785	830	mV
DIGITAL INPUTS (CNV, $\overline{CS}$, SCLK, and SDI)	VDD11 supply domain inputs				
Input Voltage Tolerance		0		2.5	
Logic Levels					
Input Low Voltage, V_{IL}		0		0.36 × VDD11	
Input High Voltage, V_{IH}		0.73 × VDD11		2.5	
DIGITAL INPUTS (GPIOx, $\overline{DCS}$, and DCLK)	IOVDD supply domain inputs				
Input Voltage Tolerance		0		1.26	V
Logic Levels					
Input Low Voltage, V_{IL}		0		0.36 × IOVDD	V
Input High Voltage, V_{IH}		0.73 × IOVDD		IOVDD	V
Input Current					
Input Low Current, I_{IL}		−1		+1	µA
Input High Current, I_{IH}		−1		+1	µA
Input Pin Capacitance			4.5		pF
DIGITAL OUTPUTS (GPIOx)	IOVDD supply domain outputs				
Logic Levels					
Output Low Voltage, V_{OL}	Sink current (I_{SINK}) = 500 µA	0		0.15	V
Output High Voltage, V_{OH}	Source current (I_{SOURCE}) = 500 µA	IOVDD − 0.115		IOVDD	V
DIGITAL OUTPUTS (SDOx)	IOVDD supply domain outputs.				
Data Format	Configured as serial data output		Twos complement		
Logic Levels					
V_{OL}	I_{SINK} = 500 µA			0.15	V
V_{OH}	I_{SOURCE} = 500 µA	IOVDD − 0.115		IOVDD	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLIES					
VDD33		3.135	3.30	3.465	V
VDDLDO		1.4		2.7	V
VDD11	Applied externally, LDO disabled	1.045	1.10	1.155	V
IOVDD	Applied externally, LDO disabled	1.045	1.10	1.26	V
Operating Current	LVDS_CNV_EN = 0				
Static	Converter and interface idle, FIFO disabled				
VDD33			5.4	7	mA
VDDLDO	VDD11 LDO disabled		0	0.02	mA
VDD11			15.3	23	mA
IOVDD			5.2	6	mA
VDDLDO	VDD11 LDO enabled		21.5	26.5	mA
Dynamic	DC input signal				
VDD33			15.7	18	mA
VDDLDO	VDD11 LDO disabled		0	0.02	mA
VDD11			23.2	32	mA
IOVDD			6	7.5	mA
VDDLDO	VDD11 LDO enabled		29.8	35.5	mA
Dynamic	−0.5 dBFS sine-wave input signal				
VDD33			14.2	16	mA
VDDLDO	VDD11 LDO disabled		0	0.02	mA
VDD11			23.2	32	mA
IOVDD			6.3	7.5	mA
VDDLDO	VDD11 LDO enabled		30.2	35.5	mA
Standby Mode					
VDD33			1.4	1.9	mA
VDDLDO	VDD11 LDO disabled		0	0.02	mA
VDD11			12	5.5	mA
IOVDD			2.6	3.5	mA
VDDLDO	VDD11 LDO enabled		1.8	5	mA
Sleep Mode					
VDD33			0.6	0.9	mA
VDDLDO	VDD11 LDO disabled		0	0.02	mA
VDD11			1.2	5.5	mA
IOVDD			2.6	3.5	mA
VDDLDO	VDD11 LDO enabled		1.5	4.5	mA
Power Dissipation					
Static	VDD11 LDO disabled		40.4	58.4	mW
Dynamic	DC input signal		83.9	108.8	mW
Dynamic	−0.5 dBFS sine-wave input signal		79.3	101.9	mW
Standby Mode	VDD11 LDO disabled		10.6	19.5	mW
Sleep Mode	VDD11 LDO disabled		6.2	13.9	mW
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

SPECIFICATIONS

TIMING SPECIFICATIONS

VDD33 = 3.3 V ± 5%, VDDLDO= 1.5 V to 2.7 V, VDD11 = 1.1 V ± 5%, IOVDD = 1.1 V − 5% to 1.2 V + 5%, V_{REFIN} = 3.0 V, f_S = 40 MHz, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

Table 2. Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Sampling Frequency	f_S	1.25		40	MHz
Conversion Time	t_{CONV}	25		800	ns
Acquisition Phase	t_{ACQ}	t_{CYC}			ns
Conversion Cycle Period	t_{CYC}	t_{CONV}			ns
LVDS Data Interface					
Data Interface Clock Count	N			10	
Active Data Lane Count	L			2	
CNV± High Time	t_{CNVH}	t_{CLK}	5 × t_{CLK}	t_{CYC} − t_{CNVL}	ns
CNV± Low Time	t_{CNVL}	t_{CLK}	5 × t_{CLK}	t_{CYC} − t_{CNVH}	ns
CNV± Edge to CLK± Rising Edge Alignment	t_{CCA}			535	ps
CNV± to Dx± (MSB) Ready	t_{MSB}				
Gain Error Correction Enabled			20.5	22.4	ns
Gain Error Correction Disabled			15.7	18	ns
CLK± Period	t_{CLK}	2.5		t_{CYC} × L/N	ns
CLK± Frequency	f_{CLK}		1/t_{CLK}	400	MHz
CLK± to Dx± Delay	t_{CLKD}			2.1	ns
CLK± to DCO± Delay (Echo Clock Mode)	t_{DCO}			2	ns
DCO± to Dx± Delay (Echo Clock Mode)	t_{DCOD}			1	ns
Serial Peripheral Interface (SPI) Data Interface					
Data Interface Clock Count, Single Conversion Result	M			24	
Active Data Lane Count	C		1	4	
Data Interface Chip Select Falling Edge ($\overline{DCS}$) to SDOB Data Valid	t_{DEN}	5	6		ns
Data Interface Clock Period (DCLK)	t_{DCK}	20			ns
Data Interface Clock Low Pulse Width (DCLK)	t_{DCKL}	t_{DCK} × 0.45			ns
Data Interface Clock High Pulse Width (DCLK)	t_{DCLKH}	t_{DCK} × 0.45			ns
Data Interface Clock Falling Edge to Data Remains Valid Delay	t_{DHSDO}	5			ns
Data Interface Clock Falling Edge to Data Valid Delay	t_{DDSDO}			9.6	ns
DCLK Rising to Data Interface Chip Select Falling	t_{DCKEN}	0			ns
Data Interface Chip Select High to DCLK Disabled	$t_{DCLKDIS}$	0			ns
Data Interface Chip Select High Between Frames	t_{DCSMIN}		(t_{DCKEN} + $t_{DCLKDIS}$) + 0.5 × t_{DCLK}		ns
Serial Configuration Interface					
SCLK Period	t_{SCK}	20			ns
SCLK Low Pulse Width	t_{SCKL}	t_{SCK} × 0.45			ns
SCLK High Pulse Width	t_{SCKH}	t_{SCK} × 0.45			ns
SCLK Falling Edge to Data Remains Valid Delay	t_{HSDO}	0.7			ns
SCLK Falling Edge to Data Valid Delay	t_{DSDO}			14.5	ns
$\overline{CS}$ Falling Edge to SCLK	t_{CSSCK}	0			ns
Last SCLK to $\overline{CS}$ Rising	t_{SCKCS}	0			ns
SDI Valid Setup Time Before SCLK Rising Edge	t_{SSDI}	1			ns
SDI Valid Hold Time After SCLK Rising Edge	t_{HSDI}	0			ns
SCLK Rising to Data Interface Chip Select Falling	t_{SCKEN}	0			ns

SPECIFICATIONS

Table 2. Timing Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Data Interface Chip Select High to SCLK Disabled	t_{SCKDIS}	0			ns
Data Interface Chip Select High to SDO Disabled	t_{CSDIS}			10.3	ns
Data Interface Chip Select High Between Frames	t_{CSMIN}		$(t_{SCKEN} + t_{SCKDIS}) + 0.5 \times t_{SCK}$		ns
Digital Filter					
$\overline{\text{FILT\_SYNC}}$ Rising Edge to CNV Rising Edge	$t_{SYNC\ MAX}$		14		ns
CNV Rising Edge to $\overline{\text{FILT\_SYNC}}$ Falling Edge	$t_{SYNC\ MIN}$		5	5	ns
Event Detection					
Input Threshold Crossed to $\overline{\text{ALERT}}$ Asserted	t_{EVT}	$2 \times t_{CYC}$		$3 \times t_{CYC}$	

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
Analog Inputs	
IN+, AUXIN+, IN−, and AUXIN− to GND	−0.3 V to +3.6 V
Analog Output	
CMO	−0.3 V to +3.6 V
Supply Voltage	
REFIN and VDD33 to GND	−0.3 V to +3.6 V
VDDLDO to GND	−0.3 V to +2.75 V
VDD11 to GND	−0.3 V to +1.26 V
IOVDD to GND	−0.3 V to +1.26 V
Digital Inputs and Outputs	
Inputs (CNV± and CLK±) to GND	−0.3 V to +2.75 V
LVDS OUTPUT (DCO±, DA±, and DB±) to GND	−0.3 V to +1.26 V
$\overline{CS}$, SCLK, and SDI to GND	−0.3 V to +2.75 V
GPIO0, GPIO1, GPIO2, and GPIO3 to GND	−0.3 V to +1.26 V
Temperature	
Storage Range	−55°C to +150°C
Operating Range	−40°C to +85°C
Maximum Reflow (Package) as per JEDEC J-STD-020	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case top thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
BC-49-8	66.6	53.1	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in and ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the AD4080

Table 5. AD4080, 49-Ball CSP_BGA

ESD Model	Withstand Threshold (V)	Class
HBM	1000	1B
FICDM	750	2B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

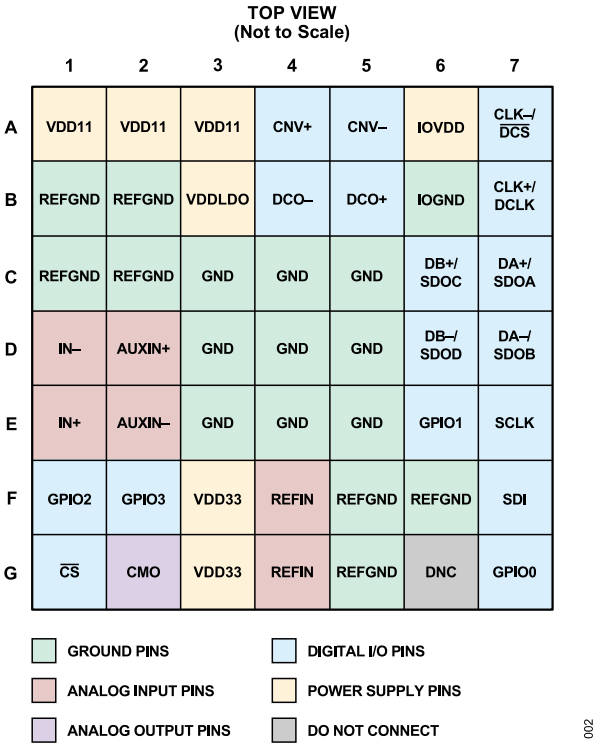

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1, A2, A3	VDD11	P	1.1 V ADC Core Supplies. These supply pins are internally decoupled by four, 470 nF capacitors to GND. When power is supplied to VDDLDO (B3), an internal LDO voltage regulator produces the 1.1 V required at these pins. The voltage regulator is automatically powered on when VDDLDO is greater than 1.4 V. If VDDLDO is left disconnected, the required 1.1 V must be supplied to these pins from an external source.
A4, A5	CNV+, CNV−	DI	Convert Start Inputs. This pin pair serves as the conversion control input; a conversion is initiated on the rising edge of the convert signal. These inputs are by default configured in complementary metal-oxide semiconductor (CMOS) mode, in which CNV− must be tied to IOGND and the convert signal is applied to CNV+. In the LVDS data interface mode, the convert start input can be optionally configured in LVDS mode, in which case, the convert signal is applied differentially to CNV+ and CNV− and an external 100 Ω termination resistor must be placed across these pins. See the ADC Conversion Control section for further details.
A6	IOVDD	P	1.1 V Digital Interface Supply Rail. This supply is internally decoupled by a 220 nF capacitor to IOGND. When power is supplied to VDDLDO (B3), an internal LDO voltage regulator produces the 1.1 V required at this pin. The voltage regulator is automatically powered on when VDDLDO is greater than 1.5 V. If VDDLDO is left disconnected, the required 1.1 V must be supplied to this pin from an external source (typically the host controller interface supply).
A7	CLK−/$\overline{\text{DCS}}$	DI	Data Interface Clock Input (CLK−)/Data Interface Chip Select ($\overline{\text{DCS}}$) Multifunction Pin. In LVDS data interface mode (default), this pin serves as half of the differential data clock input, and an external 100 Ω termination resistor must be present between it and the CLK+ pin.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
			In SPI data interface mode, this pin functions as a chip select input (data interface chip select).
B1, B2, C1, C2, F5, F6, G5	REFGND	P	Reference Grounds. Connect any external reference decoupling capacitors across REFIN and REFGND. REFGND must be tied with a low impedance path to GND.
B3	VDDLDO	P	LDO Supply Rail Input. This supply rail is internally decoupled by a 220 nF capacitor to GND. The two internal, 1.1 V, LDO voltage regulators can be supplied from a source connected to this input in the 1.5 V to 2.7 V range. If this pin is left open, the internal regulators automatically power off and both VDD11and IOVDD must be connected with an external voltage source within their allowed specification limits. If VDDLDO is connected to a voltage source, neither VDD11 nor IOVDD should be connected to any external voltage source.
B4, B5	DCO−, DCO+	DO	LVDS Echo Clock Outputs. In LVDS data interface mode (default), this pin pair outputs a buffered and delayed version of CLK+ and CLK−. Data outputs from LVDS Data Lane DA+ and Data Lane DA− (and Data Lane DB+ and Data Lane DB− if active) are clocked out in alignment with both rising and falling edges of DCO+ and DCO−. In SPI data interface mode (or if the echo clock mode is disabled while in LVDS data interface mode), these pins can be left unconnected.
B6	IOGND	P	Digital Interface Supply Ground Reference. This pin must be connected to the same ground plane as all other GND pins. All pins specified as type DI, DO, or DI/O must use this ground reference.
B7	CLK+/DCLK	DI	Data Interface Clock Input Multifunction Pin. In LVDS data interface mode (default), this pin serves as half of the differential data clock input, and an external 100 Ω termination resistor must be present between it and the CLK− pin. In SPI data interface mode, the single-ended data clock signal must be applied to this pin.
C3 to C5, D3 to D5, E3 to E5	GND	P	Grounds. All ground pins must be connected to a PCB GND plane.
C6	DB+/SDOC	DO	Data Interface Output Multifunction Pin. In LVDS data interface mode (default), this output pin along with DB− serves as the optional, secondary LVDS Data Lane B. If unused, leave unconnected. In SPI data interface mode, this pin functions as Serial Data Output C (SDOC), which is active in a four-lane configuration only. Result data is shifted out of this pin on the falling edge of the data interface clock (DCLK). This pin must left unconnected if not being used.
C7	DA+/SDOA	DO	Data Interface Output Multifunction Pin. In LVDS data interface mode (default), this output pin along with DA− serves as the primary LVDS Data Lane A. In SPI data interface mode, this pin functions as Serial Data Output A (SDOA), which is active in a four-lane configuration only. Result data is shifted out of this pin on the falling edge of the data interface clock (DCLK). This pin must left unconnected if not being used.
D1	IN+	AI	Positive Analog Differential Input.
D2	AUXIN+	AI	Positive Auxiliary Analog Differential Input.
D6	DB−/SDOD	DO	Data Interface Output Multifunction Pin. In LVDS data interface mode (default), this output pin along with DB+ serves as the optional, secondary LVDS Data Lane B. If unused, leave unconnected. In SPI data interface mode, this pin functions as Serial Data Output D (SDOD), which is active in a four-lane configuration only. Result data is shifted out of this pin on the

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
			falling edge of the data interface clock (DCLK). Note that this pin does not go into a high impedance state when used in four-lane SPI mode when $\overline{CS}$ is inactive. This pin must be left unconnected if not being used.
D7	DA−/SDOB	DO	Data Interface Output In LVDS data interface mode (default), this output pin along with DA+ serves as the primary LVDS Data Lane A. If unused, leave unconnected. In SPI data interface mode, this pin functions as Serial Data Output B (SDOB). This is the only active serial data output in single lane mode. Result data is shifted out of this pin on the falling edge of the data interface clock (DCLK).
E1	IN−	AI	Negative Analog Differential Input.
E2	AUXIN−	AI	Negative Auxiliary Analog Differential Input.
E6	GPIO1	DI/O	General-Purpose Input and Output 1 Pin.
E7	SCLK	DI	Configuration Interface Serial Data Clock. This clock input is used to shift data into and out of the device configuration memory.
F1	GPIO2	DI/O	General-Purpose Input and Output 2 Pin.
F2	GPIO3	DI/O	General-Purpose Input and Output 3 Pin.
F3, G3	VDD33	P	3.3 V Supply Rail Inputs. These supply pins are internally decoupled by a 470 nF capacitor to GND.
F4, G4	REFIN	AI	3.0 V Reference Voltage Inputs.
F7	SDI	DI	Serial Data Input. Configuration data is shifted into this input on the rising edge of the serial data clock, SCLK.
G1	$\overline{CS}$	DI	Configuration Interface Chip Select Input (Active Low). The $\overline{CS}$ input frames serial data transfers over the configuration SPI.
G2	CMO	AO	Common-Mode Voltage (V_{CM}) Output.
G6	DNC	DNC	Do Not Connect.
G7	GPIO0	DI/O	General-Purpose Input and Output 0 Pin.

[1] AI is analog input, AO is analog output, DI is digital input; DI/O is digital input and output, DO is digital output, and P is power.

TYPICAL PERFORMANCE CHARACTERISTICS

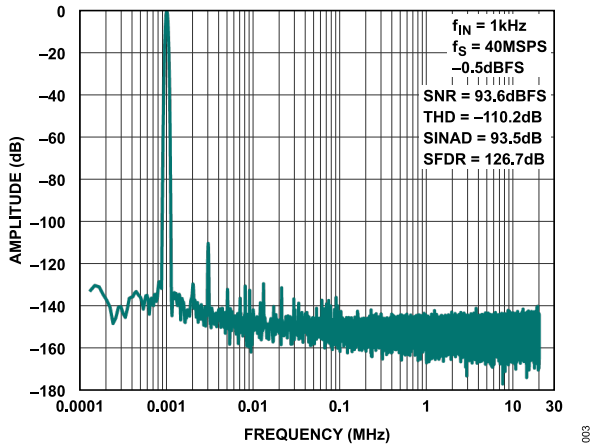

Figure 3. FFT 40 MSPS, f_{IN} = 1 kHz, −0.5 dBFS

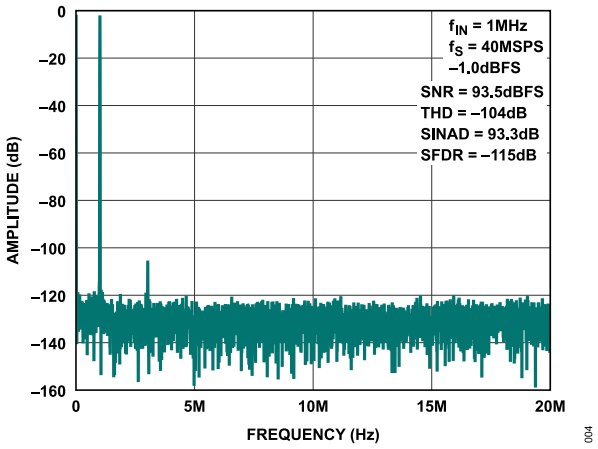

Figure 4. FFT 40 MSPS, f_{IN} = 1 MHz, −1.0 dBFS

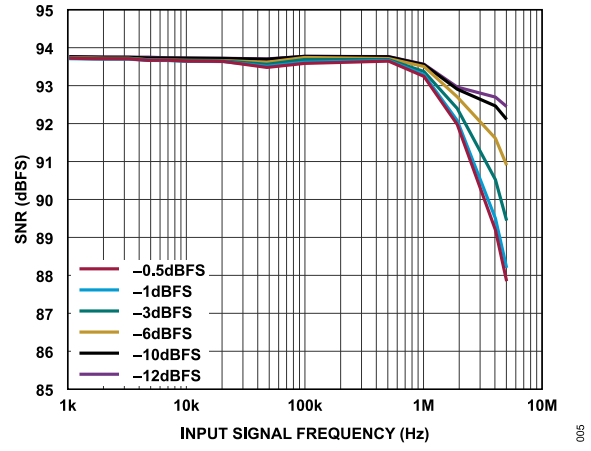

Figure 5. SNR vs. Input Signal Frequency (Amplitude = −0.5 dBFS, −1 dBFS, −3 dBFS, −6 dBFS, −10 dBFS, and −12 dBFS)

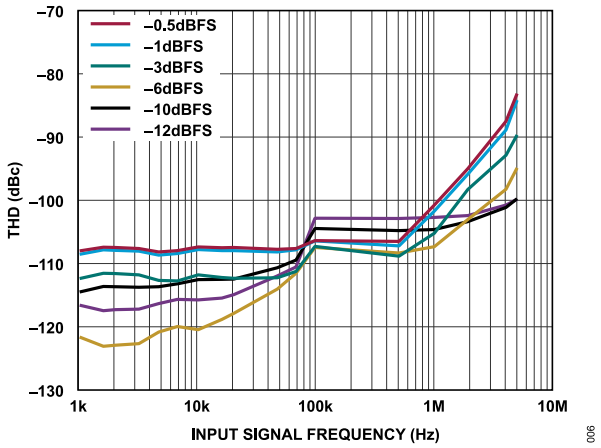

Figure 6. THD vs. Input Signal Frequency (Amplitude = −0.5 dBFS, −1 dBFS, −3 dBFS, −6 dBFS, −10 dBFS, and −12 dBFS)

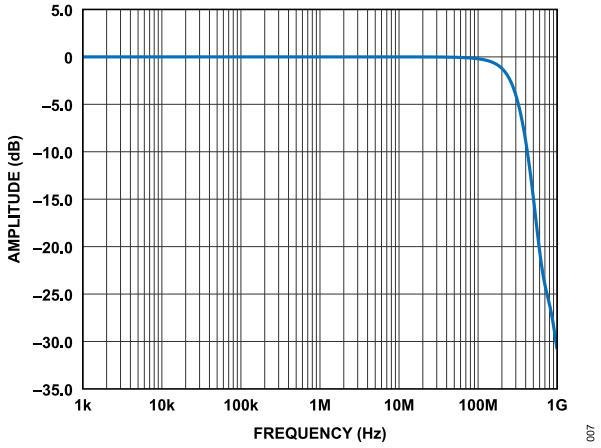

Figure 7. Small Signal −3 dB Bandwidth at 40 MSPS

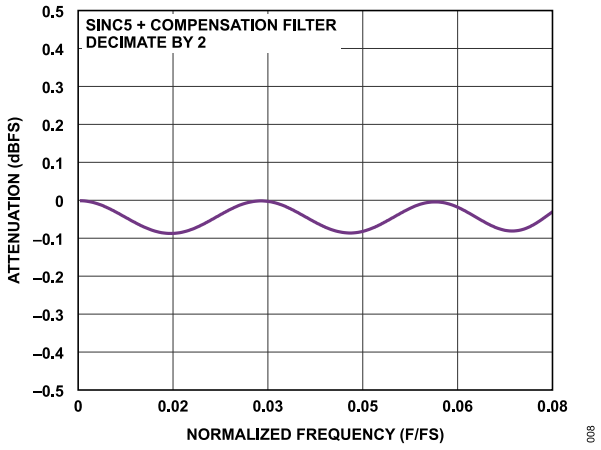

Figure 8. Sinc5 + Compensation Filter, Pass-Band Flatness

TYPICAL PERFORMANCE CHARACTERISTICS

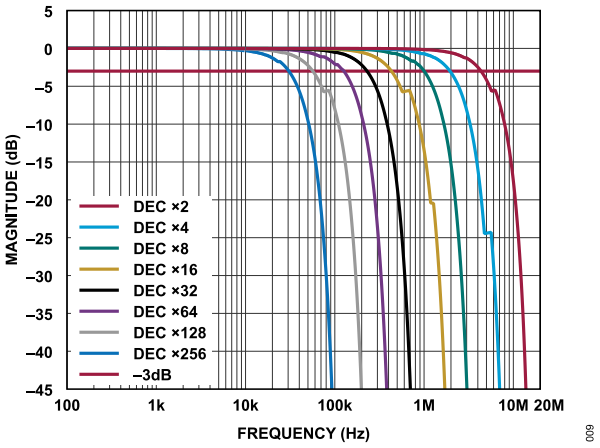

Figure 9. Sinc1 Filter Response, f_S = 40 MHz (DEC x Means Decimate By)

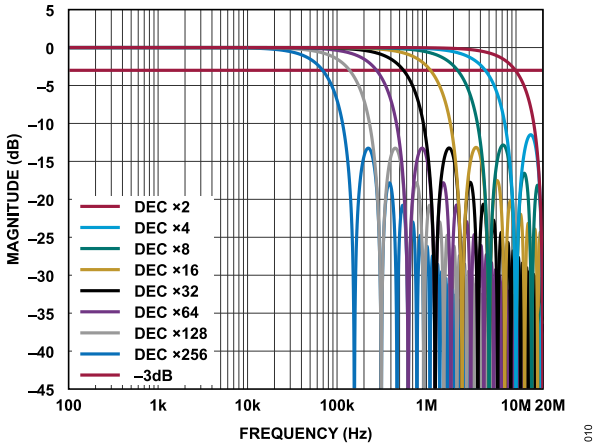

Figure 10. Sinc5 Filter Response, f_S = 40 MHz

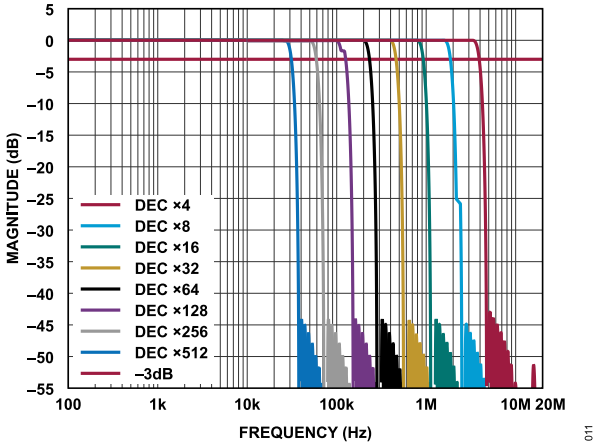

Figure 11. Sinc5 + Compensation Filter Response, f_S = 40 MHz

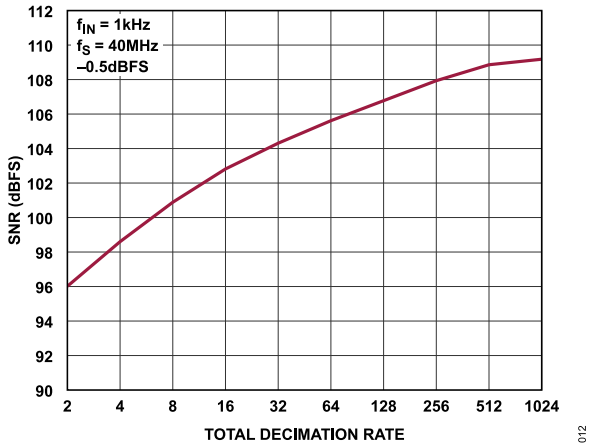

Figure 12. SNR vs. Total Decimation Rate, Sinc1

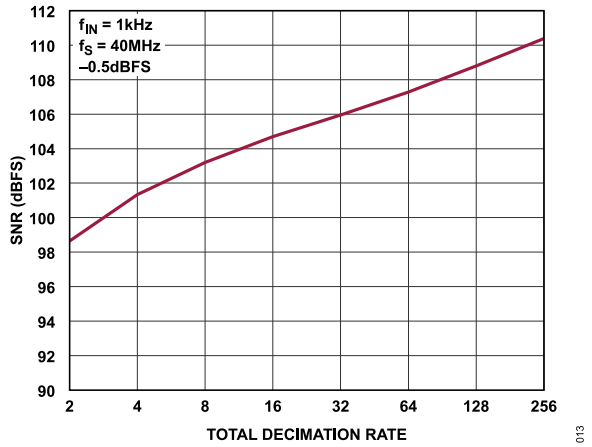

Figure 13. SNR vs. Total Decimation Rate, Sinc5

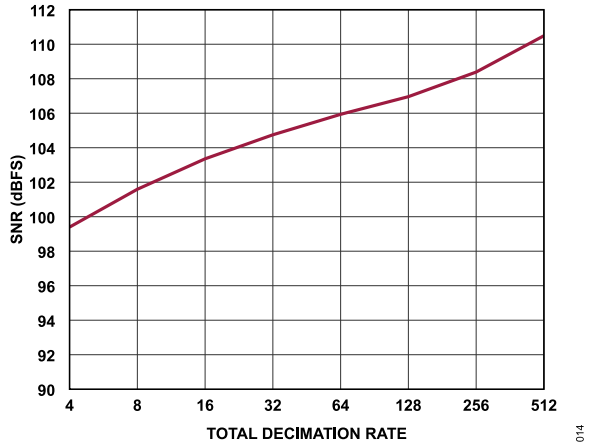

Figure 14. SNR vs. Total Decimation Rate, Sinc5 + Compensation

TYPICAL PERFORMANCE CHARACTERISTICS

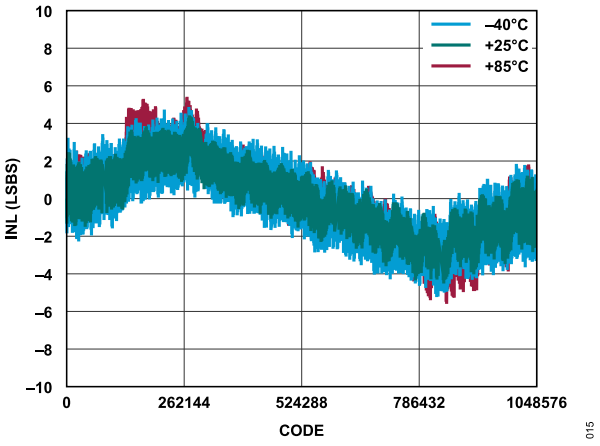

Figure 15. INL vs. Code for Various Temperatures, 40 MSPS

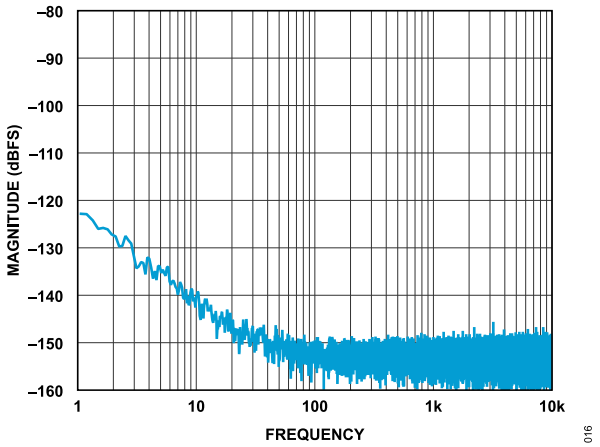

Figure 16. Low Frequency Noise, Inputs Shorted

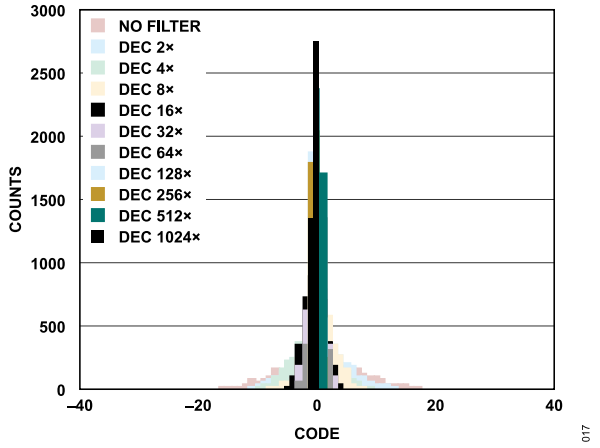

Figure 17. Histogram of Codes, Sinc1, Decimate 2×, Decimate 4× ... Decimate 1024×

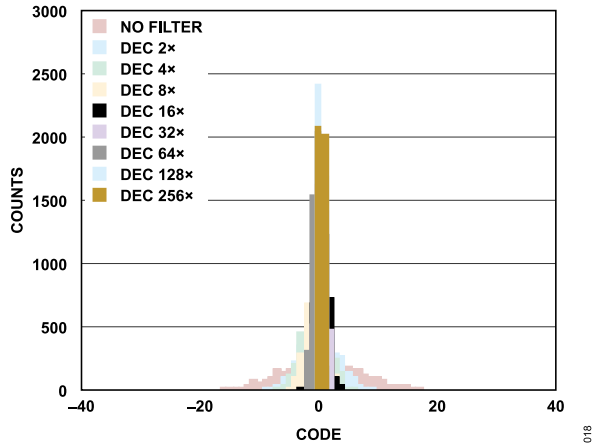

Figure 18. Histogram of Codes, Sinc5, Decimate 2×, Decimate 4× ...Decimate ×

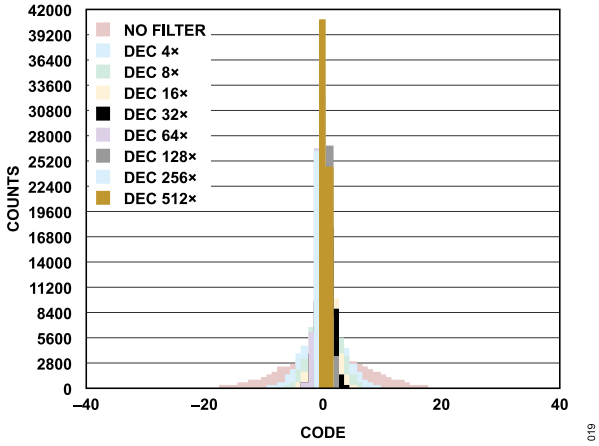

Figure 19. Histogram of Codes, Sinc5 + Compensation, Decimate 2×, Decimate 4× ... Decimate 512×

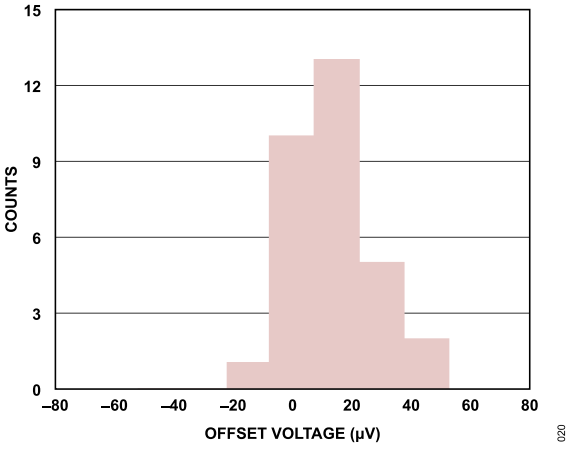

Figure 20. Offset Voltage Histogram

TYPICAL PERFORMANCE CHARACTERISTICS

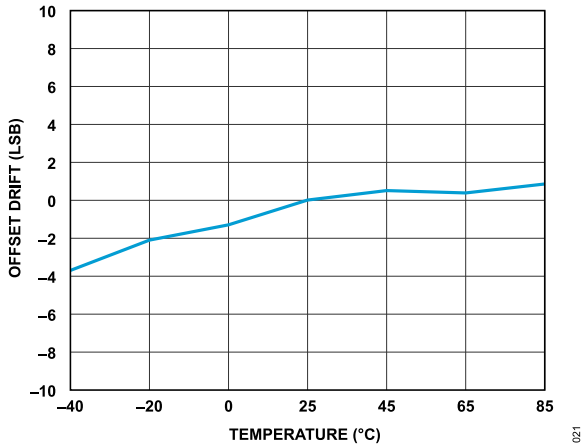

Figure 21. Offset Drift vs. Temperature

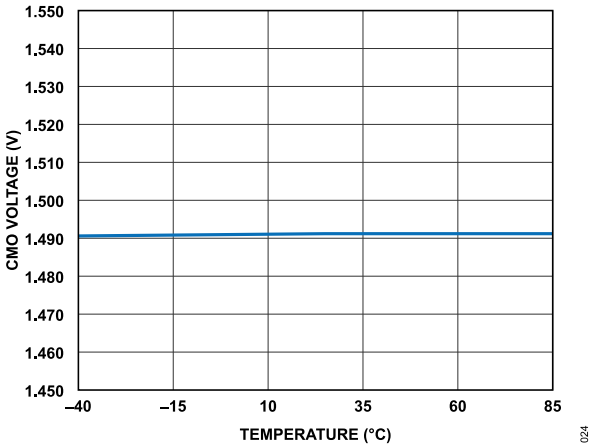

Figure 24. CMO Voltage vs. Temperature

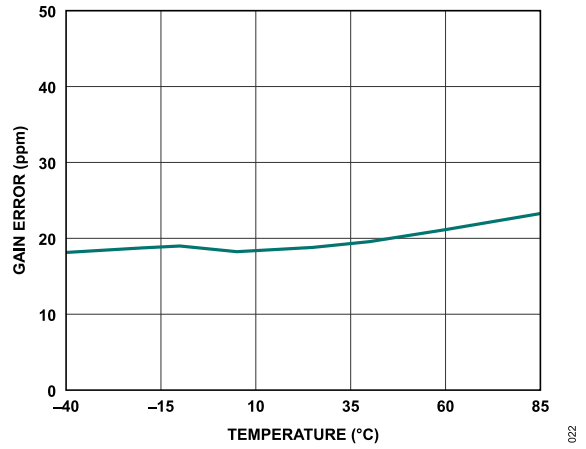

Figure 22. Gain Error vs. Temperature

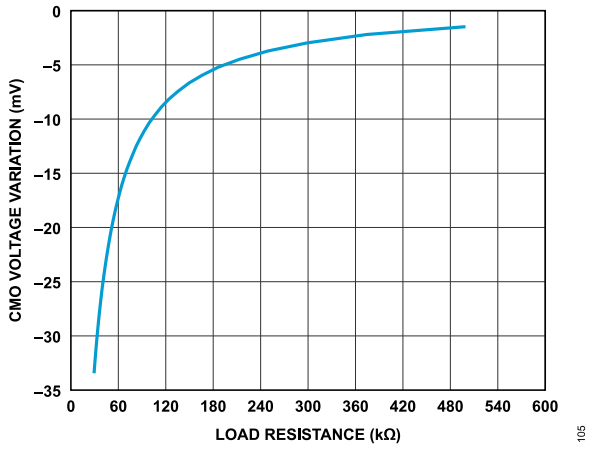

Figure 25. CMO Voltage Variation vs. Load Resistance

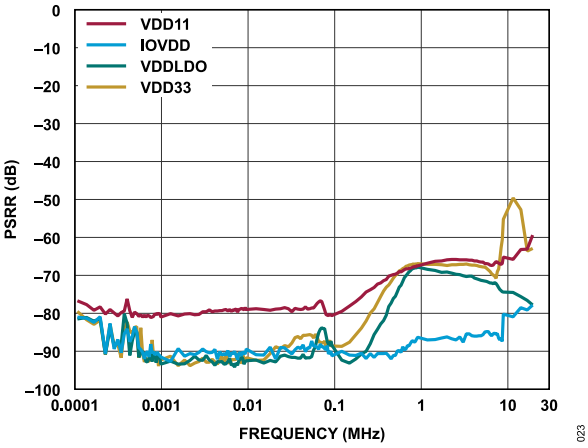

Figure 23. PSRR vs. Frequency

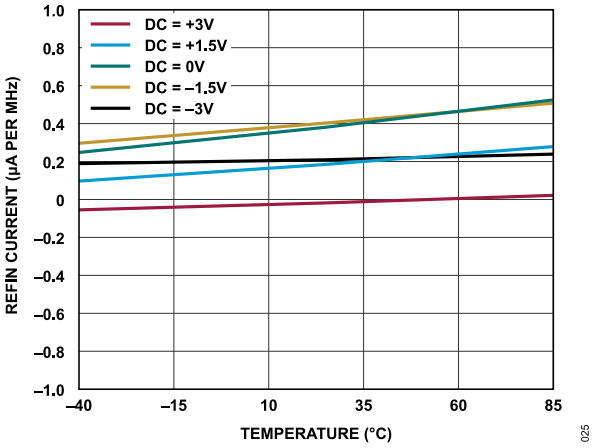

Figure 26. Dynamic REFIN Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

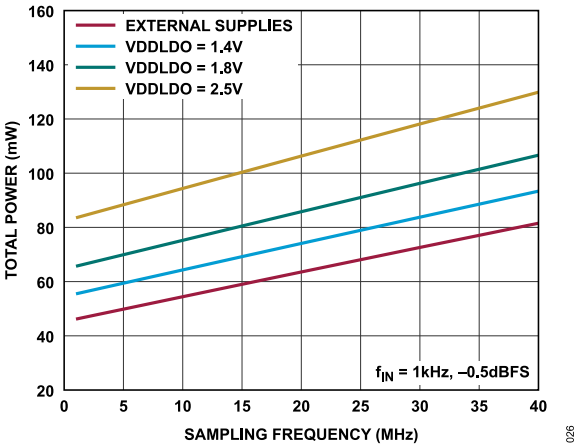

Figure 27. Total Power vs. Sampling Frequency

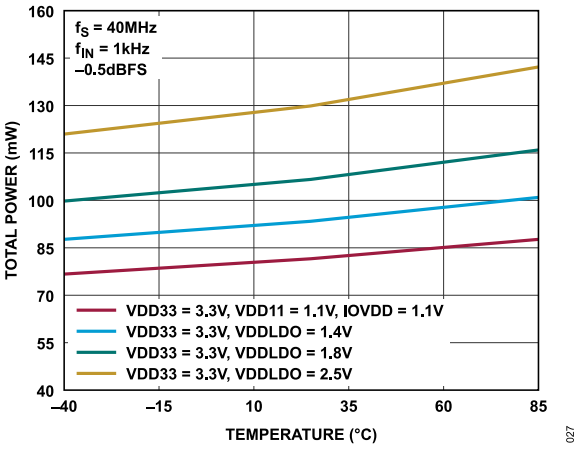

Figure 28. Total Power at 40 MSPS vs. Temperature

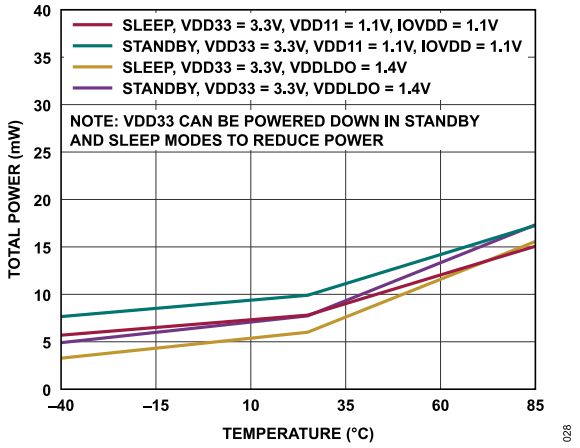

Figure 29. Total Power vs. Temperature in Sleep and Standby Modes

TERMINOLOGY

Integral Nonlinearity Error (INL)

INL refers to the deviation of each output code from a line drawn between points at negative full scale and positive full scale. The negative full-scale reference is defined by an input level equivalent to ½ LSB prior to the first code transition. The positive full-scale reference is defined as an input level that is 1½ LSB beyond the last code transition. The deviation is measured from the center of each code relative to the straight line.

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions occur at 1 LSB intervals. DNL is a measure of the maximum deviation of any code from the ideal code width. DNL is specified in terms of resolution for which no missing codes are guaranteed.

Zero Error

Zero error is the difference between the ideal midscale voltage, 0 V, and the applied voltage producing the midscale output code, 0 LSB.

Gain Error

Gain error is specified as the difference in the slope of the ADC transfer characteristic vs. that of an ideal converter. In an ideal data converter, the first code transition (100 … 00 to 100 … 01) occurs ½ LSB more than the nominal negative full-scale input (−2.999997 V for a ±3.0 V range at 20 bits) and the last code transition (011 … 10 to 011 … 11) occurs 1½ LSB less than the nominal positive full-scale input (+2.999991 V for a ±3.0 V range at 20 bits).

Signal-to-Noise Ratio (SNR)

SNR is the computed ratio of the fundamental signal amplitude measured in RMS volts and the root sum of squares of all other spectral components in the Nyquist bandwidth ($f < f_S/2$) excluding harmonics and DC components. The computed value of SNR is converted into a logarithmic scale and expressed in decibels (dB).

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the computed ratio of the fundamental signal amplitude measured in RMS volts and the root sum of squares of all other spectral components in the Nyquist bandwidth ($f < f_S/2$) including harmonic components but excluding the DC component. The computed value of SINAD is converted into a logarithmic scale and expressed in decibels (dB).

Total Harmonic Distortion (THD)

THD is the ratio of RMS sum of the amplitudes of the first five harmonic components to the RMS amplitude of a full-scale input signal expressed in decibels (dB).

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio between the RMS amplitude of the input signal and the peak spurious signal amplitude, expressed in decibels (dB).

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities creates distortion products at sum and difference frequencies of $m \times f_A$ and $n \times f_B$, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include ($f_A + f_B$) and ($f_A - f_B$), and the third-order terms include ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$), and ($f_A - 2f_B$).

The AD4080 is tested where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second-order and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the RMS sum of the individual distortion products to the RMS amplitude of the sum of the fundamentals, expressed in decibels.

Power Supply Rejection Ratio (PSRR)

PSRR is a measure of the sensitivity of the ADC to variations in the specified power supply rail vs. frequency. PSRR is computed as the ratio of the observed change in the output code in RMS volts to the RMS magnitude of the perturbing signal coupled to the supply. The resulting ratio is reported in decibels (dB).

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PRODUCT OVERVIEW

The AD4080 is a high-speed, low noise, low distortion, 20-bit, Easy Drive, SAR ADC. The device is capable of conversion rates up to 40 MSPS, with 46.25 ns result output latency. The parametric performance, bandwidth, and throughput make this product ideal for a variety of high-speed, data acquisition applications. Innovations in the AD4080 product design enable both complexity reduction and component flexibility in the design of data acquisition signal chains.

The converter architecture enables continuous acquisition of the input signal throughout the entire conversion period, t_{CONV}, reducing the input signal conditioning bandwidth required to settle to the specified resolution.

The design incorporates circuitry to reduce the nonlinear input current associated with the charge kickback typical of a switched capacitor SAR input.

Conversion result access occurs via either a multilane LVDS port operating at clock rates up to 400 MHz or via a multioutput SPI operating at clock rates up to 50 MHz.

The LVDS interface is compatible with differential signaling standards between 1.2 V and 2.5 V. To maximize throughput the previous conversion results can be read through the entirety of the conversion period as long as the CNV+ edge and CLK+ rising edges are aligned. The LVDS interface is described in detail in the LVDS Data Interface Configuration section.

The single or quad lane SPI data interface is also available for CMOS level interfacing. When configured, this interface is used to access conversion results stored in the on-chip FIFO. FIFO operation is explained in the Result FIFO section.

CONVERTER OPERATION

A conventional SAR ADC typically operates in two phases; an acquisition phase, whereby the analog input voltage is acquired on the analog input pins, followed by a conversion phase, initiated by a conversion start signal. During the conversion phase the sampled analog input voltage is converted to a digital conversion result. In a single ADC, this is typically performed by converting the voltage from one sampling circuit. In the case of the AD4080, Figure 30 details the unique feature of this converter, whereby the analog input is connected to two sampling circuits, and the input is sampled by each one in sequence. To a user, this requires no additional control or configuration, and as such, is completely transparent in usage.

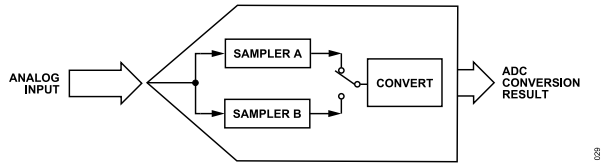

Figure 30. Simplified Representation of the AD4080 SAR ADC

The AD4080 converter seamlessly sequences back and forth from one sampler to the other, meaning that one sampler is in acquisition mode while the voltage sampled on the other is being converted. Figure 31 shows that the AD4080 timing is contrasted against a conventional SAR ADC, where it switches between sequential conversion and the acquisition phase leads to a reduced amount of time for the input signal acquisition and settling. As sampling rates increase (and therefore cycle times reduce), it is important to maintain longer acquisition times to enable settling, particularly to the higher levels of precision offered by the AD4080. Further details on the benefits of reducing driver and noise bandwidths are described in the Easy Drive Analog Inputs section.

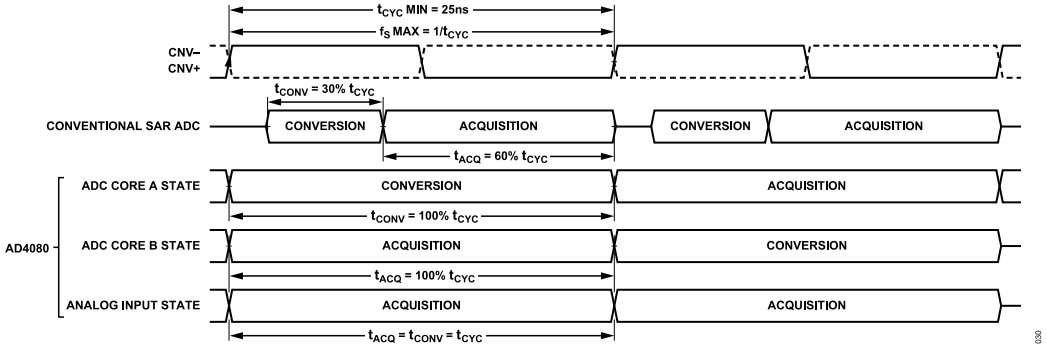

Figure 31. Conversion Cycle Compared to Conventional SAR

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TRANSFER FUNCTION

The AD4080 digitizes the full-scale difference voltage of 2 × V_{REFIN} into 2^{20} levels, resulting in an LSB size of 5.72 µV with V_{REFIN} = 3.0 V. Note that 1 LSB at 20 bits is approximately 0.95 ppm.

Table 7 summarizes the mapping of input voltages to differential output codes.

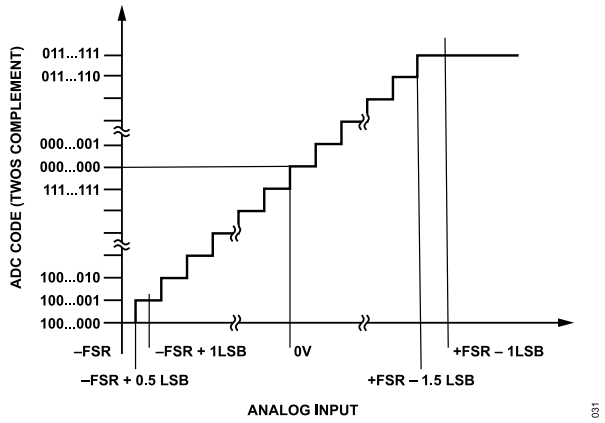

Figure 32. ADC Ideal Transfer Function for the Differential Output Codes (FSR Is Full-Scale Range)

Table 7. Input Voltage to Output Code Mapping

Description	Analog Input Voltage Difference (IN+ − IN−, Volts)	Digital Output Code (Twos Complement, Hex)
FS − 1 LSB	$+V_{REFIN} \times (1 - 1/2^{19})$	0x7FFFF
Midscale + 1 LSB	$+V_{REFIN}/2^{19}$	0x00001
Midscale	0	0x00000
Midscale − 1 LSB	$-V_{REFIN}/2^{19}$	0xFFFFF
−FS + 1 LSB	$-V_{REFIN} \times (1 - 1/2^{19})$	0x80001
−FS	$-V_{REFIN}$	0x80000

EASY DRIVE ANALOG INPUTS

The AD4080 signal input consists of a fully differential input pair (IN+ and IN−), each connected to the input sampling network (series resistance (R_S) and sampling capacitance (C_S)) and a pair of auxiliary inputs (AUXIN+ and AUXIN−) that provide a reference to the sampling network linearization circuits. An equivalent circuit model of the analog input is presented in Figure 33.

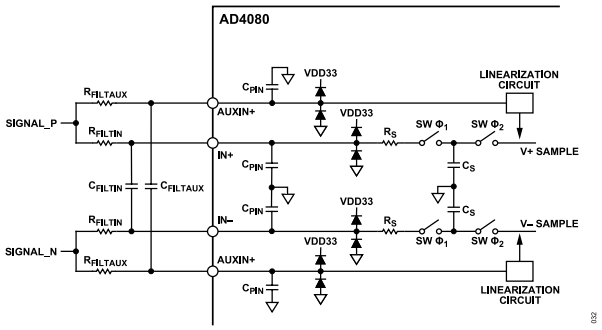

Figure 33. Equivalent Analog Input Circuit Model

In this model, the input sampling network was simplified to consist of two ideal switches, R_S and C_S, for the ADC in acquisition mode. The typical values for C_S is 23.5 pF and R_S is 26 Ω.

The parasitic capacitance related to the pin connection, C_{PIN}, is modeled as a shunt capacitor between the pin and device ground terminal (GND). The capacitance includes parasitic capacitance formed from the physical interface, routing in the package substrate and the device input protection circuits. The C_{PIN} value is typically 4.5 pF. The input protection circuit for the AD4080 is modeled as diode clamps to the GND and VDD33 supply rails.

The external low-pass filters (LPFs) constructed from R_{FILTIN} and C_{FILTIN} and $R_{FILTAUX}$ and $C_{FILTAUX}$ are band-limiting filters for the primary and auxiliary paths, respectively.

The combination of R_{FILTIN} and C_{FILTIN} are often referred to as anti-aliasing filters because these filters do introduce a single-pole filter in the analog input signal path. However, the function of C_{FILTIN} is more complex and must be carefully considered. Conversion through a SAR involves sampling the voltage from an internal capacitor, represented by C_S in the Figure 33, which typically occurs in two phases in time ϕ_1 and ϕ_2 . During the first phase, the ϕ_1 switches are closed, the ϕ_2 switches are opened, and the sampling capacitors (C_S) are charged to the analog input voltages present at IN+ and IN−. During the second phase, the ϕ_1 switches are opened, the ϕ_2 are closed, and the ADC converts the voltage onto C_S.

Another short time phase exists, where the C_S charge is reset after the conversion is complete. This process repeats for each new ADC conversion. The transfer of charge from the ADC analog input pins to C_S, due to the closing of the switches in each conversion cycle, creates a demand at the analog input pin. It is important to ensure that the voltage presented at the input pin is undisturbed by the internal ADC activity so that the voltage can be converted with the highest accuracy. Each new conversion presents a disturbance, or kick, at the input. The faster the ADC conversion rate is, the more frequent the occurrence of these kicks. An ADC driver is used to ensure that the input voltage, disturbed by the kick at each sampling instance, is fully settled to the required ADC resolution prior to the next sample being acquired. The ADC driver amplifier must have a wide enough output bandwidth to settle the voltage in time for each sample, which creates a signal chain design constraint to

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ensure that there is enough time to settle to the required voltage accuracy (or ADC resolution). For this reason, a fast ADC requires a wide bandwidth driver. For high resolution ADC converters, low signal chain noise is required to obtain high resolution. A wider bandwidth can result in more noise coming through the signal chain to the ADC, which can present a significant signal chain design challenge for a conventional SAR ADC. However, the AD4080 includes some unique Easy Drive features that simplify these aspects of signal chain design.

One such AD4080 feature is continuous signal acquisition. Due to its unique design, that the t_{AQC} is equal to the t_{CYC} of the ADC, resulting in the AD4080 being in signal acquisition mode for the full duration of each ADC conversion. The input voltage has 100% of the t_{CYC} conversion time to settle the input voltage before the next conversion, whereas a conventional ADC may need to settle in 60% of this time. More settling time results in less bandwidth required by the driver, which generally, bears a lower power requirement. In addition, because the external filters (R_{FILTIN} and C_{FILTIN}) must be designed with enough bandwidth for the driver to settle the input voltage, the additional settling time results in a lower cut-off. Because of this lower cut-off, more of the signal chain noise can be filtered at the inputs with these external filters.

Another Easy Drive feature is its highly linearized analog input current. With this feature, the AD4080 presents a less challenging load to a driver amplifier and reduces any potential distortion from a driver that can occur when presented with a nonlinear input current. Figure 34 shows the typical input currents into both the differential signal pair (IN+ and IN−) and auxiliary inputs (AUXIN+ and AUXIN−).

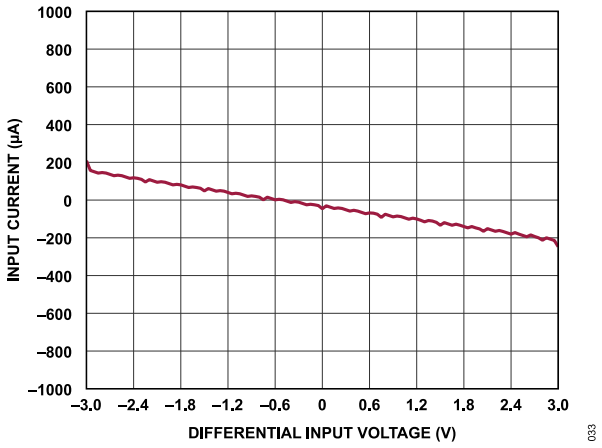

Figure 34. Typical Input Current vs. Differential Input Voltage

To design the external input filter, it is usual to calculate how many time constants (K) are needed for the required resolution. To calculate the time constant from the natural log of the required setting resolution, for example, if settling to within 1 LSB of 20 bits (n = 20) of resolution is desired, use the following equation:

$$K = \ln(2^n/1\ \text{bit}) = 13.86\ \text{time constants} \quad (1)$$

When considering a conventional ADC, as described in the Converter Operation section, where the acquisition time is only 60% of the ADC conversion cycle, there is less time available for settling. For such an ADC sampling at 40 MSPS, the driver must settle within 25 ns × 0.6 or 15 ns, and settling of the input voltage within 1 LSB also requires a time constant tau (τ) of 15 ns ÷ K = 1.082 ns or a bandwidth of 1/(2 × π × τ) = 147 MHz.

However, with the Easy Drive features of the AD4080, the result is an acquisition time of 100% of the conversion cycle, which indicates only 13.86 time constants to settle within 1 LSB of 20 bits resolution. However, additionally, the low analog input current of the AD4080 and the internal methods that reduce any kick back to the driver (as charge transfers from the analog input to the internal sampling capacitors at the sampling instance) reduce the required number of time constants by 9.5%. Therefore, for the 20-bit settling example, the required number of time constants (K) reduces from 13.86 to 12.55 without impact on settling or distortion.

These Easy Drive features significantly reduce the required driver bandwidth required to settle. For example, at 40 MSPS, settling of the input voltage within 1 LSB requires a time constant tau (τ) of 25 ns ÷ K = 1.992 ns, or a bandwidth of 1/(2 × π × τ) = 80 MHz. This significant reduction in the required bandwidth allows use of lower power, lower bandwidth drivers and the design of a lower bandwidth input filter to remove more driver or signal chain noise. Table 8 suggests some filter values for use with the AD4080 in some example use case conditions.

Another Easy Drive feature, as can be seen in the Figure 33, is the auxiliary signal input path. This path feeds the analog input signal to an internal linearization block, and this block feeds a correction signal to the sampled voltage. Recommended values are given in Table 8. The filter on the auxiliary inputs is set for the same bandwidth as the analog input, and $R_{FILTAUX}$ must be set at 4 × R_{FILTIN}. The recommended filter configuration is to use a differential C_{FILTIN} capacitor; therefore, calculate the components as τ = R_{FILTIN} × 2 × C_{FILTIN}.

Note that the minimum R_{FILTIN} must be 15 Ω, and that $R_{FILTAUX}$ can be set from a minimum of 5 Ω up to 4 × R_{FILTIN} .

Table 8. Recommended Input Filter Configurations

f_S (MSPS)	Target Accuracy (Bit)	Required Bandwidth (MHz)	R_{FILTIN} (Ω)	C_{FILTIN} (pF)	$R_{FILTAUX}$ (Ω)	$C_{FILTAUX}$ (pF)
40	20	80	25	39	100	10
40	18	72	25	47	100	10
30	20	60	25	47	100	10

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REFERENCE BUFFER AND COMMON-MODE OUTPUT

The AD4080 integrates a charge reservoir capacitor (C_{REF}) and a low-drift reference buffer at the reference input pin (REFIN), eliminating the need for dedicated external components and enabling multiple AD4080 devices to share a single voltage reference.

The integrated capacitor (C_{REF}) has a capacitance of 9.4 µF ± 20%, and it is constructed from commercially available, multilayer, high dielectric (X6S), ceramic capacitors. C_{REF} serves as the primary charge reservoir for the data converter. Integrated, in-package components, such as C_{REF}, minimize the overall solution area, mitigate potential performance errors introduced by factors like component selection, placement and routing challenges, and in general, reduce the engineering effort to first design success.

Additional external capacitance (C_{RSV}) can be placed across the REFIN and REFGND pins for improved charge capacity and noise rejection as required. As with all precision circuits, the placement of the external reference capacitors must be as close to the device pins as possible on the same side of the PCB. The routing between the capacitor and device pins must minimize the series impedance in each routing path.

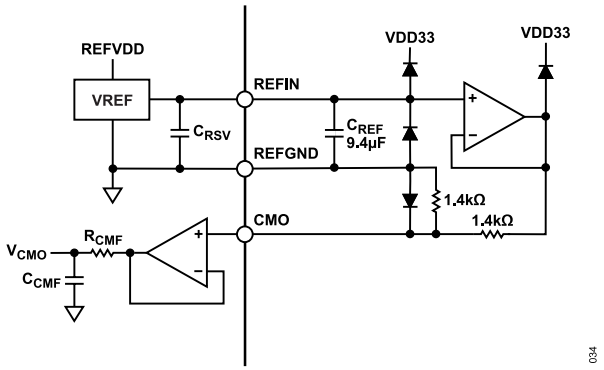

Figure 35. REFIN and CMO Internal Equivalent Circuit and Typical Application

The AD4080 internally generates a common-mode reference voltage of one-half of V_{REFIN}, which is output through the CMO pin. The absolute error in the CMO output voltage is guaranteed to be less than ±20 mV. The CMO output is used to set the common-mode output voltage of the analog front-end stage driving the AD4080 inputs, ensuring the AD4080 common-mode input requirement is satisfied. The CMO output must be filtered with a RC LPF to limit the total output noise as illustrated in Figure 35 (see R_{CMF} and C_{CMF}).

The output is generated using a resistive divider connected to the reference buffer output. The resulting output impedance at the CMO pin is typically 700 Ω. Due to the limited drive capability at the CMO pin, the external load must be carefully considered to avoid excessive start-up times or absolute errors. The CMO output may be directly connected to a high impedance common-mode input of a fully differential amplifier driving the AD4080, assuming the charging time for the preceding noise limiting filter does not impact the start-up time required for the application. In general, consider CMO buffering for the following situations:

- The VDD33 power rail of the AD4080 is frequently cycled.
- Short start-up settling times are required.
- If the external load on CMO exceeds 30 µA (R_L < 45 kΩ). See Figure 25 for the typical load regulation information.

POWER SUPPLIES

The power requirements for the AD4080 are distributed across a minimum of three supply domains including a 3.3 V analog circuit domain (VDD33), a 1.1 V core supply (VDD11), and a 1.1 V domain for the digital interface (IOVDD). An optional fourth supply rail (VDDLDO) can be used to supply power to two integrated voltage regulator used to internally power the 1.1 V core (VDD11) and interface (IOVDD) rails. Each of these two regulators can be independently turned off by software. For all details and design considerations when using the internal voltage regulators, see the Internally Regulated Supply Configuration section. On the other hand, for applications that will not use internal regulators see the Externally Generated Supply Configuration section for further details.

Power for the VDD33 supply rail must be supplied from an external source and must only be applied once power is supplied to the 1.1 V supply rails as described in the Power Supply Sequence section.

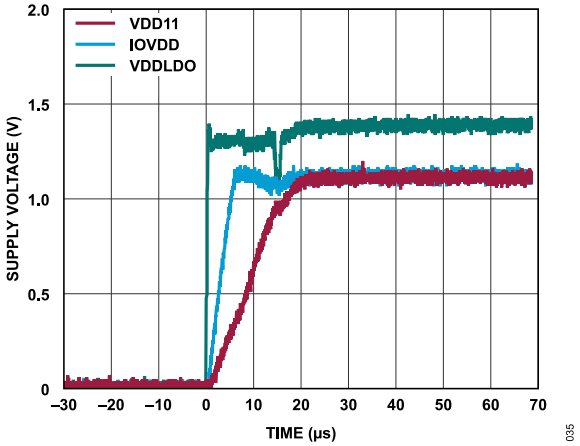

Figure 36. Typical Regulator Start-Up Transient, Converter Idle

All supply domains are internally decoupled using multilayer, high dielectric, ceramic capacitors (X6S), eliminating the need of external decoupling capacitors. However, care must be taken to understand the bulk decoupling requirements for other components in the design which share the same supply. Integrated supply decoupling capacitors in the AD4080 are listed Table 6 as well as in Table 9.

Table 9. Integrated Supply Decoupling Summary

Supply Pin	Nominal Value (µF)	Tolerance (%)	Return Path
VDD33	0.47	±10	GND
VDDLDO	0.22	±10	GND

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Table 9. Integrated Supply Decoupling Summary (Continued)

Supply Pin	Nominal Value (µF)	Tolerance (%)	Return Path
VDD11	1.88 (4× 0.47)	±10	GND
IOVDD	0.22	±10	IOGND

INTERNALLY REGULATED SUPPLY CONFIGURATION

The AD4080 includes two internal LDO regulators, one to generate the 1.1 V VDD11 supply rail and another to internally generate the 1.1V IOVDD supply rail. Upon power on or reset of the AD4080 registers, both regulators automatically power up when an external voltage source in the range of 1.4 V to 2.7 V is applied to the VDDLDO pin. The regulators are designed to supply the internal load requirement of the AD4080; therefore, no external loading is permitted. Noted that, as described in the Power Saving Operating Modes section, IOVDD is disabled in both power saving modes.

The required connectivity when using the internal regulators is illustrated in Figure 37. As shown in Figure 37, the VDD11 pins (A1, A2, and A3) must be shorted together. It is recommended that a thick trace or polygon on the device side of the PCB be used to implement this connection in the physical design to minimize routing impedance. The VDD33 rail is supplied with an external 3.3 V supply. This supply can be removed when using power saving modes. When this supply is removed, only analog circuity is held in reset, and the configuration register content remains unaffected. Refer to the Table 1 section for the applicable input voltage tolerance for each supply rail.

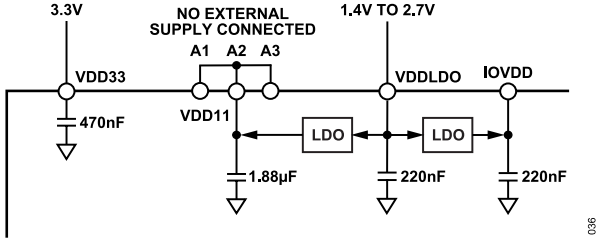

Figure 37. Internally Regulated (1.1 V) Supply Configuration

The internally regulated configuration is ideal for use in area constrained applications where the ability to eliminate external regulators is advantageous. However, noted that, in this configuration, the internal supply regulation introduces additional power dissipation.

EXTERNALLY GENERATED SUPPLY CONFIGURATION

In system using externally generated supplies VDDLDO must be left unconnected. With VDDLDO unconnected both the internal LDO powering VDD11 and the internal LDO powering IOVDDD are automatically disabled. VDD11 must be connected to an externally generated 1.1V supply rail and IOVDD should be connected to an externally generated 1.1V to 1.2V supply rail. It should be noted that if VDD11 is not present the part will be held in a POR state and all AD4080 registers reset to their default state the after the supply has been reestablished. More details on the POR circuitry can be found in the Power-On Reset (POR) Monitor section. The VDD33 rail is supplied with an external 3.3 V supply. The VDD33 supply can be removed to further reduce power in the Power Saving Operating Modes, only analog circuity is in held in reset, and the register content remains unaffected. Refer to Table 1 for the applicable input voltage tolerance for each supply rail.

As illustrated in the example of Figure 38, external voltage sources are applied to VDD11 and IOVDD pins.

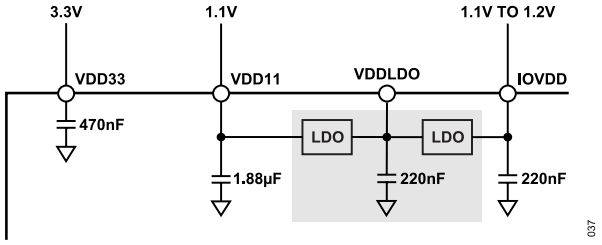

Figure 38. Externally Sourced Supply Configuration

POWER-ON RESET (POR) MONITOR

The AD4080 power supply monitoring circuits inhibit the converter functions and reset the configuration memory when supply conditions are outside the specified operating limits. This function ensures each device is in a deterministic state after power-up. The power-on function is constructed from two independent voltage monitors, the first measuring the core 1.1 V supply and a second measuring the voltage at the reference input (REFIN). Each monitor has its own comparator output that is used to decouple the analog and digital block resets as shown in Figure 39.

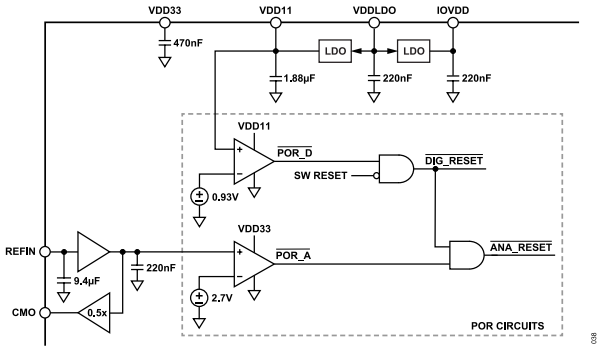

Figure 39. Simplified Diagram of POR Circuit

The core VDD (1.1 V) supply monitor compares the VDD11 supply voltage against a preset threshold of 0.93 V. If the supply voltage falls to less than this threshold, a reset signal, $\overline{\text{POR\_D}}$, asserts. The digital logic reset signal, $\overline{\text{DIG\_RESET}}$, is defined as the logical combination of the $\overline{\text{POR\_D}}$ signal and (logical AND) the compliment of the SPI software reset function. When either the $\overline{\text{POR\_D}}$ signal (VDD11 < 0.93 V) or the SW RESET signal is asserted, the internal digital circuitry is held in reset. When cleared, the contents of the configuration registers are restored to the factory default settings.

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The reference monitor compares the input voltage at the reference input pin, REFIN, against a preset threshold of 2.7 V. As illustrated in Figure 39, power for the reference monitor circuit is supplied from the VDD33 supply. For correct operation of the monitor circuit, the VDD33 supply must be applied to the AD4080 within the specified tolerance of 3.3 V ± 5% before the reference source is enabled. Assuming the device is operating within the specified supply conditions, a reference voltage less than 2.7 V results in the assertion of an internal reset signal, $\overline{\text{POR\_A}}$. The $\overline{\text{POR\_A}}$ signal and (logical AND) the $\overline{\text{DIG\_RESET}}$ signal are combined to produce a reset ($\overline{\text{ANA\_RESET}}$) for the analog circuit blocks including the ADC core, ADC timer, reference buffer, etc. If this reset signal is asserted, the analog blocks are placed in an inactive state, and the converter functionality is disabled. This event is indicated with a value of 1 in the POR_ANA_FLAG bit from the Device Status Register (Address 0x14). The state of the event detection is persistent until a Logic 1 is written to the POR_ANA_FLAG bit to clear the detection state.

POWER SUPPLY SEQUENCE

Table 10 specifies the recommended supply sequences for both internal and external generation of 1.1 V supply rails (IOVDD and VDD11). Both methods are shown in Figure 40 and Figure 41, where highlighted in blue are the supplies that must be provided to the AD4080, including the REFIN voltage. In both cases, the AD4080 requires that the supplies are applied in ascending voltage order. The design must also ensure that voltage is applied at the analog inputs (IN+ and IN−) and reference input (REFIN) concurrently with or immediately following the VDD33 supply. As described in the Power-On Reset (POR) Monitor section, the voltage at the reference input pin must only be applied once VDD33 is within the specified supply tolerance to avoid undesired behavior. Therefore, if the selected voltage reference does not provide an enable pin, it is strongly recommended to design the reference circuit to power up after VDD33.

The configuration SPI inputs, $\overline{\text{CS}}$, SCLK, and SDI, are protected with clamps to the VDD33 supply rail to allow the inputs to swing more than IOVDD. As a consequence of this architectural decision, it is necessary to drive the SPI inputs to ground or to otherwise leave the inputs floating until VDD33 is greater than IOVDD − 0.3 V. Alternatively, the VDD33 source can be connected to the device using a series power switch, like the ADP199, configured so that the switch is open when the source is less than IOVDD − 0.3 V, eliminating the parasitic current path through the digital inputs to VDD33.

Table 10. Recommended Supply Sequence

1.1 V Supplies (IOVDD and VDD11) Source	Supply Sequence
Internally Generated	**1.** VDDLDO **2.** VDD33 **3.** Digital inputs **4.** Input drive, reference
Externally Generated	**1.** IOVDD, VDD11 **2.** VDD33 **3.** Digital inputs **4.** Input drive, reference

To power down the application circuit, the power-up sequence specified in Table 10 should be reversed.

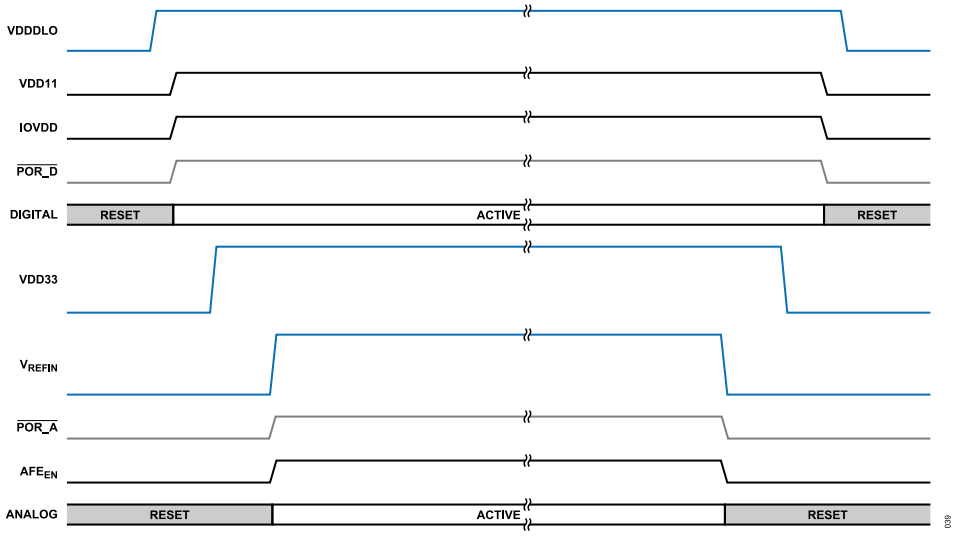

Figure 40. Power Supply Sequence, Internally Generated IOVDD, VDD11

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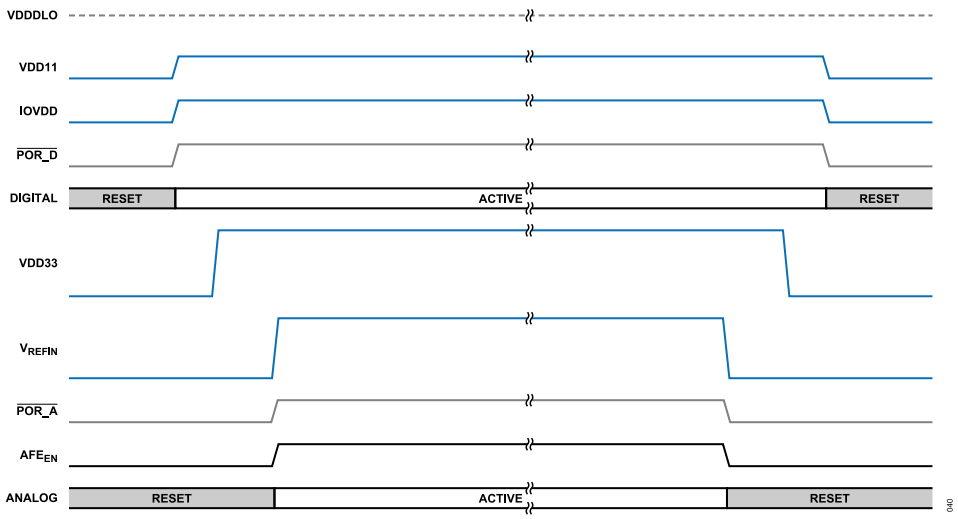

Figure 41. Power Supply Sequence, Externally Generated IOVDD, VDD11

POWER SAVING OPERATING MODES

The operating mode of AD4080 is controlled by the OPERATING_MODES bits in the Device Configuration Register (Address 0x02). On power up and after reset, the default is normal mode (OPERATING_MODES = 00). Table 11 describes all operating modes, and Figure 42 depicts the allowed transitions between these modes. Note that direct transitions between the two power saving modes (standby mode and sleep mode) are not permitted.

It is important to stop all conversion and data interface clocking before configuring the power mode.

When in either standby mode or sleep mode, the VDD33 supply can be removed to reduce power consumption. This supply must be re-established prior to issuing the SPI configuration interface command to exit either power saving mode.

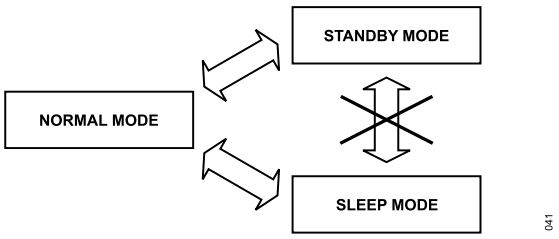

Figure 42. Operating Mode Transitions

Transitioning from normal mode to either of the two power saving modes is achieved by writing the required value to the OPERATING_MODES bits in the Device Configuration Register. Waking up (that is, transitioning back to normal mode) is achieved in a similar way because the SPI configuration interface operation is not affected by any of the power saving modes (see the SPI Configuration Interface section). Standby mode can be selected to save power, in the case where the user wants to quickly return to normal conversions. Sleep mode is a lower power state where returning to normal mode takes longer. Both standby and sleep mode can be particularly useful when used with the result FIFO (see the Result FIFO section), whereby previously stored conversion data can be accessed from the FIFO while it is still in the selected power saving mode.

To reduce power consumption in both standby and sleep mode, the internal IOVDD LDO regulator is powered down. If the user is not externally supplying IOVDD, all IOVDD domain inputs and outputs are disabled (all GPIOx and all LVDS data interface (see the LVDS Data Interface section) and SPI data interface (see the SPI Data Interface section) signals are disabled). In this specific condition, it is still possible to write to the AD4080 SPI configuration to issue a command to return to normal mode by writing to the OPERATING_MODES bits in the device configuration register (see the Device Configuration Register section) or to issue a software reset (see the Software Reset section). As GPIOx is disabled, it is not possible to perform any read activity on the SPI configuration interface bus.

When IOVDD is externally supplied, and the device is put into standby or sleep mode, the LVDS data interface is disabled; however, all GPIOx, SPI data interface, and SPI configuration interface pins remain enabled and unaffected. While power is supplied externally to IOVDD within its specified range, previously acquired data stored in the result FIFO can be access in either standby or sleep mode.

Table 11 also indicates the wake-up times associated with each of the modes. Wake-up time from sleep mode is significantly higher than that of standby mode because time must be allowed for the internal reference and common-mode buffers to re-enable and to replenish charge to the internal capacitors. When returning to normal mode, the specified wake-up time must be satisfied before applying the first conversion start pulse. This specified time is the time it takes from when the SPI command to exit the selected power saving mode is written to the device configuration register

THEORY OF OPERATION

(see the Device Configuration Register section) to update the OPERATING_MODES bits.

Table 11. Power Saving Operating Modes

Operating Mode	OPERATING_MODES Bits Value	Description	Effect	Wake-Up Time (Maximum Time to Normal Mode)
Normal	0b00	Normal operating mode	Normal operation.	Not applicable
Standby	0b01	Standby operating mode	The internal IOVDD LDO regulator is disabled. If IOVDD is not externally supplied, all GPIOx and all LVDS data interface and SPI data interface signals are disabled. For the SPI configuration interface only. writes to the device configuration register (see the Device Configuration Register section) and Interface Configuration A register (see the Interface Configuration A Register section) are allowed. If IOVDD is externally supplied, all GPIOx and SPI data interface signals are enabled. The SPI configuration interface is fully enabled. Because the SPI data interface remains enabled, the user can access data in the result FIFO (see the Result FIFO section). The ADC core is powered down. The analog circuitry remains in reset ($\overline{\text{ANA\_RESET}}$ remains asserted), and no ADC conversions can be performed. The VDD33 supply can be removed to reduce power. When in use, the internal VDD11 LDO regulator remains on. The internal reference buffer is enabled. Common-mode output buffer is enabled. The LVDS interface is disabled.	100 µs
Sleep	0b10	Low power operating mode	The internal IOVDD LDO regulator is disabled. If IOVDD is not externally supplied, all GPIOx and all LVDS data interface and SPI data interface signals are disabled. For the SPI configuration interface only, writes to the device configuration register (see the Device Configuration Register section) and Interface Configuration A register (see the Interface Configuration A Register section) are allowed. If IOVDD is externally supplied, all GPIOx and SPI data interface signals are enabled. The SPI configuration interface is fully enabled. Because the SPI data interface remains enabled, the user can access data in the result FIFO (see the Result FIFO section). The ADC core is powered down. The analog circuitry remains in reset ($\overline{\text{ANA\_RESET}}$ remains asserted), and no ADC conversions can be performed. The VDD33 supply can be removed to reduce power. The internal reference buffer is disabled When enabled, the internal VDD11 LDO regulator remains on. The common-mode output buffer is disabled. The LVDS interface is disabled. The SPI data interface remains enabled to access data in the result FIFO (see the Result FIFO section).	100 ms

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SOFTWARE RESET

This reset method must only be used once the AD4080 is in an idle state, where conversions are not being clocked, and any existing conversion is completed.

A software reset is achieved by issuing the following two writes to the Interface Configuration A register (see the Interface Configuration A Register section, Address 0x00):

1. Set SW_RESET and SW_RESETX bits to 1 by writing 0x81 to the register.
2. Then, issue another write command that sets either or both of those bits to 0.

This action returns any previously configured registers to their default settings, except for the ADDR_ASCENSION bit from the Interface Configuration A register, which keeps its previous value. The contents of the FIFO, if any, are also not affected by the software reset. The ADDR_ASCENSION bit and FIFO data only return to their default settings after a hardware reset or a full power-up happens.

APPLICATIONS INFORMATION

TYPICAL APPLICATIONS DIAGRAMS

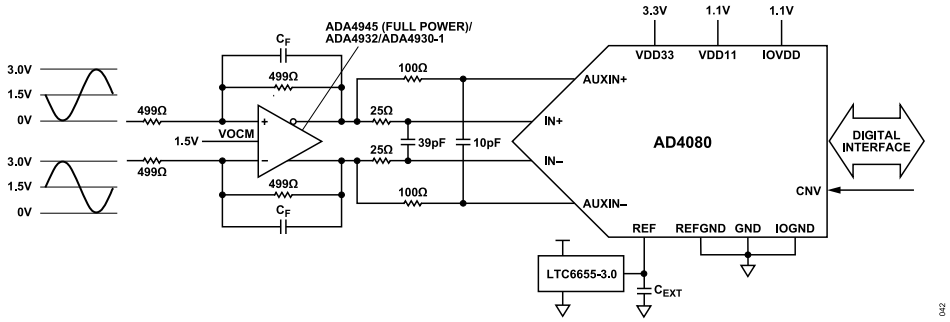

Figure 43. AD4080 Typical Applications Diagram, Fully Differential Amplifier

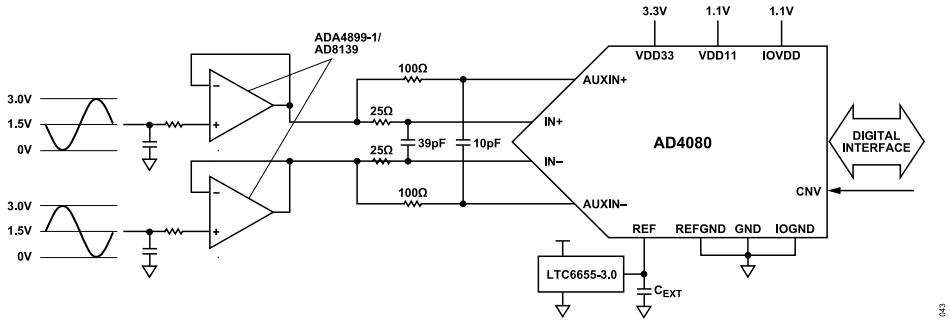

Figure 44. AD4080 Typical Applications Diagram, Single Op-Amp Drivers

APPLICATIONS INFORMATION

ANALOG FRONT END DESIGN

Driver Amplifier Choice

As described in the Easy Drive Analog Inputs section, theAD4080 has a number of unique features that opens this ADC up to being used with a wide range of driver amplifier solutions. Because the AD4080 offers exceptionally low noise, and excellent levels of precision at sampling rates up to 40 MSPS with remarkably efficient power consumption, this presents signal chain choices on which application parameters to prioritize. As is often the case, there can be some competing parameters to consider. Wider bandwidth amplifiers are required to drive faster ADCs because the settling bandwidth and signal bandwidth increase, so too does the noise bandwidth. In addition, as these speeds increase, maintaining precision in a driving amplifier becomes a greater challenge. These challenges are often met by increased power in the driver; however, Analog Devices, Inc., offers a wide choice of power efficient driver amplifiers that can be found on the Differential Amplifiers and ADC Drivers web page. Also, due to the Easy Drive features of the AD4080, where the settling bandwidth is relaxed considerably, products such as the ADA4945-1 fully differential amplifier (FDA) make an excellent low power companion product. Table 12 offers some other suggested products for consideration.

Table 12. Driver Amplifier Selection Table

Part Number	Category	Quiescent Current (I_Q)	Input Voltage Noise (V_N)	−3 dB Bandwidth (Gain = 1)	THD at 1 MHz	Application Considerations
ADA4945-1	FDA	4 mA	1.8 nV/√Hz	145 MHz	−90 dB	Lowest power
ADA4932-1	FDA	9.6 mA	3.6 nV/√Hz	560 MHz	−110 dB	Low power, wider bandwidth, improved distortion at higher signal frequencies
ADA4927-1	FDA	20 mA	1.3 nV/√Hz	2300 MHz	−112 dB	Low noise, lower distortion at higher signal frequencies
AD8139	Single op amp	24.5 mA[1]	2.25 nV/√Hz	410 MHz	−120 dB	Lowest distortion at higher signal frequencies
ADA4899-1	Single op amp	28.6 mA[1]	1.414 nV/√Hz	600 MHz	−117 dB	Lowest distortion at higher signal frequencies
ADA4930-1	FDA	35 mA	1.15 nV/√Hz	1350 MHz	−110 dB	Lowest noise

[1] Combined quiescent current of two amplifiers.

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REFERENCE CIRCUITRY DESIGN

The AD4080 requires a low noise, high precision and stability, and low temperature drift external reference of 3 V. This reference defines a differential input range for the ADC of $\pm V_{REFIN}$. The reference must be within ±5 mV of +3 V. Recommended references are LTC6655, LT6657, or ADR4530. For best performance, however, use the LTC6655 external reference. Table 13 details the typical parameters of the previously mentioned references, comparing absolute accuracy, noise, temperature drift, load regulation, and power consumption. For more detailed specifications, refer to the data sheet of the given product.

Table 13. Comparison of the Main Parameters of the LTC6655, LT6657, and ADR4530 References

Parameter	LTC6655	LT6657	ADR4530B
Accuracy	0.025%	0.1%	0.02%
Temperature Coefficient (ppm/°C)	2	1.5	2
0.1 to 10 Hz Noise (ppm p-p)	0.25	0.5	0.53
Maximum Load (mA)	±5	±10	±10
Load Regulation (ppm/mA)	3	0.7	30
Maximum Supply (V)	13.2	40	15
Shutdown	Yes	Yes	No
Supply Current, I_S (mA)	5	1.2	0.7

There is no need for the external reference capacitor because the AD4080 embeds one internally, 9.4 µF, (see Figure 45). The REFIN reference input pin is internally buffered, which substantially reduces ADC conversion transients and isolates the external reference from these transients. Therefore, no external amplifier is required to buffer the external reference. For the reference input capacitance ($C_{REF\ IN}$) and reference output capacitance ($C_{REF\ OUT}$) values, refer to the given external reference IC data sheet recommendations. As a layout recommendation, the external reference chip must be placed as close as possible to the AD4080 and its REFIN pinto minimize the series impedance of the track connecting the REFIN pin to the external reference output. It is recommended to minimize the exposure of this track to noisy signals, especially digital ones.

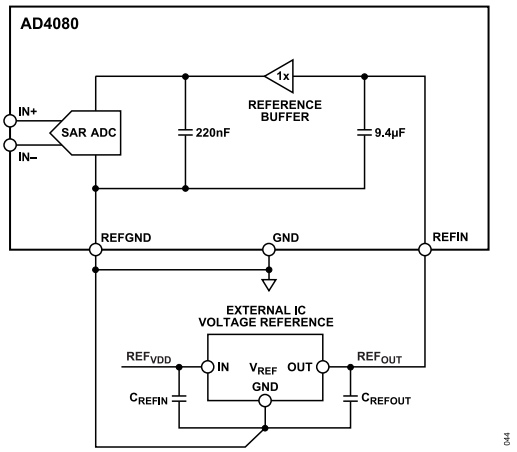

Figure 45. AD4080 General External Reference Design Functional Diagram

DATA INTERFACE CLOCKING SOLUTION

When designing the LVDS data interface (see the LVDS Data Interface section), the user must ensure the clocking solution adheres to the timing specifications of the AD4080 (see Table 2). When configured for LVDS mode data interface, the user must ensure that timing specifications stay within the maximum conversion to clock alignment time of ±535 ps (t_{CCA}). In addition, ensure that a low jitter conversion (CNV) clock is provided such that there is no unwanted impact to SNR performance. This jitter is signal frequency dependent; therefore, the level of jitter tolerable in a given system is dependent on the application use case. The Analog Devices Technical Article Maximum SNR vs Clock Jitter provides further guidance on this topic.

For example, a recommended clocking solution for where the AD4080 is configured to use the LVDS data interface with a single lane enabled and using echo clock mode. In this example, a 25 MHz oscillator is selected with low phase noise and jitter. The following MT-008 tutorial serves as an aid to convert between phase noise and RMS phase jitter, often quoted interchangeably in crystal oscillator product data sheets. The ADF4350 wideband synthesizer with an integrated voltage-controlled oscillator (VCO) serves as versatile means of generating a 400 MHz clock system clock, while maintaining low jitter and offering flexibility and control to reconfigure this frequency depending on the application needs. This clock then feeds the AD9508 clock fanout buffer with output dividers that can be configured for the desired LVDS level signaling. In the example shown in Figure 46, one output channel is set to divide by 1 to output the LVDS clock, while another output channel is configured to divide by 10 to output the AD4080 conversion clock. This 1:10 ratio of CNV:CLK frequencies ensures 20 bits of data can be read out in on the double data rate (DDR), single lane, LVDS data interface. For a dual lane configuration, such as shown in Figure 47, this ratio is adjust to 1:5.

The example shows that echo clock mode is used and aids data alignment for the host controller (in the case a field-programmable gate array (FPGA)). In self clock mode, where DCO+ and DCO−

APPLICATIONS INFORMATION

are not available for alignment, the ADC Result Latency and LVDS Interface Alignment section describes how the INTF_CHK_EN bit (Address 0x15, Bit 4) can be enabled to help align the host controller to data and to mitigate against any system propagation delays.

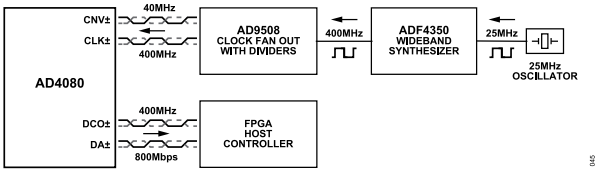

Figure 46. Single Lane, LVDS Data Interface Clocking Example

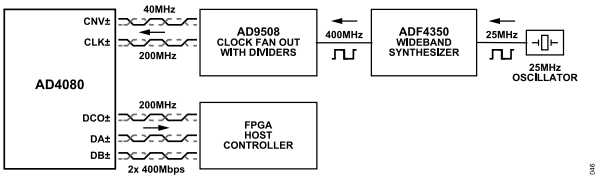

Figure 47. Dual Lane, LVDS Data Interface Clocking Example

In cases where the SPI data interface (see the SPI Data Interface section) is used to access conversion results from the result FIFO (see the Result FIFO section) again, it is important that the CNV source jitter is carefully considered to achieve the required performance. In the case shown in the SPI data interface clocking example (see Figure 48) , an oscillator directly provides the conversion clock, and the data is asynchronously clocked from the FIFO by a microcontroller unit (MCU). Optionally, as shown in Figure 48, the general-purpose input and output pins can be configured to control the result FIFO operation (see the GPIO Pins section and the Result FIFO section).

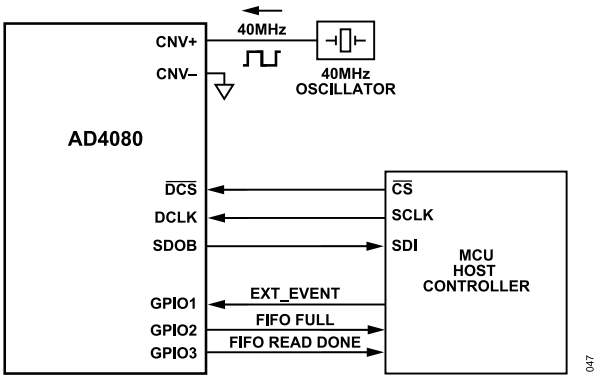

Figure 48. SPI Data Interface Clocking Example

POWER SOLUTION

With such low noise and up to a 40 MHz sampling rate, it is important that careful consideration is taken for the power solution of applications to ensure that the low noise supplies provided to the AD4080 do not become a source of performance or accuracy degradation. To aid ease of use and to help reduce external required components, two internal LDO regulators are integrated within the AD4080. Further details on these regulators can be found in the Internally Regulated Supply Configuration section. Also, note that the internal supply decoupling capacitors are included for all supply rails, whether generated internally or externally, reducing external component count, simplifying use, and offering huge benefits to PCB layout, routing, and design density.

For externally generated supply rails, excellent choice LDO regulators are the LT3045 or ADP150, which both offer ultra-low noise and excellent power supply rejection. For high efficiency, step-down switching regulators, the LT8604C is a good choice; however, great care must be taken in the design of the switching regulator circuity because switching frequencies are likely to be within the application signal bandwidth, and although the AD4080 has high AC power supply rejection on its supplies, appropriate consideration must be given to the supply rails.

DIGITAL INTERFACE

OVERVIEW

The AD4080 digital interface consists of a 4-wire SPI for device configuration, four general-purpose input and output (GPIO) pins, a conversion data access interface with selectable output format (LVDS or SPI data interface), and a conversion start input (CNV+ and CNV−) that can be configures for LVDS or CMOS level signaling.

Register Interface

The AD4080 configuration registers are accessed through the SPI configuration interface (see the SPI Configuration Interface section).

ADC Conversion Control

The ADC acquires a sample and initiates a conversion operation on the rising edge of the convert start signal, applied at the CNV+ and CNV− pins. There are two possible configurations for the electrical signaling at the convert start input pins: CMOS or LVDS.

CMOS is the default mode on power up and after reset. CMOS requires that the CNV− pin be tied to the digital interface ground (IOGND). In this mode, the convert signal must be a CMOS logic signal referenced to IOGND and applied at CNV+, with logic levels according to the digital inputs (CNV, GPIOx, $\overline{DCS}$, and DCLK) parameters in Table 1.

To switch to LVDS mode, the LVDS_CNV_EN bit of the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section, Address 0x16) must be set to 1. In this mode, an external 100 Ω termination resistor must be installed between the CNV+ and CNV− pins, as close to the AD4080 as possible. In LVDS mode, the CNV+ and CNV− pins must be driven differentially with an LVDS driver conforming to the levels specified in the LVDS I/O (EIA-644) parameters in Table 1. Care must be taken to closely match the CNV+ and CNV− differential signal pair routing and to use controlled impedance to ensure signal integrity.

ADC Conversion Data Interface

Two signaling format options are available to access conversion results:

- LVDS level signaling (LVDS data Interface)
- CMOS level signaling (SPI data interface)

The choice of interface is usually determined by the requirements and constraints of the application at hand. For example, if continuous fast data acquisition is required, then the LVDS signaling interface is typically the preferred option. If the application requires only noncontinuous bursts of data acquisitions, then either the LVDS or the SPI data interfaces can be used. The capabilities of the digital interface host can also determine which interface option is chosen.

Common to both the LVDS and SPI data interfaces are the following flexible features, which reduce the burden on the chosen digital host:

- Multilane data transfer: enables sustained data throughput at reduced interface clock speeds.
- Test pattern generation: facilitates interface integrity checks.

Additionally, for the LVDS only, there is the option to set a configurable output drive.

By default, the LVDS interface is selected on power up and after a reset. As can be seen in Figure 49, for LVDS, the data path of the ADC results is routed though the offset and gain correction block where there is the option to:

- Continuously read, directly, the raw ADC conversion results.
- Continuously read the ADC results processed by a user-selected digital filter (see the Digital Filter section for details).
- Read up to 16k unfiltered results from the FIFO.
- Read up to 16k digitally filtered results from the FIFO.

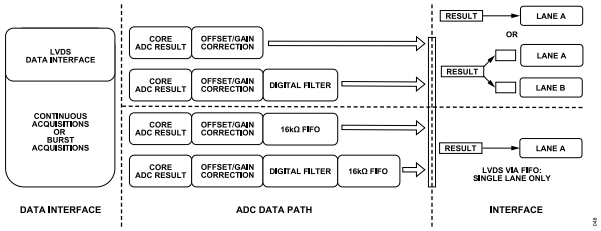

Figure 49. LVDS Data Interface Options

If configured for the SPI data interface, as can be seen in Figure 50, the available data paths are as follows:

- Read up to 16k unfiltered results from the FIFO.
- Read up to 16k digitally filtered results from the FIFO.

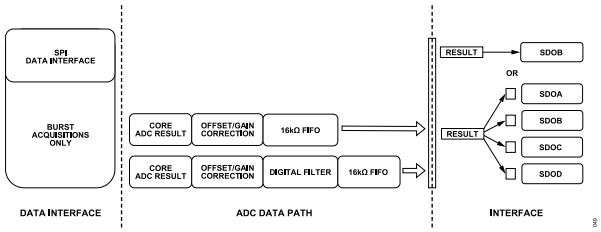

Figure 50. SPI Data Interface Data Path Options

Additional features specific to the selected interface format are also available and are described in the LVDS Data Interface section and the SPI Data Interface section.

SPI CONFIGURATION INTERFACE

All serial transactions between the system host and the AD4080 configuration registers are executed using the configuration SPI. Each serial transaction consists of at least one instruction phase during which the desired memory operation, that is, read or write,

DIGITAL INTERFACE

and the starting address for the transaction are transmitted to the AD4080. The instruction phase is immediately followed by a data transaction phase during which one or more bytes of information is exchanged between the host and the AD4080. This content is framed by a continuous assertion of the interface chip select ($\overline{CS}$) as illustrated in the generic timing presented in Figure 51 and Figure 52.

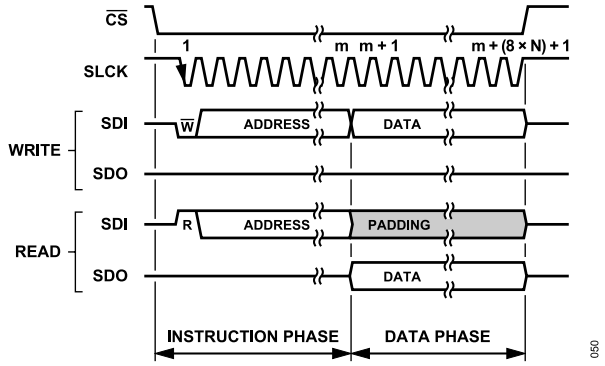

Figure 51. Generic SPI Configuration Frame, CRC Disabled

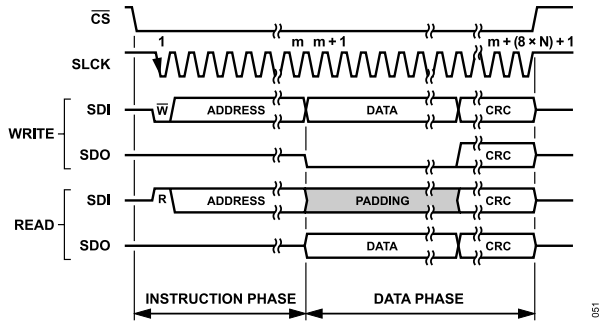

Figure 52. Generic SPI Configuration Write Operation, CRC Enabled

SPI Register Interface

The configuration register interface is an SPI that enables both device configuration and system status monitoring. This interface is configured for 4-wire, full-duplex operation. Dedicated interface pins for the interface chip select ($\overline{CS}$), serial clock (SCLK), and serial data input (SDI) are intended for direct connection to the host controller. By default, at power-up or after a software reset, the configuration interface SDO function is enabled and assigned to the GPIO0 pin.

The configuration interface timing convention implemented in this design is consistent with SPI Mode 3, clock polarity (CPOL) = 1, clock phrase (CPHA) = 1. As such, the serial clock (SCLK) is expected to idle high and the state of the data pins, SDI and SDO, are updated on the falling (leading) edge of the clock such that these pin can be sampled on the subsequent rising (trailing) edge. See the ADI Analog Dialogue, Introduction to SPI Interface article for more details regarding the SPI and SPI modes.

The memory access controller associated with this interface supports a number of user-programmable options accessible through the interface configuration memory space (Address 0x00 to Address 0x11). The available options for the AD4080 are listed and described in Table 14.

Table 14. Configuration Memory Controller Options Summary

Interface Option	Description
Software Reset (SW_RESET, SW_RESETX)	Resets the internal configuration memory to the default state (except for ADDR_ASCENSION bit). Data FIFO is unaffected. Only use this reset method once the ADC is in an idle state, where conversions are not clocked, and any existing conversion is completed. See the Software Reset section for details.
Address Ascension (ADDR_ASCENSION)	Selecting this option changes the behavior of the memory controller address counter from decrementing (default) to incrementing. This change affects multibyte transfers, for example, when accessing a multibyte register as a single entity or when streaming mode is enabled. The selection impacts the starting address for multibyte register accesses in strict register access mode. See the Address Ascension Selection section for details.
Short Instruction (SHORT_INSTRUCTION)	Selecting this option reduces the length of the address field in the instruction word from 15 bits to 7 bits.
Single Instruction (SINGLE_INST)	Selecting this option changes from the default streaming mode to single instruction mode, which requires the host controller to transmit an instruction for each register access within a given SPI frame. The size of an entity is dependent on the strict register access setting and whether or not the register is multibyte. This feature allows random access to the memory space during configuration. See the Instruction Mode Selection section for details.
Strict Register Access (STRICT_REGISTER_ACCESS)	Selecting this option instructs the memory controller to treat a multibyte register as a single entity, generating a fault when a partial access is attempted. See the Strict Access Selection and Multibyte Registers section for details.
CRC Enable (CRC_ENABLE, CRC_ENABLEB)	Selecting this option enables a cyclic redundancy check (CRC) to verify the integrity of data sent to and received from the host. See the Configuration Cyclical Redundancy Check (CRC) section for details.
Status Data Transmission (SEND_STATUS)	Selecting this options enables the transmission of status data through the SDO line during the instruction phase of the data frame. See th eStatus Data Transmission section for details.

DIGITAL INTERFACE

Table 14. Configuration Memory Controller Options Summary (Continued)

Interface Option	Description
Loop Count (LOOP_COUNT)	Sets the data byte count before looping to the start address. When streaming data, a nonzero value sets the number of data bytes written before the address loops back to the start address. A maximum of 255 bytes can be written using this approach. A value of 0x00 disables the loop back so that addressing wraps around at the upper and lower limits of the memory. After writing this register, the loop value applies only to the following SPI instruction and auto clears upon the end of that instruction.

Instruction Phase

An instruction phase immediately follows the assertion of the $\overline{CS}$ pin (Logic 0) and is terminated by transmission of a complete instruction packet or deassertion of $\overline{CS}$. The instruction packet starts with a single command bit indicating the operation type (Logic 1 for read, and Logic 0 for write), which is then followed by the start address for the operation. By default, the address is 15-bit long, but the data interface has an optional short instruction mode, in which, it is reduced to 7 bits. The short instruction mode is enabled by setting the SHORT_INSTRUCTION bit = 1 in the Interface Configuration B register (see the Interface Configuration B Register section, Address 0x01).

Data Phase

Each instruction phase is immediately followed by an associated data phase, during which data is either shifted out of the serial data output (SDO) on the falling edge of SCLK (read access) or is shifted into the device configuration memory through SDI on the rising edge of SCLK (write access). The minimum size of the data payload is defined as a single byte; however, it can include multiple bytes depending on the depth of the register addressed and the interface configuration settings for the SINGLE_INST and STRICT_REGISTER_ACCESS bits (Register 0x01, Bit 7, and Register 0x10, Bit 5, respectively.

Write Access

When $\overline{CS}$ is forced low, a new serial instruction phase begins. The first bit sent in the instruction phase is the command bit, and when it is forced low (Logic 0) this indicates a write operation. The command bit is followed by an address that, for the write operation, indicates where the information received in the subsequent data phase will be stored. As previously described in the Instruction Phase section, the address has a default length of 15 bits, but the address can be optionally shortened to 7 bits.

Following the instruction phase, an integer number of bytes containing the data payload for one or more registers in the configuration memory are transmitted to the AD4080. The size of the payload in this data phase is bounded by the selected SINGLE_INST and STRICT_REGISTER_ACCESS interface options as described in the Strict Access Selection and Multibyte Registers section. Each data byte is loaded into the addressed register as it is received, assuming the interface CRC is disabled. If the CRC is enabled, however, the addressed data register is only loaded if the internally computed checksum matches the CRC value received from the host. In the event that the computed CRC and received checksum from the host for a given entity are inconsistent, the register update terminates and all subsequent data in the given frame is treated as invalid as well. The checksum computation for the interface CRC function is described in detail in the Configuration Cyclical Redundancy Check (CRC) section.

Note that, during the data phase of a write operation, the SDO output is driven to Logic 0 when the product is not reporting the latest CRC checksum to ensure a valid data state is presented to the host controllers SDI pin.

Read Access

The SPI enables read access to the configuration registers to validate previous configuration writes, read the device identification, or verify the interface status.

When $\overline{CS}$ is forced low, a new serial instruction phase begins. The first bit sent in the instruction phase is the command bit, and when it is forced high (Logic 1) this indicates a read operation. The command bit is followed by an address that, for the read operation, indicates the start address for the register space to be accessed. As previously described in the Instruction Phase section, the address has a default length of 15 bits, but the address can be optionally shortened to 7 bits.

During the subsequent data phase, content from the addressed register space is shifted out, MSB first, on the SDO line on the falling edge of SCLK. The number of bytes transmitted in any one data frame is determined by the interface configuration setting selections for the SHORT_INSTRUCTION and STRICT_REGISTER_ACCESS options as demonstrated in the examples shown in the Instruction Mode Selection section and the Strict Access Selection and Multibyte Registers section.

Instruction Mode Selection

The configuration interface memory controller defaults to streaming mode upon power up (SINGLE_INST = 0). In streaming mode, multiple, contiguous registers are accessed in a single SPI frame, starting at the address specified in the instruction phase. In streaming mode, only one instruction phase is permitted per SPI frame, requiring a new SPI frame be initiated for changing access commands or otherwise access a noncontiguous address in the register space. For each byte transferred during the subsequent data phase, the internal address counter is automatically updated according to the setting of the ADDR_ASCENSION bit in the Interface Configuration A register (see the Interface Configuration A Register section), in the way specified by Table 15.

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Table 15. Address Ascension Selection

ADDR_ASCENSION Bit Value	Address Controller Behavior (STRICT_REGISTER_ACCESS = 1)
0 (Default)	Decrement Address. Multibyte registers are accessed by addressing the most significant byte address.
1	Increment Address. Multibyte registers are accessed by addressing the least significant byte address

Figure 53 illustrates the generic SPI frame formatting for a serial transaction using the default interface configuration. In this example, a portion of the configuration register space consisting of a byte-wide register and a multibyte register is accessed. The address for the byte-wide register resides in the most significant address (ADDRESS) and the most significant byte of the multibyte register resides in the least significant address of the register segment. By default, the ADDR_ASCENSION property is set to descending, indicating that the address for the most significant register is passed to the host controller during the instruction phase. Depending on the selected operation, the instruction word is followed by either a payload consisting of data for the byte-wide register (DATA), least significant (LSBYTE), and most significant bytes (MSBYTE) of the multibyte register, or, in the case of a read access, padding bits. As a convention, it is recommended to pass Logic 1 to SDI during a read access to avoid accidentally addressing address zero for write access.

In single instruction mode (SINGLE_INST = 1), the memory access controller requires an instruction phase to transmit for each register accessed in a given SPI frame as illustrated in Figure 54. This mode is useful when access to nonadjacent sections of the register space is required in a given SPI frame. Note that, the same access flexibility can be achieved in stream mode by initiating a new SPI frame for each unique register access.

The single instruction mode is selected by setting SINGLE_INST = 1 in the Interface Configuration B register (see the Interface Configuration B Register section, Address 0x01).

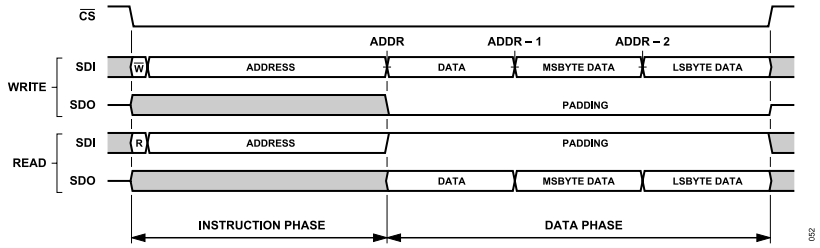

Figure 53. Interface Access Example, Default Interface Configuration, Streaming Mode (ADDR_ASCENSION = 0)

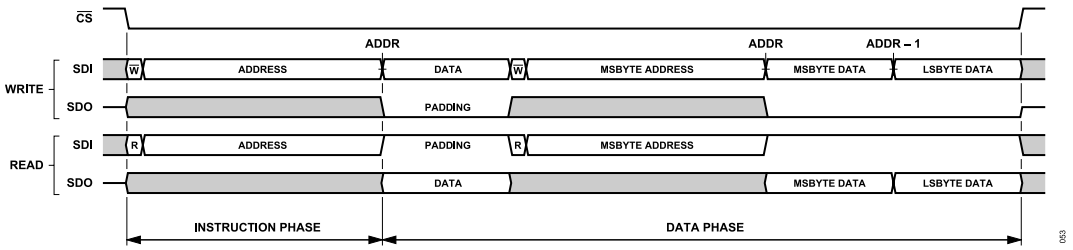

Figure 54. Interface Access Example, Single Instruction Mode (SINGLE_INST = 1), All Other Interface Options Default

DIGITAL INTERFACE

Address Ascension Selection

The address ascension selection (ADDR_ASCENSION) bit, as described in previous sections, determines how the internal interface address pointer is updated for each byte of data transmitted to the AD4080 in streaming mode (SINGLE_INST = 0). If using single instruction mode (SINGLE_INST = 1), each register is directly addressed through its own instruction phase as illustrated in Figure 54, and thus, the address pointer is not updated. Regardless of the setting for SINGLE_INST, the ADDR_ASCENSION bit directly impacts the formatting of the SPI frame in terms of selection of the instruction phase starting address and byte order of the data phase payload. This impact is described in greater detail in the Strict Access Selection and Multibyte Registers section as much of the data formatting is dependent on this interface configuration selection. The ADDR_ASCENSION selection bit is located in the Interface Configuration A register (see the Interface Configuration A Register section, Address 0x00).

As summarized in Table 15, the ADDR_ASCENSION bit is cleared by default, resulting in the address pointer decrementing by one for each data byte transmitted. In this decrement configuration (ADDR_ASCENSION = 0), the address pointer decrements from the starting address indicated in the instruction phase by one for each data phase byte received until the counter reaches Address 0x0000. If additional bytes are received, the pointer automatically rolls over to the maximum address value, 0x7FFF; the rollover behavior is fixed, and therefore, independent of the SHORT_INSTRUCTION value or the physical address space occupied by the user configurable registers. It is important to understand this behavior to avoid generating interface errors associated with attempting to access one or more invalid register addresses. Limit register access to the register address space associated with the device configuration as described in the Configuration Registers section.

Alternatively, the ADDR_ASCENSION bit can be set (ADDR_ASCENSION = 1), resulting in the address pointer incrementing by one, starting at the address identified in the instruction word, for each data phase byte received at the AD4080 in a given SPI frame. In a manner similar to the descending case, the address counter continues to increment for each data byte received until the maximum address value, 0x7FFF, is reached, after which the pointer rolls over to 0x0000.

Strict Access Selection and Multibyte Registers

Several locations in the AD4080 configuration memory have been assigned as multibyte registers to support the storage requirements. For example, the offset correct register (see the Offset Correction Register section, Address 0x25) and gain correction register (see the Gain Correction Register section, Address 0x27) are multibyte registers because the resolution of the correction coefficients they contain exceeds a single byte. For a complete listing of multibyte registers, refer to the Configuration Registers section. The length of each register, in bytes, is captured in Table 31 in addition to other characteristic information.

The function of the STRICT_REGISTER_ACCESS bit is to indicate to the interface controller that all bytes of a multibyte register must be accessed in the current frame for valid communication to have occurred. In the event a multibyte register is only partially accessed, an interface fault is generated in the Interface Status A register (see the Interface Status A Register section, Address 0x11), and the partial content update is discarded. The intent of this restriction is to ensure that corresponding configuration quantities are updated in a manner that produces the desired device operation. The access restriction function is enabled by default (STRICT_REGISTER_ACCESS = 1) and can be disabled by clearing the access bit (STRICT_REGISTER_ACCESS = 0) in the Interface Configuration C register (see the Interface Configuration C Register section, Address 0x10). With register access restriction disabled, each byte of the configuration memory can be independently addressed; however, it is then incumbent on the software to correctly configure any multibyte registers in the device memory to achieve the desired behavior.

The decision to enable or disable the register access restriction has implications with regards to the correct construction of the SPI frames containing one or more multibyte register accesses. When STRICT_REGISTER_ACCESS is disabled, each byte of a multibyte register is treated as a singular element. Furthermore, the interface does not indicate a fault if all bytes of the register are not programmed, or if the bytes are programmed in a random order, and therefore, it is incumbent on the host to ensure that the content of those registers are updated in a manner that produces the desired function in the device.

When STRICT_REGISTER_ACCESS is enabled, specific access rules are enforced to ensure consistency between the data and the expected behavior of the device. To understand how these rules apply to multibyte registers in the configuration memory, it is important to understand how the memory is organized. By convention, multibyte registers are arranged in the configuration memory such that the most significant byte of the register is stored in the most significant address of the assigned register space as illustrated in Figure 55. As a result, the byte order of the register content transmitted in the data phase is dependent on the ADDR_ASCENSION selection.

DIGITAL INTERFACE

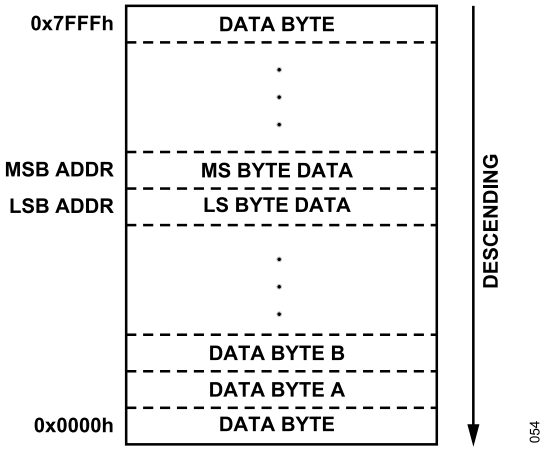

Figure 55. Generic Byte Wide Memory, Multibyte Register Example

As indicated in Figure 56, the address counter, by default, automatically decrements (ADDR_ASCENSION = 0) such that the most significant byte of the multibyte register is accessed first, followed by the remaining byte(s) in that register in ascending order. Conversely, if ADDR_ASCENSION = 1, the least significant byte of the multibyte register is accessed first followed by most significant byte.

As an extension of this concept, when STRICT_REGISTER_ACCESS = 1, any SPI frame that accesses a multibyte register as the first entity in the data transfer must correctly set the starting address in the instruction word to correspond to the ADDR_ASCENSION selection. In the case that the address counter automatically decrements (ADDR_ASCENSION = 0), the starting address is assigned to the register address for the least significant byte of that multibyte register, and conversely, if configured to increment automatically, the starting address must be set to the register address for the most significant byte. As a result of the change to ADDR_ASCENSION from automatic address decrement (0) to automatic increment (1), Figure 53 and Figure 54 will change as illustrated in Figure 56 and Figure 57 to accommodate the changes in data phase byte order and instruction phase multibyte register start address.

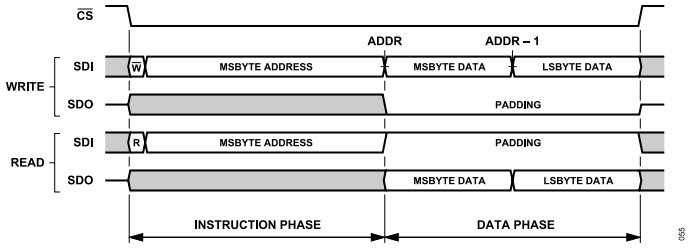

Figure 56. Single Instruction Format, ADDR_ASCENSION = 0 (Descend), STRICT_REGISTER_ACCESS = 1 (Enabled)

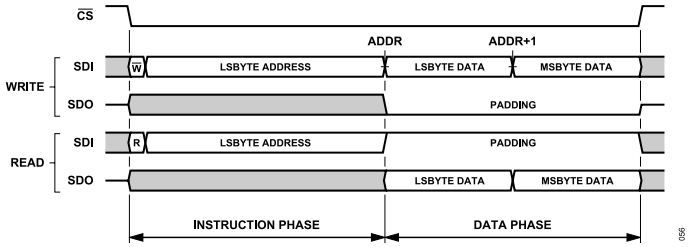

Figure 57. Single Instruction Format, ADDR_ASCENSION = 1 (Increment), STRICT_REGISTER_ACCESS = 1 (Enabled)

DIGITAL INTERFACE

Status Data Transmission

The Interface Status A register (see the Interface Status A Register section, Address 0x11) and device status register (see the Device Status Register section, Address 0x14) contain status data pertaining to the communications interface and the device itself, respectively. This data enables troubleshooting of device configuration during development and also provides continuous coverage of potential communication issues between the host and the interface once deployed. The SPI controller can access the data through regular register read operations. However, the AD4080 can be configured to autonomously transmit status data through the SDO line every time while the SPI controller is sending the SPI instruction phase data over the SDI. This feature is controlled through the SEND_STATUS bit in the Interface Configuration C register (see the Interface Configuration C Register section, Address 0x10), and it is disabled by default. To enable this bit, set SEND_STATUS = 1. The status data that is sent is taken from the Interface Status A register and from the device status register, but the content is different depending on the setting of the SHORT_INSTRUCTION bit in the Interface Configuration B register (see the Interface Configuration B Register section. (Note that the length of the instruction phase also depends on this setting). See Table 16 and Table 17 for a description of the status data sent in each case, where the status data is sent MSB first.

Table 16. Device Status Data Sent Through the SDO in Long Instruction Mode (SHORT_INSTRUCTION = 0)

Bit	Name	Description
15	Not applicable	Bit 15 is always 0.
14	Not applicable	Bit 14 is always 0.
13	FIFO_FULL	Device Status Register Bit 7: FIFO Full Status Flag. 0: FIFO Not Full. 1: FIFO Full.
12	FIFO_READ_DONE	Device Status Register Bit 6: FIFO Read Done Flag. 0: FIFO Read Not Done. 1: FIFO Read Done.
11	HI_STATUS	Device Status Register Bit 5: High Threshold Detection Status Flag. 0: High Threshold Event Not Detected. 1: High Threshold Event Detected.
10	LO_STATUS	Device Status Register Bit 4: Low Threshold Detection Status Flag. 0: Low Threshold Event Not Detected. 1: Low Threshold Event Detected.
9	ADC_CNV_ERR	Device Status Register Bit 2: ADC Conversion Error Flag. 0: ADC Conversion OK. 1: ADC Conversion Error. A. Conversion period is lower than minimum value for speed grade. B. DSP error.
8	ROM_CRC_ERR	Device Status Register Bit 1: Read Only Memory (ROM) CRC and/or Error Correction Code (ECC) Failure Flag. 0: ROM CRC Check OK. 1: ROM CRC and/or ECC Failure.
7	POR_ANA_FLAG	Device Status Register Bit 3: POR Analog Status. Allows user to detect when an analog POR event has occurred. An analog POR is triggered at power-up or when the logic supply drops to less than some threshold value, when the ADC reference drops to less than some threshold value, or when the user issues a software reset. 0: Analog POR Flag Cleared. 1: Analog POR Event Detected.
6	POR_FLAG	Device Status Register Bit 0: POR Status. Allows user to detect when a POR event has occurred. A POR is triggered at power-up or when the logic supply drops to less than some threshold value or when the user issues a software reset. 0: POR Flag Cleared. 1: POR Event Detected.
5	NOT_READY_ERR	Interface Status A Register Bit 7: Device Not Ready for Transaction. This bit is set if the user attempts to execute an SPI transaction before the completion of digital initialization.
4	CLOCK_COUNT_ERR	Interface Status A Register Bit 4: Clock Count Error. This bit is set when an incorrect number of clocks is detected in a transaction.

DIGITAL INTERFACE

Table 16. Device Status Data Sent Through the SDO in Long Instruction Mode (SHORT_INSTRUCTION = 0) (Continued)

Bit	Name	Description
3	CRC_ERR	Interface Status A Register Bit 3: CRC Error. This bit is set when the SPI controller does not send a CRC value or when the CRC value calculated by the device does not match the value received from the SPI controller.
2	WR_TO_RD_ONLY_REG_ERR	Interface Status A Register Bit 2: Write to Read Only Register Error. Write to Read Only Register Attempted. This bit is set when the user attempts a write to a register that is read-only.
1	REGISTER_PARTIAL_ ACCESS_ERR	Interface Status A Register Bit 1: Register Partial Access Error. This bit is set when a fewer than expected number of bytes are read from or written to in a multibyte register access. This bit is only valid when strict register access is enabled.
0	ADDRESS_INVALID_ERR	Interface Status A Register Bit 0: Invalid Address Error. Attempt to read or write nonexistent register address. This bit is set when the user tries to access register addresses outside the allowed memory map space.

Table 17. Device Status Data Sent Through the SDO in Short Instruction Mode (SHORT_INSTRUCTION = 1)

Bit	Name	Description
7	Not applicable	Bit 7 is always 0.
6	POR_FLAG	Device Status Register Bit 0: POR Status. Allows user to detect when a POR event has occurred. A POR is triggered at power-up or when the logic supply drops to less than some threshold value or when the user issues a software reset. 0: POR Flag Cleared. 1: POR Event Detected.
5	NOT_READY_ERR	Interface Status A Register Bit 7: Device Not Ready For Transaction Error. This bit is set if the user attempts to execute an SPI transaction before the completion of digital initialization.
4	CLOCK_COUNT_ERR	Interface Status A Register Bit 4: Clock Count Error. This bit is set when an incorrect number of clocks is detected in a transaction.
3	CRC_ERR	Interface Status A Register Bit 3: CRC Error. This bit is set when the SPI controller does not send a CRC, or when the CRC value calculated by the device does not match the value sent by the SPI controller.
2	WR_TO_RD_ONLY_REG_ERR	Interface Status A Register Bit 2: Write To Read-only Register Error. This bit is set when the user attempts a write to a register that is read only.
1	REGISTER_PARTIAL_ ACCESS_ERR	Interface Status A Register Bit 1: Register Partial Access Error. This bit is set when a fewer than expected number of bytes are read from or written to in a multibyte register access. This bit is only valid when strict register access is enabled.
0	ADDRESS_INVALID_ERR	Interface Status A Register Bit 0: Invalid Address Error. This bit is set when the user tries to read from or write to a register address outside the allowed memory map space.

Configuration Cyclical Redundancy Check (CRC)

The AD4080 includes optional configuration error detection based on an 8-bit cyclical redundancy check algorithm. When enabled, an 8-bit checksum is inserted into the serial data output stream (SDO) during the data phase after each complete register transaction. Depending on the register access type,that is, read or write, the host is expected to conditionally provide a corresponding checksum to the SDI immediately following each register access. The interface controller uses the host supplied checksum to determine if a CRC error has occurred.

A mismatch in the checksum values computed by the host and the AD4080 interface results in setting the CRC_ERR flag (CRC_ERR = 1) in the Interface Status A register (see the Interface Status A Register section, Address 0x11). During a write access, a CRC error invalidates the most recent register data as well as any subsequent register data writes if in streaming mode (SINGLE_INST = 0), which prevents loading any potentially corrupted data into the configuration memory. In response to a CRC event, the host controller is required to initiate a new SPI frame to retry configuration of the effected memory locations. In the event the CRC_ERR is detected during a data read, the host controller must discard the received data and retry the data read in a new SPI frame. Clear the CRC_ERR flag before any attempt to initiate a repeated read or write to the configuration memory to allow detection of any subsequent errors. The error flag is cleared by writing code 0x08 to the Interface Status A register to set the CRC_ERR bit to a Logic 1. It is recommended that an immediate read of the Interface Status A register follows any attempt to clear the fault to validate the attempt was successful.

The configuration CRC function is disabled by default and can be enabled through two complementary bit fields, CRC_ENABLE and CRC_ENABLEB, in the Interface Configuration C register (see the Interface Configuration C Register section, Address 0x10). To enable the CRC function, set the CRC_ENABLE bits to 1 and the CRC_ENABLEB bits to 10. Each of the complementary CRC bit fields is 2-bit wide, and any combination other than that specified results in the function remaining disabled. It is important to note that once the CRC function is enabled, a valid checksum from

DIGITAL INTERFACE

the host controller is required for all subsequent serial transactions according to the conditions described in Table 18. If used, enable and validate the CRC function before writing to any of the device configuration registers. To validate the CRC function is enabled, follow the CRC configuration write with a SPI frame consisting of a read of both the Interface Configuration C register and the Interface Status A register using a valid checksum for the read transaction. If enabled, the register contents for the CRC_ENABLE and CRC_ENABLEB bits must be 1 and 10, respectively, and the CRC_ERR bit in the Interface Status A register remains cleared (Logic 0). Once confirmed, proceed with programming the remaining configuration registers.

Table 18. Host Controller (SDI) Conditional Checksum Requirement Summary

Command	SINGLE_INST Bit Value	Check Sum Requirement
Write	Streaming (0) or single instruction (1)	After each data register payload
Read	Streaming (0)	After the first register data payload following the instruction phase
	Single instruction (1)	After each data register payload

The following CRC-8 polynomial is implemented in the AD4080 to compute the checksum for each register transaction:

$x^8 + x^2 + x + 1$

Each serial transaction is processed through this polynomial to generate the checksum on a per register basis. The data and seed values used for each checksum calculation are a function of the access command (read/write); ADDR_ASCENSION, STRICT_REGISTER_ACCESS, and SINGLE_INST settings; and the location of the register data in the data stream as summarized in Table 19.

All register write access operations, regardless of SINGLE_INST setting, require a valid CRC checksum to be sent from the host following the data payload for each register. For multibyte registers, if STRICT_REGISTER_ACCESS = 1, a valid CRC is appended to the data stream after all bytes of the addressed register are sent. If STRICT_REGISTER_ACCESS is cleared (0), each byte transmitted must be followed by a valid checksum using the computation rules that are described as follows.

For read access, the computation and transmission of a valid checksum from the host is required to validate the command and starting address only. In streaming mode (SINGLE_INST = 0), a CRC checksum is sent from the host controller after the first register data payload only. Fill all subsequent register accesses in streaming mode with padding data. The AD4080 continues to produce valid checksum values after each register read to allow validation in the host using the preceding data. As a new instruction phase is required for each register accessed in single instruction mode, a valid host CRC checksum is required for each register accessed.

In single instruction mode (SINGLE_INST = 1), the polynomial is computed for each register using the default seed value of 0xA5, the instruction phase data, and depending on the access command, the desired register or padding data. In streaming mode (SINGLE_INST = 0), the checksum computation for the first register in the data stream is computed as if single instruction mode were selected. Each subsequent register access checksum computation is seeded with the starting address for the current register and the corresponding data. Note that the starting address for multibyte registers changes with the ADDR_ASCENSION selection, assuming the register access restriction is enabled (STRICT_REGISTER_ACCESS = 1). As previously described, the memory convention dictates that if ADDR_ASCENSION is set to 0, the address for the least significant byte of the multibyte register serves as the starting address. Conversely, if the ADDR_ASCENSION bit is set to 1, the address of the most significant byte of the multibyte register is used.

Table 19. Configuration CRC Checksum Source Data Summary vs. SINGLE_INST and SPI Command

		Single Instruction Mode (SINGLE_INST = 1) or Streaming Mode First CRC		Streaming Mode (SINGLE_INST = 0) after first CRC	
Command	Checksum Source	Data Source	Seed	Data Source	Seed
Write	Controller	Instruction and data	0xA5	Register data	Current start address
	AD4080	Instruction and data		Register data	Current start address
Read	Controller	Instruction and padding data	0xA5	Not required, send padding data	
	AD4080	Instruction and register content		Register data	Current start address

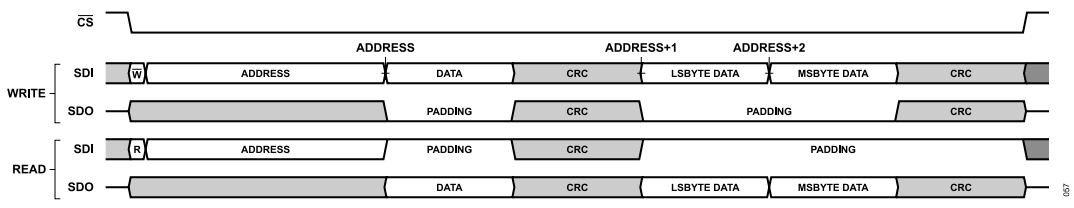

Figure 58. Streaming Mode Configuration with CRC Enabled, ADDR_ASCENSION = 1

DIGITAL INTERFACE

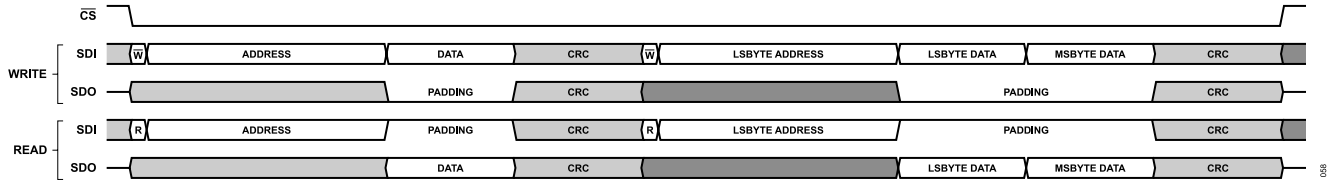

Figure 59. Single Instruction Mode Configuration with CRC Enabled, ADDR_ASCENSION = 1

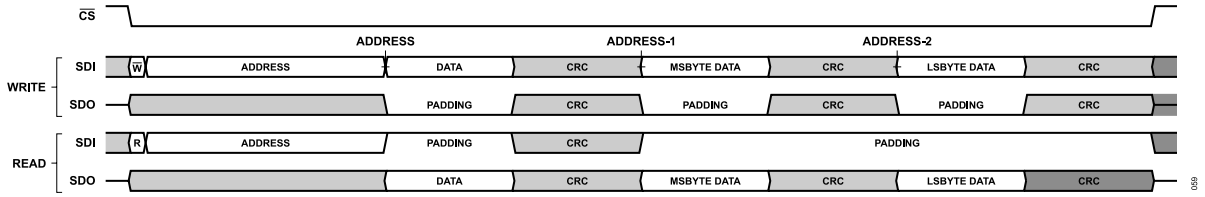

Figure 60. Streaming Mode Configuration with CRC Enabled, STRICT_REGISTER_ACCESS = 0 (Disabled) , ADDR_ASCENSION = 0

Configuration SPI Frame

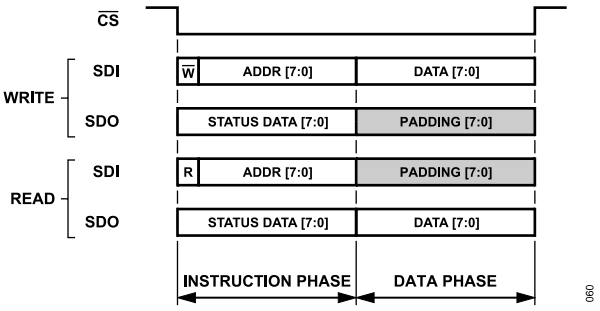

Figure 61. Short Instruction Mode, Data Status Enabled, CRC not Enabled

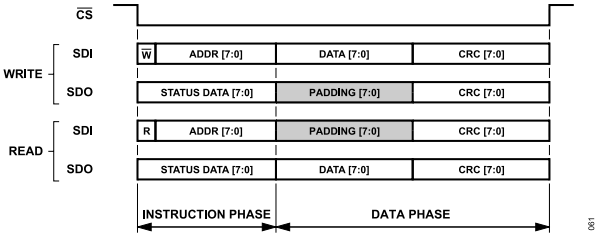

Figure 62. Short Instruction Mode, Data Status Enabled, CRC Enabled

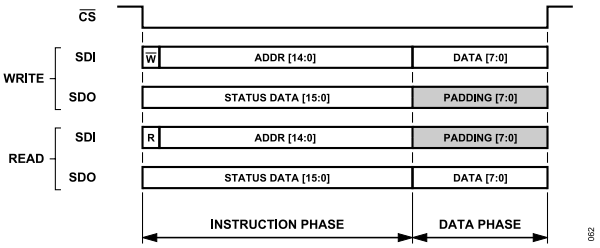

Figure 63. Long Instruction Mode, Data Status Enabled, CRC not Enabled

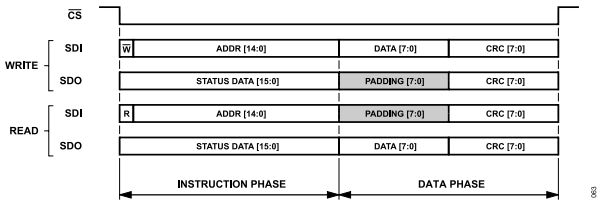

Figure 64. Long Instruction Mode, Data Status Enabled, CRC Enabled

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Configuration SPI Timing

Write Data Frame

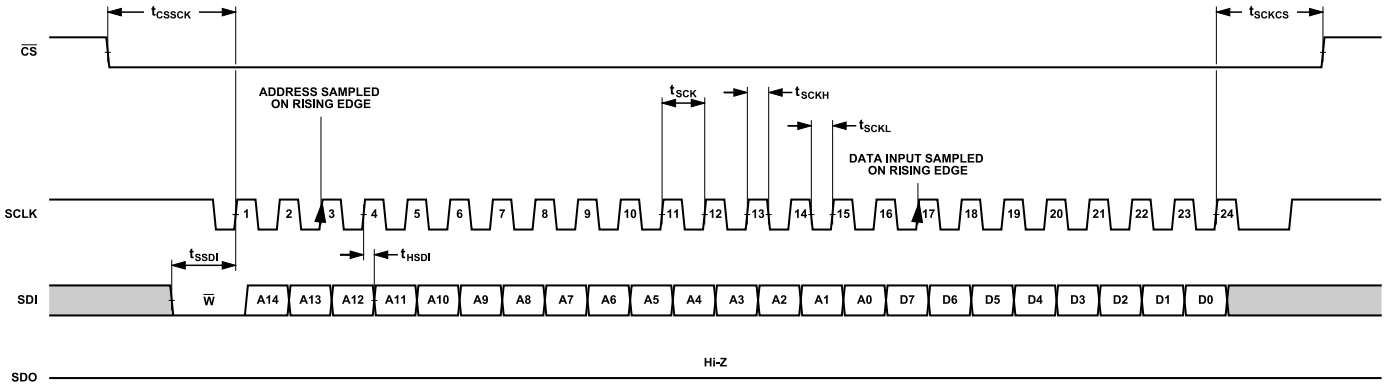

Figure 65. Configuration SPI Timing, Data Write Frame, 16-Bit Instruction Mode (Default)

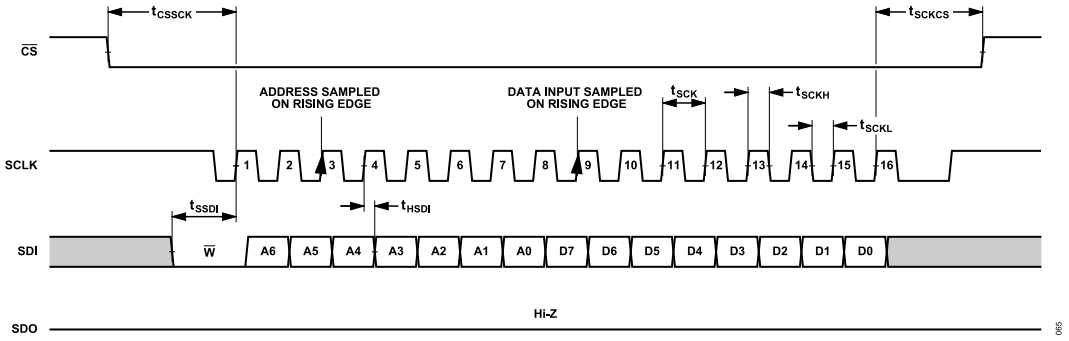

Figure 66. Configuration SPI Timing, Data Write Frame, 8-Bit Instruction Mode, Single 8-Bit Register

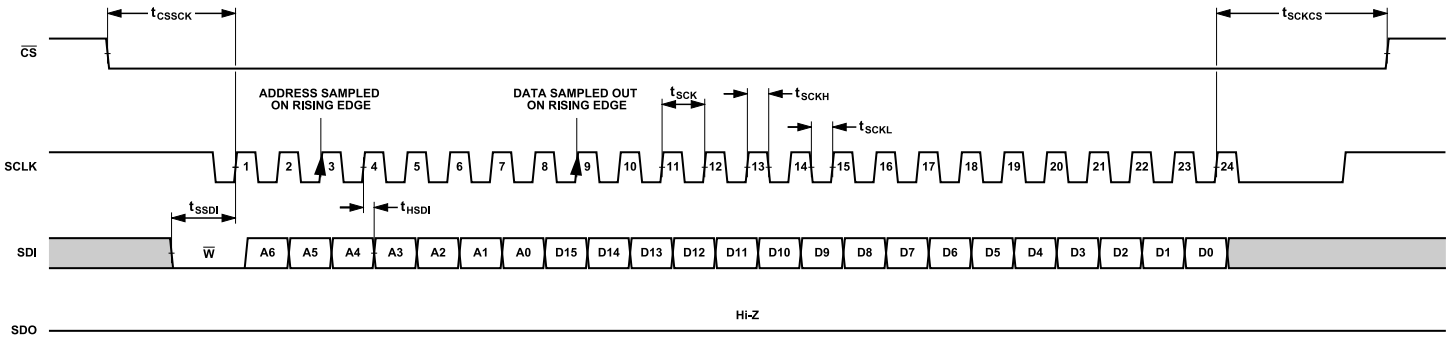

Figure 67. Configuration SPI Timing, Data Write Frame, 8-Bit Instruction Mode, Streaming Mode, Multibyte Register

DIGITAL INTERFACE

Read Data Frame

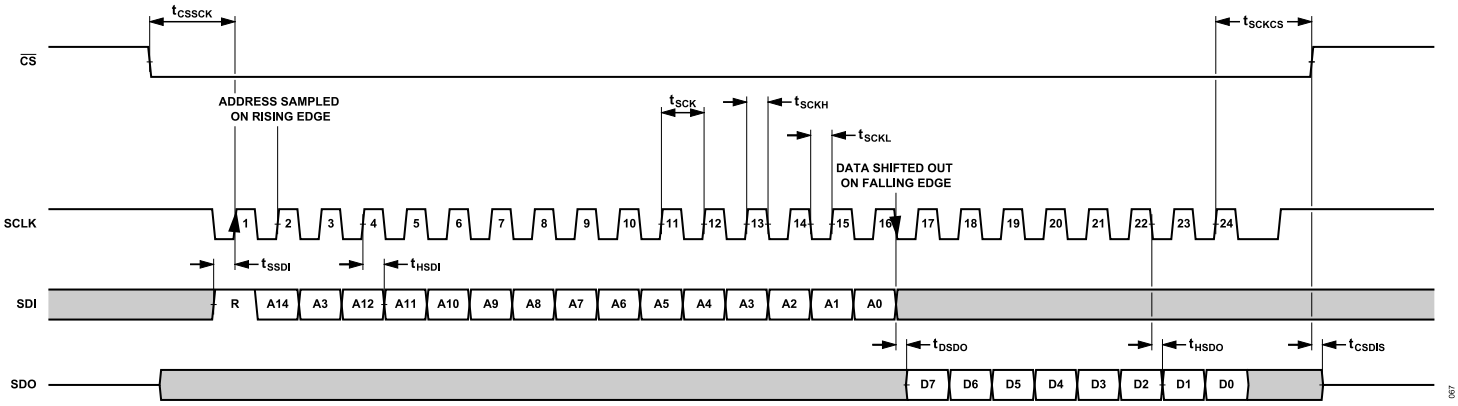

Figure 68. Configuration SPI Timing, Data Read Frame, 16-Bit Instruction Mode (Default)

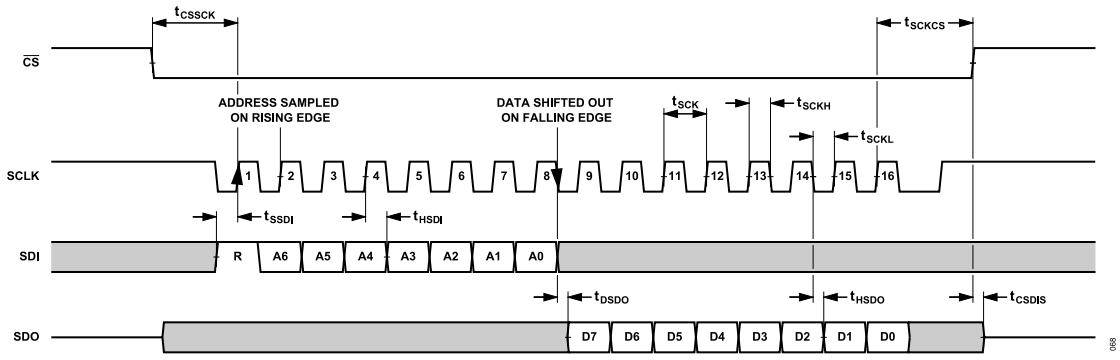

Figure 69. Configuration SPI Timing, Data Read Frame, 8-Bit Instruction Mode

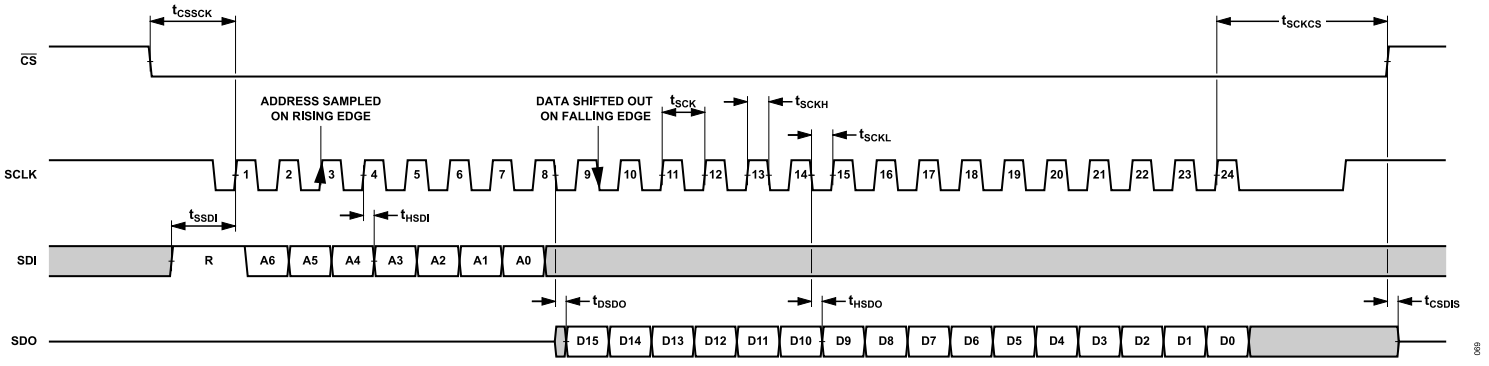

Figure 70. Configuration SPI Timing, Data Read Frame, 8-Bit Instruction Mode, Steaming Mode, Multibyte Register

DIGITAL INTERFACE

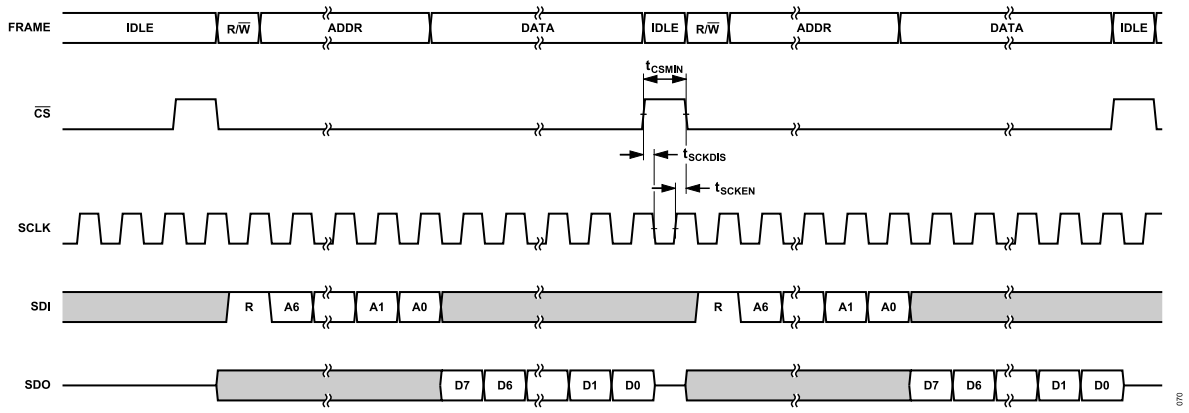

Figure 71. Configuration SPI Timing, Data Read Frame, Continuous SCLK

LVDS DATA INTERFACE

LVDS Data Interface Configuration

The LVDS interface consists of up to five pairs of differential signals. The data clock input pair (CLK+ and CLK−), echoed data clock output pair (DCO+ and DCO−), two data output lanes (DA+ and DA− , DB+ and DB−), and optionally, the conversion clock can be configured as either an LVDS pair (CNV+ and CNV−) or as a CMOS using CNV+, where for this case, CNV− is connected to GND. This user selection is configured using the LVDS_CNV_EN bit in the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section, Address 0x16). The data lanes use a DDR scheme, and each scheme can support a throughput of up to 800 (Mbps). By default, LVDS is selected as the primary data interface for accessing conversion results.

To achieve maximum throughput, it is necessary that while a conversion is performed the result of the previous conversion is read. For this reason, it is critical that both the rising and falling edges of CNV+ and CNV− are closely time aligned to the rising edge of CLK+ and CLK−. To avoid introducing noise into the conversion result, the CLK+ and CLK− edge placement must be aligned to within ±535 ps (t_{CCA}) of the interface clock (CLK±), as specified in Table 2.

The data interface is highly configurable allowing the customization of the output stream to meet a wide range of applications. Configuration options include the number of active lanes (1, 2), self clocked and echo clock modes, interface test functions, and data encoding. LVDS interface mode is used in applications where continuous conversion at rates exceeding 1 MHz is required.

Transmission of the result data occurs MSB first and is output after the amount of time specified in detail in the ADC Result Latency and LVDS Interface Alignment section.

LVDS Active Data Lane Count

The LVDS interface can be configured to output the result data on either one or two data lanes, which is controlled by the SPI_LVDS_LANES bit in the ADC Data Interface Configuration A register (see the ADC Data Interface Configuration A Register section, Address 0x15). By default, this bit is set to 0 (one lane active), and setting SPI_LVDS_LANES = 1 uses two data lanes. Note that this bit is also used to configure the number of active data lanes for the SPI.

In single lane operation, Data Lane DA+ and Data Lane DA− is enabled as the primary data output, and the conversion result is shifted out serially, MSB first, using 10 interface clocks applied to CLK+ and CLK− inputs per conversion. The result data is shifted out of the device on each edge of the echo clock outputs, DCO+ and DCO−. The result MSB (D19) and all odd numbered data bits are output on the falling edge of the interface clock. Conversely, the even numbered data bits are output on the rising edge of the interface clock.

In dual lane configuration, the result data is shifted out in parallel, 2 bits per clock edge, MSBs first. As a result, only five interface clocks are required per conversion. As the data access period is equivalent to the conversion period, the interface clock frequency is reduced by a factor of two relative to the single lane case. As a consequence of the increased interface clock period, see the ADC Result Latency and LVDS Interface Alignment section for the timing and latency implications on both the single lane and dual lane count configurations.

DIGITAL INTERFACE

Echo Clock Mode

In LVDS data interface mode, the DCO+ and DCO− pin pair is an echo clock output that provides a buffered and delayed version of CLK+ and CLK− pin pair, facilitating data clocking to the host controller data clocking. This feature is controlled by the LVDS_SELF_CLK_MODE bit in the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section, Address 0x16). By default, echo clock mode is active (LVDS_SELF_CLK_MODE = 0). Setting LVDS_SELF_CLK_MODE = 1 disables the DCO+ and DCO− output driver, putting the device in self clock mode (see the Self Clock Mode section) .

When echo clock mode is active, the interface requires a minimum of three LVDS pairs (CLK+ and CLK−, DCO+ and DCO−, and DA+ and DA−) to be connected between the host controller and the AD4080. A maximum of five LVDS pairs are required if the CNV+ and CNV− pin pair is configured as an LVDS input and the DB+ and DB− data lane is enabled. The conversion clock (CNV+ and CNV−) and data clock (CLK+ and CLK−) can be shared amongst multiple AD4080 devices as long as care is taken to fanout the clock network, such that the edge placement requirement is satisfied.

In echo clock mode, data from enabled lanes is clocked out in sync to both rising and falling edges of DCO+ and DCO− in a DDR scheme. Figure 72 and Figure 73 illustrate the relevant LVDS interface timing with respect to the DCO+ and DCO− echo clock for single lane and dual lane configurations, respectively. Calculation of t_{MSB_READ} is described in the ADC Result Latency and LVDS Interface Alignment section.

Consider matching the data clock (DCO+ and DCO−) and data lane (DA+ and DA−, DB+ and DB−) lane routing from the ADC to the host processor for the physical layout to minimize timing skew, which may affect data recovery in the host. For additional routing suggestions, see the Layout Guidelines section.

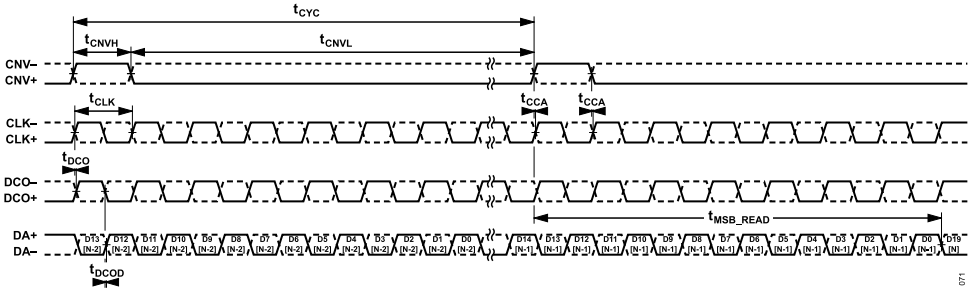

Figure 72. Continuous Conversion Timing, LVDS Data Interface, Single Data Lane, Echo Clock Mode

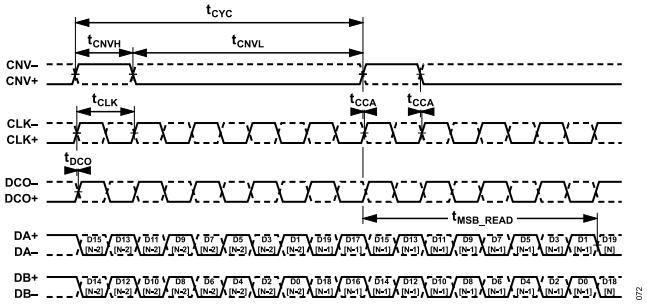

Figure 73. Continuous Conversion Timing, LVDS Data Interface, Dual Data Lane, Echo Clock Mode

DIGITAL INTERFACE

Self Clock Mode

In LVDS data interface mode, it is possible to disable the DCO+ and DCO− echo clock output (see the Echo Clock Mode section) by setting LVDS_SELF_CLK_MODE = 1 in the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section, Address 0x16). This setting puts the device in self clock mode disabling the DCO+ and DCO− output driver, with the benefit of saving interface power as well as reducing the number of LVDS pairs required to interface with the host controller. In this mode, the DCO+ and DCO− pins can be left disconnected; therefore, in single-lane configurations, a minimum of two LVDS pairs (CLK+ and CLK−, DA+ and DA−) are required to connect to each AD4080 instance. The interface connectivity can further be simplified by sharing the interface clock (CLK+ and CLK−) between multiple AD4080 instances.

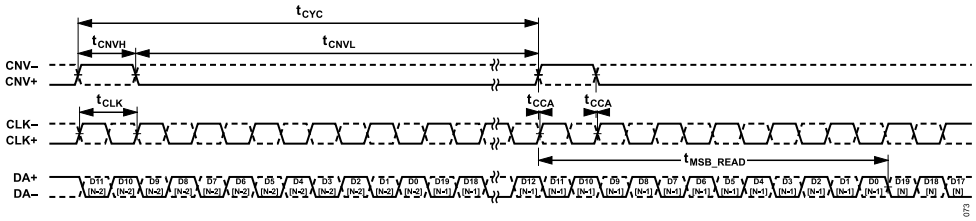

Figure 74. Continuous Conversion Timing, LVDS Data Interface, Single Data Lane, Self Clock Mode

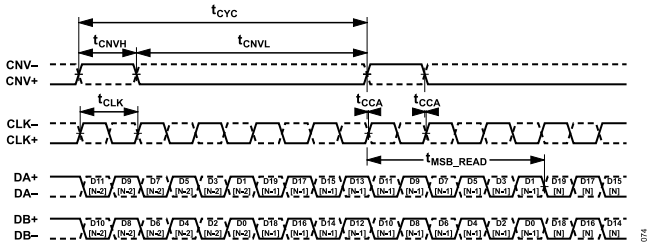

Figure 75. Continuous Conversion Timing, LVDS Data Interface, Dual Data Lane, Self Clock Mode

DIGITAL INTERFACE

LVDS Manchester Encoding Mode

This mode is accessed via the ADC_DATA_INTF_CONFIG_B register (Address 0x16), which produces Manchester encoding of the result data in compliance with IEEE 802.3. This mode can be used in isolated data applications where the converter supplies can be floated and the data outputs capacitively coupled to the host controller. By ensuring that the mean output of each data lane is 0, the receiver side common-mode voltage is not disturbed by the result pattern.

Manchester encoding is available in dual lane LVDS mode only so that the maximum data throughput is achievable with the maximum 400 MHz LVDS clock rate.

Figure 76 shows an example how this isolation can be implemented. Note that the LVDS 100 Ω termination resistor prior to the isolation capacitors is required.

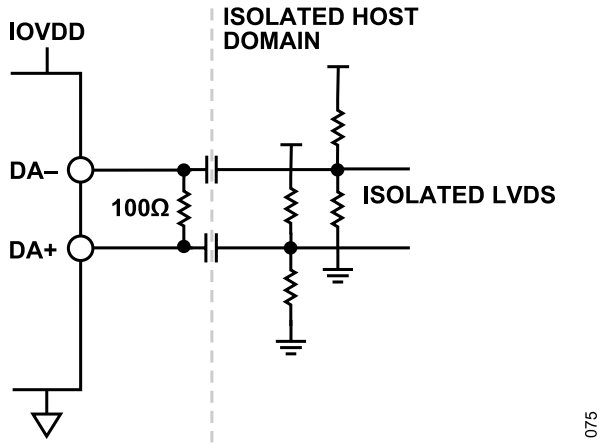

Figure 76. Isolated LVDS

ADC Result Latency and LVDS Interface Alignment

WhenAD4080 is configured for LVDS interface mode, each conversion result is placed into the LVDS interface output shift register(s). The LVDS_CNV_CLK_CNT bits in the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section, Address 0x16) is used to configure the point in time when the conversion result data is loaded into the LVDS interface output shift register(s). The total time from the rising edge of a convert pulse to when the MSB of that conversion request is internally available to transfer to the output register is defined as (t_{CYC} + t_{MSB}), both specified in Table 2. Because the transfer of this result data is under the control of the LVDS of CLK+ and CLK−, there is an additional (1.5 × t_{CLK}) that must be allowed to guarantee a fully completed result is transferred to the interface for read back. The user must calculate the correct required LVDS_CNV_CLK_CNT value and configure the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section) according to the conversion rate and t_{CLK} used.

For minimum latency, the correct LVDS_CNV_CLK_CNT value to use for a particular conversion rate is calculated as (t_{MSB}/t_{CLK} + 1.5). This number is rounded down to the nearest integer value.

The maximum t_{MSB} time is specified as 22.4 ns with gain error correction enabled (see the Gain Error Correction section). For a 40 MSPS conversion rate in single lane LVDS with a 400 MHz LVDS clock, this is calculated as 22.4 ns/2.5 ns + 1.5, yielding a setting of 10 for the LVDS_CNV_CLK_CNT. Conversion latency is then determined as time, aligned to the falling edge of the CLK signal, described as t_{MSB_READ} or latency in the timing diagram, which can be calculated as (LVDS_CNV_CLK_CNT + 0.5) × t_{CLK}. For the given example, the single lane latency is calculated as (10 + 0.5) × 2.5 ns + t_{CYC} = 46.25 ns latency.

Taking a dual lane example, the same formula is used, again taking a 40 MSPS example, again with gain error correction enabled, the LVDS clock runs at 200 MHz and yields (22.4 ns/5 ns) + 1.5, resulting in an LVDS_CNV_CLK_CNT of 5, and a total result latency of (5 + 0.5) × 5 ns + t_{CYC} = 52.5 ns latency.

Both of these examples are calculated to achieve the minimum latency, and it is possible to use a higher LVDS_CNV_CLK_CNT value, whereby latency is increased by t_{CLK} for each +1 unit increase in the LVDS_CNV_CLK_CNT value.

Figure 77 and Figure 78 serve as aids to describe the placement of the ADC result data onto the LVDS interface controlled by the LVDS_CNV_CLK_CNT. Figure 77 shows that a new result is internally completed after (t_{CYC} + t_{MSB}), and this result is now available to the interface, signified here also by a notional $t_{MSB\_AVAILABLE}$ (introduced only for the purposes of the Figure 77 explanation). As this example represents a 40 MSPS conversion rate, Figure 77 shows that the LVDS_CNV_CLK_CNT setting of 10 is the earliest the conversion result can be loaded to the LVDS interface. One additional full t_{CLK} cycle is required (a complete cycle being CLK+ falling edge to next CLK+ falling edge) is required to move the MSB to the output. This cycle is highlighted within Figure 77 also with a notional t_{MSB_READ} indicator for illustrative purposes only.

DIGITAL INTERFACE

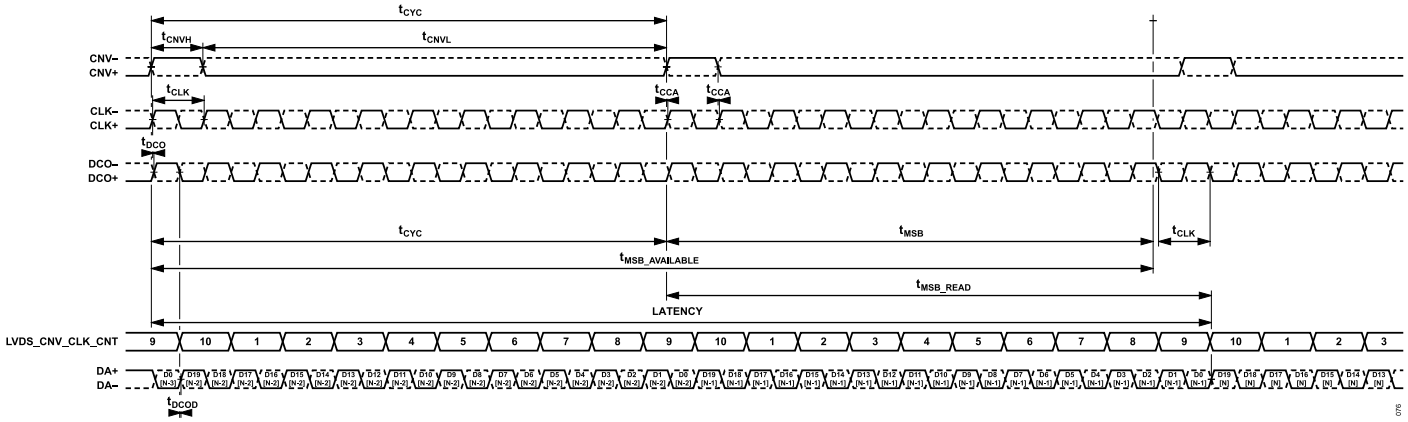

Figure 77. Single Lane LVDS, Echo Clock Mode, LVDS_CNV_CLK_CNT Position Example

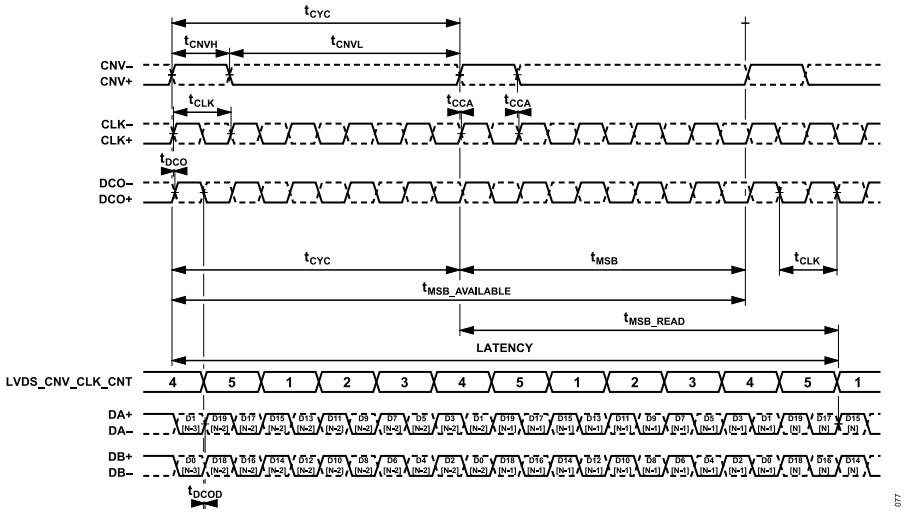

Figure 78. Dual Lane LVDS, Echo Clock Mode, LVDS_CNV_CLK_CNT Position Example

Table 20. Valid LVDS_CNV_CLK_CNT Settings

LVDS_CNV_CLK_CNT Settings	Clock Count Number	
	Single Lane Mode	Dual Lane Mode
0b0000	3	3
0b0001	4	4
0b0010	5	5
0b0011	6	1
0b0100	7	2
0b0101	8	Selection not valid
0b0110	9	Selection not valid
0b0111	10	Selection not valid
0b1000	1	Selection not valid
0b1001	2	Selection not valid

As a overview guide, Table 21 indicates the minimum required LVDS_CNV_CLK_CNT settings for various conversion rates.

The maximum t_{MSB} of 22.4 ns, that is with the gain error correction enabled (see the Gain Error Correction section), is used for all calculations in Table 21. On power-up, the value of the gain error correction is 0x200, disabling the correction and allowing for a lower latency result. In this case, t_{MSB} is 18 ns and a latency of 46.25 ns can be achieved.

Using this example, the same formula is used, again taking a single lane 40 MSPS example, the LVDS clock runs at 400 MHz and yields (18 ns/2.5 ns) + 1.5, resulting in an LVDS_CNV_CLK_CNT of 8 and a total result latency of (8 + 0.5) × 2.5 ns + t_{CYC} = 46.25 ns latency.

To aid alignment of this valid result data position with the digital host of the user, the ADC Data Interface Configuration A register (see the ADC Data Interface Configuration A Register section, Address 0x15) contains access to the interface check feature enabled by setting the INTF_CHK_EN bit. When this bit is set, the ADC results are no longer output on the interface, and the output is replaced with a fixed pattern 20b1010 1100 0101 1101 0110 (0xA C5D6).

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This feature allows the user to align and test the data interface to their digital host. When the INTF_CHK_EN bit is unset, the normal conversion results are output to the LVDS interface immediately. This method is useful for alignment, particularly for self clock mode cases where unknown PCB propagation delays may be present between the AD4080 and its digital host controller. Note that this feature was specifically designed to help output LVDS data with the LVDS clock of the digital host by using static data, and the feature does not indicate if the LVDS_CNV_CLK_CNT setting is used.

Table 21. LVDS_CNV_CLK_CNT Settings for Various Sample Rates

Sample Rate (MSPS)	LVDS Lanes	f_{CLK} (MHz)	t_{CLK} (ns)	$(t_{MSB}/t_{CLK}) + 1.5$	LVDS_CNV_CLK_CNT Setting
40	1	400	2.500	10.46	10
35	1	350	2.857	9.34	9
30	1	300	3.333	8.22	8
25	1	250	4.000	7.1	7
20	1	200	5.000	5.98	6
15	1	150	6.666	4.86	4
40	2	200	5.000	5.98	5

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LVDS Data Transfer Latency

Where the user is concerned in knowing the overall latency from when an individual ADC conversion is initiated to the time when the LSB has reached the host controller, it is important to consider the data transfer latency. The total latency observed is the sum of the ADC latency and the data transfer latency, in this case, the LVDS_CNV_CLK_CNT is set to achieve minimum ADC latency. Additional clock cycles more than the minimum required incur additional LVDS clock cycles of latency to the overall latency, as is shown in Figure 79.

The data transfer latency on the LVDS interface depends on the following parameters:

- LVDS clock period, t_{CLK}
- Number of active LVDS lanes, N_{LANES}
- Number of bits to be read, N_{BITS}

Calculate the latency as follows:

$$\text{Data Transfer Latency} = \frac{N_{BITS}}{N_{LANES}} \times t_{CLK}$$

For applications that require extremely low latencies, note that as the data is transferred MSB to LSB in both single and dual lane modes, and that there is no requirement to fully read a result from the interface, the data transfer latency can be reduced for lower resolution results (that is, N_{BITS} can be chosen to be smaller than the maximum 20 bits available).

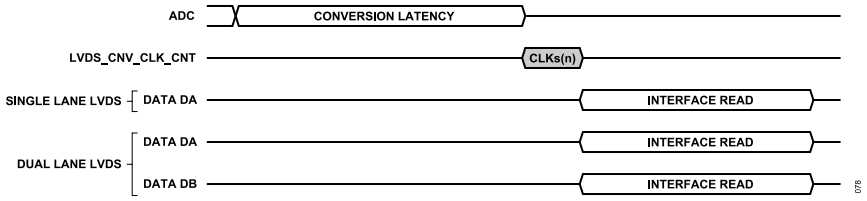

Figure 79. LVDS Data Transfer Latency

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LVDS Output Differential Drive

The AD4080 supports selection of the LVDS output differential voltage from one of three predetermined differential amplitudes of ±185 mV p-p, ±240 mV p-p, and ±325 mV p-p assuming a termination resistance of 100 Ω across the differential pair. The output common-mode voltage of the LVDS drive is adjusted for each selection automatically to ensure that the peak output voltage remains within the IOVDD rail. The current default selection sets the differential amplitude at ±240 mV p-p. The output differential voltage can be modified by writing to the LVDS_VOD bits of the ADC Data Interface Configuration C register (see the ADC Data Interface Configuration C Register section, Address 0x17).

Data Interface Test Functions

Regardless of the selected output configuration, the AD4080 is equipped with self test functions that enable verification of the integrity of the data interface physical layer, including device pads, PCB interconnect, and the host interface connections. An interface check function is available setting a fixed, 20-bit data pattern mode to output. Selection of this test function is made by writing to the INTF_CHK_EN bit in the Data Interface Configuration A register (see the ADC Data Interface Configuration A Register section, Address 0x15).

By enabling the built-in test function, access to conversion results is suspended; therefore, only use this function at either power-up or during an idle period when conversion results are not required for normal system function.

Refer to the ADC Result Latency and LVDS Interface Alignment section for further information.

SPI DATA INTERFACE

SPI Data Interface Configuration

For applications that do not require the interface bandwidth of the LVDS interface, such as when using asynchronous capture into the result FIFO, the data interface can be reconfigured into a single or quad lane, SPI data interface. In this configuration, the AD4080 outputs data on either one or four CMOS data lanes simultaneously at serial clock rates up to 50 MHz. The result data is shifted out serially on the falling edge of the interface clock (DCLK). In SPI configuration, the AD4080 results can be read at interface rates up to 200 MHz when using four SPI lanes.

To select the SPI configuration, program the DATA_INTF_MODE bit of the Data Interface Configuration A register (see the ADC Data Interface Configuration A Register section, Address 0x15) with Binary Sequence 1'b1. Once configured for SPI mode, the AD4080 LVDS drivers are automatically disabled, including the echo clock output (DCO+ and DCO−), preventing contention between LVDS and CMOS functions. As a result, the LVDS_SELF_CLK_MODE and LVDS_VOD settings no longer effect the operation of the data interface and can be left at their power-on defaults or another convenient value. Because the driver is disabled, the DCO+ and DCO− output pins can, therefore, be left disconnected in the hardware design as these pins are unused.

As detailed in Table 22, the following LVDS pins are reconfigured as CMOS input or outputs to realize the SPI data interface.

Table 22. LVDS/SPI Data Interface Pins Crossreference

LVDS Pin	CMOS Pin	Function
CLK+	DCLK	Data interface clock input
CLK−	$\overline{DCS}$	Data interface chip select input
DA+	SDOA	Serial Data Output A
DA−	SDOB	Serial Data Output B
DB+	SDOC	Serial Data Output C
DB−	SDOD	Serial Data Output D

As with LVDS configuration mode, SPI configuration selection allows control of the number of active lanes. For SPI data interface configuration, the user has the option to configure single lane SPI or quad lane SPI.

SPI Active Data Lane Count

The SPI can be configured to output the result data on either one or four data lanes, which is controlled by the SPI_LVDS_LANES bit in the ADC Interface Configuration A register (see the ADC Data Interface Configuration A Register section, Address 0x15). By default, this bit is set to 0 (one lane active), and can be set to 1 to use four data lanes. Note that this bit also sets the number of active data lanes for the LVDS interface. The data order and pin assignment to the serial data output (SDOx) pins is detailed in Table 23, and shown in Figure 86.

Table 23. SPI Data Lane(s) Data Order and Pin Assignment

	Output Data Order	
Serial Data Output Pin	One Active SPI Lane (SPI_LVDS_LANES = 0)	Four Active SPI Lanes (SPI_LVDS_LANES = 1)
SDOA	Not applicable	SDO 3
SDOB	SDO 0	SDO 2
SDOC	Not applicable	SDO 1
SDOD	Not applicable	SDO 0

Data Interface CRC

To ensure the integrity of the result data, a CRC is appended to the FIFO results. This CRC is always enabled and appended. The computation of the result checksum is independent of that of the configuration interface. The result is 24 bits in length and is appended to each data result record acquired from the FIFO.

Sign Extension

When accessing the FIFO data with the SPI data interface, the 20-bit resolution of the AD4080 is not a convenient length for interfacing with microcontroller or microprocessor hosts. To make

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data access and storage simpler, the ADC result is sign extended to 24 bits. In this way, the data format aligns better with their selected host.

GPIO PINS

The AD4080 GPIO pins are intended to simplify the development of synchronous data acquisition applications by facilitating a simplified state control interface between the host processor, the data converter, and other related signal chain components. When configured as an output, these GPIO pins can be assigned as an indicator of device status, a digital control for a related signal chain component, or a serial data lane for device configuration. In input mode, the GPIO pins allow pin programming of converter features such as digital filter synchronization (reset) and an external event trigger.

The desired function for each GPIO is defined by writing to the GPIO Configuration A through GPIO Configuration C registers (Address 0x19 through Address 0x1B), see the GPIO Configuration A Register section through the GPIO Configuration C Register section. The configuration for each GPIO includes an output enable bit, an output data bit, and a function selection. The output data bit determines the logical state of the output when the GPO data option is selected; otherwise, the output state is determined by the selected function, assuming the output is enabled. By default, GPIO0 is enabled as an output, and the configuration SPI SDO function is selected. All other GPIO outputs are disabled.

Table 25 provides a brief description of the available AD4080 GPIO functions. Each of the GPIO pins can be configured for any of the following functions.

Table 24. GPIO Registers Overview

Register	Bits	Contents
GPIO_CONFIG_A	GPIO_0_EN, GPIO_1_EN, GPIO_2_EN, GPIO_3_EN	Enable bits for each GPIO. 0: Configures the GPIO as an input. 1: Configures the GPIO as an output.
GPIO_CONFIG_A	GPIO_0_DATA, GPIO_1_DATA, GPIO_2_DATA, GPIO_3_DATA	The corresponding GPIO_x_SEL bit for each GPIO can be set to 0111b to read or write data to that GPIO. In this mode, GPIO_x_EN selects whether each of these data bits is read only or write only, depending on whether the GPIO is configured as an input or an output. When configured as an output, these bits are write only, the user can set the bits to a logic level that they need to output on the GPIO. When configured as an input, these bits are read only, the user can read the bits to determine the logic level input to on the GPIO. If the corresponding GPIO_x_SEL is not set to 0111b, the GPIO_x_DATA is not valid as the GPIO is overridden with the selected GPIO function
GPIO_CONFIG_B	GPIO_0_SEL, GPIO_1_SEL	Selection for the function mode of GPIO0 and GPIO1.
GPIO_CONFIG_C	GPIO_2_SEL, GPIO_3_SEL	Selection for the function mode of GPIO2 and GPIO3.

Table 25. GPIO_x_SEL Function Descriptions

GPIO_x_SEL	Function	Description
0000b	Configuration SPI SDO	Configuration Serial Data Output. This configures the selected GPIO to be the SDO for the configuration SPI.
0001b	FIFO full	FIFO Memory Full Indication Output. This configures the selected GPIO to function as a FIFO full indicator. The FIFO full indicator is set when the conversion result corresponding to the specified count in the FIFO watermark registers (see the FIFO Watermark Register section, Address 0x1D and Address 0x1E)is loaded into the data FIFO. The FIFO full status bit is cleared by reading data from the FIFO, and it is cleared when the first conversion result is moved from the FIFO to the data interface output shift register.
0010b	FIFO read done	FIFO Memory Read Completed Output. This configures the selected GPIO to function as a FIFO read done indicator. The FIFO read done indicator is cleared by default when the FIFO is first enabled, and each time the last conversion result is moved from the FIFO into the data interface output shift register. The FIFO read done is cleared when the MSB of the last FIFO result is read on the selected data interface.
0011b	Filter result ready	Filter Result Ready Output. When the digital filter is enabled, this configures the selected GPIO to function as an indicator that new data is available to read on the interface. This active low indication allows synchronization between the host and the AD4080 when utilizing the integrated digital filter to oversample and decimate an incoming signal. The signal is driven low at the end of each filter decimation period and is driven high again before the next decimated output is ready.

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Table 25. GPIO_x_SEL Function Descriptions (Continued)

GPIO_x_SEL	Function	Description
0100b	HI_DTCT	High Threshold Event Output. With threshold detection enabled, this configures the selected GPIO to indicate when the high level threshold is crossed. The output is active high.
0101b	LO_DTCT	Low Threshold Output. With threshold detection enabled, this configures the selected GPIO to indicate when the low level threshold is crossed. The output is active high.
0110b	$\overline{\text{ALERT}}$	Status Alert (Active Low) Output. This configures the selected GPIO to function as the status alert for threshold event detection.
0111b	GPIO data	General-Purpose Output Mode. In this mode, the state of the corresponding GPIO_x_DATA bit in the GPIO Configuration A register (see the GPIO Configuration A Register section, Address 0x19) is applied to the configured output.
1000b	$\overline{\text{FILTER\_SYNC}}$	Filter Synchronization Input (Active Low). This configures the selected GPIO to function as a synchronization signal for the digital filter. When held low, this input holds the digital filter in reset.
1001b	EXT_EVENT	External Event Trigger Input. Event triggers when a logic high is detected on the configured GPIO input. This event can be used to trigger the FIFO.

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OVERVIEW

The AD4080 includes several useful digital features that offer great solution benefits to many applications. These features can be individually enabled by the user, when required. A brief overview follows for these features, in depth explanation and definition of these features are found in the following sections.

- Event Detection: This feature allows the detection when the analog input has crossed user-configured thresholds. Such detections can be flagged in the configuration registers, output to a GPIO, or used to trigger the result FIFO.
- Result FIFO: This feature allows the acquisition of records of up to 16,384 conversion results into the on-chip memory. These acquisitions can be read back to the host controller via LVDS or the SPI data interface. The results stored in the FIFO can be either unprocessed ADC results or those that have been processed through the digital filter feature.
- Digital Filter: This feature offers three different digital filter configurations, each with a wide range of decimation rates, allowing oversampling benefits and the close control of the signal bandwidth.
- System Error Correction Coefficients: Although the AD4080 offers excellent factory calibrated precision with minimal offset and gain errors, this feature allows the user to correct for signal chain that may be present within their application.

EVENT DETECTION

The AD4080 includes an event detection feature, whereby the user can either indicate when a particular analog input threshold level is crossed or monitor a GPIO configured as an input. An internally generated event can then be used to set a flag in the configuration memory or routed to a configured GPIO output to be used to alert a host controller that a threshold condition is breached. It is also possible for a user to route an external signal to the AD4080 to be used as an external trigger. An internally or externally generated event can also be used to trigger the integrated result FIFO (see the Result FIFO section). The mechanism for this is explained in the Event Detection for FIFO section. The threshold detection compares a converted voltage code to a user-configured code because this is done in a sample by sample basis, and events immediately trigger, level hysteresis setting is also configurable to prevent unwanted triggering.

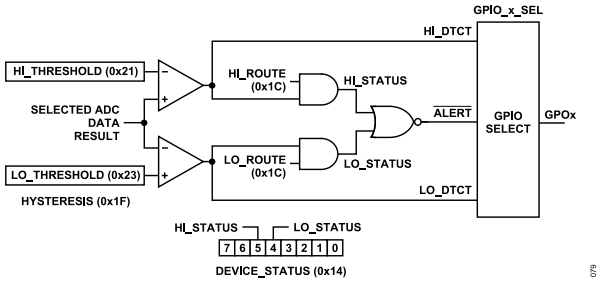

Figure 80. Internally Generated Event Detection Signal Path

The Figure 80 serves as an aid with detailing the configuration and operation of the event detection of the AD4080.

Table 26. Event Detection

INT_EVENT_EN Bit (Address 0x1C)	Mode	Trigger Source	Comment
0	External event	GPIO_x_SEL = 4b1001, that is, configured for EXT_EVENT	Event triggers when a logic high is detected on the selected GPIO input.
1	Internal event	ADC Results threshold detection is enabled.	HI_THRESHOLD (Address 0x21 and Address 0x22) and LO_THRESHOLD (Address 0x23 and Address 0x24) set the upper and lower ADC result (or the digital filter result) code threshold for the event to be triggered.

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Event Detection Timing

When event detection is enabled in the general configuration register (see the General Configuration Register section), the HI_DTCT and LO_DTCT signals indicate the occurrence of an internally generated event. These signals can be routed internally through the following paths:

- HI_DTCT and LO_DTCT are directly accessible via an enabled GPIO with GPIO_x_SEL set to 0b100 or 0b101, respectively, a threshold event can be monitored externally by a digital host via the GPIO. Logic 1 on a configured GPIO indicates detection of an event.
- HI_DTCT and LO_DTCT can each be routed by setting the HI_ROUTE and LO_ROUTE bits to 1, respectively, in the general configuration register (Address 0x1C) to allow HI_DTCT and LO_DTCT to propagate to the LO_STATUS and HI_STATUS bits in the device status register (see the Device Status Register section, Address 0x14). These status bits can be monitored by the digital host via the configuration SPI. Logic 1 on a configured GPIO indicates the detection of an event. Each of these two bits are independently cleared when a 1 is written to these bits. Power cycling or device reset also result in the bits clearing.
- HI_DTCT and LO_DTCT can each be routed by setting the HI_ROUTE and LO_ROUTE bits to 1, respectively, in the general configuration register (Address 0x1C) to allow HI_DTCT and LO_DTCT to propagate to the $\overline{\text{ALERT}}$ signal. Any enabled GPIO set to output a status alert, that is, with GPIO_x_SEL set to 0b0110, routes the $\overline{\text{ALERT}}$ signal to the GPIO to indicate when an event occurs. A GPIO configured in this mode is normally high, with a logic low indicating that an event has occurred. As indicated in the Figure 82 section, this GPIO remains low only while the threshold level is crossed, and it returns to logic high as soon as the threshold bound is no longer crossed, and the timing in Figure 81 is satisfied.

Event detection is synchronous to the rising edge of the CNV+. A latency of two conversion clock cycles exists from the first CNV+ edge where the analog input crosses a threshold to a detected event that is flagged in the device status register and to any GPIO configured to route $\overline{\text{ALERT}}$. As is evident in Figure 80, where both the HI_DTCT flag and $\overline{\text{ALERT}}$ routed to a GPIO are shown, the behavior, once the threshold level is no longer crossed, is different. When a CNV+ rising edge occurs where the analog input no longer crosses the set threshold, $\overline{\text{ALERT}}$ de-asserts two conversion cycles later, on the rising edge of CNV. Any HI_DTCT or LO_DTCT already set is not cleared at this point. These signals are only cleared by writing 1 to the relevant bits in the device status register (Address 0x14) or where a device reset occurred.

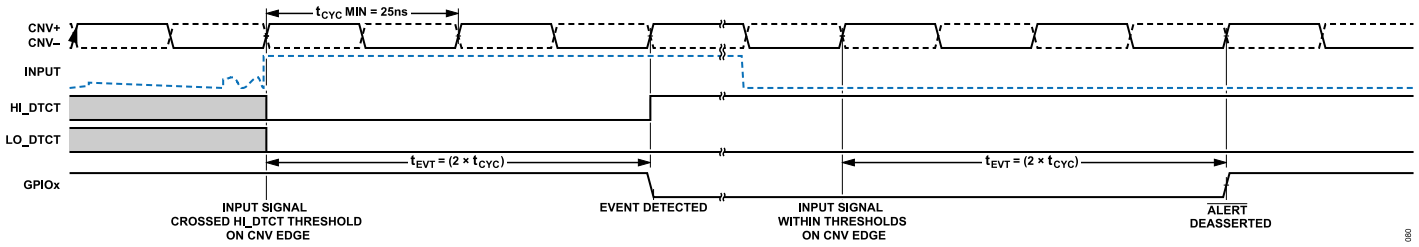

Figure 81. Event Detection Timing

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Threshold Detect Levels

The threshold detection of the AD4080 includes a hysteresis setting. By configuring this setting, the user can ensure that unwanted threshold triggering can be avoided. Figure 82 shows how this can be achieved. A single hysteresis setting is configured, that is then applied to both the HI_THRESHOLD and LO_THRESHOLD bits. The high and low detection flags remain set until the hysteresis thresholds are crossed.

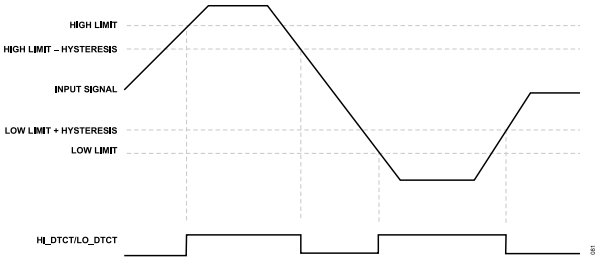

Figure 82. Threshold Detect Levels

Enabling Event Detection

By default, after power on or reset, HI_ROUTE and LO_ROUTE are set to Logic 0, masking the threshold level detection from generating any event alert. When enabled, the gated versions of these signals, HI_DTCT_GATED and LO_DTCT_GATED, are logic NOR'd to generate the $\overline{\text{ALERT}}$ signal. If a user requires the use of the HI_DTCT, LO_DTCT, or $\overline{\text{ALERT}}$ signals to flag an event occurrence externally, back to a digital host, the GPIO_x_SEL registers can be used to route any, or multiple, of these signals to the GPIO pins.

Event Detection for FIFO

Event detection can also be used to arm the on-chip FIFO. The event detection for the FIFO can be triggered using either internal or external events as detailed in the Table 26 section.

To use the $\overline{\text{ALERT}}$ signal to trigger the FIFO, the HI_ROUTE and/or the LO_ROUTE bits must be configured as required, and the INT_EVENT_EN bit must be set to 1, to use a combined $\overline{\text{ALERT}}$ output to trigger the FIFO. Alternately, when configured with the INT_EVENT_EN bit set to 0, a GPIO EXT_EVENT input must be configured, and this input triggers the FIFO when a Logic 1 is presented on the GPIO. Because this event was generated externally, there is no $\overline{\text{ALERT}}$ signal generated.

The HI_THRESHOLD (Address 021 and Address 022) and LO_THRESHOLD (Address 0x23 and Address 0x 24) bits can be used to configure the ADC output code thresholds for the internal event detection. These bits can each be masked using the HI_ROUTE and LO_ROUTE bits in the general configuration register (Address 0x1C). Setting these bits logic high, routes the bits to be used for the $\overline{\text{ALERT}}$ flag (that can be monitored using a preconfigured GPIO), it is also enabled as a FIFO event trigger as well as making these available as HI_STATUS and LO_STATUS flags in the device status register (Address 0x14).

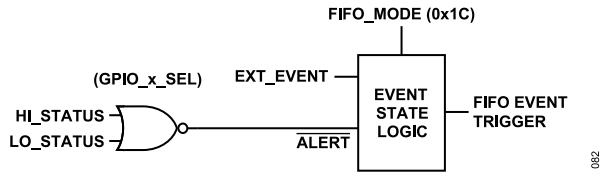

Figure 83. FIFO Event Detection Logic

Event Detection ADC Data Result

The ADC data result, as shown in Figure 80, is dependent of the selected data path. As is evident in Figure 94, where the digital filter (see the Digital Filter section) is enabled, the output of the selected filter refers to the ADC data result that is checked by the threshold detection for event detection.

RESULT FIFO

A single port data FIFO was integrated into the AD4080 for applications where a reduced data interface transmission load is required and where asynchronous data capture and access is appropriate. This FIFO can serve to reduce the requirements for the digital host controller and can, for example, enable the AD4080 to be deployed in systems using an MCU digital host. The data FIFO allows for a record of up to 16,384 data results to be captured per acquisition burst without result loss due to data overflow. As a single port memory, simultaneous data interface read and ADC conversion result write operations are not permitted to the FIFO.

To allow synchronization of FIFO access between the host controller and ADC, status flags are included to indicate if the memory is full (FIFO_FULL) or if no new data available in the FIFO (FIFO_READ_DONE), that is, there is no new data since the last trigger was set, or the last FIFO data read back of a result record has already been completed. When N = WATERMARK is reached, that is, when the conversion result corresponding to the specified count in the FIFO_WATERMARK register is loaded into the data FIFO, memory is set as full, and the FIFO_FULL bit gets asserted in device status register (see the Device Status Register section, Address 0x4). The status bits can be accessed by reading directly from the device status register (Address 0x14) via the configuration SPI, appending the status to the data SPI frame, or by assigning the desired status flags to a GPIO pin by setting the required GPIO_x_SEL bit. Further details on these GPIO can be found in the GPIO Pins section. The user can also select between various modes of initiating the burst acquisition, which will be described further in the FIFO Mode Selection and Configuration section.

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FIFO Mode Selection and Configuration

There are four distinct modes in which the data FIFO of the AD4080 can be configured. The active mode is selected by setting the FIFO_MODE bits in the general configuration register (see the General Configuration Register section, Address 0x1C). By default, the FIFO is disabled (FIFO_MODE = 00). The modes are designed to fit the use case requirements of different applications., Table 27 provides details about each FIFO mode and their applicable use cases.

Table 27. FIFO Configuration Modes (FIFO_MODE)

FIFO_MODE Bit Value	FIFO Mode	Description	Use Case
00	FIFO disabled	FIFO is not used. This value also resets and rearms the event trigger.	Continuous convert mode, and FIFO is not in use.
01	Immediate trigger mode	In this mode, the data capture is initiated immediately after receipt of the first valid converter result and continues until [N = WATERMARK] results are loaded into the FIFO memory. Upon read back from the FIFO, FIFO_READ_DONE indicates when [N = WATERMARK] results are read from the FIFO.	User is interested in burst acquisition(s) of [N = WATERMARK] results, initiated by setting this FIFO_MODE, Bits[1:0] value.
10	Event trigger capture, read latest WATERMARK	The data capture into the FIFO memory is initiated by the user-selected event method. The result counter initiates by the event, and data captures to the FIFO stop once [N = WATERMARK] results are captured. Upon read back from the FIFO, FIFO_READ_DONE indicates when [N = WATERMARK] results have been read from the FIFO.	User is interested in burst acquisition(s) of [N = WATERMARK] results, initiated by an event. Only result data after the event is of interest.
11	Event trigger capture mode, read all FIFO	The data capture immediately initiates after the receipt of the first valid converter result. The FIFO continuously fills until an event is detected. If no event is detected before the FIFO fills (that is, 16,384 results are written to memory), the memory continues to fill with the oldest results discarded on a first in, first out basis. Upon receipt of the selected event method, a result counter counts up to [N = WATERMARK]. Data capture stops once the WATERMARK is reached. In this mode, once the FIFO is filled, the position in the FIFO memory at which the event occurred gets automatically stored in the FIFO_WATERMARK register. The value read back from FIFO_WATERMARK allows the user to distinguish which of the stored results captured before the event from those that were captured after the event. Further details can be seen in the example given in the Event Trigger Capture Mode, Read All FIFO section. Upon read back from the FIFO, FIFO_READ_DONE indicates when 16,384 results are read from the FIFO. The full memory read back contains [N = WATERMARK] results after the event. If N in this case is less than 16,384, the remaining contents of the FIFO contain the conversion results prior to the event.	User is interested in burst acquisition(s) of [N = WATERMARK] results initiated by an event. The full FIFO contents are read in this mode. In this mode, the user can read [N = WATERMARK] results after the event and (16,384 − [N = WATERMARK]) before the event. Only WATERMARK values that are multiples of four are valid in this mode.

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FIFO Event Detection

The FIFO is configured for capture in event detection mode (FIFO_MODE = 10 or FIFO_MODE = 11, the following event detection options (see the Table 26 section) are available.

The general configuration register (Address 0x1C) contains the internal event enable bit (INT_EVENT_EN) which determines whether the AD4080 FIFO is to respond to an external or internal event trigger. The default state of this bit on power on and reset is INT_EVENT_EN = 0, which is configured for an external event.

Asynchronous Data Capture

To use the FIFO for asynchronous capture, first write to the FIFO watermark register (see the FIFO Watermark Register section, Address 0x1D) with the number of conversions to be captured in each burst; any integer between 1 and 16,384 can be entered. If using GPIO to pass the FIFO status bits to the host controller, program those selections into the GPIO configuration registers prior to initiating the capture. Refer to the GPIO Pins sections for further detail on GPIO configuration.

The final steps in initiating an asynchronous capture into the data FIFO include enabling the FIFO and then starting the conversion clock. To enable the data FIFO in the general configuration register (see the General Configuration Register section, Address 0x1C), the FIFO_MODE bits must be set to immediate trigger mode (01). In this mode, the FIFO stores the results of the most recent FIFO_WATERMARK samples and then automatically disables capture into the memory. The results can then be accessed through the SPI data interface or LVDS interface.

When the FIFO is enabled, each conversion result is loaded into the internal memory on the rising edge of the convert start signal, CNV. Internal timing dictates that FIFO_WATERMARK + three conversion clocks are required to write FIFO_WATERMARK sample results into the FIFO memory. See Figure 85 and Figure 86 for additional information.

The Figure 84 timing diagram shows an example where FIFO_WATERMARK is set to 1000, and the first ADC results after the event occurred is captured by the FIFO after the third CNV. After N = 1000, that is, it has reached the FIFO_WATERMARK value, FIFO_FULL is asserted, and data stops being captured into the FIFO.

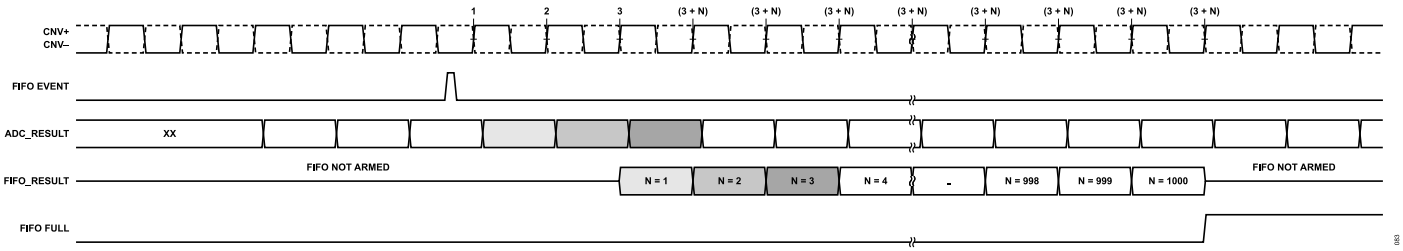

Figure 84. FIFO Data Capture Example, WATERMARK = 1000

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Asynchronous Read Access

Access to the FIFO data is made through either a LVDS configuration (single lane only) or the multioutput SPI configuration of the data interface after the capture has completed. As a result, access is asynchronous to the capture process, and there are no specific timing restrictions between the conversion and interface clocks. Synchronization between the data FIFO and the data interface clock domain requires each read access to begin with a header followed by a transfer of M bytes of conversion data; where M equals the product of the total number of results specified in the FIFO_WATERMARK register (Address 0x1D and Address 0x1E) and the integer length in bytes (for SPI data interface) of a single conversion result. Note that the number of active data lanes reduces the access period by a factor of 2 for each doubling of the number of active lanes.

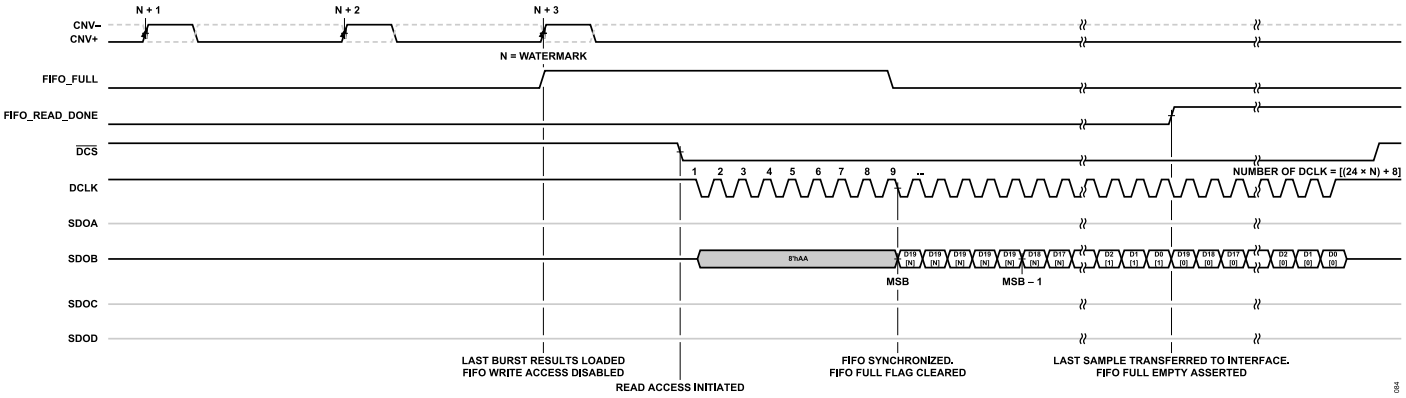

Figure 85. Asynchronous Capture Read Timing, Data FIFO Enabled, Single Data Lane

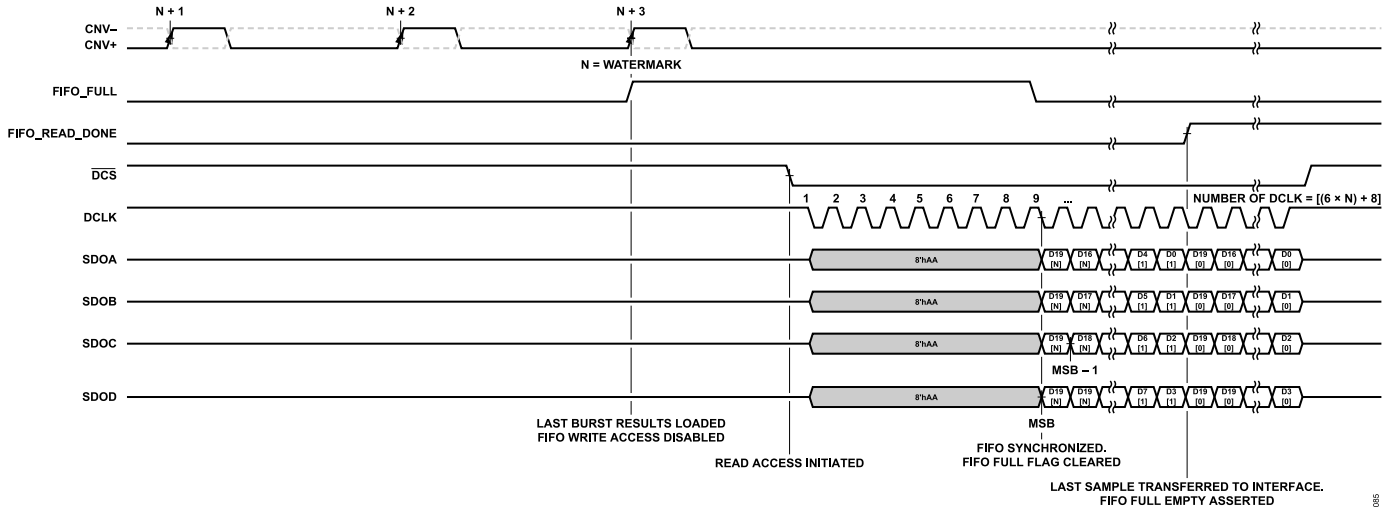

Figure 86. Asynchronous Capture Read Timing, Data FIFO Enabled, Quad Data Lane Configuration

DIGITAL FEATURES

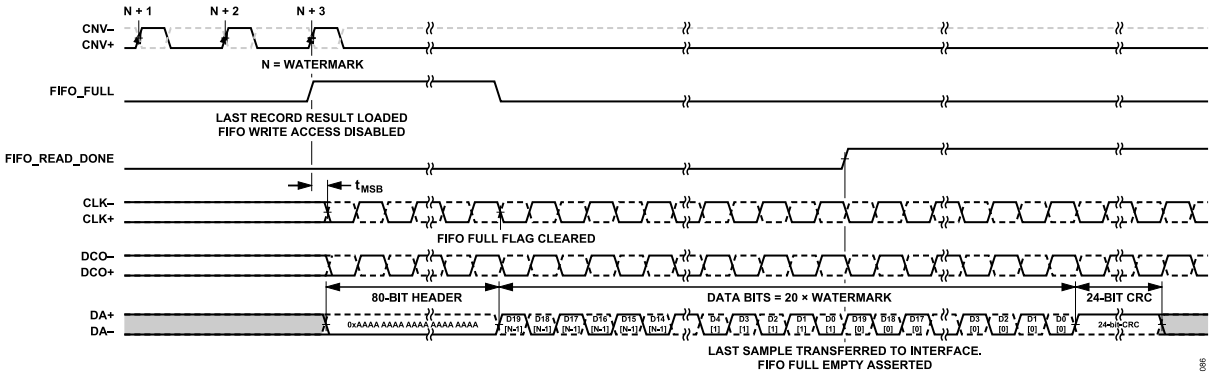

Figure 87. Asynchronous Capture Read Timing, Data FIFO Enabled, LVDS Configuration

DIGITAL FEATURES

FIFO Timing Considerations

Immediate Trigger Mode

Figure 89 illustrates the timing relationship between the command to arm the FIFO for data write access and the point at which the FIFO is armed. Figure 89 shows an example of where single lane SPI data access is configured and FIFO_FULL and FIFO_READ_DONE are output to GPIO. Because a capture has not yet been initiated, FIFO_FULL and FIFO_READ_DONE are driven low. A free running CNV clock is shown in this example. Upon receipt of the update to the general configuration register (Address 0x1C), the FIFO controller advances to an idle state on the next rising edge of CNV. The FIFO then advances to the writing state after two further CNV clock edges and begins filling the FIFO until WATERMARK results are loaded and FIFO_FULL is generated.

Upon completion of reading the FIFO data, a rearming event for immediate mode capture involves disabling the FIFO by writing 00 to FIFO_MODE then re-enabling by writing 01 to the FIFO mode to arm the FIFO for a new capture. As is the case with the initial arming, the FIFO advances to the idle state upon receipt of the first rising edge of CNV after the configure instruction to arm the FIFO is issued. The sequence and timing is the same as for the initial FIFO arming. See Figure 89.

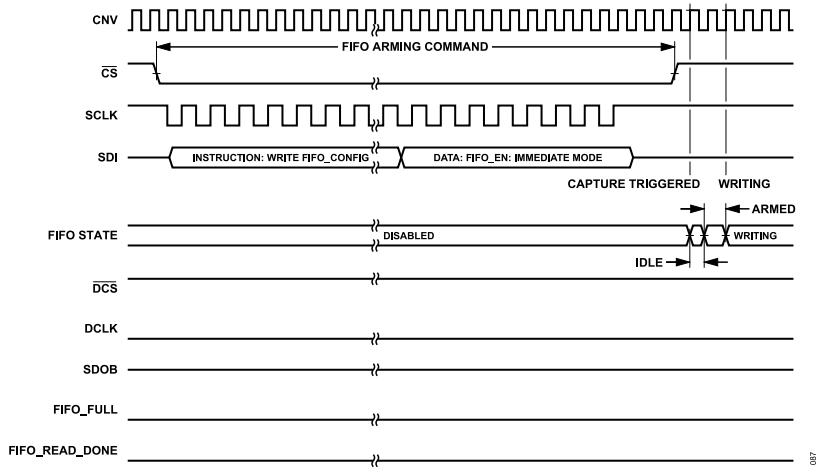

Figure 88. Immediate Trigger ModeArming

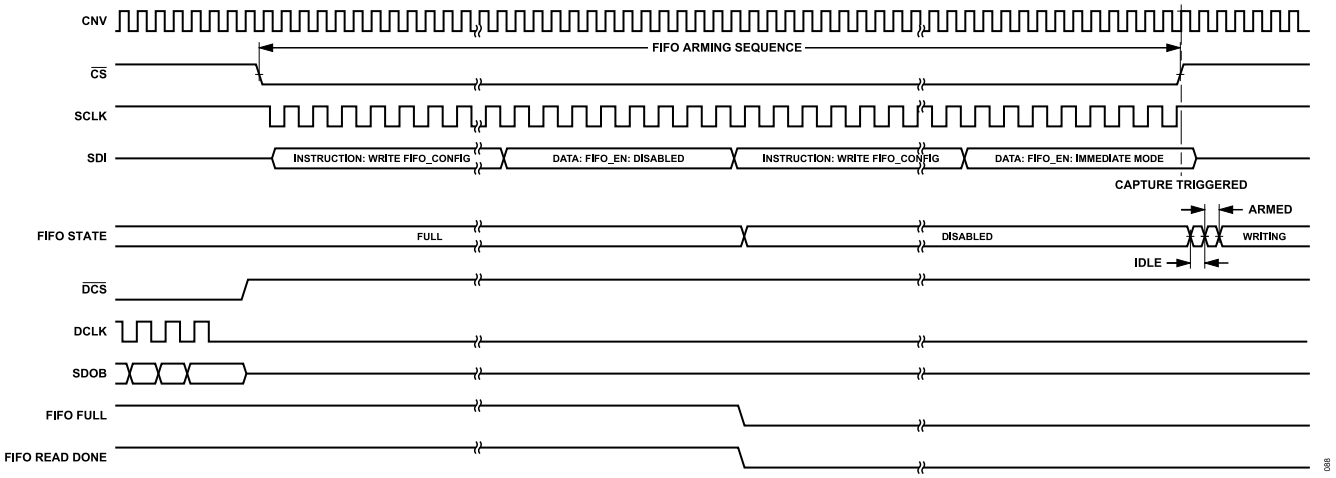

Figure 89. Immediate Trigger Mode Rearming

DIGITAL FEATURES

Event Triggered Capture, Read Latest WATERMARK

Event triggered (read latest) mode is used where there is interest only in the ADC data after an event occurs. This event can be an internally generated event, where the AD4080 is running continuously, and the threshold detection is enabled to trigger an event as soon as an ADC input threshold is crossed. Or, the user can be independently monitoring the system or ADC input for an event, and an external event trigger is user-issued via a configured GPIO.

As in all cases of arming the FIFO, the first rising edge after a FIFO_MODE write command arms the FIFO for data capture; however, no data is written to the FIFO until an event of the selected method occurs.

Rearming the trigger involves a similar process to the immediate mode rearming. The FIFO is firstly disabled by writing 00 to the FIFO_MODE bits before, and then rearmed by again enabling the required capture mode.

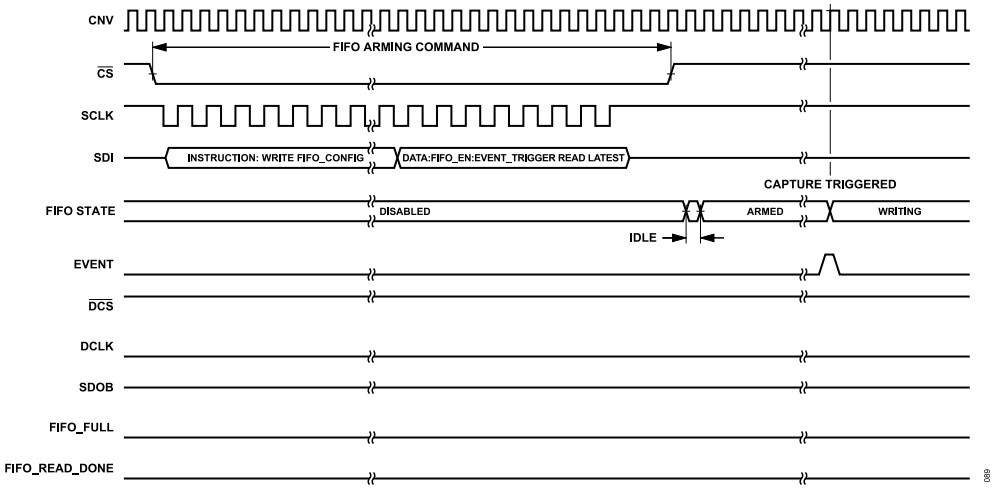

Figure 90. Event Triggered Capture, Read Latest WATERMARK Arming

DIGITAL FEATURES

Event Trigger Capture Mode, Read All FIFO

Event triggered mode can be used where ADC results immediately prior to the event, as well as those after, are of interest to the user. Once armed, the FIFO continuously fills with new ADC results, storing up to, at most, 16,384 of the most recent results, wrapping around and overwriting the oldest results in FIFO memory once 16,384 captures are made.

Once a trigger event occurs, the FIFO continues to capture WATERMARK number of results after the event. Only multiples of four are valid values to set the FIFO_WATERMARK register when using this mode. After an even has occurred, and the WATERMARK number of results have been captured in the FIFO, no further new results are captured until the FIFO is rearmed. Once the FIFO has stopped capturing, the FIFO_WATERMARK register is automatically loaded with a value that represents the location in the FIFO where the event occurred, as shown in Figure 91 and Figure 92. The user must read back all 16384 FIFO results and the value read back from FIFO_WATERMARK allows the user to determine where in the FIFO result data that the even occurred and also to distinguish between results that occurred before the event and those which occurred after the event as shown in the Figure 92 diagram.

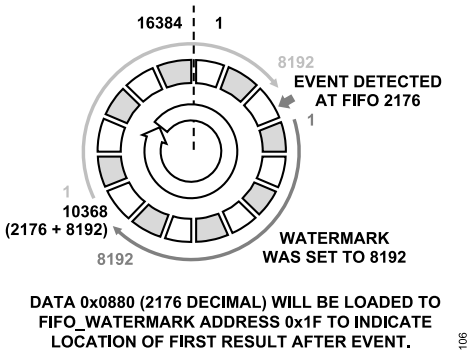

Figure 91. Event Capture Mode Read All FIFO Mode Example, FIFO Filling

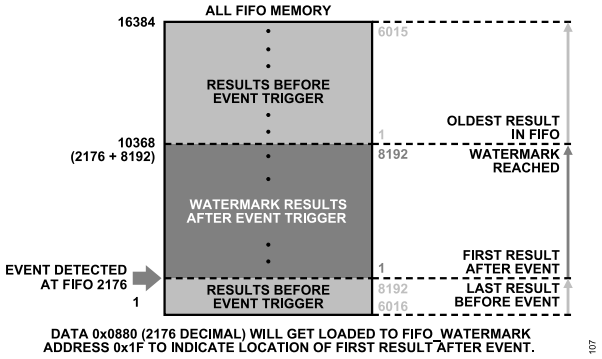

Figure 92. FIFO Event Capture Mode Read All FIFO Mode Example, Locating Event Position in FIFO

DIGITAL FEATURES

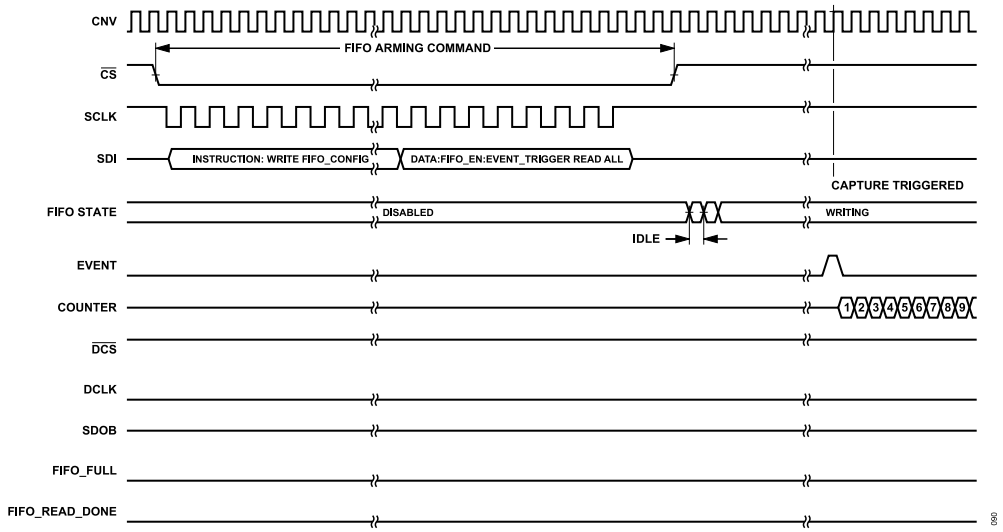

Figure 93. Event Trigger Capture Mode, Read All FIFO Rearming

DIGITAL FEATURES

DIGITAL FILTER

The AD4080 includes the option of enabling an integrated digital filter for applications where noise rejection by bandwidth limiting is desired. As shown in Figure 94 and detailed as follows, there are four paths available by which to route digital data: no digital filtering, a sinc1 filter, a sinc5 filter, or a sinc5 compensated filter.

Further details on each of these filters is described in the following sections. To ensure the first filter result produces the correct data, when a user makes a change to the filter selection, a reset must be issued via the GPIO pin configured for filter synchronization (FILTER_SYNC).

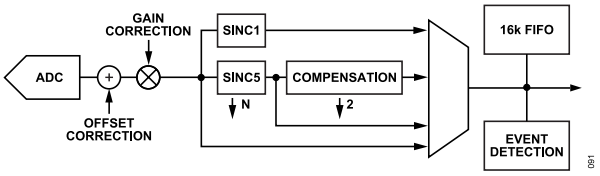

Figure 94. Digital Filter Selection Options

Benefits of Digital Filtering

The ADC result path can be configured to use the integrated digital filter feature. The filter configuration register (see the Filter Configuration Register section, Address 0x29) contains the FILTER_SEL bits that allow the user to bypass (default register setting) the digital filter or select from one of three filter options. Each filter has unique bandwidth profile properties, which allows high flexibility in allowing selection to be made depending on the end application requirements. Table 28 shows the −3 dB bandwidths achievable for each user-selectable filter type. The SINC_DEC_RATE bits controls the bandwidth and the data decimation factor.

These filters allow the user to programmatically control the noise bandwidth of their signal chain and also can offer benefits by reducing the amount filtering required in the analog front end, while offering dynamic range improvement without the need for additional components. The digital filter response sections have addition details on the different filter profiles that include the following:

- Sinc1 has a wider bandwidth but is not optimized for pass-band flatness.
- Sinc5 has a flatter pass-band response; however, with a reduced bandwidth.
- Sinc5 + compensation is a filter highly optimized to give excellent pass-band flatness with a ripple within ±0.1 dB.

Table 28. Filter Bandwidth

Filter Type	SINC_DEC_RATE	Decimation	−3 dB Bandwidth
Sinc1	0000	2	0.25 × f_S
Sinc1	0001	4	0.114 × f_S
Sinc1	0010	8	0.56 × f_S
Sinc1	0011	16	0.28 × f_S
Sinc1	0100	32	0.14 × f_S
Sinc1	0101	64	0.07 × f_S
Sinc1	0110	128	0.035 × f_S
Sinc1	0111	256	0.017 × f_S
Sinc1	1000	512	0.09 × f_S
Sinc1	1001	1024	0.004 × f_S
Sinc5	0000	2	0.117 × f_S
Sinc5	0001	4	0.525 × f_S
Sinc5	0010	8	0.0256 × f_S
Sinc5	0011	16	0.0127 × f_S
Sinc5	0100	32	0.064 × f_S
Sinc5	0101	64	0.032 × f_S
Sinc5	0110	128	0.016 × f_S
Sinc5	0111	256	0.008 × f_S
Sinc5 + Compensation	0000	4	0.1015 × f_S
Sinc5 + Compensation	0001	8	0.0506 × f_S
Sinc5 + Compensation	0010	16	0.0253 × f_S
Sinc5 + Compensation	0011	32	0.0127 × f_S

DIGITAL FEATURES

Table 28. Filter Bandwidth (Continued)

Filter Type	SINC_DEC_RATE	Decimation	−3 dB Bandwidth
Sinc5 + Compensation	0100	64	0.0063 × f_S
Sinc5 + Compensation	0101	128	0.0032 × f_S
Sinc5 + Compensation	0110	256	0.0016 × f_S
Sinc5 + Compensation	0111	512	0.0008 × f_S

DIGITAL FEATURES

Filter Decimation Configuration

Configuration of the digital filter is done through the filter configuration register (see the Filter Configuration Register section, Address 0x29). The FILTER_SEL bits select the active filtering path (that is, what filters are active), with each path having different allowed decimation rates (see Table 29).

Table 29. Digital Filters Decimation Options According to FILTER_SEL Bits Value

FILTER_SEL Bits Value	Active Filter	Allowed Decimation Rates
0b00	No filtering (default)	No decimation
0b01	SINC1 filter	2, 4, 8, 16, 32, 64, 128, 256, 512, 1024
0b10	SINC5 filter	2, 4, 8, 16, 32, 64, 128, 256
0b11	SINC5 + compensation filter	4, 8, 16, 32, 64, 128, 256, 512

The decimation factor is set via the SINC_DEC_RATE bits in the filter configuration register (see Table 62 for the encoding).

The readiness of new filter data can be indicated to the host controller via a GPIO pin by setting one of GPIO_x_SEL bits in either GPIO Configuration B register (see the GPIO Configuration B Register section, Address 0x1A) or GPIO Configuration C register (see the GPIO Configuration C Register section, Address 0x1B) to 0011 (filter result ready (active low)). Until new data is available to the interface, the data from the previous result remains in the output shift register. The user must ensure that the same LVDS clock rate is maintained, and the user can either reread or disregard the repeated result data, which is shown in Figure 95, where a decimate by 4 example is used.

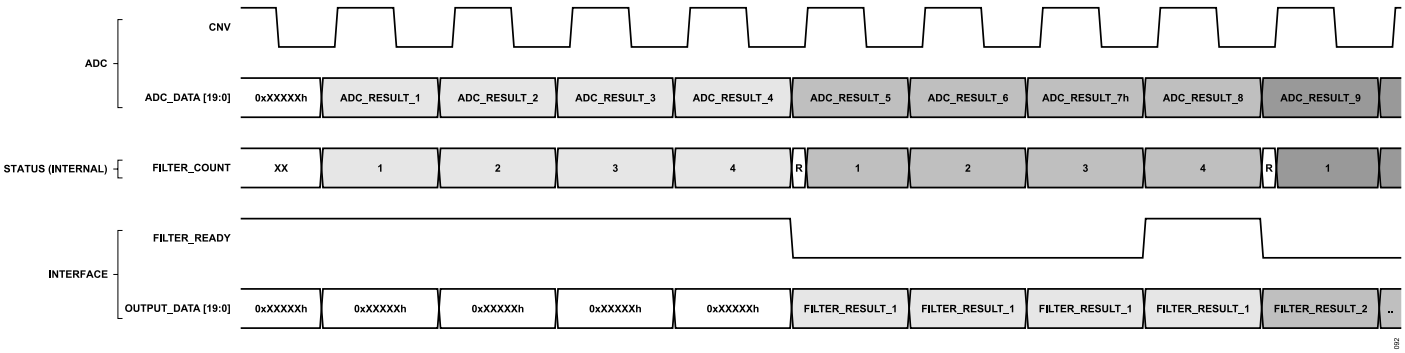

Figure 95. Digital Filter Decimate by 4 Frame Overview

DIGITAL FEATURES

Filter Reset Conditions

Direct LVDS

When accessing the filtered data directly via the LVDS interface, the AD4080 resets the filter by the following two methods:

- By configuring the filter, by issuing a write to the filter configuration register, Bits[7:0] (see the Filter Configuration Register section, Address 0x29).
- By asserting a GPIO that' is configured for $\overline{\text{FILTER\_SYNC}}$ operation.

With FIFO

When the FIFO is enabled, the user must use a GPIO configured as $\overline{\text{FILTER\_SYNC}}$ to reset the filter for each FIFO acquisition.

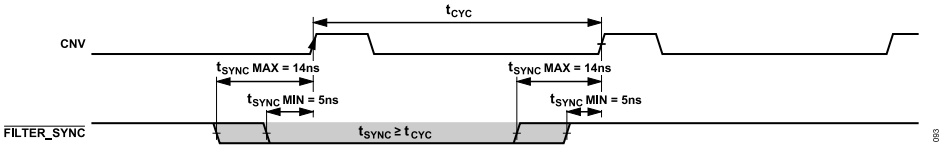

Figure 96. Filter Reset Timing

Filter Synchronization

Set GPIO_x_SEL to $\overline{\text{FILTER\_SYNC}}$ to configure this input providing synchronization to the controller of the user, which can be used to synchronize the filters across multiple AD4080 devices. The $\overline{\text{FILTER\_SYNC}}$ signal is an active low input, and this signal must be held low for a minimum of one conversion cycle to reset and synchronize the digital filter. Refer to Figure 96 for the timing requirements for a filter reset.

DIGITAL FEATURES

Filter Result Ready Indicator

Setting the GPIO_x_SEL bits to 0011 configures the GPIO to output the FILTER_RESULT_RDY signal, which is an active low logic signal that indicates to the host controller when each new filter result is complete. When LVDS is used to directly read out the filter results, this indicator can alert the user when each new filtered conversion result is available to read via the interface.

Filter Interface Timing Considerations

Continuous access to filtered data results is available only through the LVDS data interface. SPI data interface access to filtered results is only made via the FIFO. The timing considerations, in this case, are described in the Filter Interface Timing Considerations when Using the FIFO section. For use with the LVDS data interface, it is recommended to use a GPIO, configured with the appropriate GPIO_x_SEL (0011) to output the filter result ready (active low) signal, as is shown in the example Figure 95 timing diagram.

Filter Interface Timing Considerations when Using the FIFO

Figure 97 serves as an example to illustrate the sequence of events in this mode of operation. This example illustrates a sinc1 filter with a decimate by 2 setting, where three results (that is, WATERMARK = 3) are configured to be stored in the FIFO. When using the integrated digital filters with the FIFO, the filter must be reset prior to each FIFO acquisition record. This reset must be given on the first CNV rising edge, where the FILTER_SYNC signal must be brought low at least 15 ns prior to the CNV edge and then released at least 5 ns before the next rising edge. The first ADC result is ready t_{MSB} after the second CNV rising edge. This first ADC result is latched into the filter on the third CNV rising edge. The fourth CNV rising edge latches the second ADC result into the digital filter. On the fifth rising edge, the first decimate by 2 result is complete, which is indicated by the FILTER_READY signal going active on the fifth rising edge. This first filtered result is loaded into the FIFO on the sixth CNV rising edge. Because this example uses WATERMARK = 3, when three filtered (that is, six core ADC results, decimated by 2) results are loaded to the FIFO, the WATERMARK is reached, and FIFO_FULL is asserted to indicate to the user that a FIFO record is available to read via the configured data interface (that is, the LVDS data lane(s) of the SPI data lane(s)). To initiate a subsequent FIFO record acquisition of the filtered ADC results, the user must start the whole sequence over, beginning again with the reset of the digital filter by bringing the FILTER_SYNC signal low on the first rising edge of CNV.

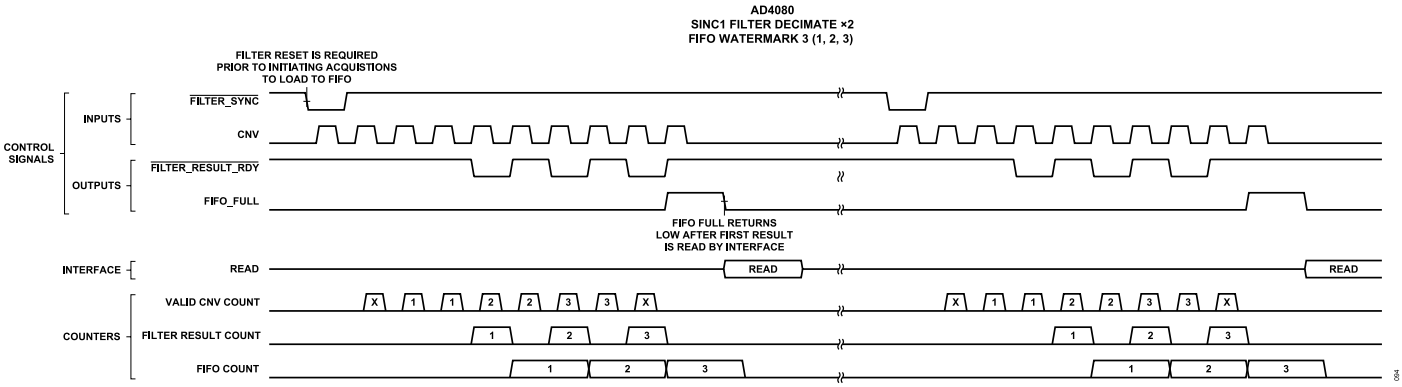

Figure 97. Description of Filter Timing with FIFO

DIGITAL FEATURES

Digital Filter Conversion Pulses

The total number of CNV pulses required for a single filter decimated result (sinc1 settling clocks) can be calculated using the following formula:

$$Settling\ CNV\ Pulses_{SINC1} = 2 + (D + 1)$$

Note that each of the three filter types has a unique formula to determine the number of clocks required.

For the sinc5 settling clocks, the equation is as follows:

$$Settling\ CNV\ Pulses_{SINC5} = 2 + (5 \times D + 4)$$

For the sinc5 with compensation settling clocks, the equation is as follows:

$$\text{Settling CNV Pulses}_{SINC5 + COMP} = 2 + (35\times\text{D}+10)$$

Where D equals the decimation rate 2, 4, 8 …

Digital Filtering Settling Time

The settling time for the selected filter is the number of settling clocks times t_{CONV}, as follows:

$$\text{Filter Settling Time} = (\text{Settling CNV Pulses}_{FILTERTYPE}) \times t_{CONV}$$

Digital Filtering Settling Time when Using FIFO

When using the FIFO with filtered data, it is important to note that each new FIFO record of results must begin by issuing a $\overline{\text{FILTER\_SYNC}}$ signal on the first CNV to reset and initialize the filter and to prevent unflushed data from being contained in the first FIFO record result.

The minimum total number of conversion pulses required to fill a full FIFO record can be calculated as follows:

$$\text{Total Required CNVs} = (\ \text{D}\times\text{WATERMARK}\ ) + \text{Settling CNV Pulses}_{\text{FILTERTYPE}}$$

Where D equals the decimation rate 2, 4, 8 …

Digital Filter Response

Sinc1 Filter

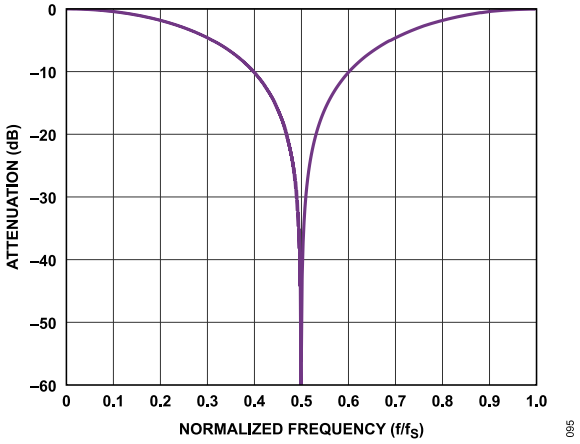

Figure 98. Sinc1 Filter Response, Decimate by 2

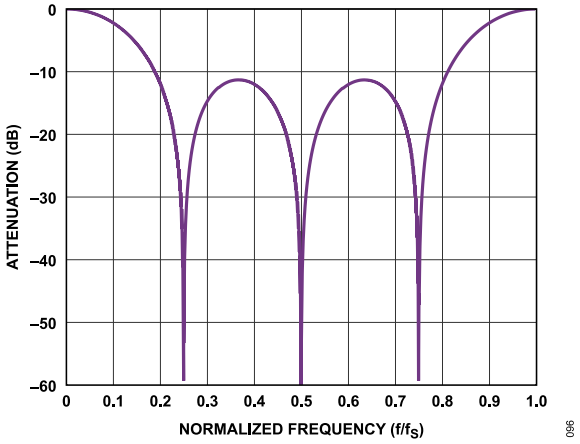

Figure 99. Sinc1 Filter Response, Decimate by 4

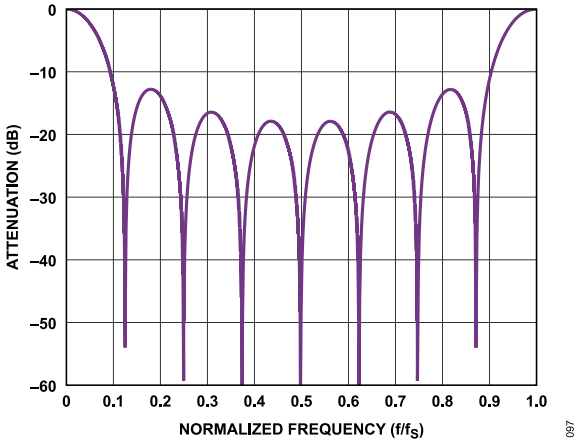

Figure 100. Sinc1 Filter Response, Decimate by 8

DIGITAL FEATURES

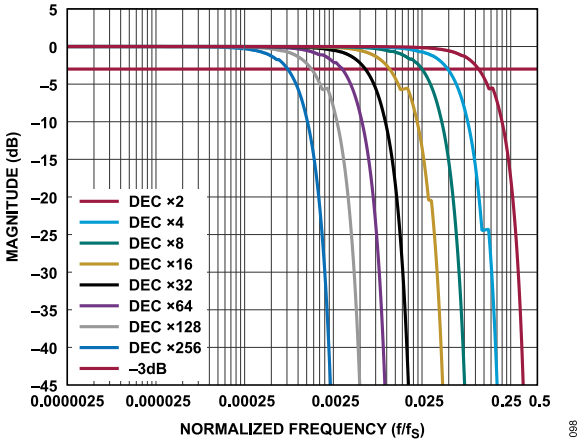

Figure 101. Sinc1 Filter Response, All Decimation Rates

Sinc5 Filter

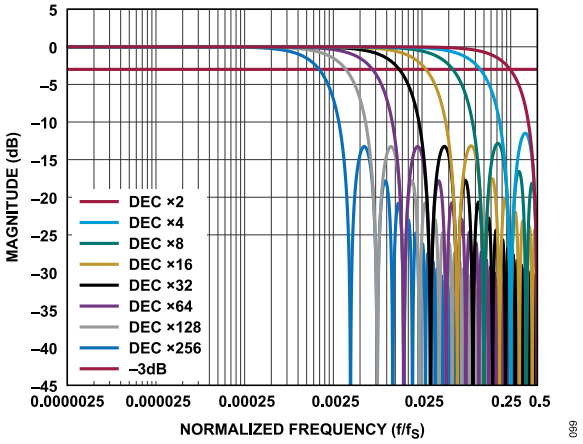

Figure 102. Sinc5 Filter Response, All Decimation Rates

Filter Sinc5 + Compensation Filter

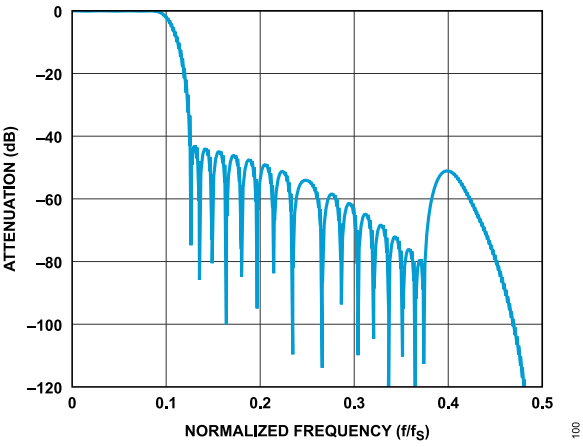

Figure 103. Sinc5 + Compensation Filter Response, Decimate by 2

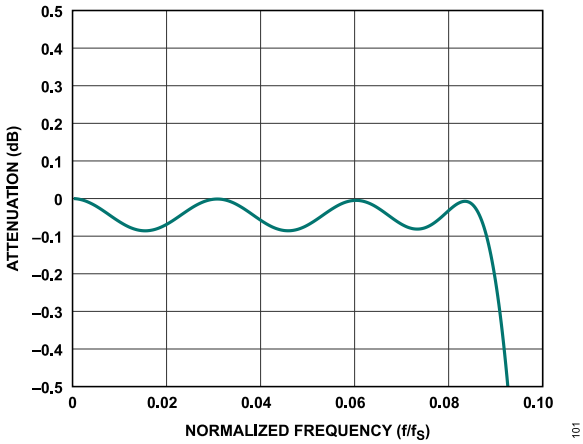

Figure 104. Sinc5 + Compensation Filter Response, Decimate by 2, Pass-Band Ripple

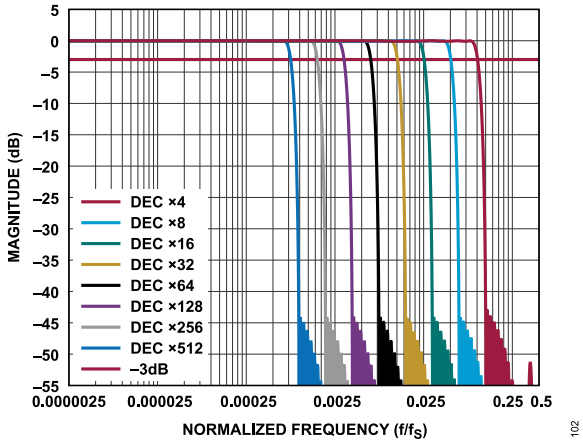

Figure 105. Sinc5 + Compensation Filter Response

DIGITAL FEATURES

SYSTEM ERROR CORRECTION COEFFICIENTS

Systematic gain and offset errors exist in all practical data acquisition circuits, and thus, the need for correction is essential to maximize the precision of the measurement channel. While these quantities can be corrected for in the host processor, implementation can be inefficient and consume more power than if integrated within the data converter. To minimize these challenges for the end user, the AD4080 has integrated both gain and offset correction on a per sample basis.

To describe the available error corrections, consider that the transfer function of an ideal ADC can be described by the straight line equation.

$$y = mx + c \quad (2)$$

This equation can be applied to the ADC transfer function where:
y is the corrected ADC result.
m is the gain or slope of the line.
x is the uncorrected ADC result.
c is the offset.

The gain or slop of the line can be described as follows:

$$m = (y2 - y1)/(x2 - x1)$$

where the following are in volts:
y2 is the input voltage at close to the positive full-scale input.
y1 is the input voltage at close to the negative full-scale input.
x2 is the converted voltage with the y2 voltage applied at the input.
x1 is the converted voltage with the y1 voltage applied at the input.

The ideal slope or gain is m = 1 V/V

The system error correction coefficients in the Offset Error Correction and Gain Error Correction sections detail how signal chain errors in offset (c) and gain (m) can be corrected using the configuration registers of the AD4080.

Offset Error Correction

The AD4080 is factory calibrated to give low zero error. To account for system offset errors that may be present in a users application signal chain, an offset error correction function was included, which allows users to correct for system offsets in their application by applying a code to the OFFSET bit field in the offset Register at Address 0x24 and Address 0x25, Bits[11:0]. This bit field is a 12-bit value in a twos compliment data format.

The bit field is a 12-bit value in a twos compliment data format and OFFSET LSB represents the value of the ADC LSB as defined in the Transfer Function section. The range of offset error correction is therefore defined as −2048 × LSB (0x800) to +2047 × LSB (0x7FF). This represents a voltage range of ±11.71 mV for the specified V_{REFIN} = 3.0 V. The default value for this register, after power on, or after a software reset, is 0x000, which represents the zero offset correction applied.

Gain Error Correction

The AD4080 is a high precision ADC with factory calibrated, gain error correction. To allow a user to correct for any signal chain gain error within their application, the GAIN register (see the Gain Correction Register, Address 0x27 and Address 0x28) can be used. The GAIN bit field is a 10-bit value that allows a nominal gain error correction of ±1.5594% of full scale. The 10-bit register is coded in a straight binary data format, where the default value after power on, or software reset, is 0x200. This value represents no gain error correction being applied to the ADC results.

With the GAIN register first set to the default 0x200 value, the user can perform a two-point voltage measurement, preferably close to positive and negative full-scale inputs, and use the slope or gain equation in the System Error Correction Coefficients section to determine their system gain error. This system error can then be adjusted with a resolution of 1.5594%/512 = 0.00305%. The required correction calculated can be input to the GAIN register.

LAYOUT GUIDELINES

The AD4080 includes all critical bypass capacitors within the device package, which greatly reduces the layout challenge for a precision, high-speed converter. These integrated capacitors are optimally placed within the device package to ensure that maximum performance is easily obtained. However, as with any precision mixed signal device, care must be taken in system device placement to ensure that there is proper partitioning of the critical analog signal chain component routing and routing of the high-speed digital signals to prevent unwanted coupling effects.

Note the following layout considerations:

- The AD4080 contains internal decoupling on all power supplies, AVDD33 (0.47 µF), VDD11 (1.88 µF), VIO11 (0.22 µF), as well as VDDLDO (0.22 µF). Therefore, no external bypass capacitors are required, saving board space and reducing bill of material (BOM) count and sensitivity.
- Ensure good partitioning of analog and digital domain signals within the design by, for example, having all analog signals in from the left-hand side and keeping dynamic digital signals on the right-hand side.
- Have a solid ground plane under the AD4080 and connect all analog ground (GND) pins, reference ground (REFGND), and digital ground (IOGND) pins to this shared plane.
- Recommended connections of ground (GND), reference ground (REFGND), and digital ground (IOGND) connections are shown in Figure 106. It is recommended to not keep the current return path of the reference IC in the same current loop as the current return loop from the other circuitry on the PCB. Connect the reference local star point to the ADC star point ground on the top layer of the PCB as shown in Figure 106.
- See Figure 107 for the side view cross-section of the PCB board showing the ground planes distribution . Note that Figure 107 only shows the ground planes but does not including the signal tracks.

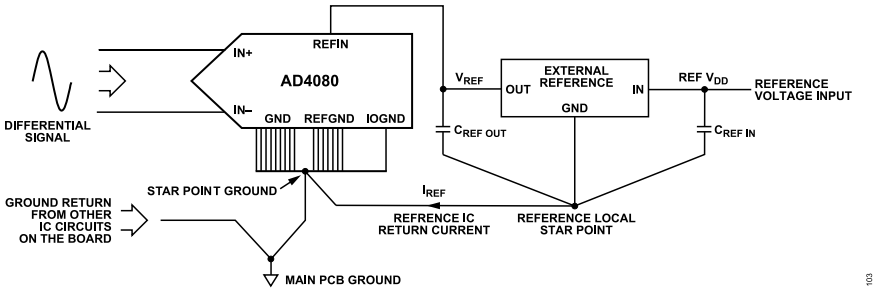

Figure 106. AD4080 External Reference Ground Connections

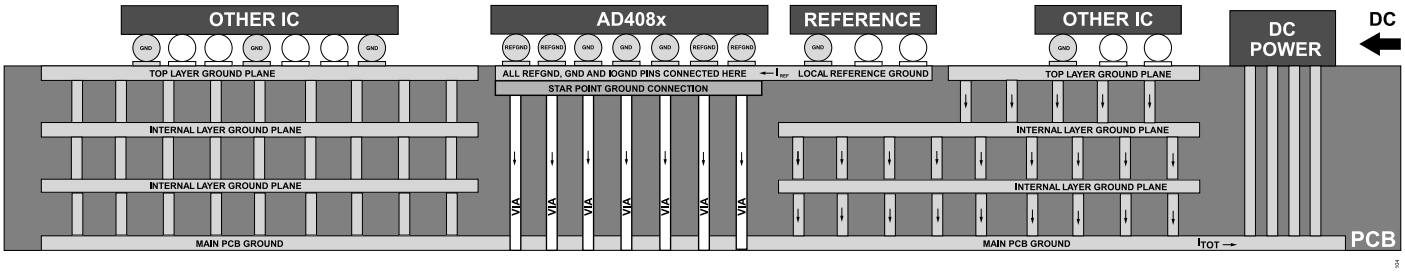

Figure 107. Recommended PCB Ground Planes Layout

CONFIGURATION REGISTERS

The features of the AD4080 family have been designed to simplify the application of low latency data capture to a broad array of measurement applications. This simplification is achieved through customization of the data interface, data path, and data access method to satisfy both measurement and the host processor interface requirements via the available configuration registers.

The register space was organized in contiguous regions by function to streamline device configuration as described in Table 30. As a result, the interface streaming functions (see Instruction Mode Selection) can be leveraged to simplify device configuration to a single SPI frame consisting of an instruction word and associated data. For most applications, modifications to the register space address range of Address 0x15 to Address 0x29 are sufficient. Modification of content in the configuration interface and product ID space (Address 0x00 to Address 0x11) is only necessary to initiate a software reset or to change the configuration access method. Note that changes to the configuration access method are outside the scope of this document. For assistance with these options, contact your local Analog Devices sales representative or submit a request for technical assistance through the **Precision ADCs** page on the *ADI Engineer Zone* at https://ez.analog.com/data_converters/precision_adcs/.

Table 30. Register Map Organization

Address Range	Function
0x00 to 0x11	Configuration interface and Product ID
0x14	Device status
0x15 to 0x17	Interface configuration
0x18 to 0x1B	Power and GPIO configuration
0x1C	General configuration
0x1C to 0x1E	FIFO configuration
0x1F to 0x24	Internal event detection
0x25 to 0x28	System error correction
0x29	Digital filter configuration

Table 31. Configuration Register Summary—Configuration Interface Functions (Address 0x00 to Address 0x11)

Addr	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	INTERFACE_CONFIG_A	[7:0]	SW_RESET	RESERVED	ADDR_ASCENSION	SDO_ENABLE	RESERVED			SW_RESETX	0x10	R/W
0x01	INTERFACE_CONFIG_B	[7:0]	SINGLE_INST	RESERVED			SHORT_INSTRUCTION	RESERVED			0x00	R/W
0x02	DEVICE_CONFIG	[7:0]	RESERVED						OPERATING_MODES		0x00	R/W
0x03	CHIP_TYPE	[7:0]	RESERVED				CHIP_TYPE				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x00	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x02	R
0x0A	SCRATCH_PAD	[7:0]	SCRATCH_VALUE								0x00	R/W
0x0B	SPI_REVISION	[7:0]	SPI_TYPE		VERSION						0x83	R
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x0E	STREAM_MODE	[7:0]	LOOP_COUNT								0x00	R/W
0x0F	TRANSFER_CONFIG	[7:0]	RESERVED					KEEP_STREAM_LENGTH_VAL	RESERVED		0x00	R/W
0x10	INTERFACE_CONFIG_C	[7:0]	CRC_ENABLE		STRICT_REGISTER_	SEND_STATUS	ACTIVE_INTERFACE_MODE		CRC_ENABLEB		0x23	R/W

CONFIGURATION REGISTERS

Table 31. Configuration Register Summary—Configuration Interface Functions (Address 0x00 to Address 0x11) (Continued)

Addr	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
					ACCESS							
0x11	INTERFACE_STATUS_A	[7:0]	NOT_READY_ERR	RESERVED		CLOCK_COUNT_ERR	CRC_ERR	WR_TO_RD_ONLY_REG_ERR	REGISTER_PARTIAL_ACCESS_ERR	ADDRESS_INVALID_ERR	0x00	R/W
0x14	DEVICE_STATUS	[7:0]	FIFO_FULL	FIFO_READ_DONE	HI_STATUS	LO_STATUS	POR_ANA_FLAG	ADC_CNV_ERR	ROM_CRC_ERR	POR_FLAG	0x09	R/W
0x15	ADC_DATA_INTF_CONFIG_A	[7:0]	RESERVED	RESERVED	RESERVED	INTF_CHK_EN	RESERVED	SPI_LVDS_LANES	RESERVED	DATA_INTF_MODE	0x40	R/W
0x16	ADC_DATA_INTF_CONFIG_B	[7:0]	LVDS_CNV_CLK_CNT				LVDS_SELF_CLK_MODE	LVDS_MNC_EN	RESERVED	LVDS_CNV_EN	0x00	R/W
0x17	ADC_DATA_INTF_CONFIG_C	[7:0]	LVDS_RX_CURRENT	LVDS_VOD			RESERVED				0x20	R/W
0x18	PWR_CTRL	[7:0]	RESERVED						ANA_DIG_LDO_PD	INTF_LDO_PD	0x00	R/W
0x19	GPIO_CONFIG_A	[7:0]	GPIO_3_DATA	GPIO_2_DATA	GPIO_1_DATA	GPIO_0_DATA	GPO_3_EN	GPO_2_EN	GPO_1_EN	GPO_0_EN	0x01	R/W
0x1A	GPIO_CONFIG_B	[7:0]	GPIO_1_SEL				GPIO_0_SEL				0x00	R/W
0x1B	GPIO_CONFIG_C	[7:0]	GPIO_3_SEL				GPIO_2_SEL				0x00	R/W
0x1C	GENERAL_CONFIG	[7:0]	INT_EVENT_EN	HI_ROUTE	LO_ROUTE	ADC_CNV_ERR_ROUTE	RESERVED		FIFO_MODE		0x00	R/W
0x1D	FIFO_WATERMARK	[7:0]	FIFO_WATERMARK[7:0]								0x00	R/W
0x1E		[15:8]	RESERVED	FIFO_WATERMARK[14:8]							0x40	R/W
0x1F	EVENT_HYSTERESIS	[7:0]	HYSTERESIS[7:0]								0x00	R/W
0x20		[15:8]	RESERVED					HYSTERESIS[10:8]			0x00	R/W
0x21	EVENT_DETECTION_HI	[7:0]	HI_THRESHOLD[7:0]								0x00	R/W
0x22		[15:8]	RESERVED				HI_THRESHOLD[11:8]				0x00	R/W
0x23	EVENT_DETECTION_LO	[7:0]	LO_THRESHOLD[7:0]								0x00	R/W
0x24		[15:8]	RESERVED				LO_THRESHOLD[11:8]				0x00	R/W
0x25	OFFSET	[7:0]	OFFSET[7:0]								0x00	R/W
0x26		[15:8]	RESERVED				OFFSET[11:8]				0x00	R/W
0x27	GAIN	[7:0]	GAIN[7:0]								0x00	R/W
0x28		[15:8]	RESERVED						GAIN[9:8]		0x02	R/W
0x29	FILTER_CONFIG	[7:0]	RESERVED	SINC_DEC_RATE				RESERVED	FILTER_SEL		0x00	R/W

CONFIGURATION REGISTERS

REGISTER DETAILS

Interface Configuration A Register

Address: 0x00, Reset: 0x10, Name: INTERFACE_CONFIG_A

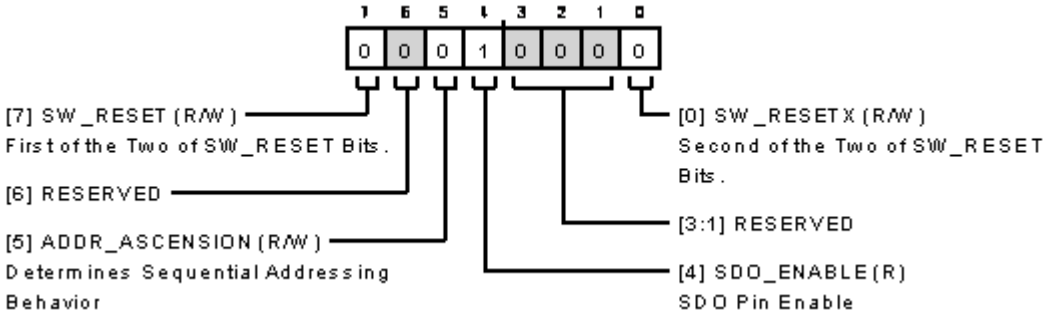

Figure 108. Interface Configuration A Settings

Table 32. Bit Descriptions for INTERFACE_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RESET	First of the Two SW_RESET Bits. This bit appears in two locations in this register. Both locations must be written to at the same time to trigger a software reset of the device. This action returns any previously configured registers to their default settings, except for the ADDR_ASCENSION bit from the Interface Configuration A Register, which keeps its previous value. Only use this reset method once the ADC is in an idle state, where conversions are not being clocked, and any existing conversions are completed.	0x0	R/W
6	RESERVED	Reserved. Write 0 to this bit.	0x0	R
5	ADDR_ASCENSION	Determines Sequential Addressing Behavior. 0: Address is decremented by one when streaming. 1: Address is Incremented by one when streaming.	0x0	R/W
4	SDO_ENABLE	SDO Pin Enable.	0x1	R
[3:1]	RESERVED	Reserved. Write 000 to these bits.	0x0	R
0	SW_RESETX	Second of the Two SW_RESET Bits. This bit appears in two locations in this register. Both locations must be written to at the same time to trigger a software reset of the device. This action returns any previously configured registers to their default settings, except for the ADDR_ASCENSION bitd from the Interface Configuration A Register, which keeps its previous value. Only use this reset method once the ADC is in an idle state, where conversions are not being clocked, and any existing conversion are completed.	0x0	R/W

CONFIGURATION REGISTERS

Interface Configuration B Register

Address: 0x01, Reset: 0x00, Name: INTERFACE_CONFIG_B

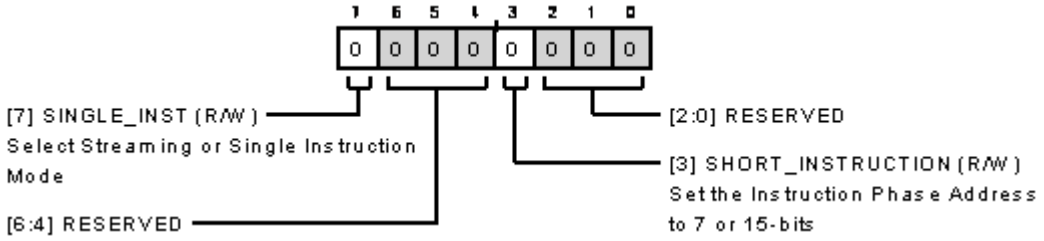

Figure 109. Additional Interface Configuration B Settings

Table 33. Bit Descriptions for INTERFACE_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INST	Select Streaming or Single Instruction Mode. 0: Streaming mode is enabled. The address increments or decrements as successive data bytes are received. 1: Single instruction mode is enabled.	0x0	R/W
[6:4]	RESERVED	Reserved. Write 0b000 to these bits.	0x0	R
3	SHORT_INSTRUCTION	Set the Instruction Phase Address to 7 or 15 bits. 0: 15-Bit Addressing. 1: 7-Bit Addressing.	0x0	R/W
[2:0]	RESERVED	Reserved. Write 0b000 to these bits.	0x0	R

Device Configuration Register

Address: 0x02, Reset: 0x00, Name: DEVICE_CONFIG

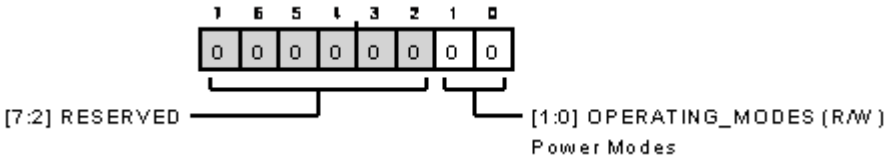

Figure 110. Device Configuration Register

Table 34. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved. Write 0b000000 to these bits.	0x0	R
[1:0]	OPERATING_MODES	Power Modes. 00: Normal Operating Mode. 10: Standby Operating Mode. 11: Sleep Mode.	0x0	R/W

CONFIGURATION REGISTERS

Chip Type Register

Address: 0x03, Reset: 0x07, Name: CHIP_TYPE

The chip type is used to identify the family of Analog Devices devices a given device belongs to. CHIP_TYPE must be used in conjunction with the Product ID to uniquely identify a given product.

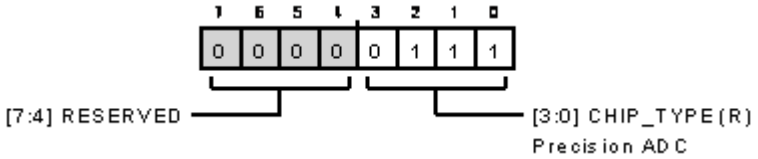

Figure 111. Chip Type Register

Table 35. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Precision ADC.	0x7	R

Product ID Low Register

Address: 0x04, Reset: 0x00, Name: PRODUCT_ID_L

This register is the low byte of the Product ID.

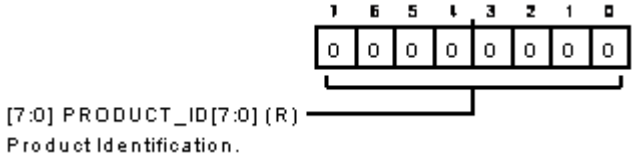

Figure 112. Product ID Low Register

Table 36. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product Identification. These bits are the device chip type/family. The PRODUCT_ID must be used in conjunction with CHIP_TYPE to identify a product.	0x1	R

CONFIGURATION REGISTERS

Product ID High Register

Address: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

This register is the high byte of the Product ID.

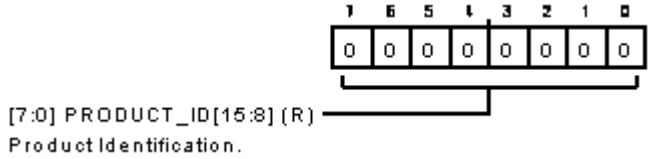

Figure 113. Product ID High Register

Table 37. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product Identification. These bits are the device chip type and family. The PRODUCT_ID must be used in conjunction with CHIP_TYPE to identify a product.	0x0	R

Chip Grade Register

Address: 0x06, Reset: 0x02, Name: CHIP_GRADE

This register identifies product variations and device revisions.

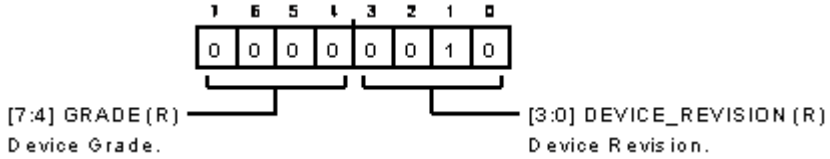

Figure 114. Chip Grade Register

Table 38. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	GRADE	Device Grade. These bits are the device performance grade.	0x0	R
[3:0]	DEVICE_REVISION	Device Revision. These bits are the device hardware revision.	0x2	R

Scratch Pad Register

Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

This register can be used to test writes and reads.

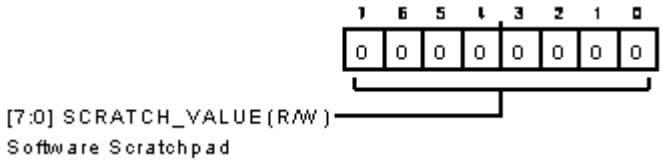

Figure 115. Scratch Pad Register

Table 39. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_VALUE	Software Scratchpad. Software can write to and read from this location without any device side effects.	0x0	R/W

CONFIGURATION REGISTERS

SPI Revision Register

Address: 0x0B, Reset: 0x83, Name: SPI_REVISION

This register indicates the SPI revision.

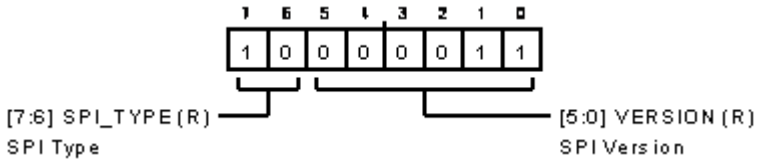

Figure 116. SPI Revision Register

Table 40. Bit Descriptions for SPI_REVISION

Bits	Bit Name	Description	Reset	Access
[7:6]	SPI_TYPE	SPI Type. These bits always read as 0x2.	0x2	R
[5:0]	VERSION	SPI Version. 11: Revision 1.1.	0x3	R

Vendor ID Low Register

Address: 0x0C, Reset: 0x56, Name: VENDOR_L

This register is the low byte of the Vendor ID.

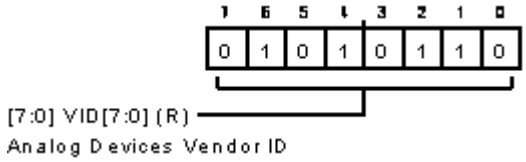

Figure 117. Vendor ID Low Register

Table 41. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Analog Devices Vendor ID.	0x56	R

Vendor ID High Register

Address: 0x0D, Reset: 0x04, Name: VENDOR_H

This register is the high byte of the Vendor ID.

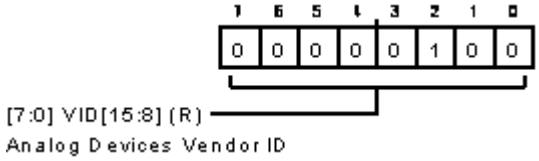

Figure 118. Vendor ID High Register

Table 42. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Analog Devices Vendor ID.	0x4	R

CONFIGURATION REGISTERS

Stream Mode Register

Address: 0x0E, Reset: 0x00, Name: STREAM_MODE

This mode is not supported.

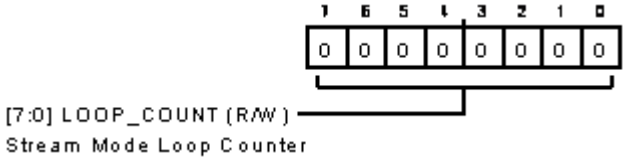

Figure 119. Stream Mode Register

Table 43. Bit Descriptions for STREAM_MODE

Bits	Bit Name	Description	Reset	Access
[7:0]	LOOP_COUNT	Stream Mode Loop Counter. These bits set the data byte count before looping to the start address. When streaming data, a nonzero value sets the number of data bytes written before the address loops back to the start address. A maximum of 255 bytes can be written using this approach. A value of 0x00 disables the loop back so that addressing wraps around at the upper and lower limits of the memory. After writing to this register, the loop value applies only to the next SPI instruction and auto clears upon the end of that instruction.	0x0	R/W

Transfer Configuration Register

Address: 0x0F, Reset: 0x00, Name: TRANSFER_CONFIG

This register controls how data moves between the controller and the target registers.

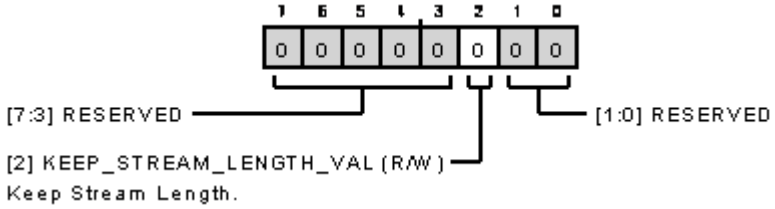

Figure 120. Transfer Configuration Register

Table 44. Bit Descriptions for TRANSFER_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved. Write 0b00000 to these bits.	0x0	R
2	KEEP_STREAM_LENGTH_VAL	Keep Stream Length. When set, the loop counter does not reset on the $\overline{CS}$ rising edge.	0x0	R/W
[1:0]	RESERVED	Reserved. Write 0b00 to these bits.	0x0	R

CONFIGURATION REGISTERS

Interface Configuration C Register

Address: 0x10, Reset: 0x23, Name: INTERFACE_CONFIG_C

This register contains additional interface configuration settings.

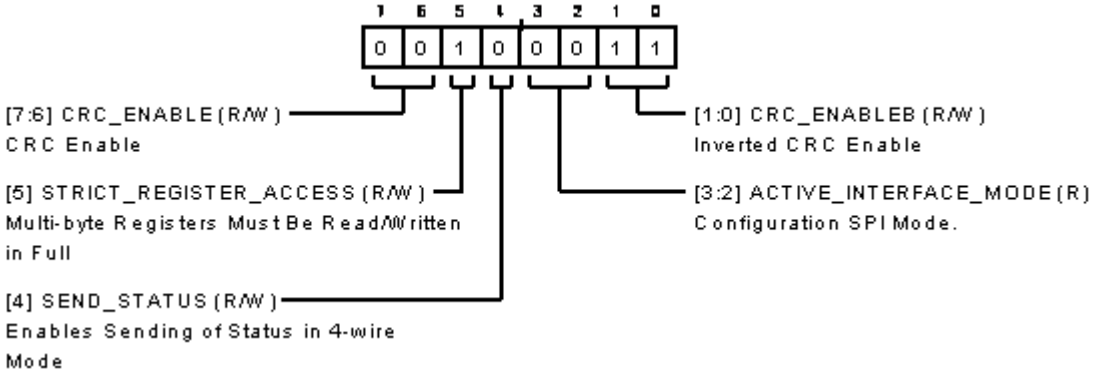

Figure 121. Interface Configuration C Register

Table 45. Bit Descriptions for INTERFACE_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:6]	CRC_ENABLE	CRC Enable. These bits are written to enable or disable the use of CRC on the interface. The $\overline{\text{CRC\_ENABLE}}$ bits must also be written to with the inverted value of these bits for the CRC to be enabled. 0: CRC Disabled. 1: CRC Enabled.	0x0	R/W
5	STRICT_REGISTER_ACCESS	Multibyte Registers Must Be Read/Written in Full. When this mode is enabled, all bytes of a multibyte register must be read/written in full. 0: Normal Mode. No access restrictions. 1: Strict Mode. Multibyte registers require all bytes accessed.	0x1	R/W
4	SEND_STATUS	Enables Sending of Status in 4-Wire Mode. When set, status information is sent by the device on SDO during the instruction phase. When clear, no status is sent during the instruction phase.	0x0	R/W
[3:2]	ACTIVE_INTERFACE_MODE	Configuration SPI Mode. These bits are the active mode the SPI operates in.	0x0	R
[1:0]	$\overline{\text{CRC\_ENABLE}}$	Inverted CRC Enable. These bits must be written to with the inverted value of the CRC_ENABLE.	0x3	R/W

CONFIGURATION REGISTERS

Interface Status A Register

Address: 0x11, Reset: 0x00, Name: INTERFACE_STATUS_A

Status bits are set to 1 to indicate an active condition. These bits can be cleared by writing a 1 to the corresponding bit location.

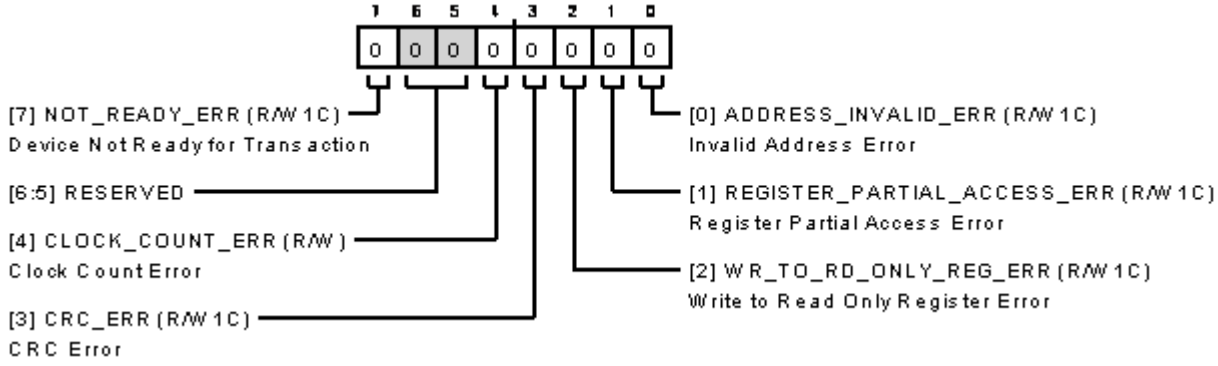

Figure 122. Interface Status A Register

Table 46. Bit Descriptions for INTERFACE_STATUS_A

Bits	Bit Name	Description	Reset	Access
7	NOT_READY_ERR	Device Not Ready for Transaction. This bit is set if the user attempts to execute an SPI transaction before the completion of digital initialization.	0x0	R/W1C
[6:5]	RESERVED	Reserved. Write 0b00 to these bits.	0x0	R
4	CLOCK_COUNT_ERR	Clock Count Error. This bit is set when an incorrect number of clocks is detected in a transaction.	0x0	R/W1C
3	CRC_ERR	CRC Error. This bit is set when the SPI controller does not send a CRC or when the CRC value calculated by the device does not match the value sent by the SPI controller.	0x0	R/W1C
2	WR_TO_RD_ONLY_REG_ERR	Write to Read Only Register Error. This bit is set when the user attempts a write to a register that is read only.	0x0	R/W1C
1	REGISTER_PARTIAL_ACCESS_ERR	Register Partial Access Error. This bit is set when a fewer than expected number of bytes are read from or written to in a multibyte register access. This bit is only valid when strict register access is enabled.	0x0	R/W1C
0	ADDRESS_INVALID_ERR	Invalid Address Error. This bit is set when the user tries to read from or write to a register address outside of the allowed memory map space.	0x0	R/W1C

CONFIGURATION REGISTERS

Device Status Register

Address: 0x14, Reset: 0x09, Name: DEVICE_STATUS

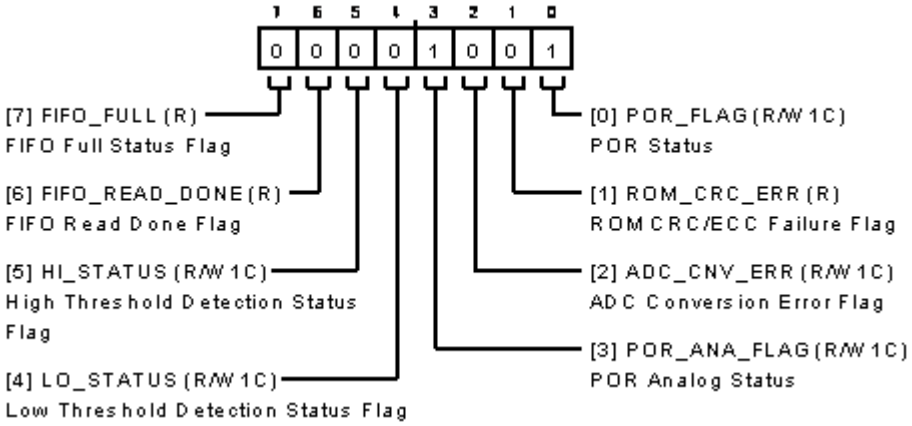

Figure 123. Device Status Register

Table 47. Bit Descriptions for DEVICE_STATUS

Bits	Bit Name	Description	Reset	Access
7	FIFO_FULL	FIFO Full Status Flag. 0: FIFO Not Full. 1: FIFO Full.	0x0	R
6	FIFO_READ_DONE	FIFO Read Done Flag. 0: FIFO Read Not Done. 1: FIFO Read Done.	0x0	R
5	HI_STATUS	High Threshold Detection Status Flag. Writing 1 to this bit clears it. 0: High Threshold Event Not Detected. 1: High Threshold Event Detected.	0x0	R/W1C
4	LO_STATUS	Low Threshold Detection Status Flag. Writing 1 to this bit clears it. 0: Low Threshold Event Not Detected. 1: Low Threshold Event Detected.	0x0	R/W1C
3	POR_ANA_FLAG	POR Analog Status. Allows user to detect when an analog POR event occurs. An analog POR is triggered at power-up or when the 1.1 V logic supply or ADC reference drops to less than the 2.7 threshold values or when the user issues a software reset. Writing 1 to this bit clears it. 0: Analog POR Flag Cleared. 1: Analog POR Event Detected.	0x1	R/W1C
2	ADC_CNV_ERR	ADC Conversion Error Flag. Writing 1 to this bit clears it. 0: ADC Conversion Okay. 1: ADC Conversion Error. The user has breached the minimum t_{CONV} specification, and the conversion results are invalid. The user must ensure that the correct clock timing specifications are met.	0x0	R/W1C
1	ROM_CRC_ERR	ROM CRC/ECC Failure Flag. 0: ROM CRC Check Okay. 1: ROM CRC/ECC Failure.	0x0	R
0	POR_FLAG	POR Status. Allows user to detect when a POR event occurs. A POR is triggered at power-up or when the 1.1 V logic supply drops to less than the 0.93 V threshold value or when the user issues a software reset. Writing 1 to this bit clears it. 0: POR Flag Cleared. 1: POR Event Detected.	0x1	R/W1C

CONFIGURATION REGISTERS

ADC Data Interface Configuration A Register

Address: 0x15, Reset: 0x40, Name: ADC_DATA_INTF_CONFIG_A

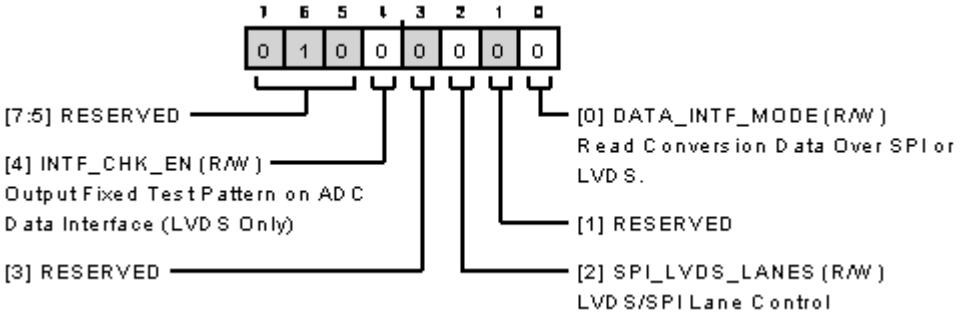

Figure 124. ADC Data Interface Configuration A Register

Table 48. Bit Descriptions for ADC_DATA_INTF_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
6	RESERVED	Reserved. Always set this bit to 1.	0x1	R/W
5	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
4	INTF_CHK_EN	Output Fixed Test Pattern on ADC Data Interface (LVDS Only). ADC output is not available when this mode is enabled. Fixed pattern = 20'b1010 1100 0101 1101 0110 (0xAC5D6). 0: Test Pattern Disabled. 1: Test Pattern Enabled.	0x0	R/W
3	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
2	SPI_LVDS_LANES	LVDS/SPI Lane Control. Determines the number of lanes that the ADC conversion data is clocked out on. 0: One Lane Active. 1: Multiple Lanes Active (Two for LVDS and Four for the SPI Data Interface).	0x0	R/W
1	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
0	DATA_INTF_MODE	Read Conversion Data Over SPI or LVDS. Acts as global LVDS enable, setting this bit to 1 powers down the LVDS transmitters/receivers. 0: Data Read Back Over LVDS. 1: Data Read Back Over SPI Data Interface ($\overline{DCS}$/DCLK). CLK+ is repurposed as the SPI data interface clock (DCLK) for reading FIFO data, and CLK− is repurposed as the SPI chip select ($\overline{DCS}$) for reading FIFO data.	0x0	R/W

CONFIGURATION REGISTERS

ADC Data Interface Configuration B Register

Address: 0x16, Reset: 0x00, Name: ADC_DATA_INTF_CONFIG_B

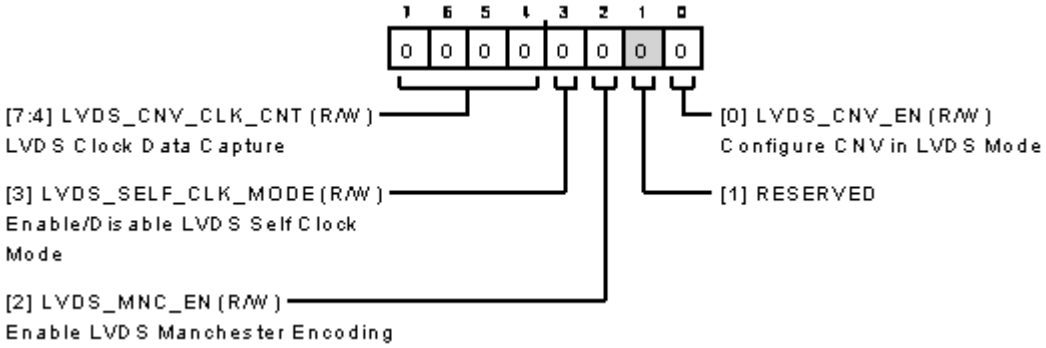

Figure 125. ADC Data Interface Configuration B Register

Table 49. Bit Descriptions for ADC_DATA_INTF_CONFIG_B

Bits	Bit Name	Description	Reset	Access
[7:4]	LVDS_CNV_CLK_CNT	LVDS Clock Data Capture. Determines the negative edge of the LVDS clock that the MSB of the conversion result is available in during conversion mode. Refer to the ADC Result Latency and LVDS Interface Alignment section of further information on setting this value.	0x0	R/W
3	LVDS_SELF_CLK_MODE	Enable/Disable LVDS Self Clock Mode. 0: Echo Clock Mode Enabled. LVDS DCO transmitter is powered up. 1: Self Clock Mode Enabled. LVDS DCO transmitter is powered down .	0x0	R/W
2	LVDS_MNC_EN	Enable LVDS Manchester Encoding. Manchester encoding is only applied for LVDS read during conversion mode in dual lane mode. This mode only operates with FILTER_SEL = 0, digital filter disabled. 0: Manchester Encoding Disabled. 1: Manchester Encoding Enabled.	0x0	R/W
1	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
0	LVDS_CNV_EN	Configure CNV in LVDS Mode. Only applicable when LVDS interface is selected. 0: CNV Pin Configured in CMOS Mode. 1: CNV Pin Configured in LVDS Mode.	0x0	R/W

ADC Data Interface Configuration C Register

Address: 0x17, Reset: 0x20, Name: ADC_DATA_INTF_CONFIG_C

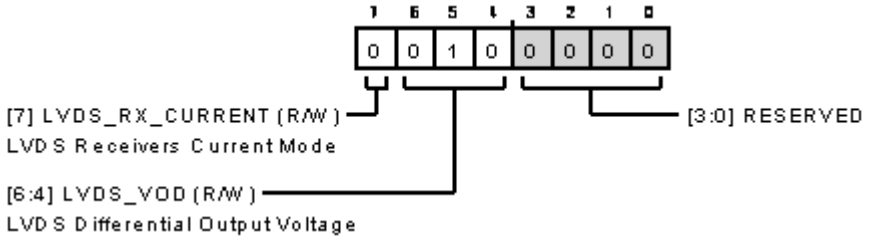

Figure 126. ADC Data Interface Configuration C Register

Table 50. Bit Descriptions for ADC_DATA_INTF_CONFIG_C

Bits	Bit Name	Description	Reset	Access
7	LVDS_RX_CURRENT	LVDS Receivers Current Mode. 1'b0 − 1× current. 1'b1 − 2x current.	0x0	R/W

CONFIGURATION REGISTERS

Table 50. Bit Descriptions for ADC_DATA_INTF_CONFIG_C (Continued)

Bits	Bit Name	Description	Reset	Access
[6:4]	LVDS_VOD	LVDS Differential Output Voltage. The valid entries are 0b001, 0b010, and 0b100 for the differential voltages of ~185 mV, ~240 mV, and ~325 mV, respectively. Writing an invalid value resets the differential voltage to its default setting of ~240 mV. However, user can read back the value written to these bits.	0x2	R/W
[3:0]	RESERVED	Reserved. Write 0b0000 to these bits.	0x0	R

Power Control Register

Address: 0x18, Reset: 0x00, Name: PWR_CTRL

It is not recommended to write to this register.

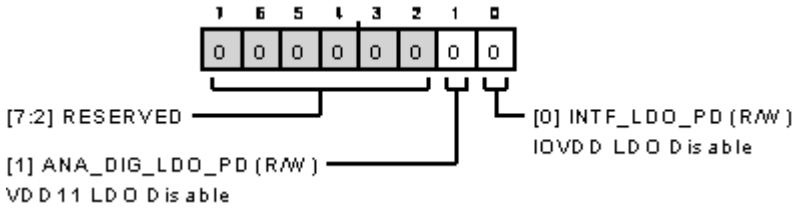

Figure 127. Power Control Register

Table 51. Bit Descriptions for PWR_CTRL

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved. Write 0b000000 to these bits.	0x0	R
1	ANA_DIG_LDO_PD	VDD11 LDO Disable. Enable or disable the LDO that powers the VDD11 rail. It is not recommended to write to this bit. 0: LDO Enabled. 1: LDO Disabled.	0x0	R/W
0	INTF_LDO_PD	IOVDD LDO Disable. Enable or disable the LDO that powers the IOVDD rail. It is not recommended to write to this bit. 0: LDO Enabled. 1: LDO Disabled.	0x0	R/W

CONFIGURATION REGISTERS

GPIO Configuration A Register

Address: 0x19, Reset: 0x01, Name: GPIO_CONFIG_A

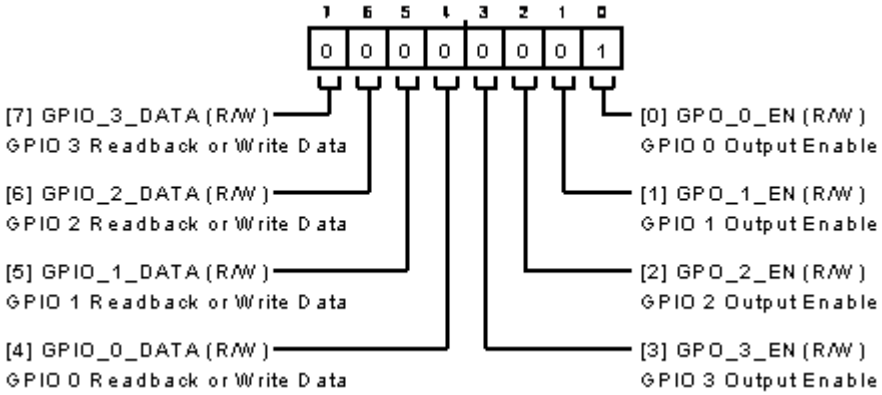

Figure 128. GPIO Configuration A Register

Table 52. Bit Descriptions for GPIO_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	GPIO_3_DATA	GPIO 3 Readback or Write Data. 0: Write 0 to GPIO 3. 1: Write 1 to GPIO 3.	0x0	R/W
6	GPIO_2_DATA	GPIO 2 Readback or Write Data. 0: Write 0 to GPIO 2. 1: Write 1 to GPIO 2.	0x0	R/W
5	GPIO_1_DATA	GPIO 1 Readback or Write Data. 0: Write 0 to GPIO 1. 1: Write 1 to GPIO 1.	0x0	R/W
4	GPIO_0_DATA	GPIO 0 Readback or Write Data. 0: Write 0 to GPIO 0. 1: Write 1 to GPIO 0.	0x0	R/W
3	GPO_3_EN	GPIO 3 Output Enable. 0: GPIO 3 Configured as an Input. 1: GPIO 3 Configured as an Output.	0x0	R/W
2	GPO_2_EN	GPIO 2 Output Enable. 0: GPIO 2 Configured as an Input. 1: GPIO 2 Configured as an Output.	0x0	R/W
1	GPO_1_EN	GPIO 1 Output Enable. 0: GPIO 1 Configured as an Input. 1: GPIO 1 Configured as an Output.	0x0	R/W
0	GPO_0_EN	GPIO 0 Output Enable. 0: GPIO 0 Configured as an Input. 1: GPIO 0 Configured as an Output.	0x1	R/W

CONFIGURATION REGISTERS

GPIO Configuration B Register

Address: 0x1A, Reset: 0x00, Name: GPIO_CONFIG_B

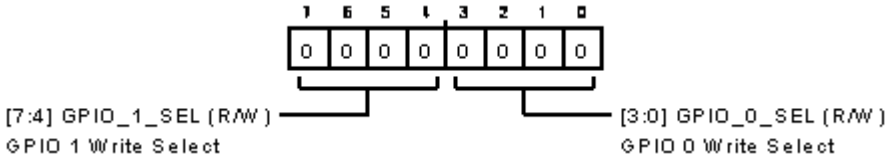

Figure 129. GPIO Configuration B Register

Table 53. Bit Descriptions for GPIO_CONFIG_B

Bits	Bit Name	Description	Reset	Access
[7:4]	GPIO_1_SEL	GPIO 1 Write Select. 0000: Configuration SPI SDO Data. 0001: FIFO Full Flag. 0010: FIFO Read Done Flag. 0011: Filter Result Ready (Active Low). 0100: High Threshold Detect. 0101: Low Threshold Detect. 0110: Status Alert (Active Low). 0111: GPIO Data. 1000: Filter Synchronization Input (Active Low). 1001: External Event Trigger Input for FIFO. 1010: Do not use this setting.	0x0	R/W
[3:0]	GPIO_0_SEL	GPIO 0 Write Select. 0000: Configuration SPI SDO Data. 0001: FIFO Full Flag. 0010: FIFO Read Done Flag. 0011: Filter Result Ready (Active Low). 0100: High Threshold Detect. 0101: Low Threshold Detect. 0110: Status Alert (Active Low). 0111: GPIO Data. 1000: Filter Synchronization Input (Active Low). 1001: External Event Trigger Input for FIFO. 1010: Do not use this setting.	0x0	R/W

CONFIGURATION REGISTERS

GPIO Configuration C Register

Address: 0x1B, Reset: 0x00, Name: GPIO_CONFIG_C

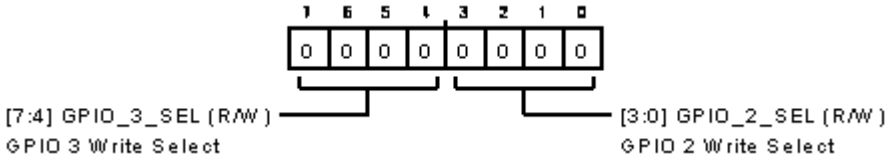

Figure 130. GPIO Configuration C Register

Table 54. Bit Descriptions for GPIO_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:4]	GPIO_3_SEL	GPIO 3 Write Select. 0000: Configuration SPI SDO Data. 0001: FIFO Full Flag. 0010: FIFO Read Done Flag. 0011: Filter Result Ready (Active Low). 0100: High Threshold Detect. 0101: Low Threshold Detect. 0110: Status Alert (Active Low). 0111: GPIO Data. 1000: Filter Synchronization Input (Active Low). 1001: External Event Trigger Input for FIFO. 1010: Do not use this setting.	0x0	R/W
[3:0]	GPIO_2_SEL	GPIO 2 Write Select. 0000: Configuration SPI SDO Data. 0001: FIFO Full Flag. 0010: FIFO Read Done Flag. 0011: Filter Result Ready (Active Low). 0100: High Threshold Detect. 0101: Low Threshold Detect. 0110: Status Alert (Active Low). 0111: GPIO Data. 1000: Filter Synchronization Input (Active Low). 1001: External Event Trigger Input for FIFO. 1010: Do not use this setting.	0x0	R/W

CONFIGURATION REGISTERS

General Configuration Register

Address: 0x1C, Reset: 0x00, Name: GENERAL_CONFIG

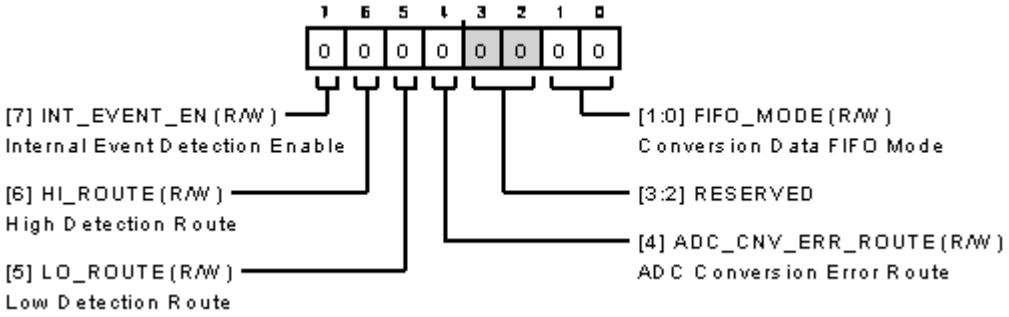

Figure 131. General Configuration Register

Table 55. Bit Descriptions for GENERAL_CONFIG

Bits	Bit Name	Description	Reset	Access
7	INT_EVENT_EN	Internal Event Detection Enable. ADC result or filtered data is only used for internal event detection after this bit is set to 1. 0: Internal event detection is disabled. 1: Internal event detection is enabled.	0x0	R/W
6	HI_ROUTE	High Detection Route. Allows high detection status to be used for FIFO event detection, status register, and alert function (via the GPIO). 0: Mask High Detection. 1: Route High Detection to Alert Pin, Status Register, and FIFO.	0x0	R/W
5	LO_ROUTE	Low Detection Route. Allows low detection status to be used for FIFO event detection, status register, and alert function (via the GPIO). 0: Mask Low Detection. 1: Route Low Detection to Alert Pin, Status Register, and FIFO.	0x0	R/W
4	ADC_CNV_ERR_ROUTE	ADC Conversion Error Route. Allows ADC conversion error status to be routed to the status register and alert function (via the GPIO). 0: Mask ADC Conversion Error. 1: Route ADC Conversion Error to Alert Pin and Status Register.	0x0	R/W
[3:2]	RESERVED	Reserved. Write 0b0 to these bits.	0x0	R
[1:0]	FIFO_MODE	Conversion Data FIFO Mode. 00: FIFO Disabled. 01: Immediate Trigger Mode. 10: Event Trigger Capture, Read Latest WATERMARK. 11: Event Trigger Capture Mode, Read All FIFO.	0x0	R/W

CONFIGURATION REGISTERS

FIFO Watermark Register

Address: 0x1D and Address: 0x1E, Reset: 0x4000, Name: FIFO_WATERMARK

In event trigger capture mode, read all FIFO, the FIFO event address can be read. Otherwise, it is the watermark value. If the user writes a value <1, it is clipped at 1. If >16,384, clipped at 16,384.

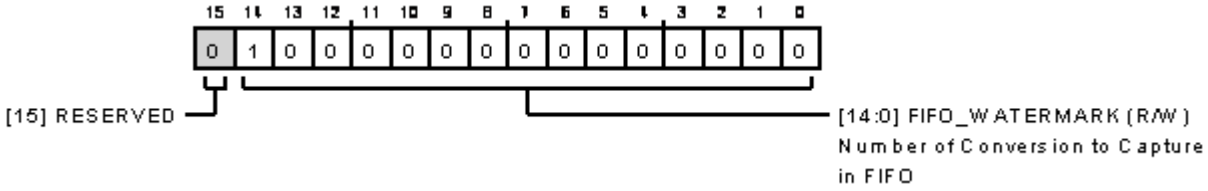

Figure 132. FIFO Watermark Register

Table 56. Bit Descriptions for FIFO_WATERMARK

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
[14:0]	FIFO_WATERMARK	Number of Conversion to Capture in FIFO. In event trigger capture mode, read all FIFO, this value must be set as a multiple of four only. In this mode, once a WATERMARK number of results have been written to the FIFO, these bits contain the location in the FIFO where the event occurred.	0x4000	R/W

Event Detection Hysteresis Configuration Register

Address: 0x20 and Address: 0x1F, Reset: 0x0000, Name: EVENT_HYSTERESIS

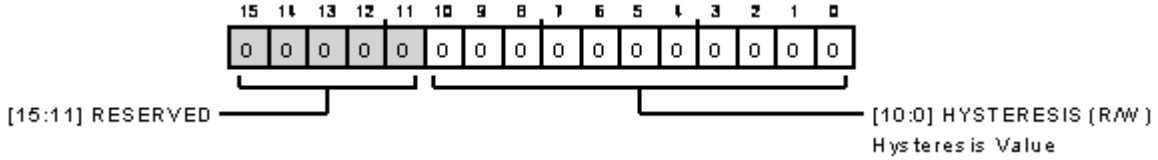

Figure 133. Event Detection Hysteresis Configuration Register

Table 57. Bit Descriptions for EVENT_HYSTERESIS

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved. Write 0b00000 to these bits.	0x0	R
[10:0]	HYSTERESIS	Hysteresis Value. Unsigned data format where LSB = 1.46484 mV. 0x000 represents 0 × LSB, and 0x7FF represents 2047 × LSB.	0x0	R/W

CONFIGURATION REGISTERS

Event Detection High Threshold Configuration Register

Address: 0x21 and Address: 0x22, Reset: 0x0000, Name: EVENT_DETECTION_HI

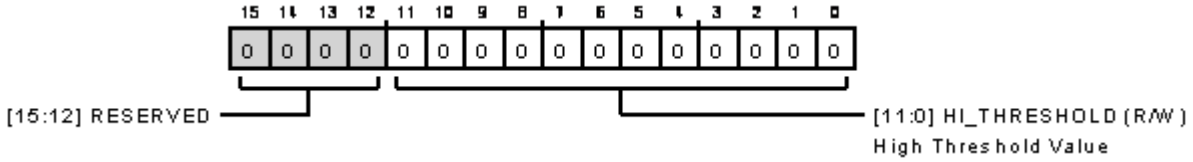

Figure 134. Event Detection High Threshold Configuration Register

Table 58. Bit Descriptions for EVENT_DETECTION_HI

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved. Write 0b0000 to these bits.	0x0	R
[11:0]	HI_THRESHOLD	High Threshold Value. Twos complement data format where LSB = 1.46484 mV. 0x800 represents −2048 × LSB, and 0x7FF represents +2047 × LSB.	0x0	R/W

Event Detection Low Threshold Configuration Register

Address: 0x23 and Address: 0x24, Reset: 0x0000, Name: EVENT_DETECTION_LO

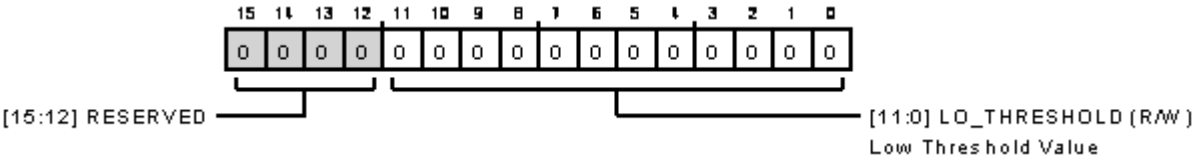

Figure 135. Event Detection Low Threshold Configuration Register

Table 59. Bit Descriptions for EVENT_DETECTION_LO

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved. Write 0b0000 to these bits.	0x0	R
[11:0]	LO_THRESHOLD	Low Threshold Value. Twos complement data format where LSB = 1.46484 mV. 0x800 represents −2048 × LSB, and 0x7FF represents +2047 × LSB.	0x0	R/W

Offset Correction Register

Address: 0x25 and Address: 0x26, Reset: 0x0000, Name: OFFSET

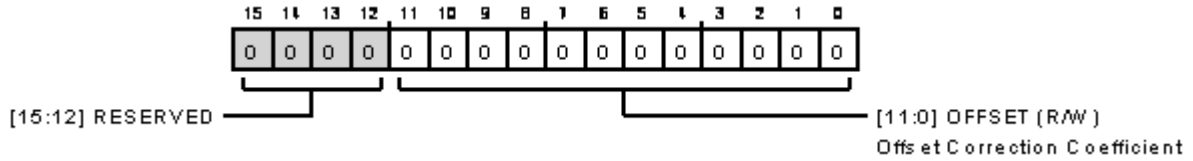

Figure 136. Offset Correction Register

Table 60. Bit Descriptions for OFFSET

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved. Write 0b0000 to this bit field.	0x0	R
[11:0]	OFFSET	Offset Correction Coefficient. Twos complement data format where LSB = 0.00572 mV. 0x800 represents −2048 × LSB, and 0x7FF represents +2047 × LSB.	0x0	R/W

CONFIGURATION REGISTERS

Gain Correction Register

Address: 0x27 and Address: 0x28, Reset: 0x0200, Name: GAIN

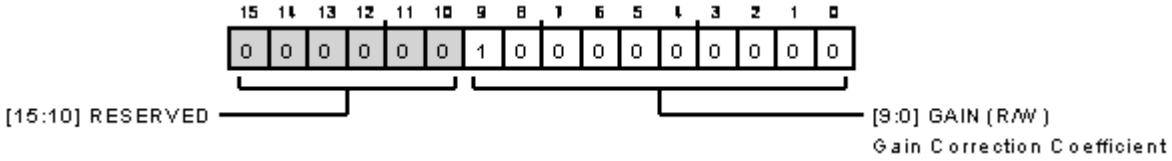

Figure 137. Gain Correction Register

Table 61. Bit Descriptions for GAIN

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved. Write 0b000000 to these bits.	0x0	R
[9:0]	GAIN	Gain Correction Coefficient. . GAIN = 0x3FF results in an overall system gain of 1.0 + 0.015594. GAIN = 0x200 disables the gain correction function and allows for lower latency operation. GAIN = 0x001 results in an overall system gain of 1.0 − 0.015594.	0x200	R/W

CONFIGURATION REGISTERS

Filter Configuration Register

Address: 0x29, Reset: 0x00, Name: FILTER_CONFIG

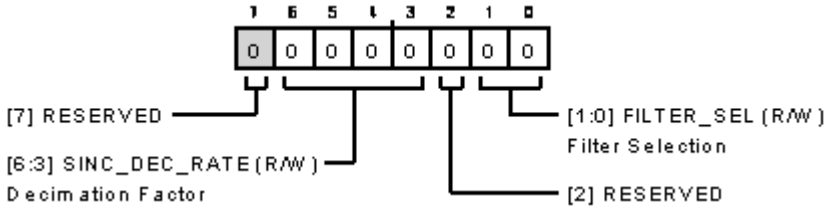

Figure 138. Filter Configuration Register

Table 62. Bit Descriptions for FILTER_CONFIG

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved. Write 0b0 to this bit field.	0x0	R
[6:3]	SINC_DEC_RATE	Decimation Factor. These bits set the Sinc Decimation Factor N. The filter compensation block incurs an additional 2× decimation. The total decimation for a selected filter is sinc1 = N, sinc5 = N, or sinc5 + compensation = N × 2. For a selected filter, setting invalid values, outside of those specified here, will set the filter at the maximum decimation rate 0000: N = 2. 0001: N = 4. 0010: N = 8. 0011: N = 16. 0100: N = 32. 0101: N = 64. 0110: N = 128. 0111: N = 256. 1000: N = 512 (sinc1 only). 1001: N = 1024 (sinc1 only).	0x0	R/W
2	RESERVED	Reserved.	0x0	R
[1:0]	FILTER_SEL	Filter Selection. To ensure the first filter result produces the correct data, when a user makes a change to the filter selection, a reset must be issued via the GPIO pin configured for filter synchronization ($\overline{\text{FILTER\_SYNC}}$). 00: Filter Disabled. 01: Sinc1 Filter Selected. 10: Sinc5 Filter Selected. 11: Sinc5 + Compensation Filter Selected.	0x0	R/W

OUTLINE DIMENSIONS

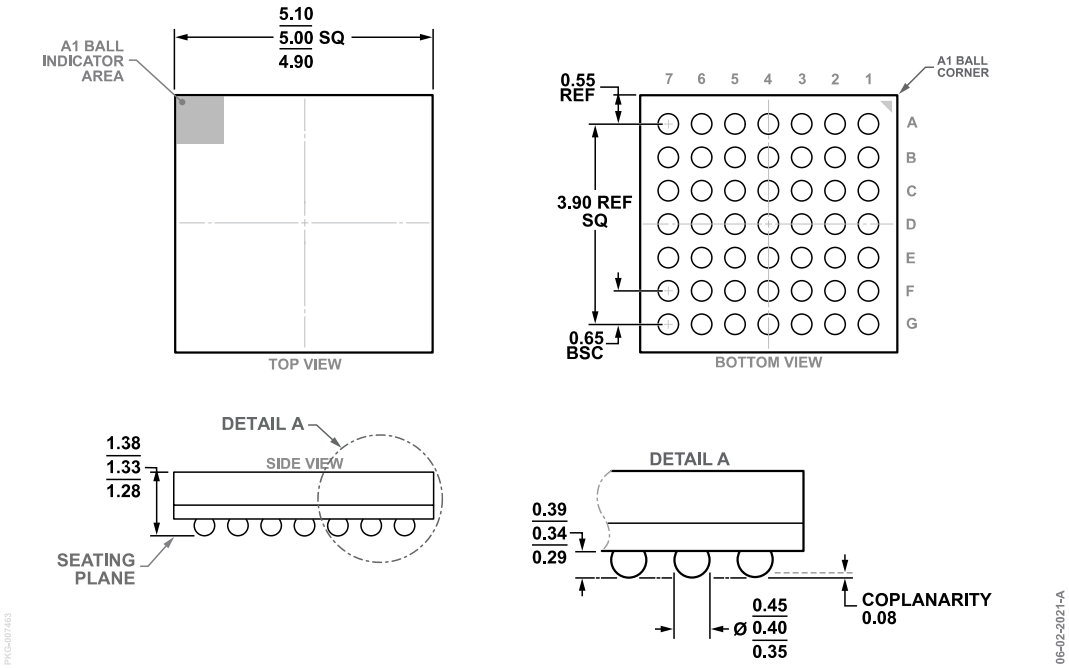

Figure 139. 49-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-49-8)
Dimensions shown in millimeters

Updated: February 29, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD4080BBCZ	−40°C to +85°C	CHIP SCALE BGA	Tray, 640	BC-49-8
AD4080BBCZ-RL	−40°C to +85°C	CHIP SCALE BGA	Reel, 4000	BC-49-8
AD4080BBCZ-RL7	−40°C to +85°C	CHIP SCALE BGA	Reel, 1000	BC-49-8

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 63. Evaluation Boards

Model[1]	Description
EVAL-AD4080-FMCZ	FMC Evaluation Board

[1] Z = RoHS-Compliant Part.