8-Channel, 12-Bit, Configurable ADC/DAC with On-Chip Reference, SPI Interface

Known Good Die

AD5592R-1-KGD

FEATURES

8-channel, configurable ADC/DAC/GPIO
Configurable as any combination of
- **8 × 12-bit DAC channels**
- **8 × 12-bit ADC channels**
- **8 × general-purpose digital input/output pins**

Integrated temperature sensor
SPI interface

APPLICATIONS

Control and monitoring
General-purpose analog and digital inputs/outputs

GENERAL DESCRIPTION

The AD5592R-1-KGD has eight I/Ox pins (I/O0 to I/O7) that can be independently configured as digital-to-analog converter (DAC) outputs, analog-to-digital converter (ADC) inputs, digital outputs, or digital inputs. When an I/Ox pin is configured as an analog output, it is driven by a 12-bit DAC. The output range of the DAC is 0 V to V_{REF} or 0 V to 2 × V_{REF}. When an I/Ox pin is configured as an analog input, it is connected to a 12-bit ADC via an analog multiplexer. The input range of the ADC is 0 V to V_{REF} or 0 V to 2 × V_{REF}. The ADC has a total throughput rate of 400 kSPS. The I/Ox pins can also be configured as digital, general-purpose input or output (GPIO) pins. The state of the GPIO pins can be set or read back by accessing the GPIO write data register or the GPIO read configuration register, respectively, via a serial peripheral interface (SPI) write or read operation.

Additional application and technical information can be found in the AD5592R data sheet.

Known good die (KGD): these die are fully guaranteed to data sheet specifications.

FUNCTIONAL BLOCK DIAGRAM

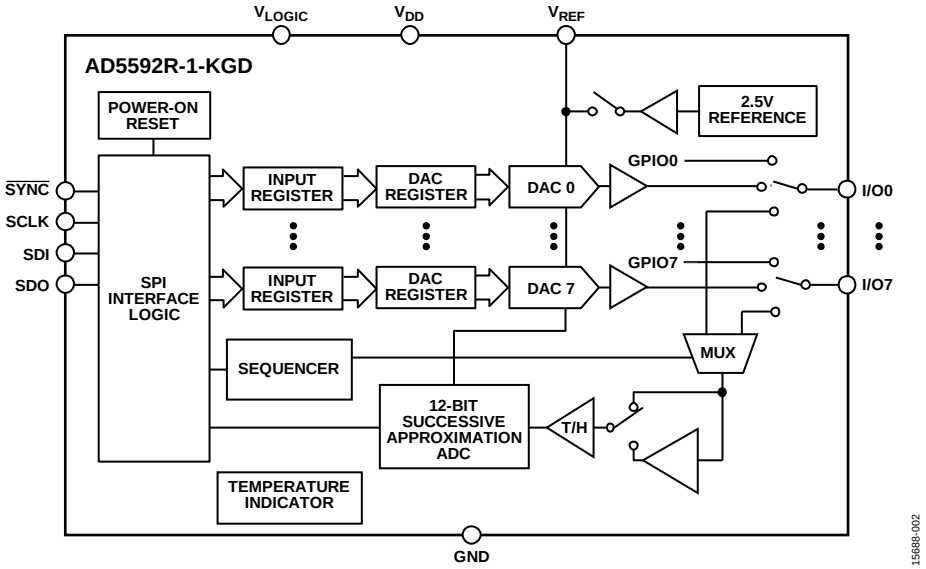

Figure 1.

Rev. 0 **Document Feedback**

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REVISION HISTORY

2/2018—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V (external), R_L = 2 kΩ to GND, C_L = 200 pF to GND, T_A = T_{MIN} to T_{MAX}, temperature range = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
ADC PERFORMANCE					f_{IN} = 10 kHz sine wave
Resolution		12		Bits	
Input Range	0		V_{REF}	V	When using the internal ADC buffer, there is a dead band of 0 V to 5 mV
	0		2 × V_{REF}	V	
Integral Nonlinearity (INL)	−2		+2	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	
Offset Error			±5	mV	
Gain Error			0.3	% FSR	
Throughput Rate			400	kSPS	
Track Time (t_{TRACK})	500			ns	
Conversion Time (t_{CONV})			2	µs	
Signal-to-Noise Ratio (SNR)		69		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		67		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		61		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Signal-to-Noise-and-Distortion (SINAD) Ratio		69		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		67		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		60		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Total Harmonic Distortion (THD)		−91		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		−89		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		−72		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Peak Harmonic or Spurious Noise (SFDR)		91		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		91		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		72		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Aperture Delay		15		ns	V_{DD} = 3 V
		12		ns	V_{DD} = 5 V
Aperture Jitter		50		ps	
Channel-to-Channel Isolation		−95		dB	f_{IN} = 5 kHz
Input Capacitance		45		pF	
Full Power Bandwidth		8.2		MHz	At 3 dB
		1.6		MHz	At 0.1 dB
DAC PERFORMANCE[2]					
Resolution		12		Bits	
Output Range	0		V_{REF}	V	
	0		2 × V_{REF}	V	
Integral Nonlinearity (INL)	−1		+1	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	
Offset Error	−3		+3	mV	
Offset Error Drift		8		µV/°C	
Gain Error			±0.2	% FSR	Output range = 0 V to V_{REF}
			±0.1	% FSR	Output range = 0 V to 2 × V_{REF}
Zero Code Error		0.65	2	mV	
Total Unadjusted Error		±0.03	±0.25	% FSR	Output range = 0 V to V_{REF}
		±0.015	±0.1		Output range = 0 V to 2 × V_{REF}
Capacitive Load Stability			2	nF	R_{LOAD} = ∞
			10	nF	R_{LOAD} = 1 kΩ

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
Resistive Load	1			kΩ	
Short-Circuit Current		25		mA	
DC Crosstalk	−4		+4	μV	Due to single channel, full-scale output change
DC Output Impedance		0.2		Ω	
DC Power Supply Rejection Ratio (PSRR)		0.15		mV/V	DAC code = midscale, V_{DD} = 3 V ± 10% or 5 V ± 10%
Load Impedance at Rails[3]		25		Ω	
Load Regulation		200		μV/mA	V_{DD} = 5 V ± 10%, DAC code = midscale, −10 mA ≤ I_{OUT} ≤ +10 mA
		200		μV/mA	V_{DD} = 3 V ± 10%, DAC code = midscale, −10 mA ≤ I_{OUT} ≤ +10 mA
Power-Up Time		7		μs	Coming out of power-down mode, V_{DD} = 5 V
AC SPECIFICATIONS					
Slew Rate		1.25		V/μs	Measured from 10% to 90% of full scale
Settling Time		6		μs	¼ scale to ¾ scale settling to 1 LSB
DAC Glitch Impulse		2		nV-sec	
DAC to DAC Crosstalk		1		nV-sec	
Digital Crosstalk		0.1		nV-sec	
Analog Crosstalk		1		nV-sec	
Digital Feedthrough		0.1		nV-sec	
Multiplying Bandwidth		240		kHz	DAC code = full scale, output range = 0 V to V_{REF}
Output Voltage Noise Spectral Density		200		nV/√Hz	DAC code = midscale, output range = 0 V to 2 × V_{REF}, measured at 10 kHz
Signal-to-Noise Ratio (SNR)		81		dB	
Peak Harmonic or Spurious Noise (SFDR)		77		dB	
Signal-to-Noise-and-Distortion (SINAD) Ratio		74		dB	
Total Harmonic Distortion (THD)		−76		dB	
REFERENCE INPUT					
V_{REF} Input Voltage	1		V_{DD}	V	
DC Leakage Current	−1		+1	μA	No I/Ox pins configured as DACs
Reference Input Impedance		12		kΩ	DAC output range = 0 V to 2 × V_{REF}
		24		kΩ	DAC output range = 0 V to V_{REF}
REFERENCE OUTPUT					
V_{REF} Output Voltage	2.495	2.5	2.505	V	At ambient
V_{REF} Temperature Coefficient		20		ppm/°C	
Capacitive Load Stability		5		μF	R_L = 2 kΩ
Output Impedance		0.15		Ω	V_{DD} = 2.7 V
		0.7		Ω	V_{DD} = 5 V
Output Voltage Noise		10		μV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		240		nV/√Hz	At ambient, f = 10 kHz, C_L = 10 nF
Line Regulation		20		μV/V	At ambient, sweeping V_{DD} from 2.7 V to 5.5 V
		10		μV/V	At ambient, sweeping V_{DD} from 2.7 V to 3.3 V
Load Regulation					
Sourcing		210		μV/mA	At ambient, −5 mA ≤ load current ≤ +5 mA
Sinking		120		μV/mA	At ambient, −5 mA ≤ load current ≤ +5 mA
Output Current Load Capability		±5		mA	V_{DD} ≥ 3 V
GPIO OUTPUT					
I_{SOURCE}, I_{SINK}		1.6		mA	
Output Voltage					
High (V_{OH})	V_{DD} − 0.2			V	I_{SOURCE} = 1 mA
Low (V_{OL})			0.4	V	I_{SOURCE} = 1 mA

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
GPIO INPUT					
Input Voltage					
High (V_{IH})	$0.7 \times V_{DD}$			V	
Low (V_{IL})			$0.3 \times V_{DD}$	V	
Input Capacitance		20		pF	
Hysteresis		0.2		V	
Input Current		±1		µA	
LOGIC INPUTS					
Input Voltage					
High (V_{INH})	$0.7 \times V_{LOGIC}$			V	
Low (V_{INL})			$0.3 \times V_{LOGIC}$	V	
Input Current (I_{IN})	−1		+1	µA	Typically 10 nA
Input Capacitance (C_{IN})			10	pF	
LOGIC OUTPUT (SDO)					
Output High Voltage (V_{OH})	$V_{LOGIC} - 0.2$			V	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5. 5 V
Output Low Voltage (V_{OL})			0.4	V	I_{SINK} = 200 µA
Floating-State Output Capacitance		10		pF	
TEMPERATURE SENSOR					
Resolution		12		Bits	
Operating Range	−40		+105	°C	
Accuracy		±3		°C	5 sample averaging
Track Time			5	µs	ADC buffer enabled
			20	µs	ADC buffer disabled
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD}			2.7	mA	Digital inputs = 0 V or V_{DD}, I/O0 to I/O7 configured as DACs and ADCs, internal reference on, ADC buffer on, DAC code = 0xFFF, range is 0 V to $2 \times V_{REF}$ for DACs and ADCs
Power-Down Mode			3.5	µA	
V_{DD} = 5 V (Normal Mode)		1.6		mA	I/O0 to I/O7 are DACs, internal reference, gain = 2
		1		mA	I/O0 to I/O7 are DACs, external reference, gain = 2
		2.4		mA	I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 2
		1.1		mA	I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 2
		1		mA	I/O0 to I/O7 are ADCs, internal reference, gain = 2
		0.75		mA	I/O0 to I/O7 are ADCs, external reference, gain = 2
		0.5		mA	I/O0 to I/O7 are general-purpose outputs
		0.5		mA	I/O0 to I/O7 are general-purpose inputs
		0.5		mA	I/O0 to I/O3 are general-purpose outputs, I/O4 to I/O7 are general-purpose inputs
V_{DD} = 3 V (Normal Mode)		1.1		mA	I/O0 to I/O7 are DACs, internal reference, gain = 1
		1		mA	I/O0 to I/O7 are DACs, external reference, gain = 1
		1.1		mA	I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 1
		0.78		mA	I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 1
		0.75		mA	I/O0 to I/O7 are ADCs, internal reference, gain = 1

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
		0.5		mA	I/O0 to I/O7 are ADCs, external reference, gain = 1
		0.45		mA	I/O0 to I/O7 are general-purpose outputs
		0.45		mA	I/O0 to I/O7 are general-purpose inputs
V_{LOGIC}	1.62		V_{DD}	V	
I_{LOGIC}			3	µA	

[1] All specifications expressed in decibels are referred to full-scale input (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise noted.
[2] DC specifications tested with the outputs unloaded, unless otherwise noted. Linearity calculated using a code range of 8 to 4095. There is an upper dead band of 10 mV when $V_{REF} = V_{DD}$.
[3] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	1.62 V ≤ V_{LOGIC} < 3 V	3 V ≤ V_{LOGIC} ≤ 5.5 V	Unit	Test Conditions/Comments
t_1	33	20	ns min	SCLK cycle time, write operation
	65	50	ns min	SCLK cycle time, read operation
t_2	16	10	ns min	SCLK high time
t_3	16	10	ns min	SCLK low time
t_4	15	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
	2	2	µs max	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	7	7	ns min	Data setup time
t_6	5	5	ns min	Data hold time
t_7	15	10	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	30	30	ns min	Minimum $\overline{SYNC}$ high time for write operations
	60	60	ns min	Minimum $\overline{SYNC}$ high time for register read operations
t_9	0	0	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge
t_{10}	56	25	ns max	SCLK rising edge to SDO valid

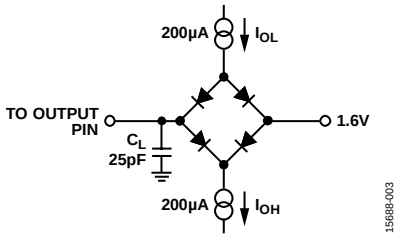


Figure 2. Load Circuit for Logic Output (SDO) Timing Specifications

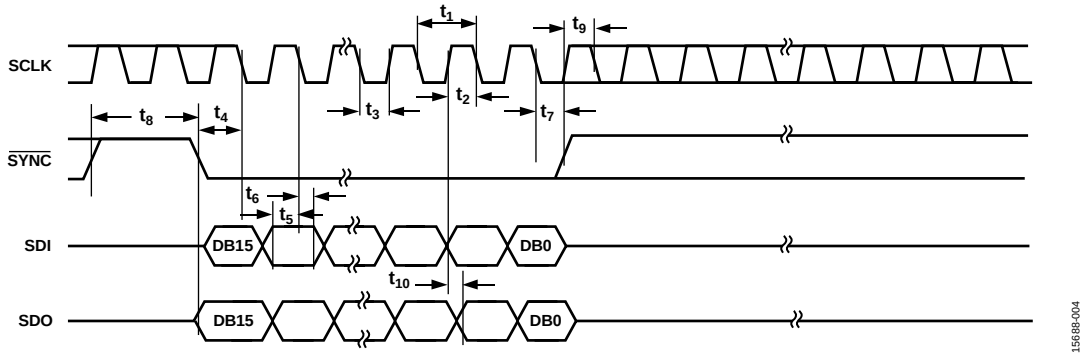


Figure 3. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 3.

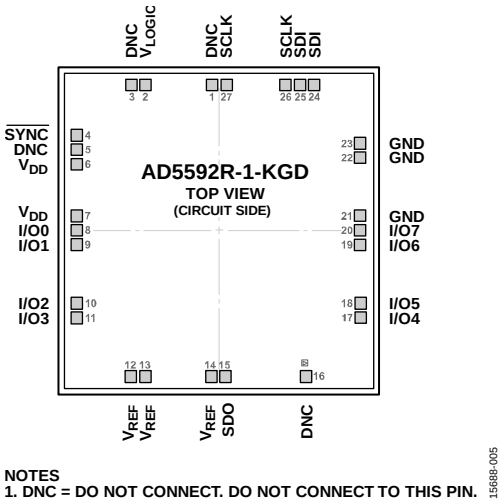
Parameter	Rating
V_{DD} to GND	−0.3 V to + 7 V
V_{LOGIC} to GND	−0.3 V to + 7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 4. Pad Configuration

Table 4. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
1	−43.545	882	DNC	Do Not Connect.
2	−457.925	882	V_{LOGIC}	Interface Power Supply.
3	−542.925	882	DNC	Do Not Connect.
4	−882	585.115	$\overline{SYNC}$	Synchronization. Active low control input. SYNC is the frame synchronization signal for the input data. When SYNC goes low, data is transferred in on the falling edges of the next 16 clocks.
5	−882	500.115	DNC	Do Not Connect.
6	−882	415.115	V_{DD}	Power Supply Input. The AD5592R-1-KGD operates from 2.7 V to 5.5 V.
7	−882	84.685	V_{DD}	Power Supply Input. The AD5592R-1-KGD operates from 2.7 V to 5.5 V.
8	−882	−0.315	I/O0	Input/Output 0. This pin can be independently configured as a DAC, ADC, or general-purpose digital input or output.
9	−882	−85.355	I/O1	Input/Output 1. This pin can be independently configured as a DAC, ADC, or general-purpose digital input or output.
10	−882	−456.09	I/O2	Input/Output 2. This pin can be independently configured as a DAC, ADC, or general-purpose digital input or output.
11	−882	−541.13	I/O3	Input/Output 3. This pin can be independently configured as a DAC, ADC, or general-purpose digital input or output.
12	−542.925	−882	V_{REF}	Reference Input/Output.
13	−457.925	−882	V_{REF}	Reference Input/Output.
14	−43.545	−882	V_{REF}	Reference Input/Output.
15	41.455	−882	SDO	Data Out. Logic output.
16	542.65	−882	DNC	Do Not Connect.
17	882	−541.09	I/O4	Input/Output 4. This pin can be independently configured as a DAC, ADC, or general-purpose digital input or output.
18	882	−456.09	I/O5	Input/Output 5. This pin can be independently configured as a DAC, ADC, or general-purpose digital input or output.
19	882	−85.355	I/O6	Input/Output 6. This pin can be independently configured as a DAC, ADC, or general-purpose digital input or output.
20	882	−0.315	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. I/O7 can also be configured as a $\overline{BUSY}$ signal to indicate when an ADC conversion is taking place.
21	882	84.685	GND	Ground Reference.
22	882	450.105	GND	Ground Reference.
23	882	535.105	GND	Ground Reference.

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
24	585.145	882	SDI	Data Input. Logic input.
25	500.145	882	SDI	Data Input. Logic input.
26	415.105	882	SCLK	Serial Clock Input.
27	41.455	882	SCLK	Serial Clock Input.

OUTLINE DIMENSIONS

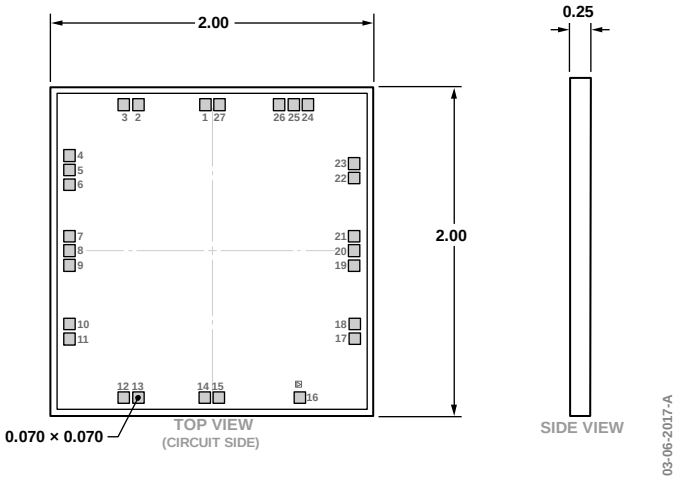


Figure 5. 27-Pad Bare Die [CHIP]
(C-27-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 5. Die Specifications

Parameter	Value	Unit
Die Size (Maximum)	2000 × 2000	µm
Bond Pad (Minimum)	70 × 70	µm
Thickness	250	µm
Scribe Line Width	80	µm
Bond Pad Composition	AlCu (0.5%)	%
Passivation Type	Polyimide	Not applicable
Backside Bias	GND	Not applicable

Table 6. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy Adhesive
Bonding Method	1.0 mil, 2N gold wire[1]

[1] Evaluate gold wire for suitability before use at elevated temperatures for extended durations.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5592R-1-KGD-PT	−40°C to +105°C	27-Pad Bare Die [CHIP]	C-27-1