Data Sheet

ADA4620-1, ADA4620-2

36 V, Precision, Low Noise, 16 MHz JFET Op Amp with Rail-to-Rail Output

FEATURES

- Low offset voltage: ±25 µV typ
- Low offset voltage drift
  - 0.2 µV/°C typ
- Low input bias current: 1 pA typ, 6 pA max
- Low 1/f noise: 0.2 µV p-p, 0.1 Hz to 10 Hz typ
- Voltage noise density: 5 nV/√Hz at 1 kHz typ
- Gain bandwidth product: 16 MHz typ
- High slew rate: 30 V/µs typ
- Low THD + N: −133 dB at 1 kHz typ
- Low supply current: 1.3 mA per amplifier typ
- Wide power supply range
  - Single supply: 4.5 V to 36 V
  - Dual supplies: ±2.25 V to ±18 V
- No phase reversal
- Unity-gain stable
- Low supply current inrush during power up
- Extended high input common-mode range

APPLICATIONS

- Transimpedance amplifiers
- Electronic test and measurement
- Scientific and field instruments
- Semiconductor test
- Data acquisition systems
- High impedance sensors

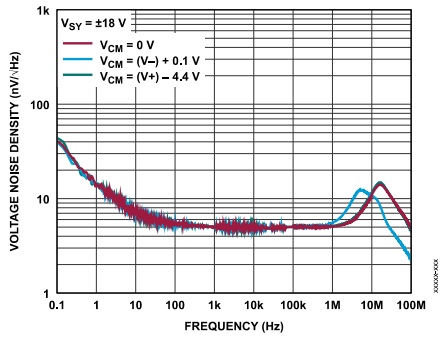

Figure 1. Input Voltage Noise vs. Frequency

TYPICAL APPLICATION DIAGRAM

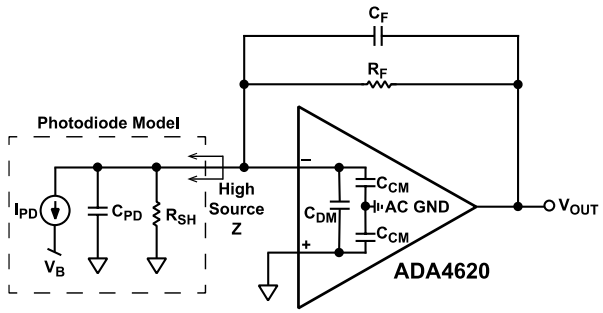

Figure 2. Photodiode Application with Key Elements

GENERAL DESCRIPTION

The ADA4620-1 and ADA4620-2 are a series of 36 V, precision, low noise, low offset drift, JFET Op Amps. The parts offer the combination of top precision parameters at speed, and at extended operating range and temperature. The ADA4620 is ideal for customers who need to design systems to meet high DC precision and AC performance. The specifications make the ADA4620 optimal as a front-end amplifier in a data acquisition (DAQ) system, or for a TIA circuit with high input impedance.

For only 1.3 mA of supply current per amplifier, the ADA4620 has a gain-bandwidth product of 16 MHz, a 30 V/µs slew rate, 5 nV/√Hz of broadband noise, and 200 nV p-p of 1/f noise. The input voltage range includes the negative supply, and the output swings rail-to-rail.

The ADA4620 is specified for operating over the temperature range of −40°C to +125°C, and dual supplies ranging from ±2.25 V to ±18 V, or on a single supply ranging from +4.5 V to +36 V. The ADA4620-1 and ADA4620-2 are available in an **8-lead SOIC_N package.**

Please reach out to **ADA4620@analog.com** for more information.

PRELIMINARY

REVISION HISTORY

06/2024 – Rev. PrG

Preliminary release

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PRELIMINARY

SPECIFICATIONS

Electrical Characteristics

Table 1. Electrical Characteristics

(Supply voltage (V_{SY}) = ±2.25 V to ±18 V for dual supplies, or 4.5 V to 36 V for single supply; Common-mode voltage (V_{CM}) = 0 V for dual supplies, or (V+)/2 V for single supply; T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}	V_{CM} = 0 V, V_{SY} = ±18 V			±25	TBD	µV
		0°C < T_A < +85°C			±35	TBD	
		−40°C < T_A < +85°C			±40	TBD	
		−40°C < T_A < +125°C			±45	TBD	
		V_{CM} = (V+) − 4.4 V, V_{SY} = ±18 V			±25	TBD	
		0°C < T_A < +85°C				TBD	
		−40°C < T_A < +85°C				TBD	
		−40°C < T_A < +125°C				TBD	
		V_{CM} = (V-) − 0.1 V, V_{SY} = ±18 V			±25	TBD	
		0°C < T_A < +85°C			±35	TBD	
		−40°C < T_A < +85°C			±40	TBD	
		−40°C < T_A < +125°C			±45	TBD	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	V_{CM} = 0 V, −40°C < T_A < +125°C	Box Method		±0.2	TBD	µV/°C
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C	Box Method		±0.2	TBD	µV/°C
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	0°C < T_A < +85°C	Box Method		±0.13	TBD	µV/°C
		V_{CM} = (V+) − 4.4 V, −40°C < T_A < +125°C			TBD	TBD	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C			TBD	TBD	µV/°C
		0°C < T_A < +85°C			TBD	TBD	
Input Bias Current	I_B	V_{CM} = 0 V			0.7	6	pA
		−40°C < T_A < +85°C			55	TBD	
		−40°C < T_A < +125°C			750	TBD	
		V_{CM} = (V+) - 4.4 V, V_{SY} = ±18 V			0.5	5	
		−40°C < T_A < +85°C			50	TBD	
		−40°C < T_A < +125°C			560	TBD	
Input Offset Current	I_{OS}	V_{CM} = 0 V, V_{SY} = ±18 V			±0.5	±3	pA
		−40°C < T_A < +85°C			±2.5	TBD	
		−40°C < T_A < +125°C			±25	TBD	
		V_{CM} = (V+) - 4.4 V, V_{SY} = ±18 V			±0.03	TBD	
		−40°C < T_A < +85°C			±4.5	TBD	
		−40°C < T_A < +125°C			±30	TBD	

PRELIMINARY

(Supply voltage (V_{SY}) = ±2.25 V to ±18 V for dual supplies, or 4.5 V to 36 V for single supply; Common-mode voltage (V_{CM}) = 0 V for dual supplies, or (V+)/2 V for single supply; T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input Voltage Range	IVR	Guaranteed by CMRR	(V-)-0.1		(V+)-4.4	V
Common-Mode Rejection Ratio	CMRR	(V-) - 0.1 V < V_{CM} < (V+) - 4.4 V	TBD	135		dB
Common-Mode Rejection Ratio	CMRR	−40°C < T_A < +85°C	TBD	133		dB
	CMRR	−40°C < T_A < +125°C	TBD	131		
Open-Loop Voltage Gain	A_{VOL}	R_L = 10 kΩ, V_{OUT} = ±17.8 V, V_{SY} = ±18 V	TBD	135		dB
		−40°C < T_A < +85°C	TBD			
		−40°C < T_A < +125°C	TBD			
		R_L = 2 kΩ, V_{OUT} = ±17.8 V, V_{SY} = ±18 V	TBD	106		
		−40°C < T_A < +85°C	TBD			
		−40°C < T_A < +125°C	TBD			
Input Capacitance	C_{INDM}	Differential mode		5		pF
	C_{INCM}	Common mode		7		
Input Resistance	R_{INDM}	Differential mode		TBD		Ω
	R_{INCM}	Common mode		10^{13}		
OUTPUT CHARACTERISTICS						
Output Swing High [(V+) - V_{OUT}]	V_{OH}	R_L = 10 kΩ, A_{OL} > TBD, V_{SY} = ±18 V		38	TBD	mV
		−40°C < T_A < +85°C	TBD			
		−40°C < T_A < +125°C	TBD			
		R_L = 2 kΩ, A_{OL} > TBD dB, V_{SY} = ±18 V		TBD	TBD	
		−40°C < T_A < +85°C			TBD	
		−40°C < T_A < +125°C			TBD	
Output Swing Low [V_{OUT} - (V-)]	V_{OL}	R_L = 10 kΩ, A_{OL} > TBD dB, V_{SY} = ±18 V		36	TBD	mV
		−40°C < T_A < +85°C			TBD	
		−40°C < T_A < +125°C			TBD	
		R_L = 2 kΩ, A_{OL} > TBD dB, V_{SY} = ±18 V		TBD	TBD	
		−40°C < T_A < +85°C			TBD	
		−40°C < T_A < +125°C			TBD	
Short-Circuit Current	I_{SC}	V_{SY} = ±5 V, V_{OUT} = 0 V, | (V_{IN}+) - (V_{IN}-) | = 250 mV, Sourcing/Sinking		60/43		mA
		V_{SY} = ±15 V, V_{OUT} = 0 V, | (V_{IN}+) - (V_{IN}-) | = 250 mV, Sourcing/Sinking		82/79		
		V_{SY} = ±18 V, V_{OUT} = 0 V, | (V_{IN}+) - (V_{IN}-) | = 250 mV, Sourcing/Sinking		87/86		
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.5		mΩ
		f = 1 kHz, A_V = +10		3		
		f = 1 kHz, A_V = +100		30		
Open-Loop Output Impedance	Z_O	f = 1 MHz, V_{SY} = ±18 V		3.3		Ω

PRELIMINARY

(Supply voltage (V_{SY}) = ±2.25 V to ±18 V for dual supplies, or 4.5 V to 36 V for single supply; Common-mode voltage (V_{CM}) = 0 V for dual supplies, or (V+)/2 V for single supply; T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power Supply Rejection Ratio	PSRR+	V- = 0 V, V_{IN}+ = 0V, V+ stepped from 4.5 V to 36 V		TBD	135		dB
		−40°C < T_A < +85°C		TBD			
		−40°C < T_A < +125°C		TBD			
	PSRR-	V+ = 4.5 V, V_{IN}+ = 0 V, V- stepped from -31.5 V to 0 V		TBD	TBD		
		−40°C < T_A < +85°C		TBD			
		−40°C < T_A < +125°C		TBD			
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA, V_{SY} = ±18 V			1.3	TBD	mA
		−40°C < T_A < +85°C				1.85	
		−40°C < T_A < +125°C				TBD	
		I_{OUT} = 0 mA, V_{SY} = ±2.25 V			1.3	TBD	
		−40°C < T_A < +85°C				1.85	
		−40°C < T_A < +125°C				TBD	
Operating Range	V_{SY}	Guaranteed by PSRR		4.5		36	V
DYNAMIC PERFORMANCE							
Slew Rate	SR	R_L = 2 kΩ, V_{OUT} = ±5 V, A_V = +1, V_{SY} = ±18 V	Low to high transition (10-90%)		30		V/µs
			High to low transition (90-10%)		30		
		R_L = 2 kΩ, V_{OUT} = ±5 V, A_V = -1, V_{SY} = ±18 V	Low to high transition (10-90%)		30		
			High to low transition (90-10%)		30		
Gain Bandwidth Product	GBP	V_{SY} = ±18 V, R_L = 2 kΩ, C_L = 50 pF, Measured at 100 kHz			16		MHz
Unity-Gain Crossover	UGC	V_{SY} = ±18 V, R_L = 2 kΩ, C_L = 50 pF			17		MHz
-3 dB Bandwidth	-3 dB	V_{SY} = ±18 V, R_L = 2 kΩ, C_L = 50 pF, A_V = +1			51		MHz
Phase Margin	PM	V_{SY} = ±18 V, R_L = 2 kΩ, C_L = 50 pF			56		Degrees
Settling Time	t_S	V_{OUT} = ±5 V, A_V = -1, V_{SY} = ±18 V, R_F = R_G = 1 kΩ, R_L = 10 kΩ, C_L = 50 pF	To 0.01%		565		ns
			To 0.0245% (12-Bit)		550		
			To 0.0015% (16-Bit)		TBD		

PRELIMINARY

(Supply voltage (V_{SY}) = ±2.25 V to ±18 V for dual supplies, or 4.5 V to 36 V for single supply; Common-mode voltage (V_{CM}) = 0 V for dual supplies, or (V+)/2 V for single supply; T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Overload Recovery Time	OLR+	R_L = 2 kΩ, C_L = 50 pF, A_V = +10, V_{SY} = ±18 V, Step = 2.2 V		187		ns
	OLR-	R_L = 2 kΩ, C_L = 50 pF, A_V = -10, V_{SY} = ±18 V, Step = 2.2 V		159		
Total Harmonic Distortion	THD	R_L = 2 kΩ, V_{OUT} = 10 V p-p, A_V = +1, f = 1 kHz, V_{SY} = ±18 V		-144		dB
		R_L = 2 kΩ, V_{OUT} = 10 V p-p, A_V = -1, f = 1 kHz, V_{SY} = ±18 V		-145		
		R_L = 2 kΩ, V_{OUT} = 10 V p-p, A_V = +1, f = 100 kHz, V_{SY} = ±18 V		-80		
		R_L = 2 kΩ, V_{OUT} = 10 V p-p, A_V = -1, f = 100 kHz, V_{SY} = ±18 V		-97		
Total Harmonic Distortion + Noise	THD + N	R_L = 2 kΩ, V_{OUT} = 10 V p-p, A_V = +1, f = 1 kHz, Bandwidth = 90 kHz, V_{SY} = ±18 V		-133		dB
		R_L = 2 kΩ, V_{OUT} = 10 V p-p, A_V = -1, f = 1 kHz, Bandwidth = 90 kHz, V_{SY} = ±18 V		-133		
EMI REJECTION RATIO						
Frequency = 1000 MHz	EMIRR	V_{IN} = 200 mV p-p		64		dB
Frequency = 2400 MHz	EMIRR	V_{IN} = 200 mV p-p		84		dB
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p-p}$	0.1 Hz to 10 Hz, V_{CM} = 0 V, V_{SY} = ±18 V		0.2		µV p-p
Voltage Noise Density	e_n	f = 1 Hz, V_{CM} = 0 V, V_{SY} = ±18 V		15.3		nV/√Hz
		f = 10 Hz, V_{CM} = 0 V, V_{SY} = ±18 V		7.3		
		f = 100 Hz, V_{CM} = 0 V, V_{SY} = ±18 V		5.6		
		f = 1 kHz, V_{CM} = 0 V, V_{SY} = ±18 V		5		
		f = 10 kHz, V_{CM} = 0 V, V_{SY} = ±18 V		5		
Current Noise Density	I_n	f = 10 Hz, V_{CM} = 0 V, V_{SY} = ±18 V		0.6		fA/√Hz
MATCHING ADA4620-2 - (Ch A - Ch B)						
Offset Voltage	V_{OS}	V_{CM} = 0 V, T_A = 25°C,		TBD		µV
		V_{CM} = 0 V, −40°C		TBD		
		V_{CM} = 0 V, 85°C		TBD		
		V_{CM} = 0 V, 125°C		TBD		
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	V_{CM} = 0 V, −40°C < T_A < +125°C		TBD	TBD	µV/°C
Input Bias Current	I_B	V_{CM} = 0 V, T_A = 25°C		TBD	TBD	pA
		V_{CM} = 0 V, -40°C < T_A < +85°C		TBD	TBD	
		V_{CM} = 0 V, -40°C < T_A < +125°C		TBD	TBD	
CROSSTALK ADA4620-2 - (Ch A - Ch B)						
Crosstalk	XTLK	Frequency = 1 kHz; R_L = TBD, V_{IN} = TBD		TBD		dB

PRELIMINARY

(Supply voltage (V_{SY}) = ±2.25 V to ±18 V for dual supplies, or 4.5 V to 36 V for single supply; Common-mode voltage (V_{CM}) = 0 V for dual supplies, or (V+)/2 V for single supply; T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Crosstalk	XTLK	Frequency = 10 kHz; R_L = TBD, V_{IN} = TBD		TBD		dB
		Frequency = 100 kHz; R_L = TBD, V_{IN} = TBD		TBD		

High Common-Mode Voltage Operation

Table 2. High Common-Mode Voltage Operation

(V_S = ±18 V for dual supplies or 36 V for single supply; V_{CM} = (V+) - 2 V; T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1.75	TBD	mV
		−40°C < T_A < +85°C		1.8	TBD	
		−40°C < T_A < +125°C		3	TBD	
		V_{CM} = V+		TBD	TBD	
		−40°C < T_A < +85°C		TBD	TBD	
		−40°C < T_A < +125°C		TBD	TBD	
Input Bias Current	I_B			1	6	pA
		−40°C < T_A < +85°C		TBD	TBD	
		−40°C < T_A < +125°C		TBD	TBD	
Input Offset Current	I_{OS}			TBD	TBD	pA
		−40°C < T_A < +85°C		TBD	TBD	
		−40°C < T_A < +125°C		TBD	TBD	
Common-Mode Rejection Ratio	CMRR	(V+) - 3.8 V < V_{CM} < (V+) - 2 V		70.8		dB
		(V+) - 3.5 V < V_{CM} < (V+) - 2 V		77		
		V- < V_{CM} < (V+) - 2 V	TBD	85		
		−40°C < T_A < +85°C	TBD	TBD		
		−40°C < T_A < +125°C		120		
Open-Loop Voltage Gain	A_{VOL}	R_L = 10 kΩ, V_{OUT} = ±17.8 V	TBD	135		dB
		−40°C < T_A < +85°C	TBD	TBD		
		−40°C < T_A < +125°C	TBD	TBD		
		R_L = 2 kΩ, V_{OUT} = ±17.8 V	TBD	106		
		−40°C < T_A < +85°C	TBD			
		−40°C < T_A < +125°C	TBD			
Input Capacitance	C_{INDM}	Differential mode		TBD		pF
	C_{INCM}	Common mode		TBD		
Input Resistance	R_{INDM}	Differential mode		TBD		Ω
	R_{INCM}	Common mode		TBD		
OUTPUT CHARACTERISTICS						
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		1		mΩ
		f = 1 kHz, A_V = +10		TBD		
		f = 1 kHz, A_V = +100		TBD		
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR+	V- = 0 V, V_{IN}+ = 33 V, V+ stepped from 35 V to 36 V	TBD	135		dB
		−40°C < T_A < +85°C	TBD			

PRELIMINARY

(V_S = ±18 V for dual supplies or 36 V for single supply; V_{CM} = (V+) - 2 V; T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	PSRR+	−40°C < T_A < +125°C		TBD			dB
Power Supply Rejection Ratio	PSRR-	V+ = 4.5 V, V_{IN}+ = (V+) - 2 V, V- stepped from -31.5 V to 0 V		TBD	TBD		dB
		−40°C < T_A < +85°C		TBD			
		−40°C < T_A < +125°C		TBD			
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA, V_{SY} = ±2.25V			1.1		mA
		−40°C < T_A < +85°C			TBD		
		−40°C < T_A < +125°C			1.44		
		I_{OUT} = 0 mA, V_{SY} = ±18V			TBD		
		−40°C < T_A < +85°C			TBD		
		−40°C < T_A < +125°C			TBD		
Operating Range	V_{SY}	Guaranteed by PSRR		4.5		36	V
DYNAMIC PERFORMANCE							
Slew Rate	SR	R_L = 2 kΩ, V_{OUT} = ±5 V, A_V = -10, V_{IN}+ = TBD	Low to high transition (10 - 90 %)		TBD		V/µs
			High to low transition (90 - 10 %)		TBD		
Gain Bandwidth Product	GBP	R_L = Open, C_L = 50 pF, Measured at 100 kHz			13		MHz
Unity-Gain Crossover	UGC	R_L = Open, C_L = 50 pF			11		MHz
Phase Margin	PM	R_L = Open, C_L = 50 pF			47		Degrees
Overload Recovery Time	OLR+	R_L = 2 kΩ, C_L = 50 pF, A_V = -10, Step = +6 V to +16 V, V_{CM} = +16 V			1.47		µs
	OLR-	R_L = 2 kΩ, C_L = 50 pF, A_V = -10, Step = +26 V to +16 V, V_{CM} = +16 V			0.23		
NOISE PERFORMANCE							
Voltage Noise	$e_{n\ p-p}$	0.1 Hz to 10 Hz, V_{CM} = 0 V			TBD		µV p-p
Voltage Noise Density	e_n	f = 1 Hz			TBD		nV/√Hz
		f = 10 Hz			TBD		
		f = 100 Hz			TBD		
		f = 1 kHz			TBD		
		f = 10 kHz			TBD		
Current Noise Density	I_n	f = 10 Hz			TBD		fA/√Hz

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
V_{SUPPLY}	
V_{SY} (V+) – (V-)	40 V
Input Voltage	
Single-Ended	(V-) - 0.3 V to (V+) + 0.3 V
Differential	((V+) - (V-)) + 0.6 V
Output Voltage	
V_{OUT}	(V-) - 0.3 V to (V+) + 0.3 V
Input Current	
I_{IN+}, I_{IN-}	10 mA
Output Short-Circuit Duration	TBD s
Temperature Range	
Storage	-65 °C to +150 °C
Operating	-40 °C to +125 °C
Junction	-65 °C to +150 °C
Lead Temperature	
Soldering, 10 sec	300°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PRELIMINARY

Thermal Characteristics

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Θ_{JA} is the junction-to-ambient thermal resistance.

Θ_{JC} is the junction-to-case thermal resistance.

Table 4. Thermal Resistance

Package Type	Θ_{JA}	Θ_{JC}	$\Theta_{JC(BOTTOM)}$	Unit
ADA4620-1				
SOIC_N (R-8)	115.5	46.3	N/A	°C/W

Electrostatic Discharge (ESD) Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD4620-1

Table 5. ADA4620-1, 8-Lead SOIC_N (R-8)

ESD Model	Withstand Threshold (V)	Class
HBM	±TBD	TBD
FICDM	±TBD	TBD

ESD Ratings for AD4620-2

Table 6. ADA4620-2, 8-Lead SOIC_N (R-8)

ESD Model	Withstand Threshold (V)	Class
HBM	±TBD	TBD
FICDM	±TBD	TBD

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PRELIMINARY

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

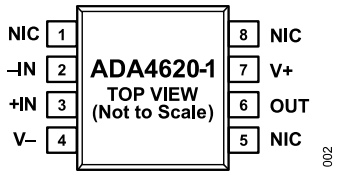

Figure 3. ADA4620-1, 8-Lead SOIC_N (R-8) Pin Configuration

Table 7. ADA4620-1 Pin Descriptions, 8-Lead SOIC (R-8)

PIN	NAME	DESCRIPTION
1, 5, 8	NIC	Not Internally Connected.
2	-IN	Inverting Input.
3	+IN	Noninverting Input.
4	V-	Negative Supply Voltage.
6	OUT	Output.
7	V+	Positive Supply Voltage.

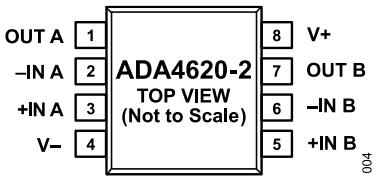

Figure 4. ADA4620-2, 8-Lead SOIC_N (R-8) Pin Configuration

Table 8. ADA4620-2 Pin Descriptions, 8-Lead SOIC (R-8)

PIN	NAME	DESCRIPTION
1	OUT A	Output, Channel A.
2	-IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V-	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	-IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.

OUTLINE DIMENSIONS

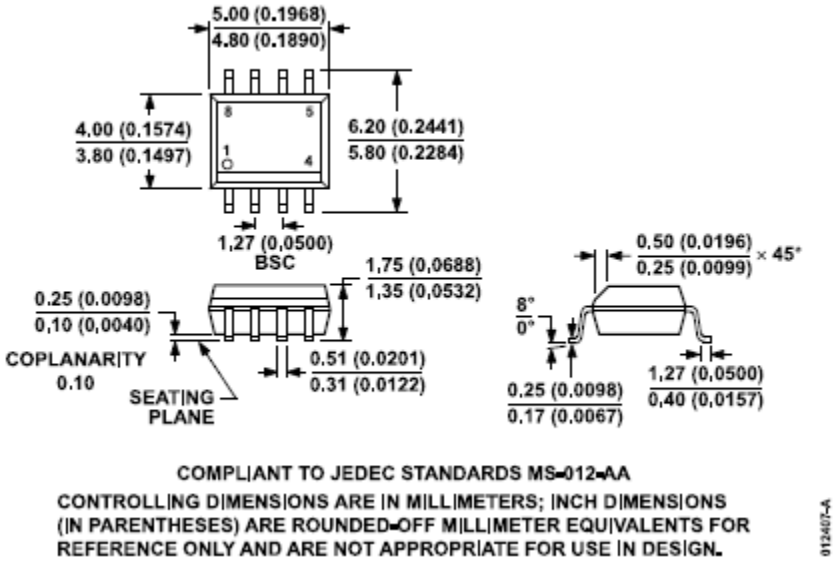

Figure 5. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions show in millimeters and (inches)

PRELIMINARY

PRELIMINARY