ADL6332

0.38 GHz to 12 GHz RxVGA

FEATURES

- Broadband RxVGA interfacing LNA and beamformer to RF ADC
- Operating frequency range: 0.38 GHz to 12 GHz, two product variants
  - ADL6332-A: 0.38 GHz to 8.0 GHz
  - ADL6332-B: 1.0 GHz to 12.0 GHz
- Differential signal chain optimizes common-mode rejection of RF ADC, even order harmonics, and intermodulation
- 50 Ω single-ended input and 50 Ω differential outputs
- Integrated broadband RF input balun
- 70 dB of gain control range in 1 dB step
- RF DSA range: 24.0 dB with 1.0 dB step
- Amplifier bypass loss of 12 dB each
- Asynchronous toggle between multiple predefined attenuation values and bypass amplifier stages
- Power gain at 4 GHz: 15.0 dB (ADL6332-A), 15.4 dB (ADL6332-B)
- Noise figure at 4 GHz: 8.5 dB (ADL6332-A), 8.3 dB (ADL6332-B)
- OIP3 at 4 GHz: 32.8 dBm (ADL6332-A), 32.5 dBm (ADL6332-B)
- OIP2 at 4 GHz: 59.6 dBm (ADL6332-A), 62 dBm (ADL6332-B)
- OP1dB at 4 GHz: 11.8 dBm (ADL6332-A), 13.0 dBm (ADL6332-B)
- Fully programmable through a 3-wire/4-wire SPI
- Single 3.3 V supply
- 24-terminal, 4.0 mm x 4.0 mm LGA

APPLICATIONS

- Aerospace and defense
- Instrumentation and test equipment
- Communication systems

GENERAL DESCRIPTION

The ADL6332 RxVGA provides an interface from LNA/beam former/Rx front end to RF analog-to-digital converters (RF-ADC). Each ADL6332 IC is composed of a balun, two differential RF amplifiers with bypass attenuators, and a digital step attenuator (DSA) to provide suitable receiver performance in a 24-terminal, 4.0 mm x 4.0 mm LGA package.

Serial-port interface (SPI) control is available to configure RF signal path or to optimize supply current vs. performance.

An integrated RF balun is used to provide a single-ended input over 0.38 GHz to 8.0 GHz (ADL6332-A) or 1.0 GHz to 12.0 GHz (ADL6332-B) with good impedance match.

Table 1. ADL6332 Frequency Ranges

ADL6332 Variant	Frequency Range (GHz)
A	0.38 to 8.0
B	1.0 to 12.0

FUNCTIONAL BLOCK DIAGRAM

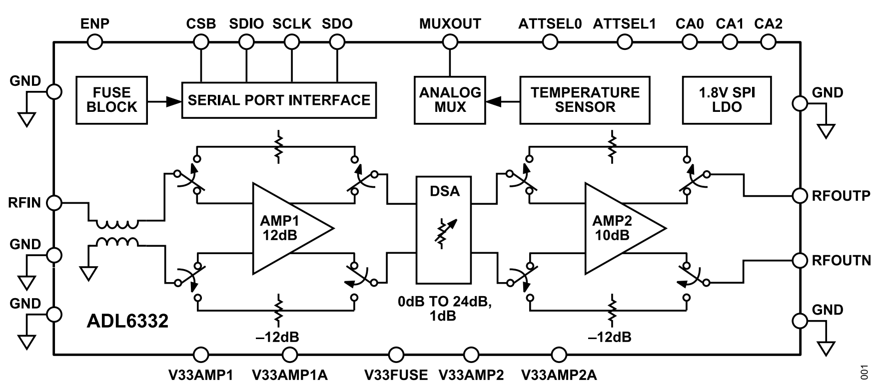

Figure 1. Functional Block Diagram

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SPECIFICATIONS

V33AMP1 voltage (V_{33AMP1}) = V33AMP1A voltage ($V_{33AMP1A}$) = V33AMP2 voltage (V_{33AMP2}) = V33AMP2A voltage ($V_{33AMP2A}$) = V33FUSE voltage (V_{33FUSE}) = 3.3V, T_A = 25°C, fixed gain mode, DSA attenuation = 0 dB, source resistance (R_S) = 50 Ω single-ended, load resistance (R_L) = 50 Ω differential, unless otherwise noted.

Table 2. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
FREQUENCY RANGE (ADL6332-A)		0.38		8.0	GHz
Power Gain					
Full Fixed Gain Mode[1]	0.38 GHz		12.0		dB
	1.0 GHz		15.4		dB
	2.0 GHz		15.5		dB
	4.0 GHz		15.0		dB
	8.0 GHz		13.7		dB
AMP1 Bypass Attenuation Mode[2]: AMP2 = Fixed Gain Mode	0.38 GHz		−15.0		dB
	1.0 GHz		−9.9		dB
	2.0 GHz		−9.8		dB
	4.0 GHz		−10.5		dB
	8.0 GHz		−12.6		dB
AMP2 Bypass Attenuation Mode[2]: AMP1 = Fixed Gain Mode	0.38 GHz		− 12.8		dB
	1.0 GHz		−7.5		dB
	2.0 GHz		−7.4		dB
	4.0 GHz		−7.8		dB
	8.0 GHz		−8.6		dB
Full Bypass Attenuation Mode[2]	0.38 GHz		−37.0		dB
	1.0 GHz		−32.3		dB
	2.0 GHz		−32.5		dB
	4.0 GHz		−33.5		dB
	8.0 GHz		−34.5		dB
NOISE/HARMONIC PERFORMANCE (ADL6332-A)					
Input Signal Frequency 0.4 GHz					
Full Fixed Gain Mode[1]					
Output Second-Order Intercept (OIP2L/OIP2H[3])	Pin = −22 dBm/tone		53.5/67.4		dBm
Output Third-Order Intercept (OIP3)	Pin = −22 dBm/tone		31.4		dBm
Output 1dB Compression Point (OP1dB)			12.3		dBm
Noise Figure (NF)			10.2		dB
AMP1 Bypass Attenuation Mode[2]					
Input Second-Order Intercept (IIP2L/IIP2H[4])	Pin = +2 dBm/tone		51.9/45.2		dBm
Input Third-Order Intercept (IIP3)	Pin = +2 dBm/tone		31.7		dBm
Input 1dB Compression Point (IP1dB)[5]			> 10		dBm
NF			30.3		dB
Input Signal Frequency 1.0 GHz					
Full Fixed Gain Mode[1]					
OIP2L/OIP2H[3]	Pin = −22 dBm/tone		63.1/64.0		dBm
OIP3	Pin = −22 dBm/tone		33.2		dBm
OP1dB			13.1		dBm
NF			8.1		dB
AMP1 Bypass Attenuation Mode[2]					
IIP2L/IIP2H[4]	Pin = +2 dBm/tone		67.6/61.5		dBm
IIP3	Pin = +2 dBm/tone		30.1		dBm
IP1dB[5]			> 10		dBm
NF			25.8		dB

SPECIFICATIONS

Table 2. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Input Signal Frequency 2.0 GHz					
Full Fixed Gain Mode[1]					
OIP2L/OIP2H[3]	Pin = −22 dBm/tone		62.4/60.4		dBm
OIP3	Pin = −22 dBm/tone		33.0		dBm
OP1dB			12.8		dBm
NF			8.2		dB
AMP1 Bypass Attenuation Mode[2]					
IIP2L/IIP2H[4]	Pin = +2 dBm/tone		66.1/63.3		dBm
IIP3	Pin = +2 dBm/tone		29.8		dBm
IP1dB[5]			> 10		dBm
NF			25.7		dB
Input Signal Frequency 4.0 GHz					
Full Fixed Gain Mode[1]					
OIP2L/OIP2H[3]	Pin = −22 dBm/tone		59.6/N/A[6]		dBm
OIP3	Pin = −22 dBm/tone		32.8		dBm
OP1dB			11.8		dBm
NF			8.5		dB
AMP1 Bypass Attenuation Mode[2]					
IIP2L/IIP2H[4]	Pin = +2 dBm/tone		63.9/N/A[6]		dBm
IIP3	Pin = +2 dBm/tone		29.1		dBm
IP1dB[5]			> 10		dBm
NF			26.5		dB
Input Signal Frequency 8.0 GHz					
Full Fixed Gain Mode[1]					
OIP2L/OIP2H[3]	Pin = −22 dBm/tone		56.1/N/A[6]		dBm
OIP3	Pin = −22 dBm/tone		33.4		dBm
OP1dB			11.8		dBm
NF			8.2		dB
AMP1 Bypass Attenuation Mode[2]					
IIP2L/IIP2H[4]	Pin = +2 dBm/tone		63.4/N/A[6]		dBm
IIP3	Pin = +2 dBm/tone		29.0		dBm
IP1dB[5]			> 10		dBm
NF			26.7		dB
INPUT/OUTPUT CHARACTERISTICS					
Input Impedance	Single-ended		50		Ω
Input Return Loss	Single-ended		12.0		dB
Output Impedance	Differential		50		Ω
Output Return Loss	In band, includes output balun single-ended		12.0		dB
GAIN FLATNESS					
1.0 GHz to 12 GHz	In a 1 GHz bandwidth		0.5		dB
1.5 GHz to 12 GHz	In a 3 GHz bandwidth		1.1		dB
DSA ATTENUATION					
Range			24.0		dB
Step	Through SPI		1.0		dB
Differential Nonlinearity (DNL)		0	0.16	0.2	dB
SWITCHING TIME	1.0 dB step through ATTSEL pins		25		ns
DIGITAL LOGIC					
Input Voltage	SCLK, SDO, SDIO, CSB, ENP, CA0, CA1, CA2, ATTSEL0, ATTSEL1				

SPECIFICATIONS

Table 2. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
High (V_{IH})		1.07			V
Low (V_{IL})				0.68	V
Input Current					
High (I_{IH})				−100	µA
Low (I_{IL})				100	µA
Output Voltage	SDO, SDIO (3-wire SPI mode)				
At 1.8 V					
High (VOH)	Output high current (I_{OH}) = −100 µA or −1 mA static load	1.5			V
Low (V_{OL})	Output low current (I_{OL}) = 100 µA or 1 mA static load			0.2	V
At 3.3 V					
High (V_{OH})	I_{OH} = −100 µA or −1 mA static load	2.7			V
Low (V_{OL})	I_{OL} = 100 µA or 1 mA static load			0.2	V
POWER SUPPLY					V
Voltage					
V33AMP1A		3.135	3.3	3.465	V
V33AMP1		3.135	3.3	3.465	V
V33AMP2A		3.135	3.3	3.465	V
V33AMP2		3.135	3.3	3.465	V
V33FUSE		3.135	3.3	3.465	V
Current					
Full Fixed Gain Mode[1]	3.3 V supply				
V33AMP1A			80		mA
V33AMP1			160		mA
V33AMP2A			80		mA
V33AMP2			160		mA
V33FUSE			35		mA
AMP1 Bypass Attenuation Mode[2]	3.3 V supply				
V33AMP1A			2		mA
V33AMP1			0.1		mA
V33AMP2A			80		mA
V33AMP2			160		mA
V33FUSE			22		mA
AMP2 Bypass Attenuation Mode[2]	3.3 V supply				
V33AMP1A			80		mA
V33AMP1			160		mA
V33AMP2A			0.1		mA
V33AMP2			0.1		mA
V33FUSE			22		mA
AMP1 and AMP2 Bypass Attenuation Mode[2]	3.3 V supply				
V33AMP1A			2		mA
V33AMP1			0.1		mA
V33AMP2A			0.1		mA
V33AMP2			0.1		mA
V33FUSE			12		mA
Power-Down Mode	3.3 V supply		3		mA

1 The full fixed gain mode is configured with the fixed gain configurations in AMP1 and AMP2, and DSA = 0 dB with the factory optimized parameters.

2 The bypass attenuation mode is configured with the bypass settings in AMP1 or AMP2, and DSA = 0 dB with the factory optimized parameters. Bypassing an amplifier with the attenuation mode reduces the total current typically by 230 mA per amplifier.

SPECIFICATIONS

[3] OIP2L refers to the two tone difference frequency, OIP2H refers to the two tone summation frequency.

[4] IIP2L refers to the two tone difference frequency, IIP2H refers to the two tone summation frequency.

[5] Exceeds the absolute maximum rating.

[6] Not applicable. An input signal frequency ≥ 4 GHz makes OIP2H/IIP2H beyond the operating frequency range.

DIGITAL LOGIC TIMING

C_{LOAD} = 25 pF

Table 3. SPI Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
f_{SCLK}	Maximum serial-clock rate			25	MHz
t_{PWH}	Minimum period that SCLK is in logic-high state	10			ns
t_{PWL}	Minimum period that SCLK is in logic-low state	10			ns
t_{DS}	Setup time between data and rising edge of SCLK	10			ns
t_{DH}	Hold time between data and rising edge of SCLK	5			ns
t_{DCS}	Setup time between falling edge of CSB and SCLK	10			ns
t_{DV}	Maximum time delay between falling edge of SCLK and output data valid for a read operation			10	ns

SPI Timing Diagrams

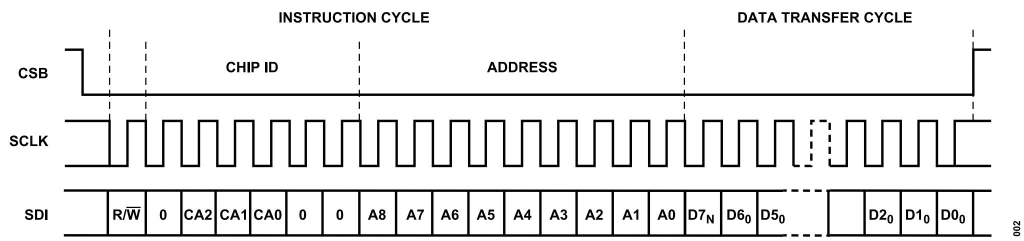


Figure 2. SPI Register Timing, MSB First

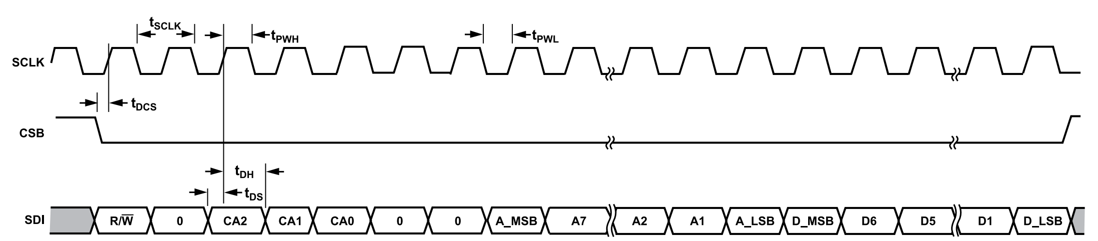


Figure 3. Timing Diagram for the SPI Register Write (3- and 4-Wire SPI Mode)

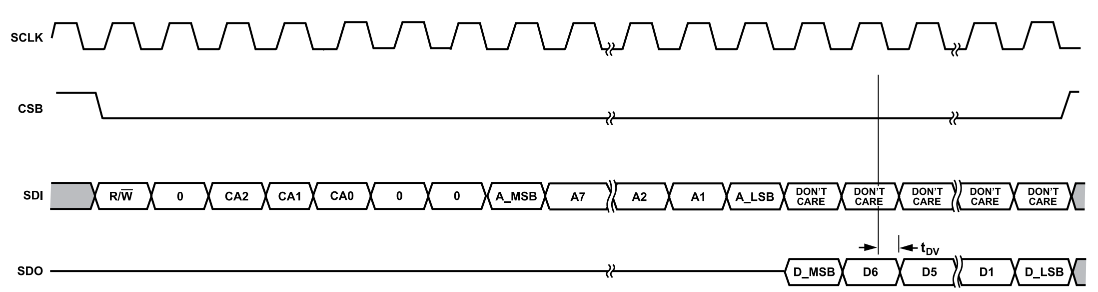


Figure 4. Timing Diagram for SPI Register Read (4-Wire SPI Mode)

SPECIFICATIONS

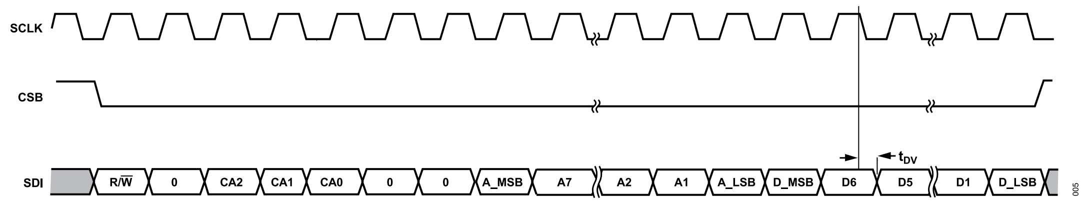


Figure 5. Timing Diagram for SPI Register Read (3-Wire SPI Mode, SDIO Pin Is Bidirectional Mode, Input (Write) and Output (Read))

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
V33AMP1, V33AMP1A, V33AMP2, V33AMP2A, V33FUSE	−0.3 V to +3.6 V
RFIN	10 dBm
SCLK, SDO, SDIO, CSB, CA0, CA1, CA2, ENP, ATTSEL0, ATTSEL1	−0.3 V to +3.6 V
Maximum Junction Temperature	125°C
Operating Temperature Range (Measured at the Exposed Pad)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

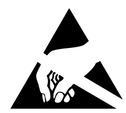
θ_{JC} is the conduction thermal resistance from junction to case, where the case temperature is measured at the bottom of the package.

The thermal resistance value specified in Table 5 is simulated based on JEDEC specifications (unless specified otherwise) and must be used in compliance with JESD51-12.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-24-17	9.6	°C/W

ESD CAUTION

	**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

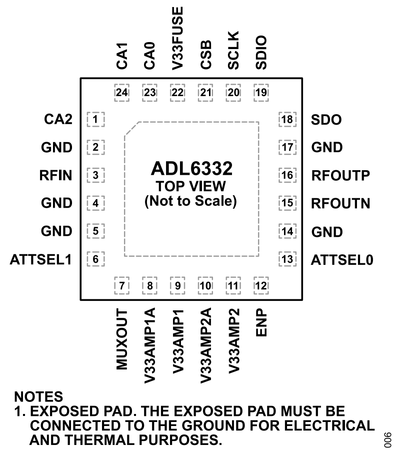


Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	CA2	Input	SPI Chip Address (MSB).
2, 4, 5, 14, 17	GND	Input/Output	Ground Reference.
3	RFIN	Input	Single-Ended RF Input.
6	ATTSEL1	Input	Preprogrammed Mode Selection (A, B, C, and D State).
7	MUXOUT	Output	Voltage Measurement Pin for Reading Chip Temperature. Leave as no connect when not in use.
8	V33AMP1A	Input	Analog 3.3 V Power-Supply Input for AMP1.
9	V33AMP1	Input	Analog 3.3 V Power-Supply Input for AMP1.
10	V33AMP2A	Input	Analog 3.3 V Power-Supply Input for AMP2.
11	V33AMP2	Input	Analog 3.3 V Power-Supply Input for AMP2.
12	ENP	Input	Power Up/Enable Input. Active High.
13	ATTSEL0	Input	Preprogrammed Mode Selection (A, B, C, and D State).
15	RFOUTN	Output	Negative Side of Balanced Differential RF Output.
16	RFOUTP	Output	Positive Side of Balanced Differential RF Output.
18	SDO	Output	Serial-Port Data Output.
19	SDIO	Input/Output	Serial-Port Bidirectional Data Input/Output.
20	SCLK	Input	Serial-Port Clock Input.
21	CSB	Input	Serial-Port Enable Input. Active low.
22	V33FUSE	Input	Digital 3.3 V Power-Supply Input.
23	CA0	Input	SPI Chip Address (LSB).
24	CA1	Input	SPI Chip Address.
	EPAD	Input/Output	Exposed Pad. The exposed pad must be connected to ground for electrical and thermal purposes.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{33AMP1} = $V_{33AMP1A}$ = V_{33AMP2}= $V_{33AMP2A}$ = V_{33FUSE} = 3.3 V, and T_A = 25°C, unless otherwise noted.

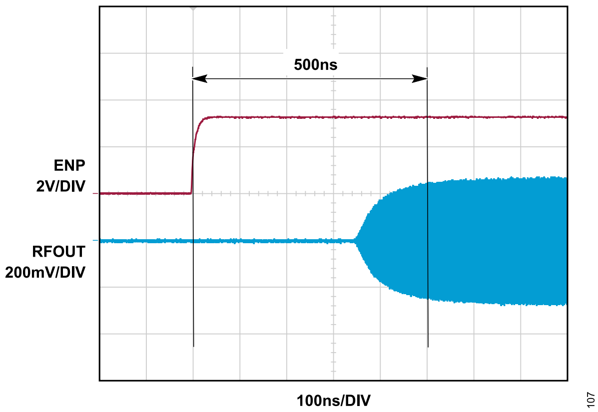


Figure 7. ENP Enable Response at Fixed Gain Mode, Minimum DSA Attenuation

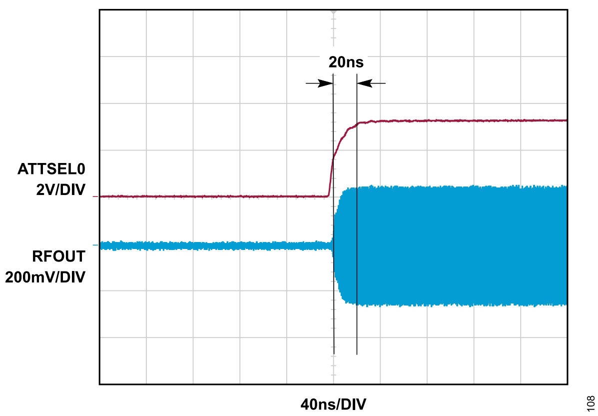


Figure 8. Gain Settling Time at Fixed Gain Mode, DSA from 24.0 dB to 0.0 dB

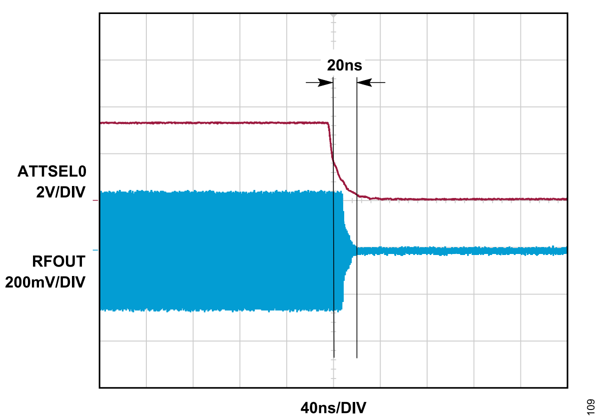


Figure 9. Gain Settling Time at Fixed Gain Mode, DSA from 0.0 dB to 24.0 dB

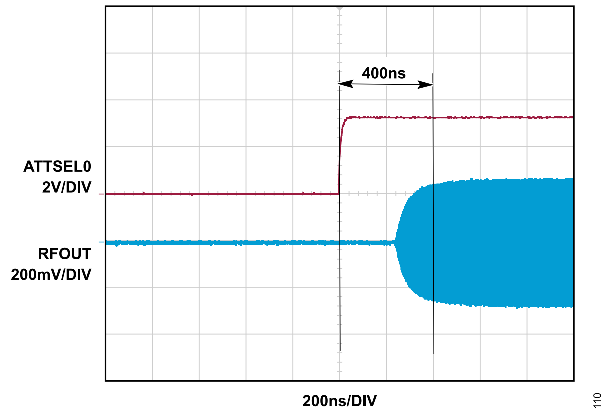


Figure 10. Gain Settling Time from Minimum Gain (AMP1/AMP2 Bypass and DSA = 24.0 dB) to Maximum Gain (No AMP Bypass and DSA = 0.0 dB)

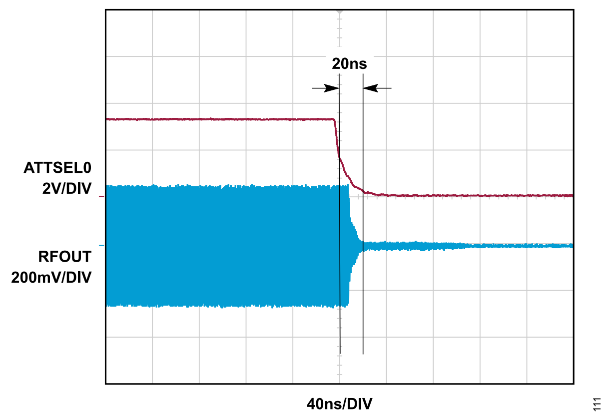


Figure 11. Gain Settling Time from Maximum Gain (NO AMP Bypass and DSA = 0.0 dB) to Minimum Gain (AMP1/AMP2 Bypass and DSA = 24.0 dB)

TYPICAL PERFORMANCE CHARACTERISTICS

ADL6332-A

V33AMP1 voltage (V_{33AMP1}) = V33AMP1A voltage ($V_{33AMP1A}$) = V33AMP2 voltage (V_{33AMP2}) = V33AMP2A voltage ($V_{33AMP2A}$) = V33FUSE voltage (V_{33FUSE}) = 3.3 V, T_A = 25°C, fixed gain mode, DSA attenuation = 0 dB, source resistance (R_S) = 50 Ω single-ended, load resistance (R_L) = 50 Ω differential, unless otherwise noted.

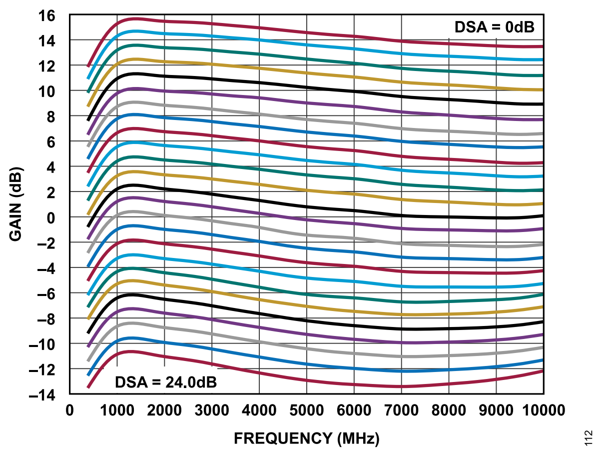


Figure 12. Gain vs. Frequency; 1.0 dB DSA Steps

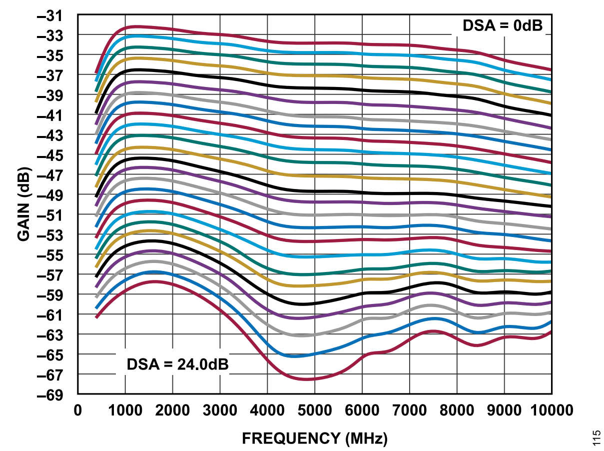


Figure 15. Gain vs. Frequency; 1.0 dB DSA Steps , AMP1 and AMP2 Bypass

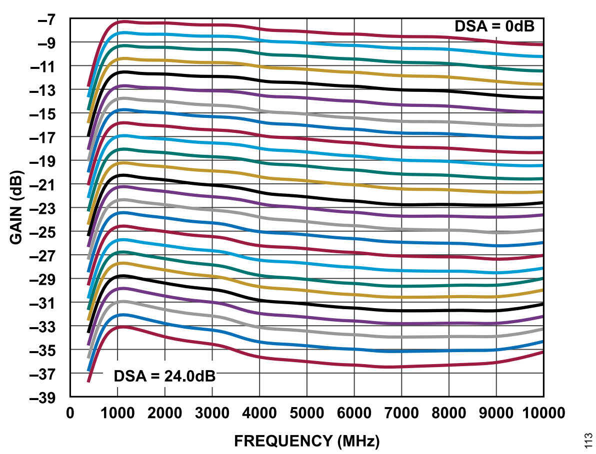


Figure 13. Gain vs. Frequency; 1.0 dB DSA Steps , AMP2 Bypass

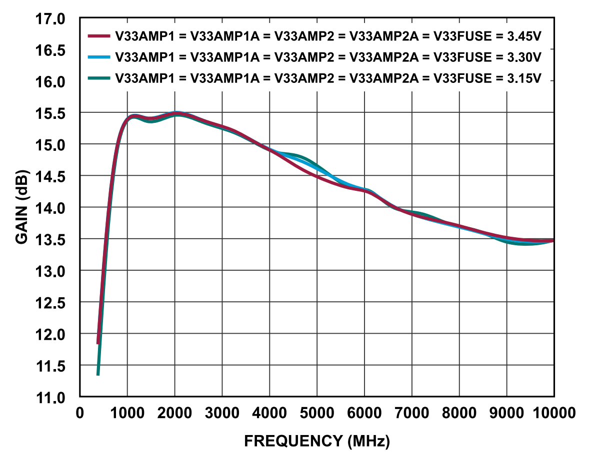


Figure 16. Gain vs. Frequency for Various Supplies

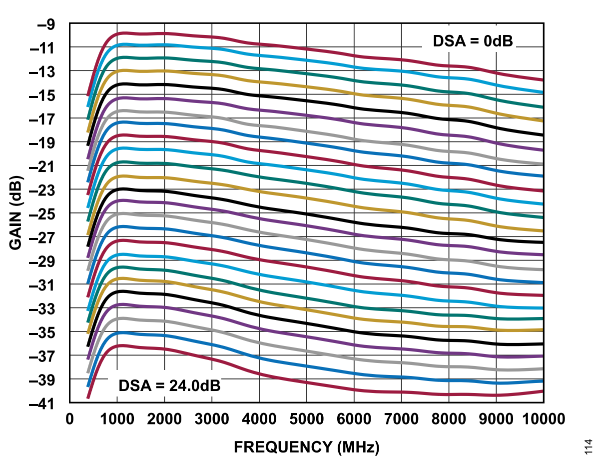


Figure 14. Gain vs. Frequency; 1.0 dB DSA Steps , AMP1 Bypass

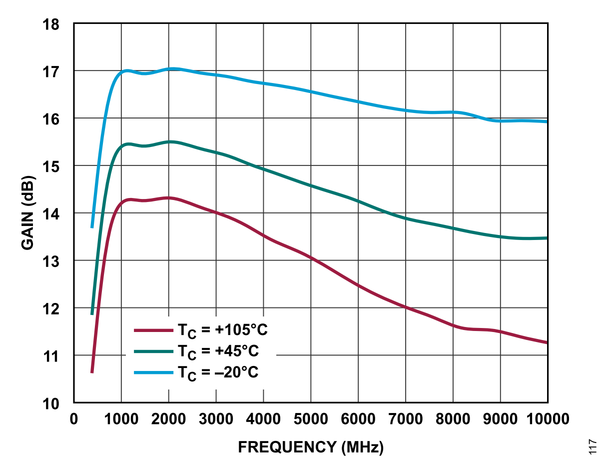


Figure 17. Gain vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

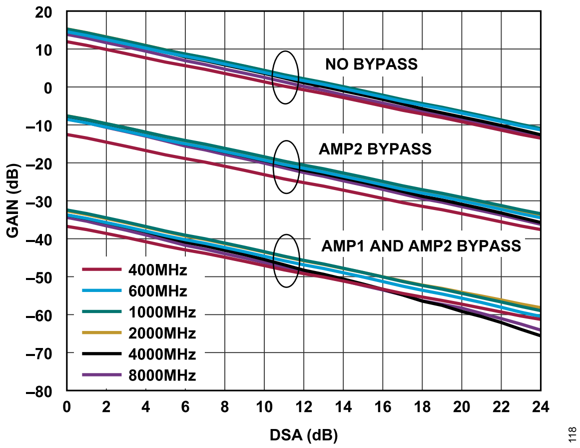


Figure 18. Gain vs. 1.0 dB DSA Steps for Various Frequencies, AMP2 Bypass

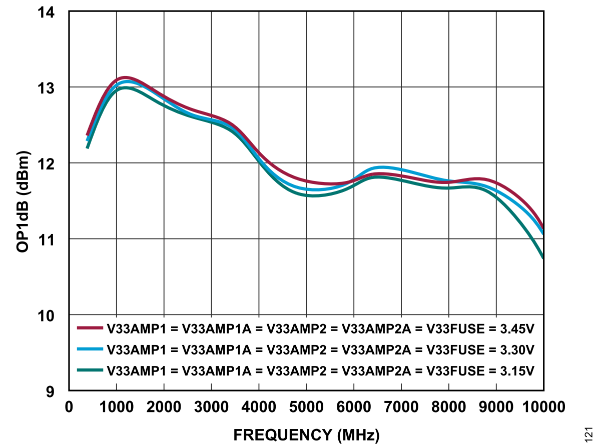


Figure 21. OP1dB vs. Frequency for Various Supplies

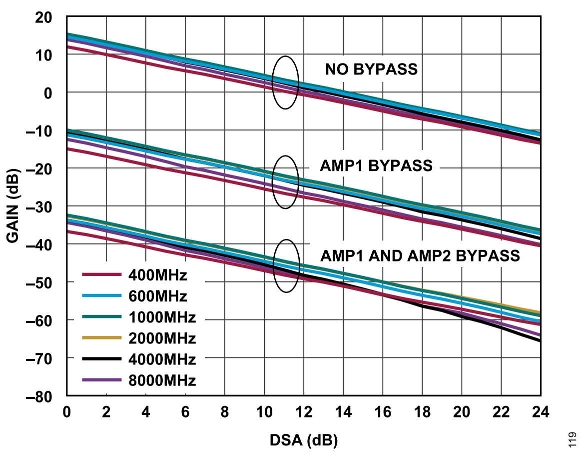


Figure 19. Gain vs. 1.0 dB DSA Steps for Various Frequencies, AMP1 Bypass

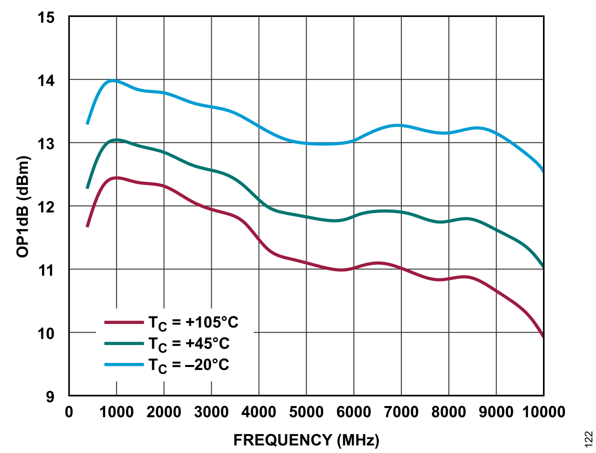


Figure 22. OP1dB vs. Frequency for Various Temperatures

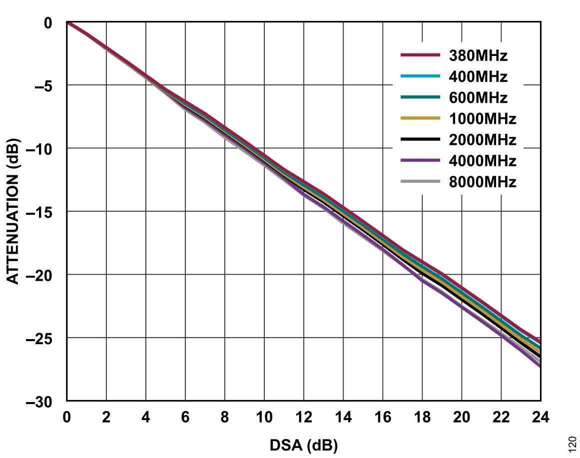


Figure 20. Attenuation vs. DSA for Various Frequencies

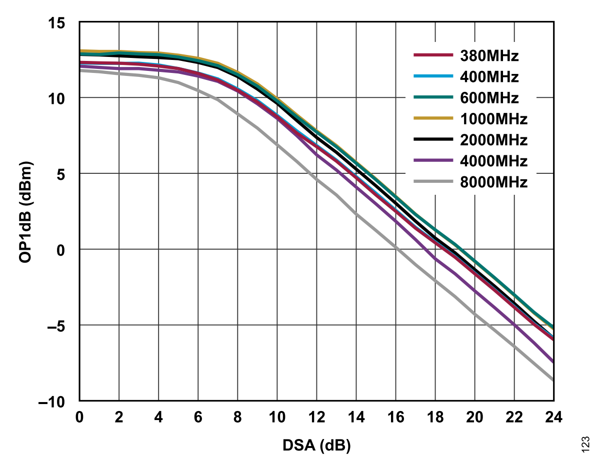


Figure 23. OP1dB vs. 1.0 dB DSA Steps for Various Frequencies

TYPICAL PERFORMANCE CHARACTERISTICS

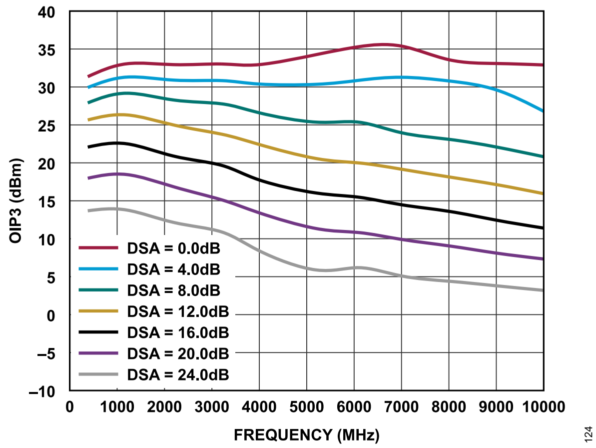


Figure 24. OIP3 vs. Frequency at Various DSA Values

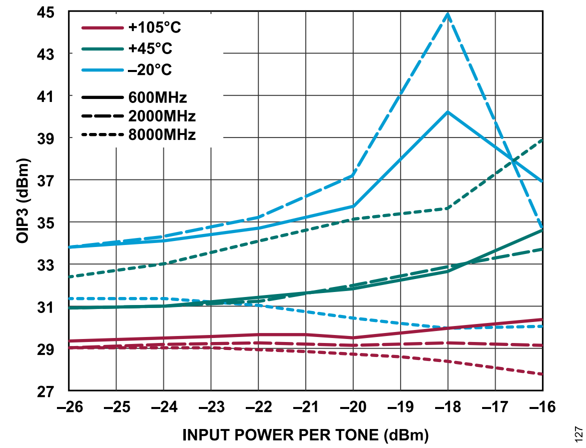


Figure 27. OIP3 vs. Input Power Per Tone for Various Temperatures at 600 MHz, 2000 MHz, and 8000 MHz

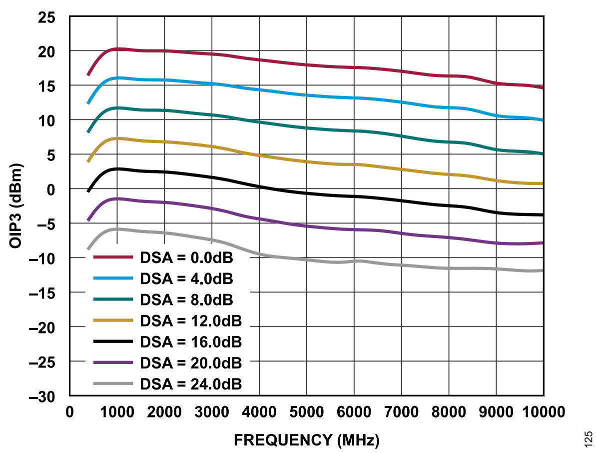


Figure 25. OIP3 vs. Frequency at Various DSA Values, AMP1 Bypass

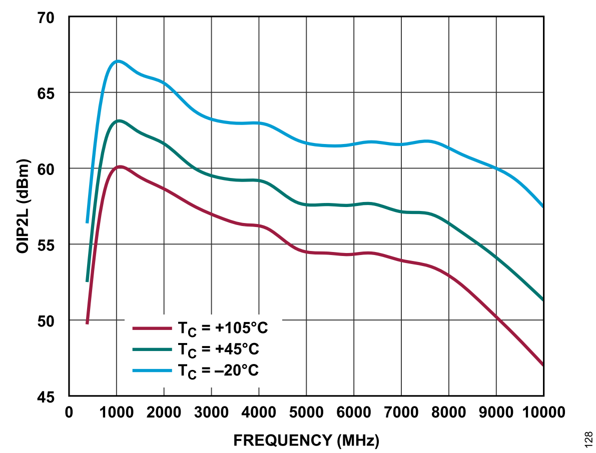


Figure 28. OIP2L vs. Frequency for Various Temperatures

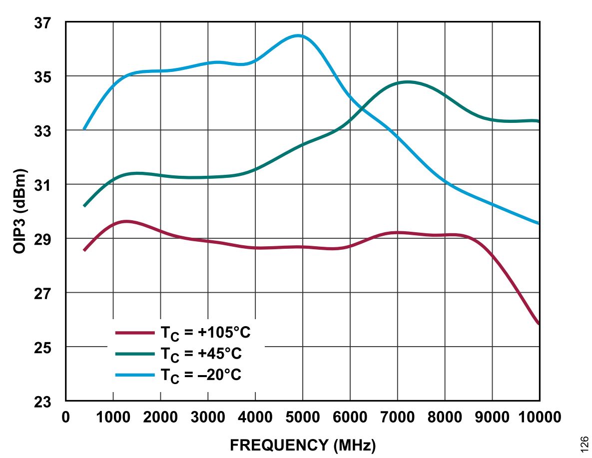


Figure 26. OIP3 vs. Frequency for Various Temperatures

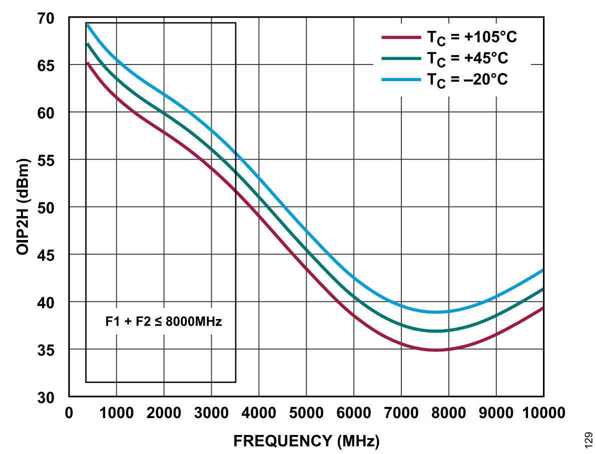


Figure 29. OIP2H vs. Frequency for Various Temperatures, Tone Spacing Equals to 1010 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

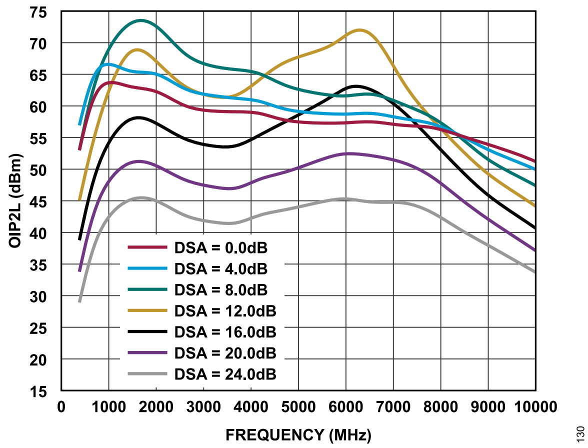


Figure 30. OIP2L vs. Frequency at Various DSA Values

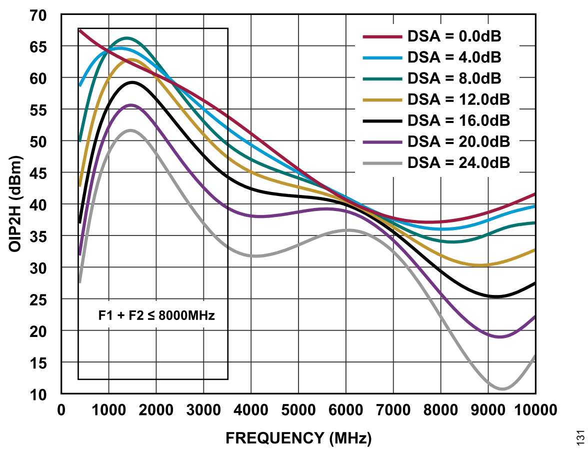


Figure 31. OIP2H vs. Frequency at Various DSA Values, Tone Spacing Equals to 1010 MHz

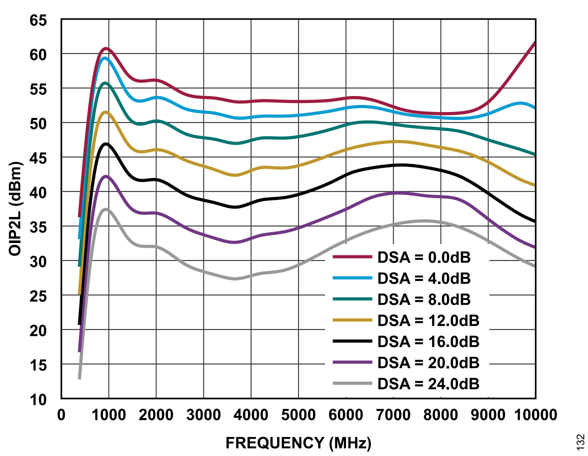


Figure 32. OIP2L vs. Frequency at Various DSA Values, AMP1 Bypass

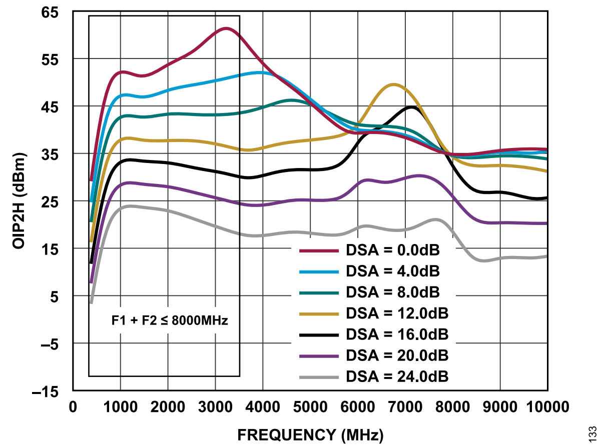


Figure 33. OIP2H vs. Frequency at Various DSA Values, AMP1 Bypass, Tone Spacing Equals to 1010 MHz

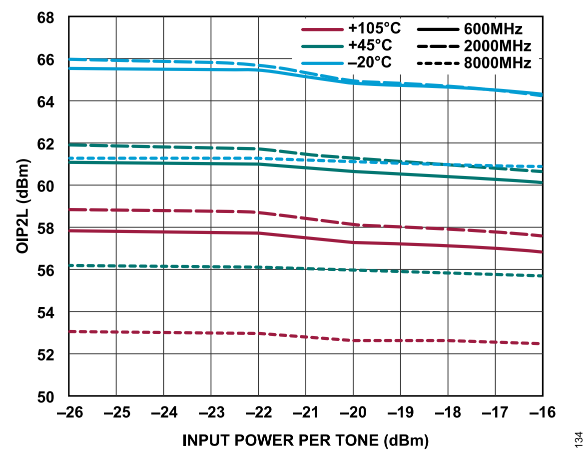


Figure 34. OIP2L vs. Input Power per Tone for Various Temperatures at 600 MHz, 2000 MHz, and 8000 MHz

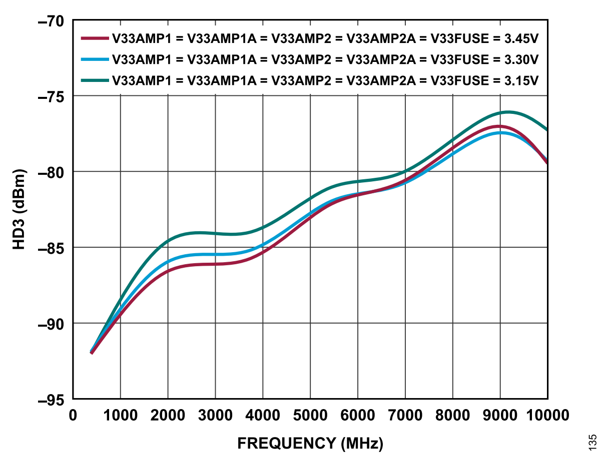


Figure 35. Third Harmonic Distortion (HD3) vs. Frequency for Various Supplies

TYPICAL PERFORMANCE CHARACTERISTICS

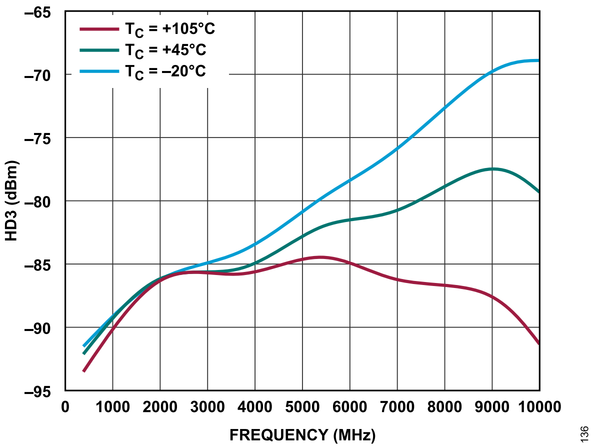


Figure 36. HD3 vs. Frequency for Various Temperatures

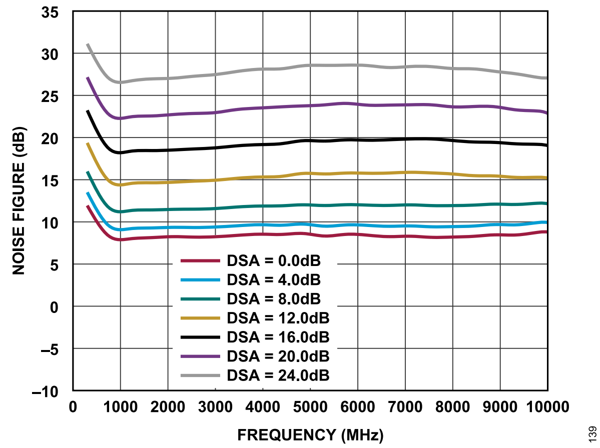


Figure 39. Noise Figure vs. Frequency at Various DSA Values

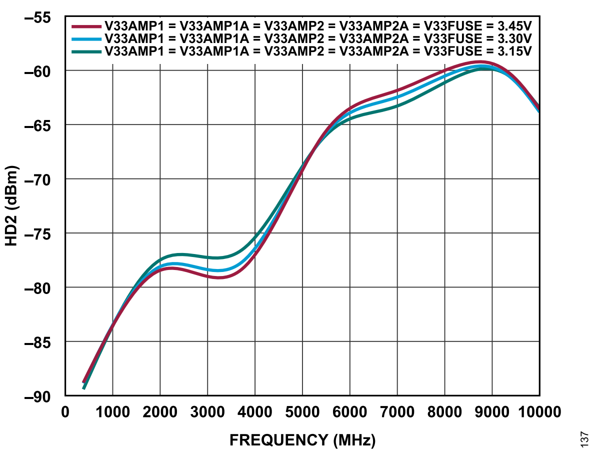


Figure 37. Second Harmonic Distortion (HD2) vs. Frequency for Various Supplies

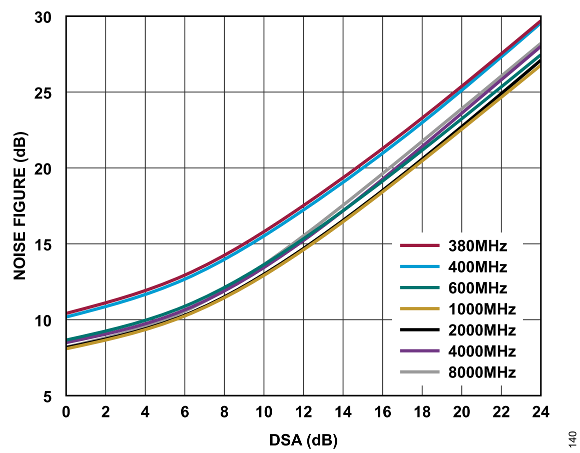


Figure 40. Noise Figure vs. 1.0 dB DSA Steps for Various Frequencies

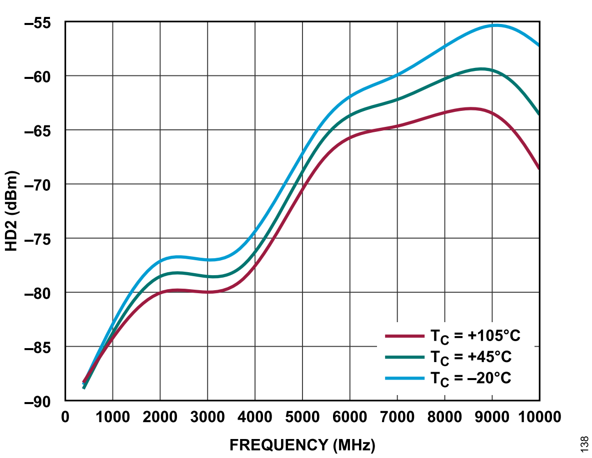


Figure 38. HD2 vs. Frequency for Various Temperatures

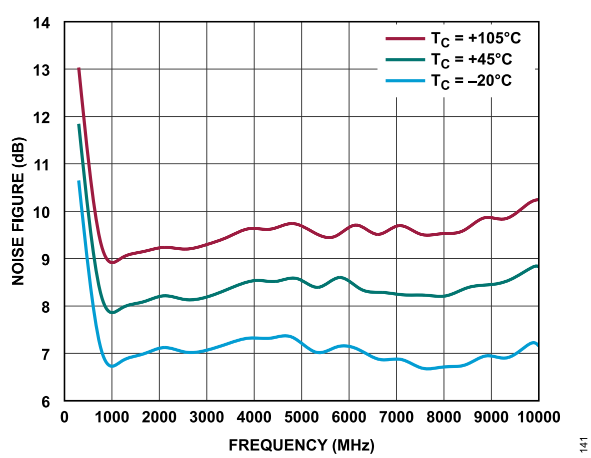


Figure 41. Noise Figure vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

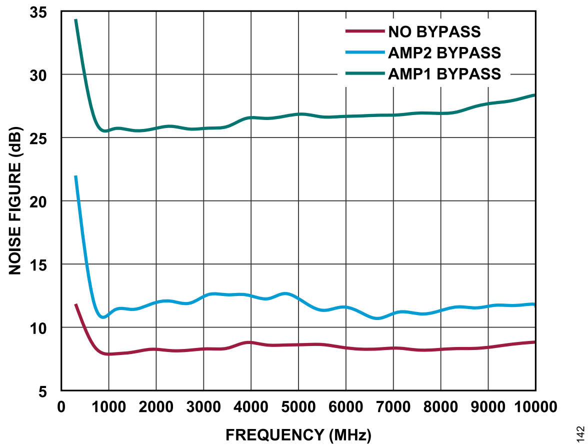


Figure 42. Noise Figure vs. Frequency for Various Bypass Modes

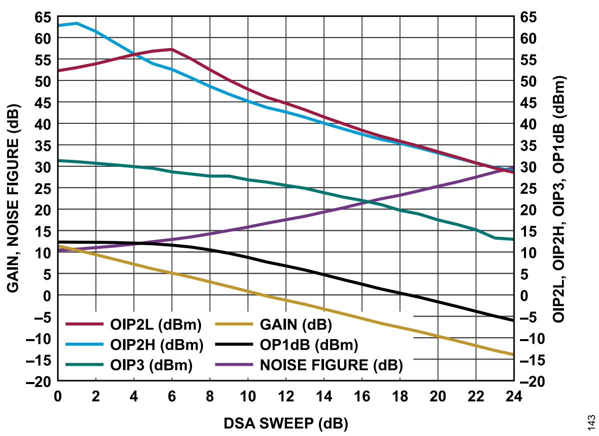


Figure 43. Gain, Noise Figure, OIP2L, OIP2H, OIP3, OP1dB vs. DSA Sweep, Frequency = 380 MHz

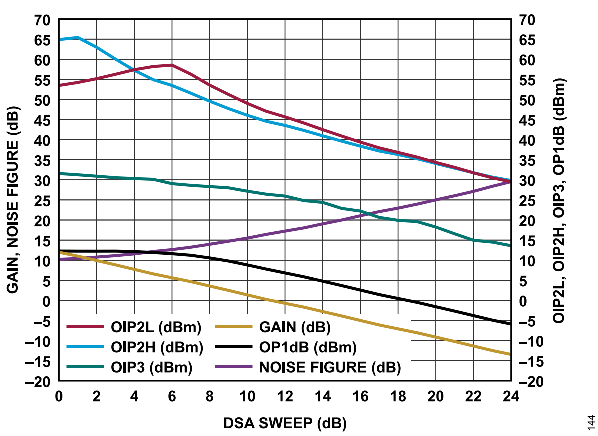


Figure 44. Gain, Noise Figure, OIP2L, OIP2H, OIP3, OP1dB vs. DSA Sweep, Frequency = 400 MHz

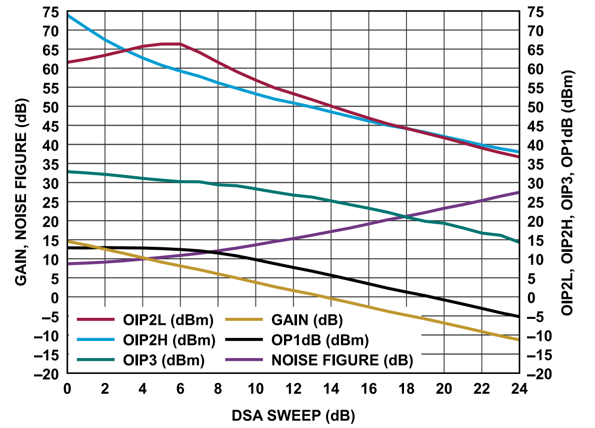


Figure 45. Gain, Noise Figure, OIP2L, OIP2H, OIP3, OP1dB vs. DSA Sweep, Frequency = 600 MHz

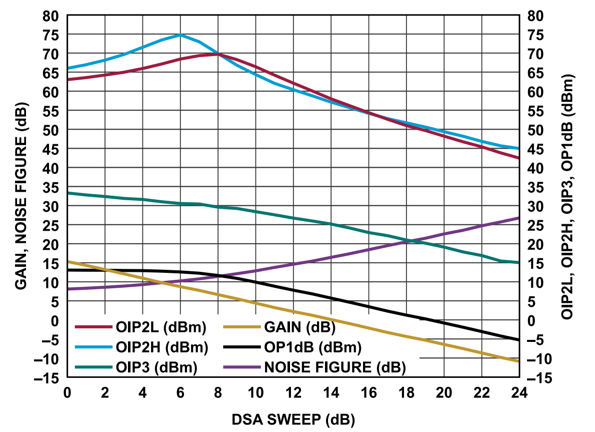


Figure 46. Gain, Noise Figure, OIP2L, OIP2H, OIP3, OP1dB vs. DSA Sweep, Frequency = 1000 MHz

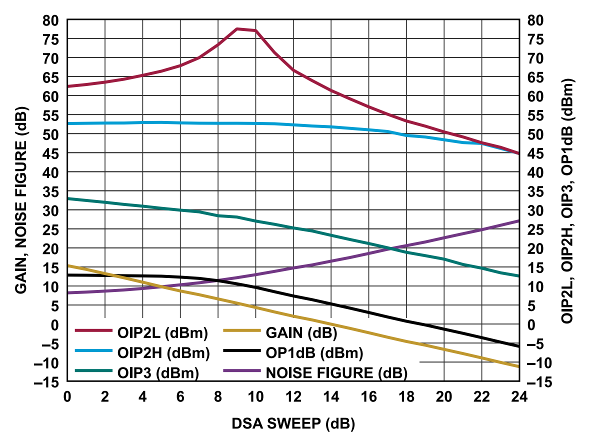


Figure 47. Gain, Noise Figure, OIP2L, OIP2H, OIP3, OP1dB vs. DSA Sweep, Frequency = 2000 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

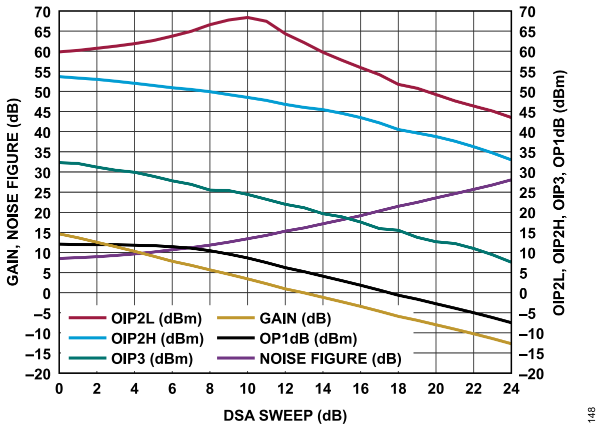


Figure 48. Gain, Noise Figure, OIP2L, OIP2H, OIP3, OP1dB vs. DSA Sweep, Frequency = 4000 MHz

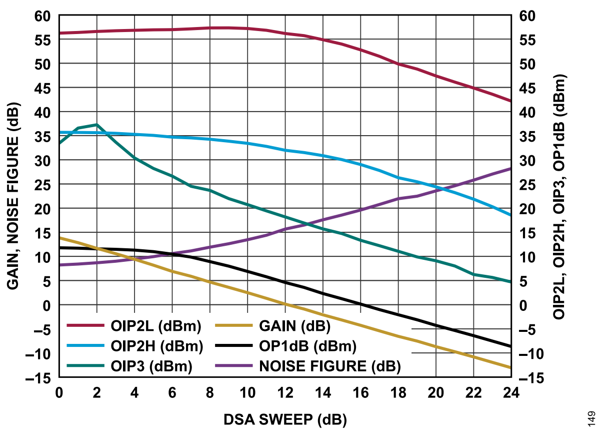


Figure 49. Gain, Noise Figure, OIP2L, OIP2H, OIP3, OP1dB vs. DSA Sweep, Frequency = 8000 MHz

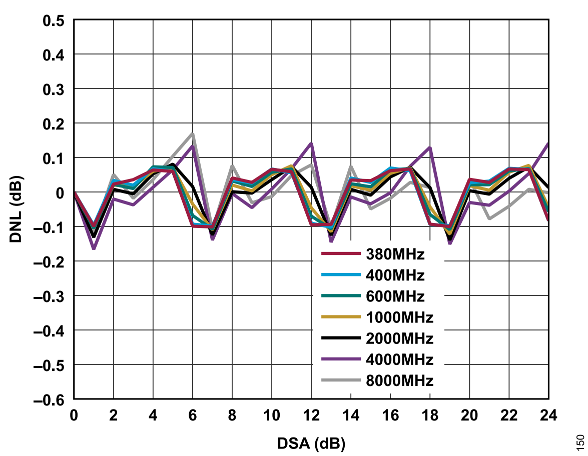


Figure 50. DSA Gain Step Error

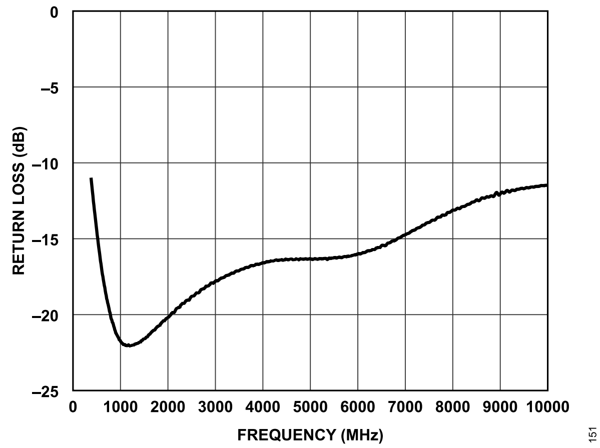


Figure 51. Return Loss of Single-Ended RF Input S11 at 50 Ω Match

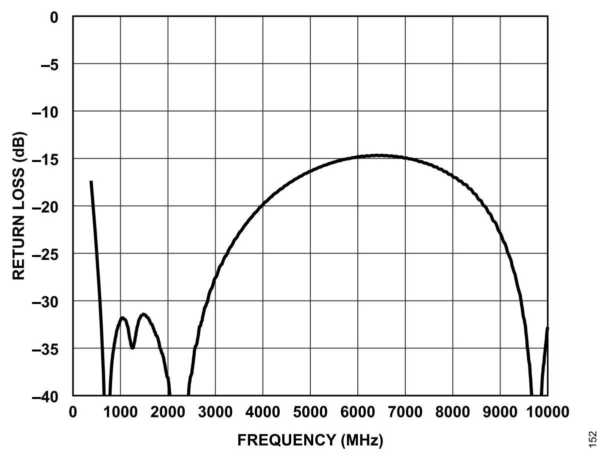


Figure 52. Return Loss of Differential RF Output S22 at 50 Ω Match

THEORY OF OPERATION

The ADL6332 integrates two amplifiers with fixed gain (AMP1 ≈ 12 dB and AMP2 ≈ 10 dB) and a DSA, which is adjustable from 0 dB to 24 dB in 1 dB step. The AMP1 and AMP2 have a bypass attenuation mode, which allows to disable these amplifiers individually and route the RF signals through the fixed 12 dB attenuators. When an amplifier is configured in the bypass attenuation mode, the gain drops by approximately 24 dB for AMP1 and 22 dB for AMP2 (delta gain from AMP enabled to bypass attenuation mode); therefore, enabling an overall gain control range of 70 dB in 1 dB step when used with the 24 dB DSA.

Additionally, in the bypass attenuation mode, the amplifiers' current drops to almost zero.

All circuit blocks of the ADL6332, as shown in Figure 53, are programmable through the SPI.

RF INPUT AND OUTPUT

The ADL6332 input impedance is 50 Ω single-ended, and the output impedance is 50 Ω differential, which provides an interface from a 50 Ω single-ended LNA to RF-ADCs with 50 Ω differential input impedance in a signal chain without any matching networks.

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The register map can be subdivided into seven functional groups, as shown in Table 7. See the Register Summary section for a complete list of all the registers on the ADL6332.

Table 7. Memory Map Functional Groups

Register Address	Functional Blocks
0x000 to 0x011	SPI configuration
0x100 to 0x101	Function enable
0x104 to 0x109	AMP1 performance trimming and tuning
0x10A to 0x10D	RF path four preconfigurations: AMP1, AMP2, fixed gain/bypass, DSA attenuation
0x10F to 0x115	AMP2 performance trimming and tuning
0x120 to 0x121	Auxiliary mux selection (debug only), SPI supply control
0x140 to 0x145	FUSE space. Read only. Trimmed parameters for AMP1 and AMP2 are stored.

FUNCTION AND SIGNAL PATH ENABLE

The enable bits for each circuit block are in registers 0x100 and 0x101 (Table 8 and Table 9). Figure 53 shows a breakdown of the individual blocks highlighted in red that have corresponding enable controls in registers 0x100 and 0x101. ENP pin 12 is a primary enable pin for the ADL6332 and is active high. The bits in the enable registers can be configured independent of the state of ENP.

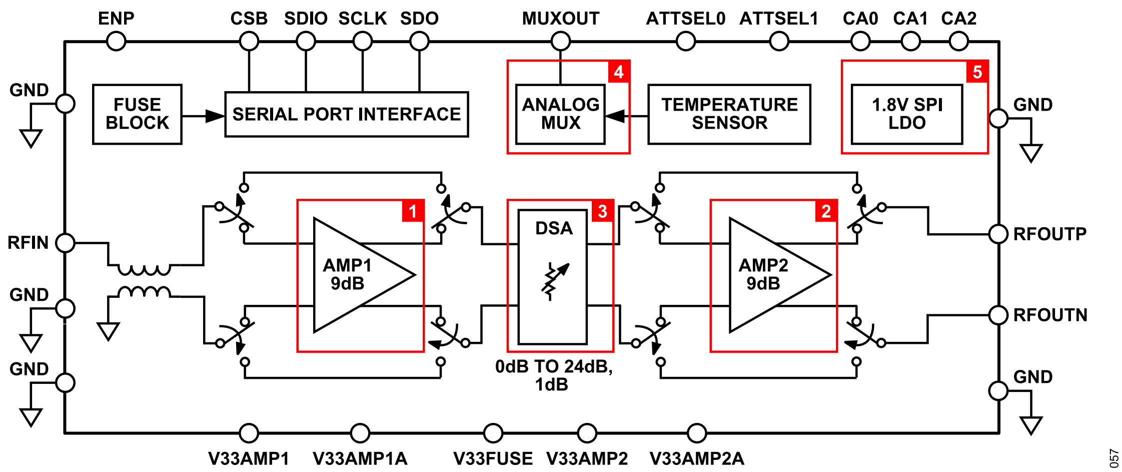

Figure 53. Signal Path Enable Block Diagram

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Table 8. Register 0x100: Enable Register for MUX and LDO

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	AMUX_BG_EN	AMUX Bandgap Enable. If MUXOUT pin 7 is not used, set to 0. 0: Disable AMUX Bandgap. 1: Enable AMUX Bandgap.	0x1	R/W
3	RESERVED	Reserved	0x0	R
2	RESERVED	Reserved	0x0	R/W
1	RESERVED	Reserved	0x0	R
0	LDO18_EN	1.8V LDO Enable for AMUX block. If MUXOUT pin 7 is not used, set to 0. 0: Disable 1: Enable	0x1	R/W

Table 9. Register 0x101: Enable Register for AMP1/AMP2 and DSA

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	AMP2_EN	AMP2 Enable . 0: Disable 1: Enable	0x0	R/W
1	RESERVED	DSA Enable. 0: Disable 1: Enable	0x0	R/W
0	LDO18_EN	AMP1 Enable. 0: Disable 1: Enable	0x0	R/W

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AMP1 AND AMP2 TRIMMING AND TUNING

Initial optimization of the amplifiers is performed at the factory and the optimized/trimmed parameters are stored in the non-volatile memory (NVM) referred to as the FUSE block. When the MSB in registers 0x104, 0x105, 0x106 for AMP1 and in registers 0x110, 0x111, 0x112 for AMP2 is 1 (default), the factory trimmed parameters are automatically used in the operation (normal operation mode). These values are readable in registers 0x140, 0x141, 0x142, 0x143, 0x144, 0x145 (Table 16). When the MSB in registers 0x104, 0x105, 0x106 for AMP1 and 0x110, 0x111, 0x112 for AMP2 is set to 0, the following registers are tunable. Use the default (reset) values in 0x103 to 0x115 registers in Table 10. If the lower current consumption is required, see the Applications Information section.

- AMP1_IGREF in register 0x104
- AMP1_IDREF_Z in register 0x105
- AMP1_IDREF_P in register 0x106
- AMP2_IGREF in register 0x110
- AMP2_IDREF_Z in register 0x111
- AMP2_IDREF_P in register 0x112

Table 10. AMP1 and AMP2 Trimming and Tuning Register

Reg	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x103	[7:0]	RESERVED				AMP1_MON_EN	AMP1_CROSS_EN	AMP1_IM3_EN	AMP1_LP_MODE
0x104	[7:0]	NVM_TRM_AMP1_IGREF	RESERVED			AMP1_IGREF			
0x105	[7:0]	NVM_TRM_AMP1_IDREF_Z	RESERVED	AMP1_IDREF_Z					
0x106	[7:0]	NVM_TRM_AMP1_IDREF_P	RESERVED			AMP1_IDREF_P			
0x107	[7:0]	RESERVED		AMP1_CROSS_Z					
0x108	[7:0]	RESERVED				AMP1_CROSS_P			
0x109	[7:0]	SPARE_010B				AMP1_IM3_CAP			
0x10F	[7:0]	RESERVED				AMP2_MON_EN	AMP2_CROSS_EN	AMP2_IM3_EN	AMP2_LP_MODE
0x110	[7:0]	NVM_TRM_AMP2_IGREF	RESERVED			AMP2_IGREF			
0x111	[7:0]	NVM_TRM_AMP2_IDREF_Z	RESERVED	AMP2_IDREF_Z					
0x112	[7:0]	NVM_TRM_AMP2_IDREF_P	RESERVED			AMP2_IDREF_P			
0x113	[7:0]	RESERVED		AMP2_CROSS_Z					
0x114	[7:0]	RESERVED				AMP2_CROSS_P			
0x115	[7:0]	SPARE_011B				AMP2_IM3_CAP			

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RF PATH PRECONFIGURATION

ADL6332 has four preconfigurable RF gain settings, which are selected with the ATTSEL0 and ATTSEL1 pins. The configurable parameters (fixed gain or bypass attenuation mode in AMP1 and AMP2, and DSA attenuation level) are stored in four register spaces (Table 11, Table 12, Table 13, Table 14, Table 15), which are called RF State A, B, C, and D.

- State A: SIG_PATH0_2 in Register 0x10A

- State B: SIG_PATH1_2 in Register 0x10B

- State C: SIG_PATH2_2 in Register 0x10C

- State D: SIG_PATH3_2 in Register 0x10D

Each mode can configure the full RF chain after reset is asserted. Table 11 shows the default settings for each mode. Overwrite the parameters before or during operation.

This feature allows to switch the RF performance rapidly using asynchronous external control.

Table 11. Four Preconfiguration Registers with Default/Reset RF Parameters

						Bit 7	Bit 6	
RF State	**ATTSEL1 (Pin 6)**	**ATTSEL0 (Pin 13)**	**Reg. Address**	**Reg. Name**	**Bits**	**AMP2 Setting: Bypass Attenuation/ Fixed Gain**	**AMP1 Setting: Bypass Attenuation/ Fixed Gain**	**Bits[5:0], DSA Setting 0 dB to 24.0 dB at 1.0 dB Step**
A	0	0	0x10A	SIG_PATH0_2	[7:0]	Default = Bypass Attenuation	Default = Bypass attenuation	Default = 24.0 dB Attenuation
B	0	1	0x10B	SIG_PATH1_2	[7:0]	Default = Fixed Gain	Default = Fixed Gain	Default = 16.0 dB Attenuation
C	1	0	0x10C	SIG_PATH2_2	[7:0]	Default = Fixed Gain	Default = Fixed Gain	Default = 8.0 dB Attenuation
D	1	1	0x10D	SIG_PATH3_2	[7:0]	Default = Fixed Gain	Default = Fixed Gain	Default = 0.0 dB Attenuation

Table 12. Register 0x10A: State A

Bits	Bit Name	Description	Reset	Access
7	AMP2_BYPASS0	Amp 2 Bypass State A Setting. 0: Fixed gain mode **1: Bypass attenuation mode**	**0x1**	R/W
6	AMP1_BYPASS0	Amp 1 Bypass State A Setting. 0: Fixed gain mode **1: Bypass attenuation mode**	**0x1**	R/W
[5:0]	DSA_ATTN0	DSA Attenuator State A Setting. 0: 0 dB 1: 1 dB 2: 2 dB ... **24: 24 dB**	**0x18**	R/W

Table 13. Register 0x10B: State B

Bits	Bit Name	Description	Reset	Access
7	AMP2_BYPASS1	Amp 2 Bypass State B Setting. **0: Fixed gain mode** 1: Bypass attenuation mode	**0x0**	R/W
6	AMP1_BYPASS1	Amp 1 Bypass State B Setting. **0: Fixed gain mode** 1: Bypass attenuation mode	**0x0**	R/W
[5:0]	DSA_ATTN1	DSA Attenuator State B Setting. 0: 0 dB	**0x10**	R/W

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Table 13. Register 0x10B: State B (Continued)

Bits	Bit Name	Description	Reset	Access
		1: 1 dB ... **16: 16 dB** ... 24: 24 dB		

Table 14. Register 0x10C: State C

Bits	Bit Name	Description	Reset	Access
7	AMP2_BYPASS2	Amp 2 Bypass State C Setting. **0: Fixed gain mode** 1: Bypass attenuation mode	**0x0**	R/W
6	AMP1_BYPASS2	Amp 1 Bypass State C Setting. **0: Fixed gain mode** 1: Bypass attenuation mode	**0x0**	R/W
[5:0]	DSA_ATTN2	DSA Attenuator State C Setting. 0: 0 dB 1: 1 dB ... **8: 8 dB** ... 24: 24 dB	**0x8**	R/W

Table 15. Register 0x10D: State D

Bits	Bit Name	Description	Reset	Access
7	AMP2_BYPASS3	Amp 2 Bypass State D Setting. **0: Fixed gain mode** 1: Bypass attenuation mode	**0x0**	R/W
6	AMP1_BYPASS3	Amp 1 Bypass State D Setting. **0: Fixed gain mode** 1: Bypass attenuation mode	**0x0**	R/W
[5:0]	DSA_ATTN3	DSA Attenuator State D Setting. **0: 0 dB** 1: 1 dB ... 24: 24 dB	**0x0**	R/W

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AUXILIARY MUX OUT/TEMPERATURE SENSOR

The ADL6332 has multiple auxiliary mux control blocks that allow various modes of operation and monitoring point. All are available, but many parameters are used for monitoring during the manufacturing process by ADI. The default (reset) register configuration allows to monitor an internal voltage that is proportional to temperature, which can be used to track temperature changes from MUXOUT pin 7. If there is no need to use the temperature sensor feature, it may be disabled by setting zeros in AMUX_BG_EN[4] and LDO18_EN[0] at 0x100 register.

NVM (FUSE) SPACE (REFERENCE ONLY)

Non-volatile memory (NVM) space is invisible but values from NVM are loaded to registers 0x140, 0x141, 0x142, 0x143, 0x144, 0x145 (Table 16), and these values are used when the MSB in registers 0x104, 0x105, 0x106 for AMP1 and 0x110, 0x111, 0x112 for AMP2 is 1 (default/reset).

Table 16. NVM Register

Reg. Address	Reg. Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x140	FUSE_READBACK_0	[7:0]	RESERVED				TRM_AMP1_IGREF_RDBK			
0x141	FUSE_READBACK_1	[7:0]	RESERVED		TRM_AMP1_IDREF_Z_RDBK					
0x142	FUSE_READBACK_2	[7:0]	RESERVED				TRM_AMP1_IDREF_P_RDBK			
0x143	FUSE_READBACK_3	[7:0]	RESERVED				TRM_AMP2_IGREF_RDBK			
0x144	FUSE_READBACK_4	[7:0]	RESERVED		TRM_AMP2_IDREF_Z_RDBK					
0x145	FUSE_READBACK_5	[7:0]	RESERVED				TRM_AMP2_IDREF_P_RDBK			

SERIAL PORT INTERFACE (SPI)

The SPI of the ADL6332 allows to configure the device for specific functions or operations through 3-wire or 4-wire SPI mode. This serial port interface consists of four control lines: SCLK, SDIO, SDO, and CSB for 4-wire SPI mode. SCLK, SDIO, and CSB are used for 3-wire SPI mode, which is the default state for the SPI mode. To enable 4-wire SPI mode, set SDOACTIVE[3] and SDOACTIVE_[4] in register 0x000 to 1. Table 3 shows the timing requirements for the SPI port.

The ADL6332 protocol consists of a read/write bit, four chip address bits (MSB is always 0), nine register address bits, followed by eight data bits. Both the address and data fields are organized with the MSB first and end with the LSB by default. To address the device correctly, the chip address prefix bits must match the externally configured chip address pins CA2, CA1, and CA0.

The ADL6332 input logic levels to write to the SPI are 1.8 V or 3.3 V.

On a readback cycle, the SDO is configurable for either 1.8 V (default) or 3.3 V readback output levels by setting SPI_1P8_3P3_CTRL bit (register 0x121, bit 4).

CONFIGURING MULTIPLE CHIPS TO SHARE THE SPI BUS

Up to eight ADL6332 devices can be addressed using the same 3-wire or 4-wire SPI, using a single CSB line for all devices. For this capability, the chip address pins (CA2, CA1, CA0) of the ADL6332 are used to identify the chip with the SPI write chip address prefix (see the SPI port as shown in Figure 2).

The ADL6332 ignores any writes to addresses where the four MSBs are not equal to the chip address as set by the chip address pins and only accepts access for addresses where the four MSB chip address prefix bits are equal to the chip address pins. The only exception is the software reset in the address 0x000. All ADL6332 chips on the shared bus accept 0x81 software reset in 0x000 register from the SPI host controller.

Figure 54 shows how to configure the chip address pins CA2, CA1, and CA0 with the associated chip address prefix bits.

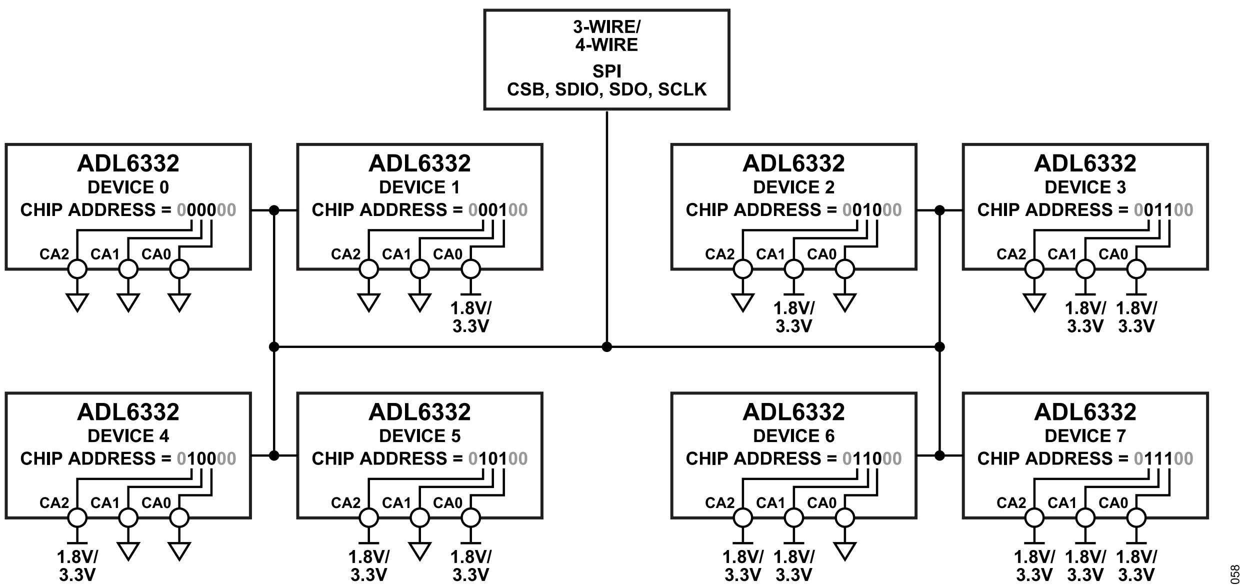


Figure 54. Multiple Chip Configuration to Share SPI Bus

SERIAL PORT INTERFACE (SPI)

INITIALIZATION SEQUENCE

ADL6332 has a built-in initialization sequence triggered by software reset to correctly load data from the NVM into memory for normal amplifier operation. The calibrated/trimmed settings for AMP1 and AMP2 are programmed in Analog Devices' factory and stored in NVM before shipping. After a software reset is performed, the data in the NVM must be loaded into the digital registers 0x140 to 0x145 for operation. This loading process takes four SPI cycles, write or read, after the software reset is asserted. The loading process is independent of the state of the ENP pin, high or low.

The full procedure for initializing the part is:

1. Supply 3.3 V.
2. Apply software reset.
3. Send four SPI commands to ADL6332, read or write.

The software reset, sending 0x81 in register 0x000, is always recommended right after 3.3 V is supplied.

Example 1 (Table 17):

After 3.3 V is supplied:

1. Write 0x81 in register 0x000 for the software reset.
2. Write 0x18 in register 0x000 for configuring 4-wire SPI mode.
3. Write 0x01 in register 0x00A: Scratch pad.
4. Write 0x02 in register 0x00A: Scratch pad.
5. Write 0x03 in register 0x00A: Scratch pad.
6. Write 0x07 in register 0x101 for enabling AMP2, DSA, and AMP1 to start the normal amplifier operation.

Register 0x00A is called 'Scratch Pad', which is a read and write register for SPI communication testing. It does not affect any performance in the ADL6332.

After four write cycles are sent, the data in registers 0x140 to 0x145 are correctly loaded for use in operation.

Example 1 is the basic sequence to start ADL6332 in normal operation. After the sequence is complete, the registers are set to default configuration. It is recommended to enable AMP2, DSA, and AMP1 in register 0x101, in the last SPI cycle in step 6 to avoid any unexpected output signals from ADL6332 when ENP pin is set to high together with the 3.3 V supply.

Table 17. Example 1: SPI Command Writes

Address	Write Data	Notes
0x000	0x81	Software reset
0x000	0x18	1st Cycle: Configure 4-wire SPI mode.
0x00A	0x01	2nd Cycle: Scratch pad writing. Any data is fine.
0x00A	0x02	3rd Cycle: Scratch pad writing. Any data is fine.
0x00A	0x03	4th Cycle: Scratch pad writing. Any data is fine.
0x101	0x07	The data in registers 0x140 to 0x145 are correctly loaded to use for operation. Enable AMP2, DSA, AMP1 functions to start operations. Default register values are used for RF performance.

BASIC CONNECTIONS

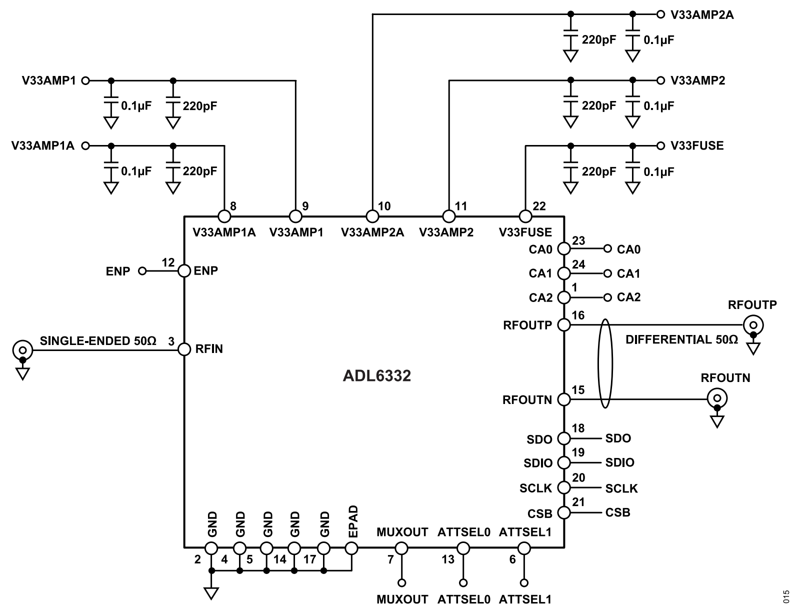


Figure 55. Basic Connections

Table 18. Basic Connections

Functional Blocks	Pin No.	Mnemonic	Description	Basic Connection
3.3 V	8, 9, 10, 11	V33AMP1A, V33AMP1, V33AMP2A, V33AMP2	Amplifier, analog supply voltage	Decouple this pin through 220 pF, 0.1 µF capacitors to ground. Ensure that the decoupling capacitors are located close to the pin.
3.3 V	22	V33FUSE	Digital, DSA, other bias voltage	Decouple this pin through 220 pF, 0.1 µF capacitors to ground. Ensure that the decoupling capacitors are located close to the pin.
Preprogrammed Mode	13, 6	ATTSEL0, ATTSEL1	Preprogrammed mode selection	
RF Input	3	RFIN	RF single-ended input	50 Ω single-ended input. AC-coupled is always recommended.
RF Output	15, 16	RFOUTN, RFOUTP	RF differential output	50 Ω differential outputs. AC-coupled is always recommended.
Serial Port	21	CSB	Active-low chip select	1.8 V to 3.3 V tolerant logic levels.
	20	SCLK	SPI clock	1.8 V to 3.3 V tolerant logic levels.
	18	SDO	SPI data input	1.8 V to 3.3 V tolerant logic levels.
	19	SDIO	SPI date input/output	1.8 V to 3.3 V tolerant logic levels.
Chip Address Selection	23, 24, 1	CA0, CA1, CA2	SPI chip address selects	Chip address selection.
Device Enable	12	ENP	Active-high for normal operation	
Ground	2, 4, 5, 14, 17	GND	Ground	Connect these pins to the ground of the printed circuit board.
EPAD	Exposed pad	Exposed pad	Exposed pad	Exposed pad. The exposed pad must be connected to ground for electrical and thermal purposes.
MUXOUT	7	MUXOUT	Analog voltage output from the temperature sensor	Voltage measurement pin for reading chip temperature. Leave as no connect when not in use.

APPLICATIONS INFORMATION

CURRENT CONSUMPTION OPTIMIZATION

When the MSB in registers 0x104, 0x105, 0x106 for AMP1 and 0x110, 0x111, 0x112 for AMP2 are set to 0, these six registers are tunable. If a lower current consumption is needed, the settings of both AMP1_IGREF in register 0x104 and AMP2_IGREF in register 0x110 can be reduced according to the readback value of IGREF in registers 0x140 and 0x143 for AMP1 and AMP2, respectively (see Figure 56). As a result, the OIP3 performance is degraded, as shown in Figure 57.

It is not recommended to increase the IGREF settings greater than the readback value for AMP1 and AMP2. Doing so could impact the long term reliability of the part.

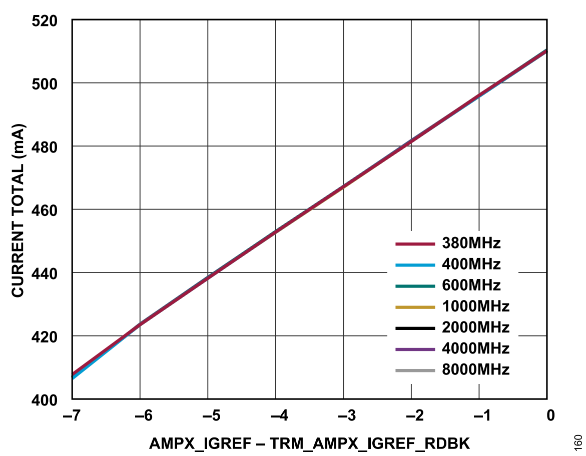


Figure 56. Total Current vs. IGREF Settings for Various Frequencies

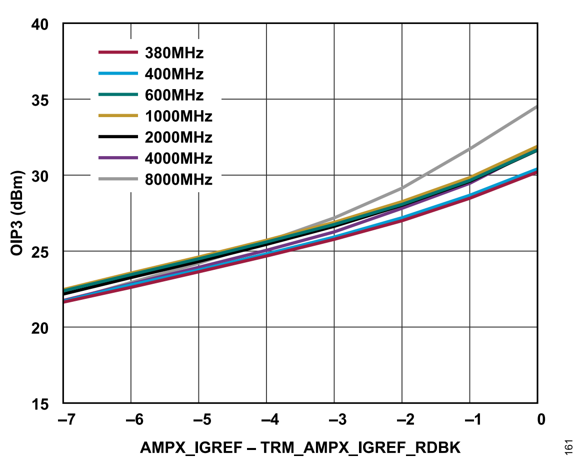


Figure 57. OIP3 vs. IGREF Settings for Various Frequencies

COMMON-MODE VOLTAGE

The ESD clamps are located right after input ports and before the output port (see Figure 58). When a DC voltage greater than or equal to 1.0 V is applied as common-mode, there is a risk of latching the silicon controlled rectifier (SCR) clamps in the ESD protection block with a single spike. Even with a DC voltage less than 1 V, intermodulation (IM) performance of the part may be degraded. An external DC block capacitor for AC-coupled is always recommended.

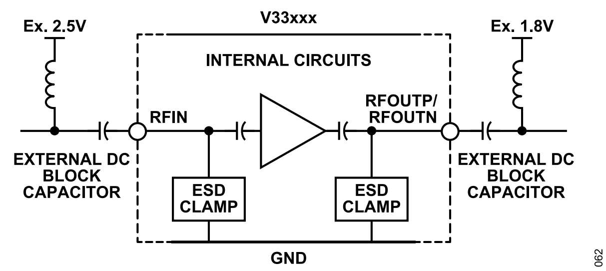


Figure 58. Simplified RF Input and Output Port Structure

REGISTER SUMMARY

Table 19. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x000	ADI_SPI_CONFIG	[7:0]	SOFTRESET_	LSB_FIRST_	ENDIAN_	SDOACTIVE_	SDOACTIVE	ENDIAN	LSB_FIRST	SOFTRESET	0x00	R/W
0x001	REG_0X0001	[7:0]	SINGLE_INSTRUCTION	CSB_STALL	MASTER_SLAVE_RB	RESERVED		SOFT_RESET		MASTER_SLAVE_TRANSFER	0x00	R/W
0x003	CHIPTYPE	[7:0]	CHIPTYPE								0x00	R
0x004	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x00	R
0x005	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x00A	SCRATCHPAD	[7:0]	SCRATCHPAD								0x00	R/W
0x00B	SPI_REV	[7:0]	SPI_REV								0x00	R
0x010	VARIANT_FEOL	[7:0]	FEOL				VARIANT				0x00	R
0x011	BEOL_SIF	[7:0]	SIF				BEOL				0x00	R
0x012	SPARE_0012	[7:0]	SPARE_0012								0x00	R
0x013	SPARE_0013	[7:0]	SPARE_0013								0x00	R
0x100	SIG_PATH0_0	[7:0]	RESERVED			AMUX_BG_EN	RESERVED			LDO18_EN	0x11	R/W
0x101	SIG_PATH1_0	[7:0]	RESERVED					AMP2_EN	DSA_EN	AMP1_EN	0x00	R/W
0x102	SIG_PATH2_0	[7:0]	RESERVED					SIGCHAIN_BYPASS	SEL_IBIASGEN_BG	RESERVED	0x00	R/W
0x103	SIG_PATH0_1	[7:0]	RESERVED				AMP1_MON_EN	RESERVED	AMP1_IM3_EN	AMP1_LP_MODE	0x06	R/W
0x104	SIG_PATH1_1	[7:0]	NVM_TRM_AMP1_IGREF	RESERVED			AMP1_IGREF				0x89	R/W
0x105	SIG_PATH2_1	[7:0]	NVM_TRM_AMP1_IDREF_Z	RESERVED	AMP1_IDREF_Z						0xAA	R/W
0x106	SIG_PATH3_1	[7:0]	NVM_TRM_AMP1_IDREF_P	RESERVED			AMP1_IDREF_P				0x83	R/W
0x109	SIG_PATH6_1	[7:0]	SPARE_010B				AMP1_IM3_CAP				0x07	R/W
0x10A	SIG_PATH0_2	[7:0]	AMP2_BYPASS0	AMP1_BYPASS0	DSA_ATTN0						0xD8	R/W
0x10B	SIG_PATH1_2	[7:0]	AMP2_BYPASS1	AMP1_BYPASS1	DSA_ATTN1						0x10	R/W
0x10C	SIG_PATH2_2	[7:0]	AMP2_BYPASS2	AMP1_BYPASS2	DSA_ATTN2						0x08	R/W
0x10D	SIG_PATH3_2	[7:0]	AMP2_BYPASS3	AMP1_BYPASS3	DSA_ATTN3						0x00	R/W
0x10F	SIG_PATH0_3	[7:0]	RESERVED				AMP2_MON_EN	AMP2_CROSS_EN	AMP2_IM3_EN	AMP2_LP_MODE	0x06	R/W
0x110	SIG_PATH1_3	[7:0]	NVM_TRM_AMP2_IGREF	RESERVED			AMP2_IGREF				0x89	R/W
0x111	SIG_PATH2_3	[7:0]	NVM_TRM_AMP2_IDREF_Z	RESERVED	AMP2_IDREF_Z						0xAA	R/W

REGISTER SUMMARY

Table 19. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x112	SIG_PATH3_3	[7:0]	NVM_TRM_AMP2_IDREF_P	RESERVED			AMP2_IDREF_P				0x83	R/W
0x113	SIG_PATH4_3	[7:0]	RESERVED		AMP2_CROSS_Z						0x2A	R/W
0x114	SIG_PATH5_3	[7:0]	RESERVED				AMP2_CROSS_P				0x03	R/W
0x115	SIG_PATH6_3	[7:0]	SPARE_011B				AMP2_IM3_CAP				0x07	R/W
0x120	AMUX_SEL	[7:0]	RESERVED	AMUX_3_SEL			AMUX_2_SEL	AMUX_1_SEL			0x20	R/W
0x121	MULTI_FUNC_CTRL_0111	[7:0]	RESERVED			SPI_1P8_3P3_CTRL	RESERVED				0x00	R/W
0x140	FUSE_READBACK_0	[7:0]	RESERVED				TRM_AMP1_IGREF_RDBK				0x00	R
0x141	FUSE_READBACK_1	[7:0]	RESERVED		TRM_AMP1_IDREF_Z_RDBK						0x00	R
0x142	FUSE_READBACK_2	[7:0]	RESERVED				TRM_AMP1_IDREF_P_RDBK				0x00	R
0x143	FUSE_READBACK_3	[7:0]	RESERVED				TRM_AMP2_IGREF_RDBK				0x00	R
0x144	FUSE_READBACK_4	[7:0]	RESERVED		TRM_AMP2_IDREF_Z_RDBK						0x00	R
0x145	FUSE_READBACK_5	[7:0]	RESERVED				TRM_AMP2_IDREF_P_RDBK				0x00	R
0x146	GENERIC_READBACK_0	[7:0]	RESERVED		AMP1_CROSS_Z_RDBK						0x00	R
0x147	GENERIC_READBACK_1	[7:0]	RESERVED				AMP1_CROSS_P_RDBK				0x00	R
0x148	GENERIC_READBACK_2	[7:0]	RESERVED		AMP2_CROSS_Z_RDBK						0x00	R
0x149	GENERIC_READBACK_3	[7:0]	RESERVED				AMP2_CROSS_P_RDBK				0x00	R
0x14A	GENERIC_READBACK_4	[7:0]	AMP2_BYPASS_RDBK	AMP1_BYPASS_RDBK	DSA_ATTN_RDBK						0x00	R

REGISTER DETAILS

Address: 0x000, Reset: 0x00, Name: ADI_SPI_CONFIG

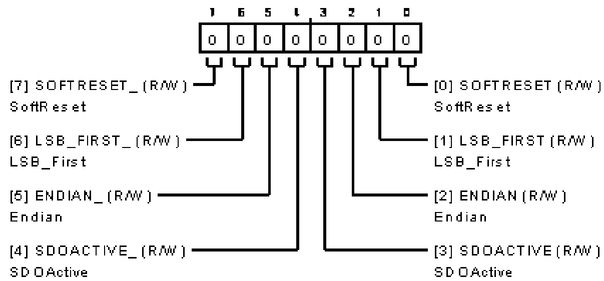


Table 20. Bit Descriptions for ADI_SPI_CONFIG

Bits	Bit Name	Description	Reset	Access
7	SOFTRESET_	SoftReset. 0: Reset Not Asserted. 1: Reset Asserted.	0x0	R/W
6	LSB_FIRST_	LSB_First. 0: MSB First. 1: LSB First.	0x0	R/W
5	ENDIAN_	Endian. 0: Address Descending. 1: Address Ascending.	0x0	R/W
4	SDOACTIVE_	SDOActive. 0: SDO Inactive (3-wire SPI Mode). 1: SDO Active (4-wire SPI Mode).	0x0	R/W
3	SDOACTIVE	SDOActive. 0: SDO Inactive (3-wire SPI Mode). 1: SDO Active (4-wire SPI Mode).	0x0	R/W
2	ENDIAN	Endian. 0: Address Descending. 1: Address Ascending.	0x0	R/W
1	LSB_FIRST	LSB_First. 0: MSB First. 1: LSB First.	0x0	R/W
0	SOFTRESET	SoftReset. 0: Reset Not Asserted. 1: Reset Asserted.	0x0	R/W

Address: 0x001, Reset: 0x00, Name: REG_0X0001

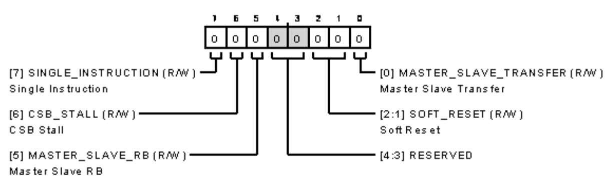


Table 21. Bit Descriptions for REG_0X0001

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INSTRUCTION	Single Instruction.	0x0	R/W
6	CSB_STALL	CSB Stall.	0x0	R/W
5	MASTER_SLAVE_RB	Master Slave RB.	0x0	R/W

REGISTER DETAILS

Table 21. Bit Descriptions for REG_0X0001 (Continued)

Bits	Bit Name	Description	Reset	Access
[4:3]	RESERVED	Reserved.	0x0	R
[2:1]	SOFT_RESET	Soft Reset.	0x0	R/W
0	MASTER_SLAVE_TRANSFER	Master Slave Transfer.	0x0	R/W

Address: 0x003, Reset: 0x00, Name: CHIPTYPE

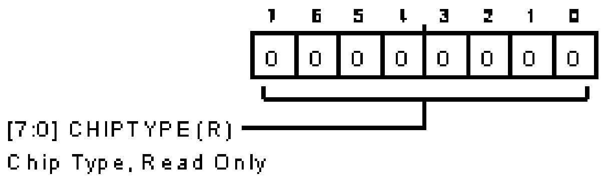


Table 22. Bit Descriptions for CHIPTYPE

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIPTYPE	Chip Type, Read Only.	0x0	R

Address: 0x004, Reset: 0x00, Name: PRODUCT_ID_L

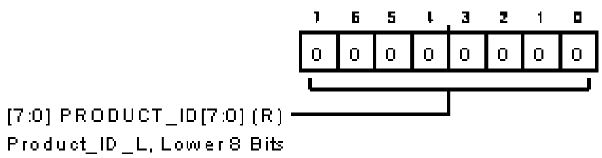


Table 23. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product_ID_L, Lower 8 Bits.	0x0	R

Address: 0x005, Reset: 0x00, Name: PRODUCT_ID_H

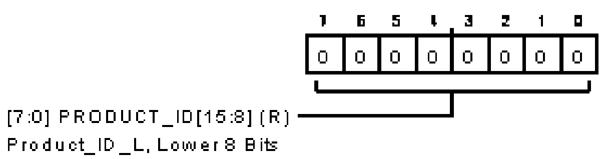


Table 24. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product_ID_L, Lower 8 Bits.	0x0	R

Address: 0x00A, Reset: 0x00, Name: SCRATCHPAD

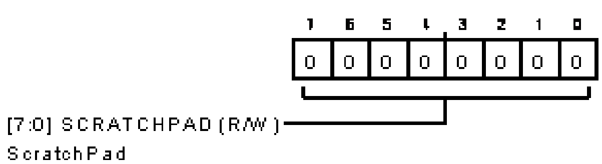


Table 25. Bit Descriptions for SCRATCHPAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCHPAD	ScratchPad.	0x0	R/W

REGISTER DETAILS

Address: 0x00B, Reset: 0x00, Name: SPI_REV

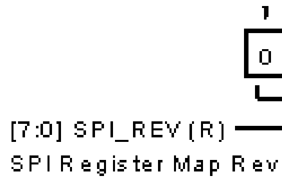


Table 26. Bit Descriptions for SPI_REV

Bits	Bit Name	Description	Reset	Access
[7:0]	SPI_REV	SPI Register Map Rev.	0x0	R

Address: 0x010, Reset: 0x00, Name: VARIANT_FEOL

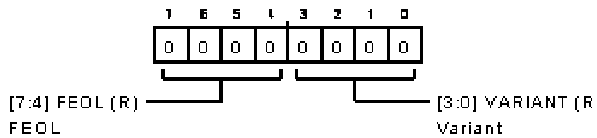


Table 27. Bit Descriptions for VARIANT_FEOL

Bits	Bit Name	Description	Reset	Access
[7:4]	FEOL	FEOL.	0x0	R
[3:0]	VARIANT	Variant.	0x0	R

Address: 0x011, Reset: 0x00, Name: BEOL_SIF

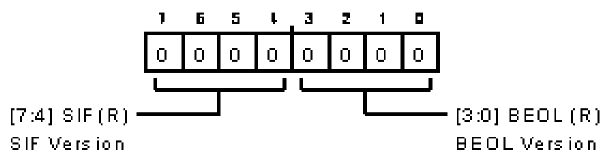


Table 28. Bit Descriptions for BEOL_SIF

Bits	Bit Name	Description	Reset	Access
[7:4]	SIF	SIF Version.	0x0	R
[3:0]	BEOL	BEOL Version.	0x0	R

Address: 0x012, Reset: 0x00, Name: SPARE_0012

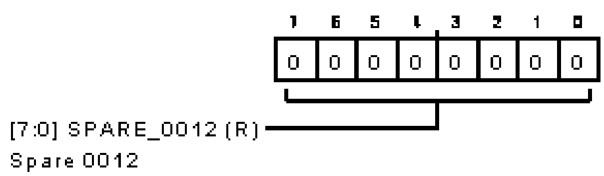


Table 29. Bit Descriptions for SPARE_0012

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_0012	Spare 0012.	0x0	R

Address: 0x013, Reset: 0x00, Name: SPARE_0013

REGISTER DETAILS

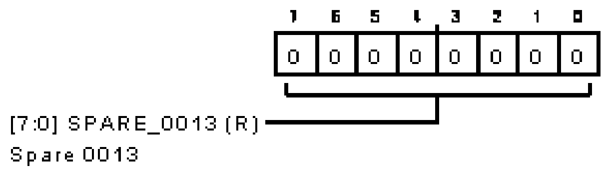


Table 30. Bit Descriptions for SPARE_0013

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_0013	Spare 0013.	0x0	R

Address: 0x100, Reset: 0x11, Name: SIG_PATH0_0

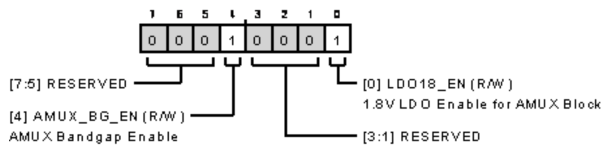


Table 31. Bit Descriptions for SIG_PATH0_0

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	AMUX_BG_EN	AMUX Bandgap Enable. 0: Disable AMUX Bandgap. 1: Enable AMUX Bandgap.	0x1	R/W
[3:1]	RESERVED	Reserved.	0x0	R/W
0	LDO18_EN	1.8V LDO Enable for AMUX Block. 0: Disable. 1: Enable.	0x1	R/W

Address: 0x101, Reset: 0x00, Name: SIG_PATH1_0

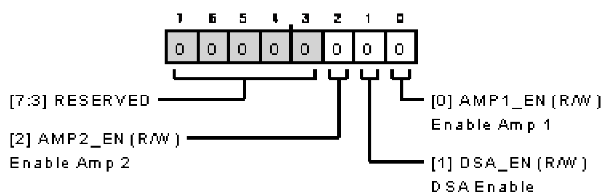


Table 32. Bit Descriptions for SIG_PATH1_0

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	AMP2_EN	Enable Amp 2. 0: Disable. 1: Enable.	0x0	R/W
1	DSA_EN	DSA Enable. 0: Disable. 1: Enable.	0x0	R/W
0	AMP1_EN	Enable Amp 1. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x102, Reset: 0x00, Name: SIG_PATH2_0

REGISTER DETAILS

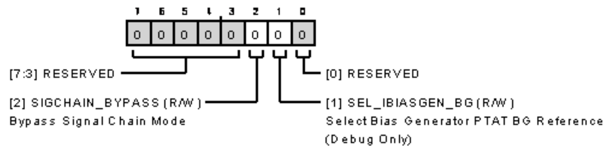


Table 33. Bit Descriptions for SIG_PATH2_0

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	SIGCHAIN_BYPASS	Bypass Signal Chain Mode. 0: Based on Individual Amp Bypass Setting. 1: Bypass Both Amps.	0x0	R/W
1	SEL_IBIASGEN_BG	Select Bias Generator PTAT BG Reference (Debug Only). 0: Use Dedicated PTAT Generator (Default). 1: Use Bandgap Based PTAT Generator.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x103, Reset: 0x06, Name: SIG_PATH0_1

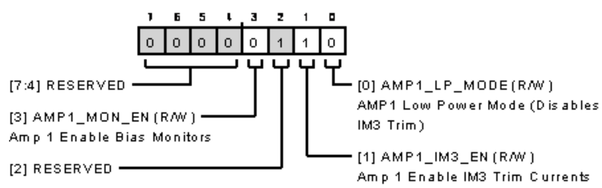


Table 34. Bit Descriptions for SIG_PATH0_1

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	AMP1_MON_EN	Amp 1 Enable Bias Monitors. 0: Disable Bias Monitoring. 1: Enable Bias Monitoring (Debug Only).	0x0	R/W
2	RESERVED	Reserved.	0x1	R/W
1	AMP1_IM3_EN	Amp 1 Enable IM3 Trim Currents. 0: Disable IM3 Trim Currents. 1: Enable IM3 Trim Currents.	0x1	R/W
0	AMP1_LP_MODE	AMP1 Low Power Mode (Disables IM3 Trim). 0: Disable. Use Default Bias. 1: Enable Low Bias.	0x0	R/W

Address: 0x104, Reset: 0x89, Name: SIG_PATH1_1

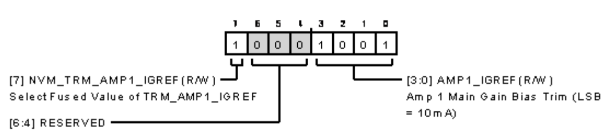


Table 35. Bit Descriptions for SIG_PATH1_1

Bits	Bit Name	Description	Reset	Access
7	NVM_TRM_AMP1_IGREF	Select Fused Value of TRM_AMP1_IGREF.	0x1	R/W
[6:4]	RESERVED	Reserved.	0x0	R
[3:0]	AMP1_IGREF	Amp 1 Main Gain Bias Trim (LSB = 10mA).	0x9	R/W

REGISTER DETAILS

Address: 0x105, Reset: 0xAA, Name: SIG_PATH2_1

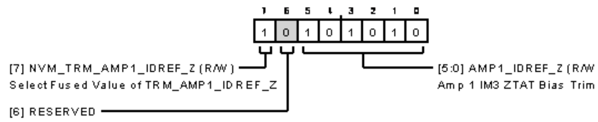


Table 36. Bit Descriptions for SIG_PATH2_1

Bits	Bit Name	Description	Reset	Access
7	NVM_TRM_AMP1_IDREF_Z	Select Fused Value of TRM_AMP1_IDREF_Z.	0x1	R/W
6	RESERVED	Reserved.	0x0	R
[5:0]	AMP1_IDREF_Z	Amp 1 IM3 ZTAT Bias Trim.	0x2A	R/W

Address: 0x106, Reset: 0x83, Name: SIG_PATH3_1

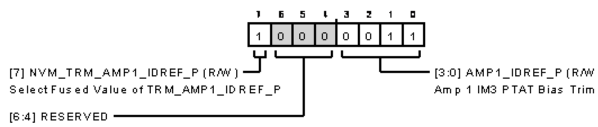


Table 37. Bit Descriptions for SIG_PATH3_1

Bits	Bit Name	Description	Reset	Access
7	NVM_TRM_AMP1_IDREF_P	Select Fused Value of TRM_AMP1_IDREF_P.	0x1	R/W
[6:4]	RESERVED	Reserved.	0x0	R
[3:0]	AMP1_IDREF_P	Amp 1 IM3 PTAT Bias Trim.	0x3	R/W

Address: 0x109, Reset: 0x07, Name: SIG_PATH6_1

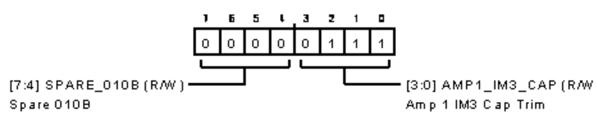


Table 38. Bit Descriptions for SIG_PATH6_1

Bits	Bit Name	Description	Reset	Access
[7:4]	SPARE_010B	Spare 010B.	0x0	R/W
[3:0]	AMP1_IM3_CAP	Amp 1 IM3 Cap Trim.	0x7	R/W

Address: 0x10A, Reset: 0xD8, Name: SIG_PATH0_2

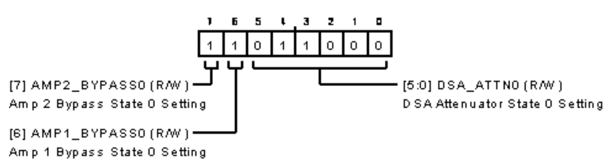


Table 39. Bit Descriptions for SIG_PATH0_2

Bits	Bit Name	Description	Reset	Access
7	AMP2_BYPASS0	Amp 2 Bypass State 0 Setting. 0: Fixed Gain Mode. 1: Bypass Mode Enable.	0x1	R/W
6	AMP1_BYPASS0	Amp 1 Bypass State 0 Setting. 0: Fixed Gain Mode. 1: Bypass Mode Enable.	0x1	R/W

REGISTER DETAILS

Table 39. Bit Descriptions for SIG_PATH0_2 (Continued)

Bits	Bit Name	Description	Reset	Access
[5:0]	DSA_ATTN0	DSA Attenuator State 0 Setting. 00000: 0dB. 00001: 1dB. 00010: 2dB. 00011: 3dB. 00100: 4dB. 00101: 5dB. 00110: 6dB. 00111: 7dB. 01000: 8dB. 01001: 9dB. 01010: 10dB. 01011: 11dB. 01100: 12dB. 01101: 13dB. 01110: 14dB. 01111: 15dB. 10000: 16dB. 10001: 17dB. 10010: 18dB. 10011: 19dB. 10100: 20dB. 10101: 21dB. 10110: 22dB. 10111: 23dB. 11000: 24dB.	0x18	R/W

Address: 0x10B, Reset: 0x10, Name: SIG_PATH1_2

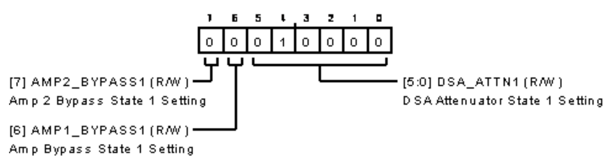


Table 40. Bit Descriptions for SIG_PATH1_2

Bits	Bit Name	Description	Reset	Access
7	AMP2_BYPASS1	Amp 2 Bypass State 1 Setting. 0: Fixed Gain Mode. 1: Bypass Mode Enable.	0x0	R/W
6	AMP1_BYPASS1	Amp Bypass State 1 Setting. 0: Fixed Gain Mode. 1: Bypass Mode Enable.	0x0	R/W
[5:0]	DSA_ATTN1	DSA Attenuator State 1 Setting. 00000: 0dB. 00001: 1dB. 00010: 2dB. 00011: 3dB. 00100: 4dB.	0x10	R/W

REGISTER DETAILS

Table 40. Bit Descriptions for SIG_PATH1_2 (Continued)

Bits	Bit Name	Description	Reset	Access
		00101: 5dB. 00110: 6dB. 00111: 7dB. 01000: 8dB. 01001: 9dB. 01010: 10dB. 01011: 11dB. 01100: 12dB. 01101: 13dB. 01110: 14dB. 01111: 15dB. 10000: 16dB. 10001: 17dB. 10010: 18dB. 10011: 19dB. 10100: 20dB. 10101: 21dB. 10110: 22dB. 10111: 23dB. 11000: 24dB.		

Address: 0x10C, Reset: 0x08, Name: SIG_PATH2_2

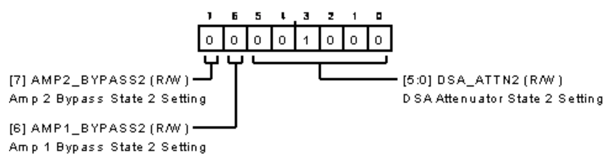


Table 41. Bit Descriptions for SIG_PATH2_2

Bits	Bit Name	Description	Reset	Access
7	AMP2_BYPASS2	Amp 2 Bypass State 2 Setting. 0: Fixed Gain Mode. 1: Bypass Mode Enable.	0x0	R/W
6	AMP1_BYPASS2	Amp 1 Bypass State 2 Setting. 0: Fixed Gain Mode. 1: Bypass Mode Enable.	0x0	R/W
[5:0]	DSA_ATTN2	DSA Attenuator State 2 Setting. 00000: 0dB. 00001: 1dB. 00010: 2dB. 00011: 3dB. 00100: 4dB. 00101: 5dB. 00110: 6dB. 00111: 7dB. 01000: 8dB. 01001: 9dB. 01010: 10dB.	0x8	R/W

REGISTER DETAILS

Table 41. Bit Descriptions for SIG_PATH2_2 (Continued)

Bits	Bit Name	Description	Reset	Access
		01011: 11dB. 01100: 12dB. 01101: 13dB. 01110: 14dB. 01111: 15dB. 10000: 16dB. 10001: 17dB. 10010: 18dB. 10011: 19dB. 10100: 20dB. 10101: 21dB. 10110: 22dB. 10111: 23dB. 11000: 24dB.		

Address: 0x10D, Reset: 0x00, Name: SIG_PATH3_2

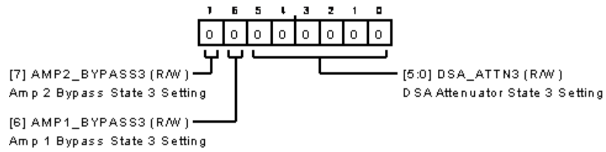


Table 42. Bit Descriptions for SIG_PATH3_2

Bits	Bit Name	Description	Reset	Access
7	AMP2_BYPASS3	Amp 2 Bypass State 3 Setting. 0: Fixed Gain Mode. 1: Bypass Mode Enable.	0x0	R/W
6	AMP1_BYPASS3	Amp 1 Bypass State 3 Setting. 0: Fixed Gain Mode. 1: Bypass Mode Enable.	0x0	R/W
[5:0]	DSA_ATTN3	DSA Attenuator State 3 Setting. 00000: 0dB. 00001: 1dB. 00010: 2dB. 00011: 3dB. 00100: 4dB. 00101: 5dB. 00110: 6dB. 00111: 7dB. 01000: 8dB. 01001: 9dB. 01010: 10dB. 01011: 11dB. 01100: 12dB. 01101: 13dB. 01110: 14dB. 01111: 15dB. 10000: 16dB.	0x0	R/W

REGISTER DETAILS

Table 42. Bit Descriptions for SIG_PATH3_2 (Continued)

Bits	Bit Name	Description	Reset	Access
		10001: 17dB. 10010: 18dB. 10011: 19dB. 10100: 20dB. 10101: 21dB. 10110: 22dB. 10111: 23dB. 11000: 24dB.		

Address: 0x10F, Reset: 0x06, Name: SIG_PATH0_3

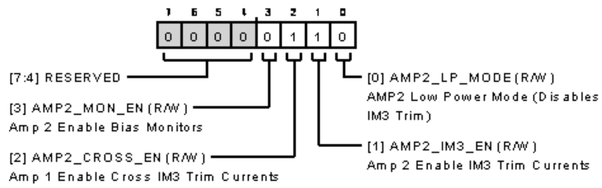


Table 43. Bit Descriptions for SIG_PATH0_3

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	AMP2_MON_EN	Amp 2 Enable Bias Monitors. 0: Disable Bias Monitoring. 1: Enable Bias Monitoring (Debug Only).	0x0	R/W
2	AMP2_CROSS_EN	Amp 1 Enable Cross IM3 Trim Currents. 0: Disable Cross-Coupled Stage IM3 Trim. 1: Enable Cross-Coupled Stage IM3 Trim.	0x1	R/W
1	AMP2_IM3_EN	Amp 2 Enable IM3 Trim Currents. 0: Disable IM3 Trim Currents. 1: Enable IM3 Trim Currents.	0x1	R/W
0	AMP2_LP_MODE	AMP2 Low Power Mode (Disables IM3 Trim). 0: Disable. Use Default Bias. 1: Enable Low Bias.	0x0	R/W

Address: 0x110, Reset: 0x89, Name: SIG_PATH1_3

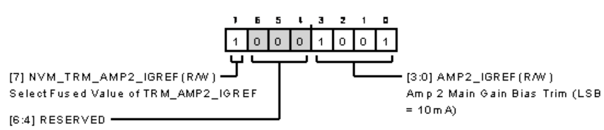


Table 44. Bit Descriptions for SIG_PATH1_3

Bits	Bit Name	Description	Reset	Access
7	NVM_TRM_AMP2_IGREF	Select Fused Value of TRM_AMP2_IGREF.	0x1	R/W
[6:4]	RESERVED	Reserved.	0x0	R
[3:0]	AMP2_IGREF	Amp 2 Main Gain Bias Trim (LSB = 10mA).	0x9	R/W

Address: 0x111, Reset: 0xAA, Name: SIG_PATH2_3

REGISTER DETAILS

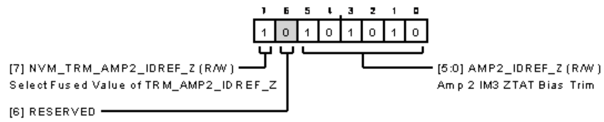


Table 45. Bit Descriptions for SIG_PATH2_3

Bits	Bit Name	Description	Reset	Access
7	NVM_TRM_AMP2_IDREF_Z	Select Fused Value of TRM_AMP2_IDREF_Z.	0x1	R/W
6	RESERVED	Reserved.	0x0	R
[5:0]	AMP2_IDREF_Z	Amp 2 IM3 ZTAT Bias Trim.	0x2A	R/W

Address: 0x112, Reset: 0x83, Name: SIG_PATH3_3

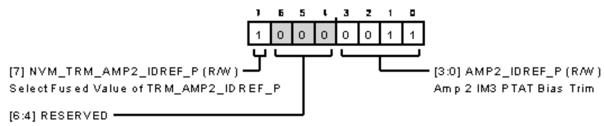


Table 46. Bit Descriptions for SIG_PATH3_3

Bits	Bit Name	Description	Reset	Access
7	NVM_TRM_AMP2_IDREF_P	Select Fused Value of TRM_AMP2_IDREF_P.	0x1	R/W
[6:4]	RESERVED	Reserved.	0x0	R
[3:0]	AMP2_IDREF_P	Amp 2 IM3 PTAT Bias Trim.	0x3	R/W

Address: 0x113, Reset: 0x2A, Name: SIG_PATH4_3

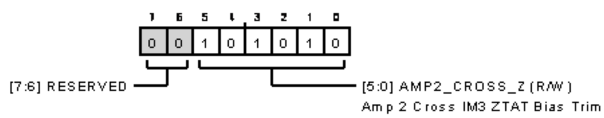


Table 47. Bit Descriptions for SIG_PATH4_3

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	AMP2_CROSS_Z	Amp 2 Cross IM3 ZTAT Bias Trim.	0x2A	R/W

Address: 0x114, Reset: 0x03, Name: SIG_PATH5_3

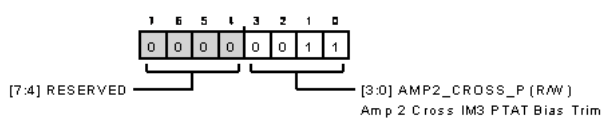
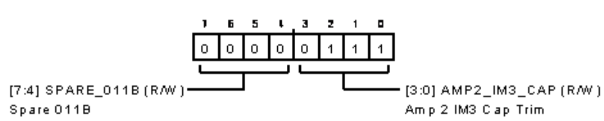


Table 48. Bit Descriptions for SIG_PATH5_3

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	AMP2_CROSS_P	Amp 2 Cross IM3 PTAT Bias Trim.	0x3	R/W

Address: 0x115, Reset: 0x07, Name: SIG_PATH6_3



REGISTER DETAILS

Table 49. Bit Descriptions for SIG_PATH6_3

Bits	Bit Name	Description	Reset	Access
[7:4]	SPARE_011B	Spare 011B.	0x0	R/W
[3:0]	AMP2_IM3_CAP	Amp 2 IM3 Cap Trim.	0x7	R/W

Address: 0x120, Reset: 0x20, Name: AMUX_SEL

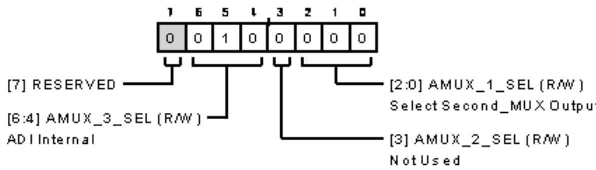


Table 50. Bit Descriptions for AMUX_SEL

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R/W
[6:4]	AMUX_3_SEL	ADI Internal.	0x2	R/W
3	AMUX_2_SEL	Not Used.	0x0	R/W
[2:0]	AMUX_1_SEL	Select Second_MUX Output. 000: PTAT (Temperature Sensor).	0x0	R/W

Address: 0x121, Reset: 0x00, Name: MULTI_FUNC_CTRL_0111

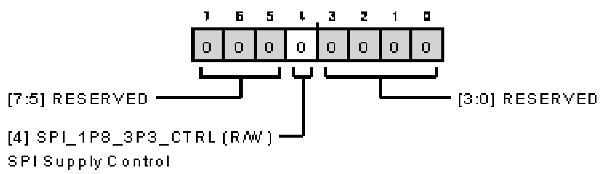


Table 51. Bit Descriptions for MULTI_FUNC_CTRL_0111

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	SPI_1P8_3P3_CTRL	SPI Supply Control. 0: 1.8V Read Back. 1: 3.3V Read Back.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x140, Reset: 0x00, Name: FUSE_READBACK_0

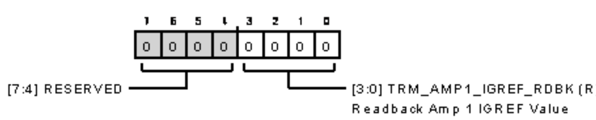


Table 52. Bit Descriptions for FUSE_READBACK_0

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	TRM_AMP1_IGREF_RDBK	Readback Amp 1 IGREF Value.	0x0	R

Address: 0x141, Reset: 0x00, Name: FUSE_READBACK_1

REGISTER DETAILS

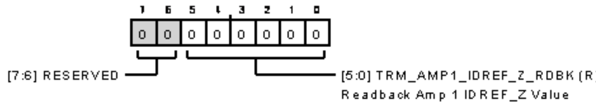


Table 53. Bit Descriptions for FUSE_READBACK_1

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	TRM_AMP1_IDREF_Z_RDBK	Readback Amp 1 IDREF_Z Value.	0x0	R

Address: 0x142, Reset: 0x00, Name: FUSE_READBACK_2

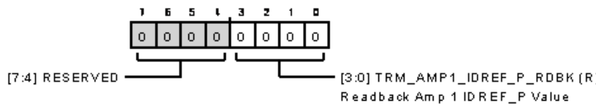


Table 54. Bit Descriptions for FUSE_READBACK_2

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	TRM_AMP1_IDREF_P_RDBK	Readback Amp 1 IDREF_P Value.	0x0	R

Address: 0x143, Reset: 0x00, Name: FUSE_READBACK_3

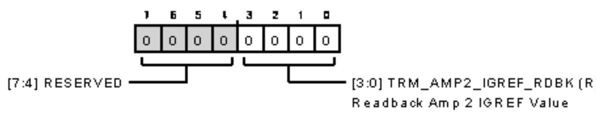


Table 55. Bit Descriptions for FUSE_READBACK_3

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	TRM_AMP2_IGREF_RDBK	Readback Amp 2 IGREF Value.	0x0	R

Address: 0x144, Reset: 0x00, Name: FUSE_READBACK_4

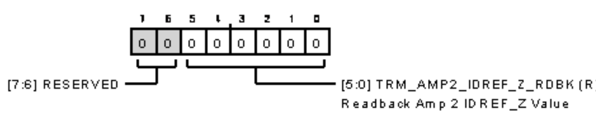


Table 56. Bit Descriptions for FUSE_READBACK_4

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	TRM_AMP2_IDREF_Z_RDBK	Readback Amp 2 IDREF_Z Value.	0x0	R

Address: 0x145, Reset: 0x00, Name: FUSE_READBACK_5

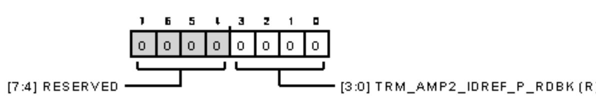


Table 57. Bit Descriptions for FUSE_READBACK_5

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 57. Bit Descriptions for FUSE_READBACK_5 (Continued)

Bits	Bit Name	Description	Reset	Access
[3:0]	TRM_AMP2_IDREF_P_RDBK	Readback Amp 2 IDREF_P Value.	0x0	R

Address: 0x146, Reset: 0x00, Name: GENERIC_READBACK_0

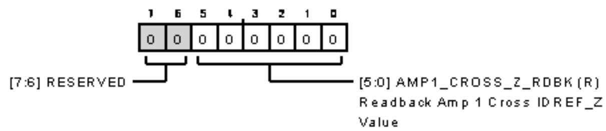


Table 58. Bit Descriptions for GENERIC_READBACK_0

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	AMP1_CROSS_Z_RDBK	Readback Amp 1 Cross IDREF_Z Value.	0x0	R

Address: 0x147, Reset: 0x00, Name: GENERIC_READBACK_1

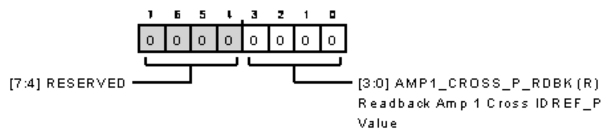


Table 59. Bit Descriptions for GENERIC_READBACK_1

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	AMP1_CROSS_P_RDBK	Readback Amp 1 Cross IDREF_P Value.	0x0	R

Address: 0x148, Reset: 0x00, Name: GENERIC_READBACK_2

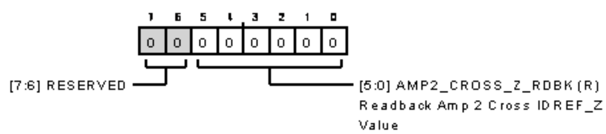


Table 60. Bit Descriptions for GENERIC_READBACK_2

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	AMP2_CROSS_Z_RDBK	Readback Amp 2 Cross IDREF_Z Value.	0x0	R

Address: 0x149, Reset: 0x00, Name: GENERIC_READBACK_3

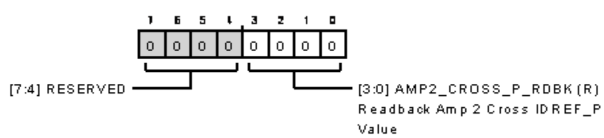


Table 61. Bit Descriptions for GENERIC_READBACK_3

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	AMP2_CROSS_P_RDBK	Readback Amp 2 Cross IDREF_P Value.	0x0	R

Address: 0x14A, Reset: 0x00, Name: GENERIC_READBACK_4

REGISTER DETAILS

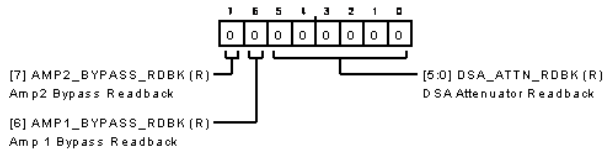


Table 62. Bit Descriptions for GENERIC_READBACK_4

Bits	Bit Name	Description	Reset	Access
7	AMP2_BYPASS_RDBK	Amp2 Bypass Readback.	0x0	R
6	AMP1_BYPASS_RDBK	Amp 1 Bypass Readback.	0x0	R
[5:0]	DSA_ATTN_RDBK	DSA Attenuator Readback.	0x0	R

OUTLINE DIMENSIONS

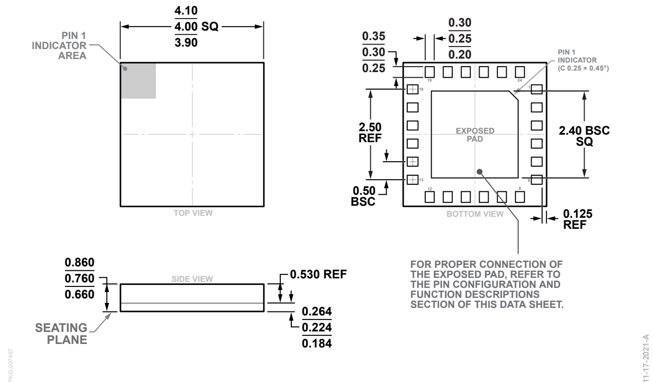


Figure 59. 24-Terminal Land Grid Array [LGA]
(CC-24-17)
Dimensions shown in millimeters

Updated: March 14, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL6332ACCZA	-40°C to +105°C	24-Lead LGA (4mm x 4mm x 0.76mm w/ EP)	Tray, 0	CC-24-17
ADL6332ACCZA-R7	-40°C to +105°C	24-Lead LGA (4mm x 4mm x 0.76mm w/ EP)	Reel, 1500	CC-24-17

1 Z = RoHS Compliant Part.

EVALUATION BOARD

Model[1]	Description
ADL6332-EVALZA	Version A (0.38 GHz to 8.0 GHz) Evaluation Board

1 Z = RoHS Compliant Part.