Silicon SPST Switch, NonReflective, 100 MHz to 55 GHz

FEATURES

- Ultrawideband Frequency range: 0.1 GHz to 55 GHz
- Nonreflective ports, High power terminated path
- Symmetrical ports
- Low insertion loss
  - 1.0 dB typical to 20 GHz
  - 1.5 dB typical to 40 GHz
  - 2.0 dB typical to 55 GHz
- Isolation
  - 30 dB typical to 50 GHz
  - 28 dB typical to 55 GHz
- High input linearity
  - P0.1dB: >33 dBm typical
  - Input IP3 >60 dBm typical
- High power handling T_{case}= 85 °C
  - Through path
    - Peak: 36 dBm
    - Pulse: 33 dBm
    - CW: 30 dBm
  - Terminated path
    - Peak: 33 dBm
    - Pulse 33 dBm
    - CW: 30 dBm
  - Hot switching
    - Peak: 33 dBm
    - Pulse: 33 dBm
    - CW: 30 dBm
- CMOS/LVTTL compatible
- RF switching time: 30 ns
- RF settling time (0.1 dB final RF output): 50 ns
- Dual supply operation: ±3.3 V
- 14-lead, 2.25 mm x 2.25 mm, LGA package

APPLICATIONS

- Test and instrumentation
- Cellular infrastructure: 5G mmWave
- Military radios, radars, electronic counter measures
- Microwave radios and very small aperture terminals
- Industrial scanners

FUNCTIONAL BLOCK DIAGRAM

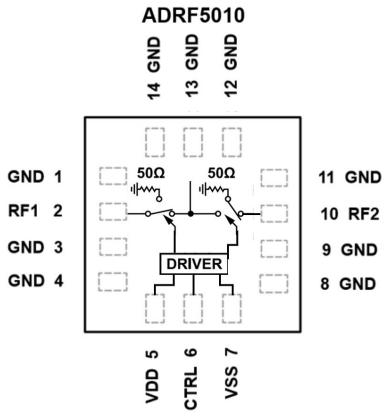

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5010 is a non-reflective, single-pole single-throw (SPST) switch manufactured in the silicon process.

The ADRF5010 operates from 0.1 GHz to 55 GHz with insertion loss of lower than 2 dB and isolation of higher than 28 dB. The device has a RF input power handling capability of 30 dBm for through path and 30 dBm for hot switching.

The ADRF5010 requires dual supply voltages of ±3.3 V. The device employs CMOS and LVTTL compatible control.

The ADRF5010 can also operate with a single positive supply voltage (VDD) applied while the negative supply voltage (VSS) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance is derated. See Figure 2 for more details.

The ADRF5010 comes in a 14-lead, 2.25 mm x 2.25 mm, land grid array [LGA] package and can operate from -40°C to +105°C.

TABLE OF CONTENTS

SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or VDD, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted. RFx refers to RF1 or RF2.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		55	GHz
INSERTION LOSS						
Between RFx and RFx (On)		0.1 GHz to 20 GHz		1.0		dB
		20 GHz to 40 GHz		1.5		dB
		40 GHz to 55 GHz		2.0		dB
ISOLATION						
Between RFx and RFx		0.1 GHz to 20 GHz		31		dB
		20 GHz to 40 GHz		30		dB
		40 GHz to 55 GHz		28		dB
RETURN LOSS						
RFx (Through path)		0.1 GHz to 20 GHz		20		dB
		20 GHz to 40 GH		19		dB
		40 GHz to 55 GHz		21		dB
RFx (Terminated)		0.1 GHz to 55 GHz		22		dB
SWITCHING						
Rise and Fall Time	t_{RISE},t_{FALL}	10% to 90% of RF output		27		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		30		ns
RF Settling Time (0.1dB)		50% V_{CTL} to 0.1 dB of final RF output		50		ns
INPUT LINEARITY[1]		f = 0.1 GHz to 60 GHz				
Input Compression	P0.1dB			33		dBm
Third-Order Intercept	IP3	Two-tone input power = TBD dBm each tone, Δf = 1 MHz		62		dBm
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			140		µA
Negative Supply Current	I_{SS}			500		µA
DIGITAL CONTROL INPUTS		CTRL				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	$I_{INL,}$			<1		µA
High	I_{INH}			<1		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Inputs Voltage	V_{CTRL}		0		VDD	V
RF Input Power[2]	P_{IN}	f = 0.1 GHz to 55 GHz, T_{CASE} = 85°C				
	Peak			36		dBm
Through Path	Pulse	RF signal is applied to RFx at Insertion Loss state		33		dBm
	CW			30		dBm
	Peak			33		dBm
Terminated Path	Pulse	RF signal is applied to RFx at Isolation state		33		dBm
	CW			30		dBm
	Peak			33		dBm
Hot Switching	Pulse	RF signal is applied to RFx while switching in between Insertion Loss and Isolation states		33		dBm

SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
	CW			30		dBm
Case Temperature	T_{CASE}		−40		+85	°C

[1] For input linearity performance over frequency, see Figure 12 to Figure 15.

[2] For power derating over frequency, see Figure 2.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Input[1]	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power, Dual Supply[2] (V_{DD} = 3.3 V, V_{SS} = −3.3 V, f = 0.1 GHz to 55 GHz, T_{CASE} = 85°C[3])	
Through Path	37 dBm
Terminated Path	33.5 dBm
Hot Switching (RF1/2 to Termination)	33.5 dBm
RF Input Power, Single Supply (V_{DD} = 3.3 V, V_{SS} = 0 V, f = 0.1 GHz to 55 GHz, T_{CASE} = 85°C[3])	
Through Path	20 dBm
Terminated Path	20 dBm
Hot Switching (RF1/2 to Termination)	20 dBm
RF Input Power, Unbiased (V_{DD}, V_{SS} = 0 V)	18 dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

1 Overvoltages at the digital control input are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB for dual supply and 1 dB for single supply.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at a time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-14-5, Through Path	135.5	°C/W
CC-14-5, Terminated Path	50	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

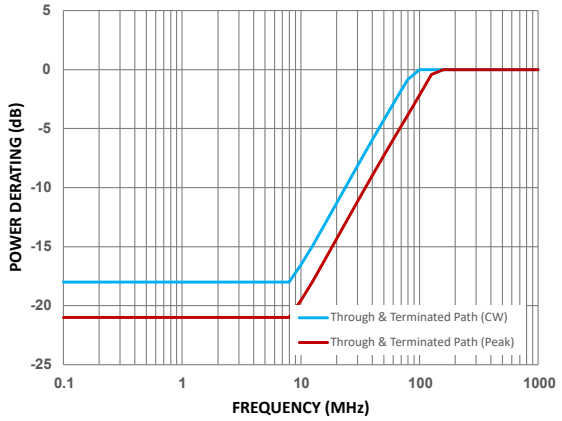

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

Table 4. ADRF5010, 14-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	750V for RF Pins	1B
	750V for Supply and Digital Control Pins	1B
CDM	500V for All Pins	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

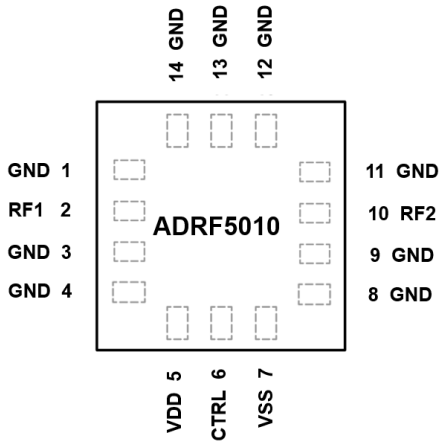

Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 8, 9, 11,12, 13, 14	GND	Ground. These pins must be connected to the RF/dc ground of the PCB.
2	RF1	RF Port 1. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
5	VDD	Positive Supply Voltage. See Figure 6 for the interface schematic.
6	CTRL	Control Input Voltage. See Figure 5 for the interface schematic.
7	VSS	Negative Supply Voltage. See Figure 7 for the interface schematic.
10	RF2	RF Port 2. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

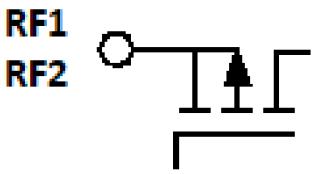

Figure 4. RF1, RF2 Pins Interface Schematic

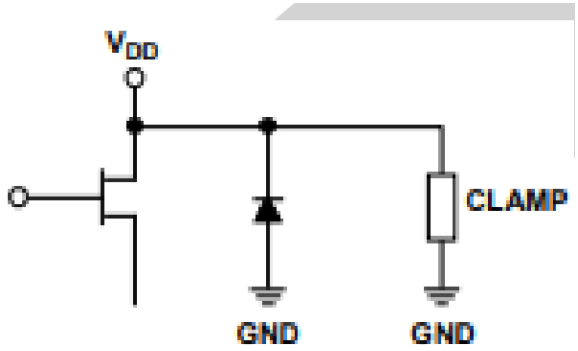

Figure 6. V_{DD} Interface Schematic

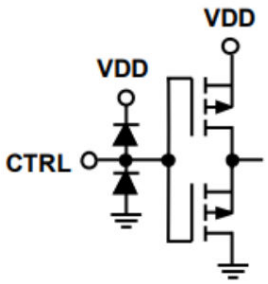

Figure 5. CTL Pin Interface Schematic

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

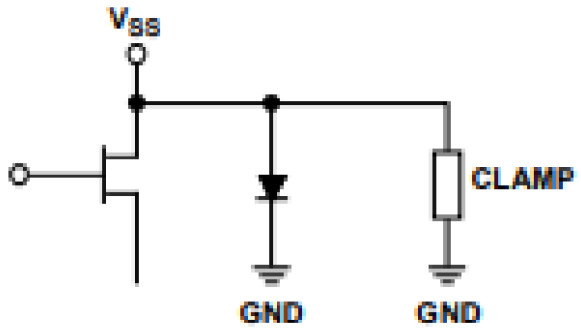

Figure 7. V_{SS} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or VDD, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

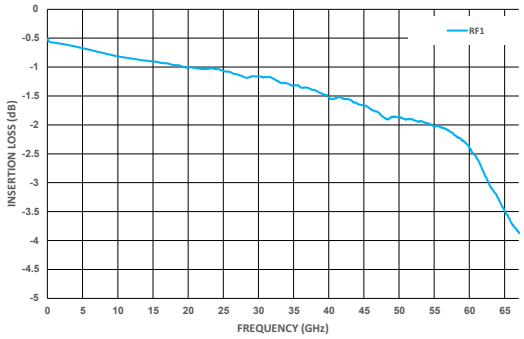

Figure 8. Insertion Loss vs. Frequency

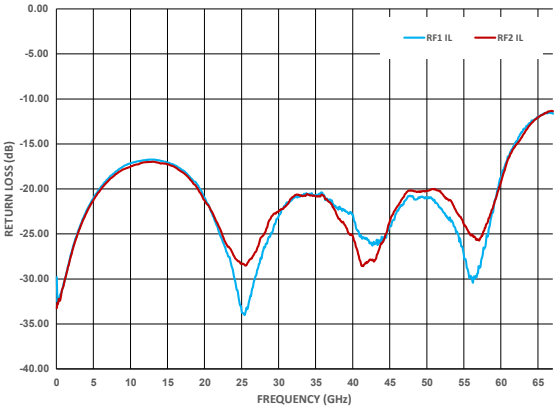

Figure 9. Return Loss vs. Frequency, Insertion Loss

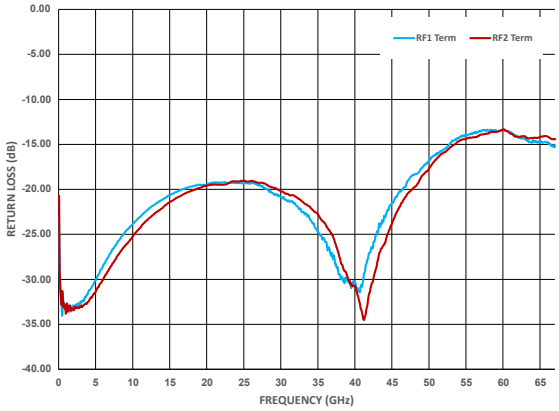

Figure 10. Return Loss vs. Frequency, Termination

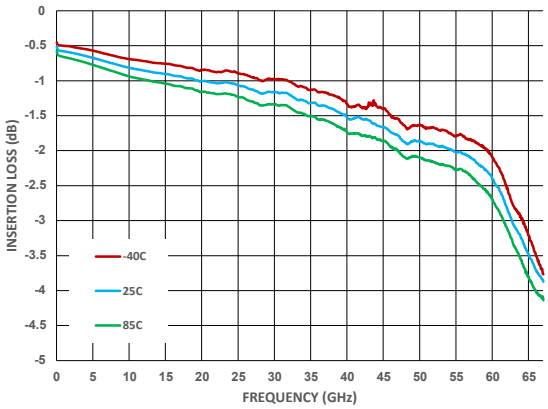

Figure 11. Insertion Loss vs. Frequency over Temperature

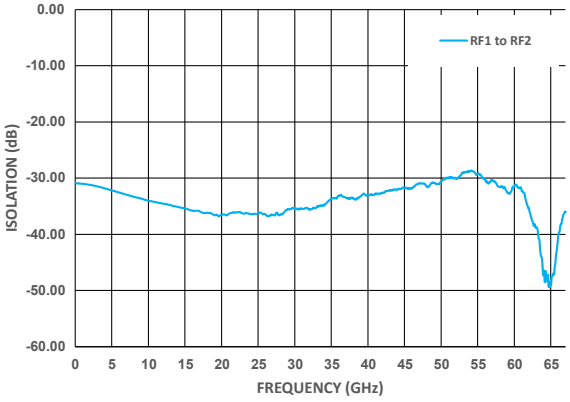

Figure 12. Isolation Loss vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or VDD, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

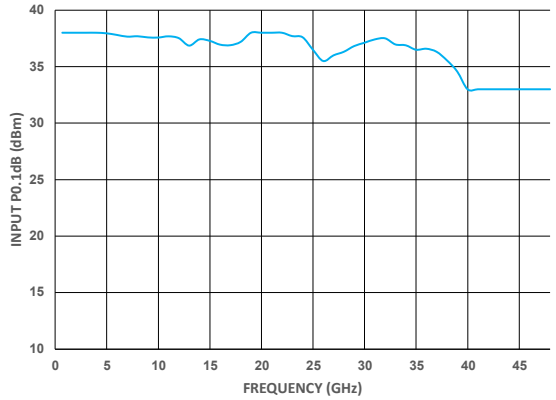

Figure 13. Input 0.1dB Power Compression vs. Frequency

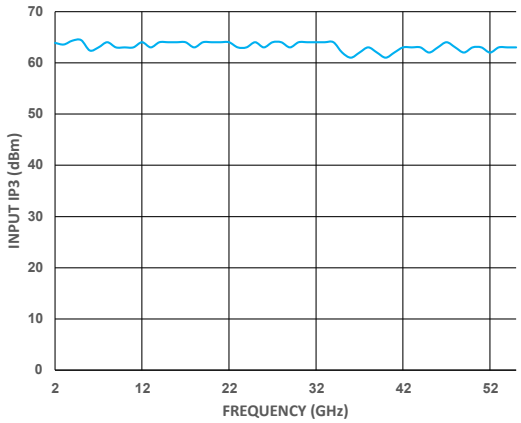

Figure 14. Input IP3 vs. Frequency

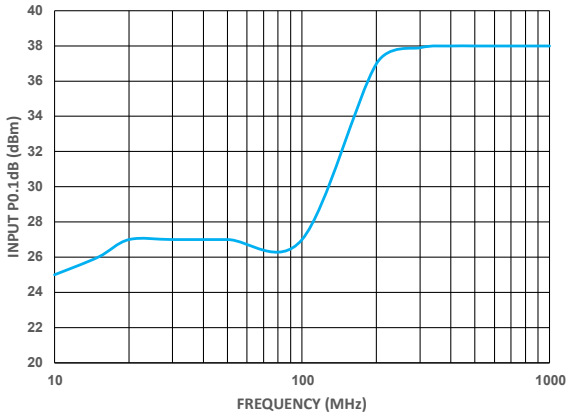

Figure 15. Input 0.1dB Power Compression vs. Frequency (Low Frequency Detail)

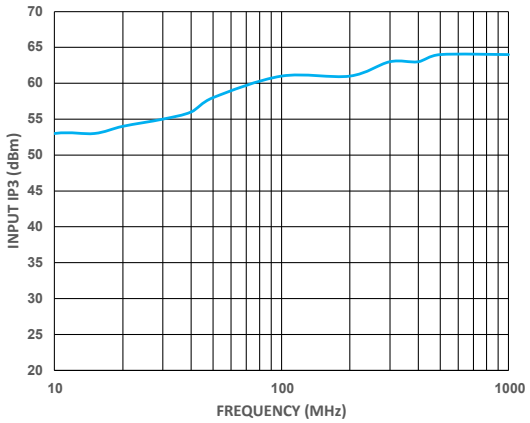

Figure 16. Input IP3 vs. Frequency (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5010 can interface CMOS/LVTTL compatible control interfaces directly.

CTRL determines which RF ports are in the insertion loss state and in the isolation state. See Table 6 for the control voltage truth table.

RF INPUT AND OUTPUT

RF ports (RF1 and RF2) are dc coupled to 0V and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. However, impedance matching on transmission lines can be used to improve insertion loss and return loss performance at high frequencies.

The ADRF5010 is bidirectional with equal power handling capabilities.

The insertion loss path conducts the RF signal between the RF1 and RF2 ports. The isolation path provides high loss between RF1 and RF2 ports which are 50 Ω terminated.

The power handling of the ADRF5010 derates with frequency below 0.1 GHz. See Figure 2 for derating of the RF power towards lower frequencies.

The ADRF5010 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures.
4. Apply signals to the RF input ports.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 6. Control Voltage Truth Table

Digital Control Input	RFx Paths
CTRL	**RF1 to RF2**
Low	Insertion loss (on)
High	Isolation (off)

APPLICATION INFORMATION

EVALUATION BOARD

The ADRF5010 has two power supply pins (VDD & VSS) and one control pin (CTRL). Figure 17 shows the external components and connections for the supply pin. The VDD and VSS pins are decoupled with a 100pF multilayer ceramic capacitor. The device pin-out allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0 V. See Pin Configuration and Function Description section for details.

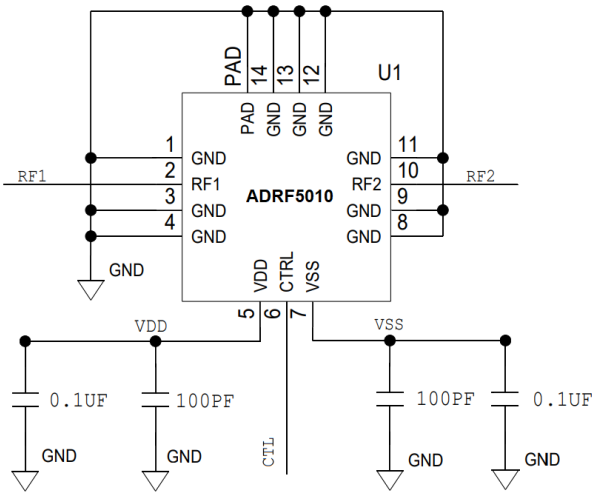

Figure 17. Recommended Schematic

RECOMMENDATIONS FOR PRINTED CIRCUIT BOARD DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 18 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003C dielectric material. RF trace with 14 mil width and 7 mil clearance is recommended for 1.5 mil finished copper thickness.

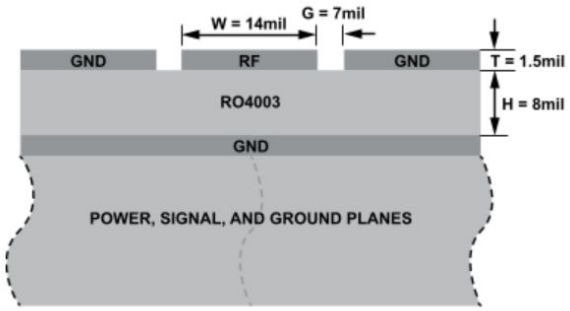

Figure 18. Example PCB Stack-up

Figure 19 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with densely filled through vias for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

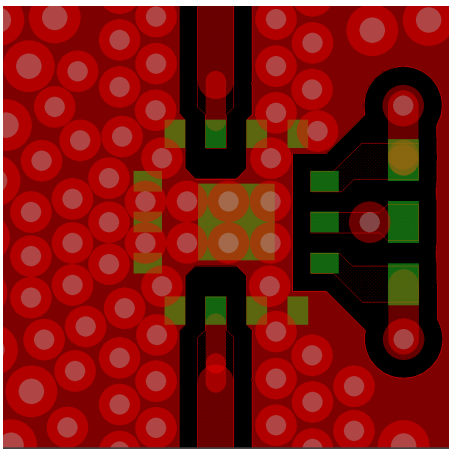

Figure 19. PCB routing

Figure 20 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn soldermask defined and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width till the package edge and tapered to RF trace. The paste mask is designed to match the device pads without any aperture reduction. The paste mask is divided into multiple openings for the paddle.

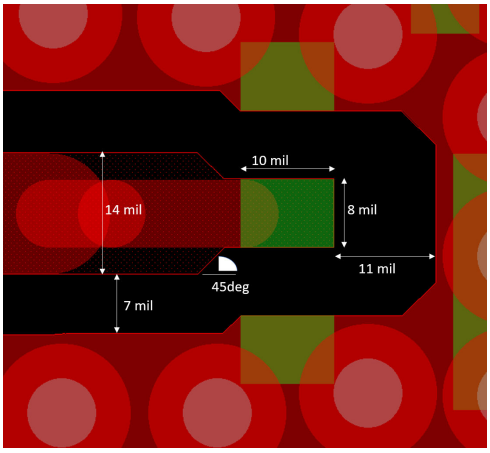

Figure 20. Recommended RF Pin Transition

For alternate PCB stack-ups with different dielectric thickness and RF trace design, contact Analog Devices Inc., Technical Support Request for further recommendations.

OUTLINE DIMENSIONS

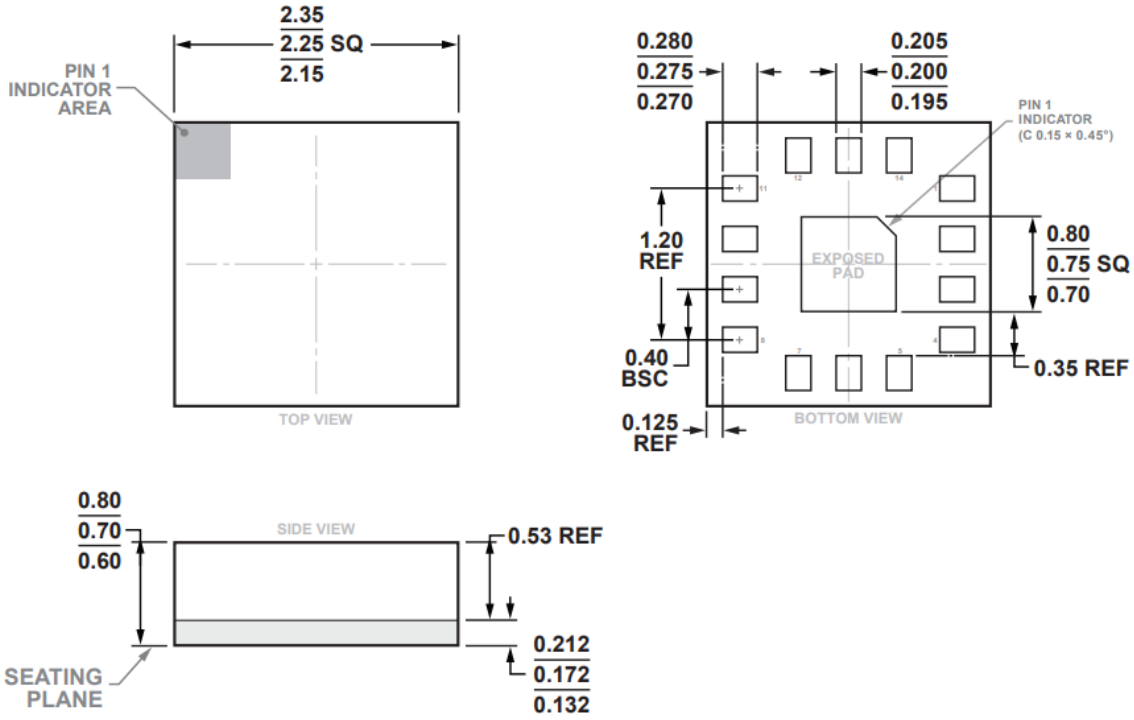

Figure 21. 14-Terminal Land Grid Array [LGA]
2.25 mm × 2.25 mm Body and 0.75 mm Package Height
(CC-14-5)
Dimensions shown in millimeters