Narrow-Band and Wideband RF Transceiver with Integrated Application Processor

FEATURES

- Integrated 1 Tx × 2 Rx RF transceiver
- Operating frequency range of 70 MHz to 6000 MHz
- Transmitter and wideband receiver signal bandwidth from 12 kHz to 40 MHz
- Narrowband receiver signal bandwidth from 12 kHz to 2 MHz
- 2 fully integrated, fractional-N, RF synthesizers
- 2 fully integrated, fractional-N, RF PLLs to control external VCO banks
- Supports external LO
- LVDS and CMOS synchronous serial data interface options
- Low power monitor and sleep modes
- Fully integrated DPD for narrowband waveforms
- User-programmable ARM core with 928 kB memory
- Interfaces include 2× UART, 2× I^2S, I^2C, QSPI, SPI, JTAG
- Library of hardware accelerators
- Fully programmable via a 4-wire SPI
- Package: 196-ball, 10 mm × 10 mm, CSP_BGA

APPLICATIONS

- Land Mobile Radios
- Mobile Satellite and Satellite IoT
- Wireless microphones
- Mission critical communications systems
- Smart Meters
- Factory Automation

GENERAL DESCRIPTION

The ADRV9104 is a highly integrated RF transceiver with an integrated application processor that has a single transmitter, dual receivers, integrated synthesizers, and digital signal processing functions. Its high performance, highly linear, high dynamic range transceiver designed for the lowest power consumption to support portable, and battery powered equipment. The ADRV9104 operates from 70 MHz to 6000 MHz and covers the UHF, VHF (from 70MHz), industrial, scientific, and medical (ISM) bands, and cellular frequency bands in narrow-band (kHz) and wideband operation up to 40 MHz. The ADRV9104 is capable of both TDD and uncalibrated FDD operation.

The transceiver consists of two direct conversion signal paths with state-of-the-art noise figure, dynamic range and linearity. Dedicated Narrow Band Receiver path can support up to 2MHz of RF signal BW. Dedicated Wide Band Receiver path can support up to 40MHz of RF signal BW. Each complete receiver and transmitter subsystem includes dc offset correction (Rx only), quadrature error correction (QEC), and programmable digital filters, which eliminate the need for these functions in the digital baseband. In addition, several auxiliary functions, such as auxiliary analog-to-digital converters (ADCs), auxiliary digital-to-analog converters (DACs), and general-purpose inputs/outputs (GPIOs), are integrated to provide additional monitoring and control capability.

The transmitter has internal modulator functions that can support modulation schemes for typical Land Mobile Radio (LMR) standards, such as Analog FM, Digital Mobile Radio (DMR), P25. The modulator integrates the symbol mapping, interpolation and pulse shaping functions which allow the basedband processor to send the 2bit symbols to ADRV9014 transmitter for modulation.

The fully integrated phase-locked loops (PLLs) provide high performance, low power, fractional-N frequency synthesis for the transmitter, receiver, and clock sections. Careful design and layout techniques provide the isolation required in high performance personal radio applications.

All voltage-controlled oscillator (VCO) and loop filter components are integrated to minimize the external component count. Integrated synthesizer is capable to interface with external Voltage Controlled Oscillator (VCO) to improve overall phase noise performance. The local oscillators (LOs) have flexible configuration options and include fast lock modes.

The fully integrated phase-locked loops (PLLs) with the necessary external VCO interface are capable of operating with banks of external VCOs to provide ultra low noise LOs for the transmitter and receivers.

The transceiver includes low power sleep and monitor modes to save power and extend the battery life of portable devices while monitoring communications.

The fully integrated, low power digital predistortion (DPD) is optimized for narrow-band TDD signals and enables linearization of high efficiency power amplifiers.

The ADRV9104 hosts a second processor, Processor Subsystem 2 (PS2), for users application specific programming. The ARM M4 has 928kB of useable memory, hardware accelerators, peripheral interfaces and runs up to 200MHz. This application processor can be used to implement modem like features on the transceiver customized to individual use cases.

The ADRV9104 core can be powered directly from 1.0 V and 1.8 V regulators and is controlled via a standard 4-wire serial port.

High data rate and low data rate interfaces are supported using configurable CMOS or low voltage differential signaling (LVDS) serial synchronous interface (SSI) choice. The ADRV9104 is packaged in a 10 mm × 10 mm, 0.65 pitch 196-ball chip scale package ball grid array (CSP_BGA).

Rev. PrA

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FUNCTIONAL BLOCK DIAGRAM

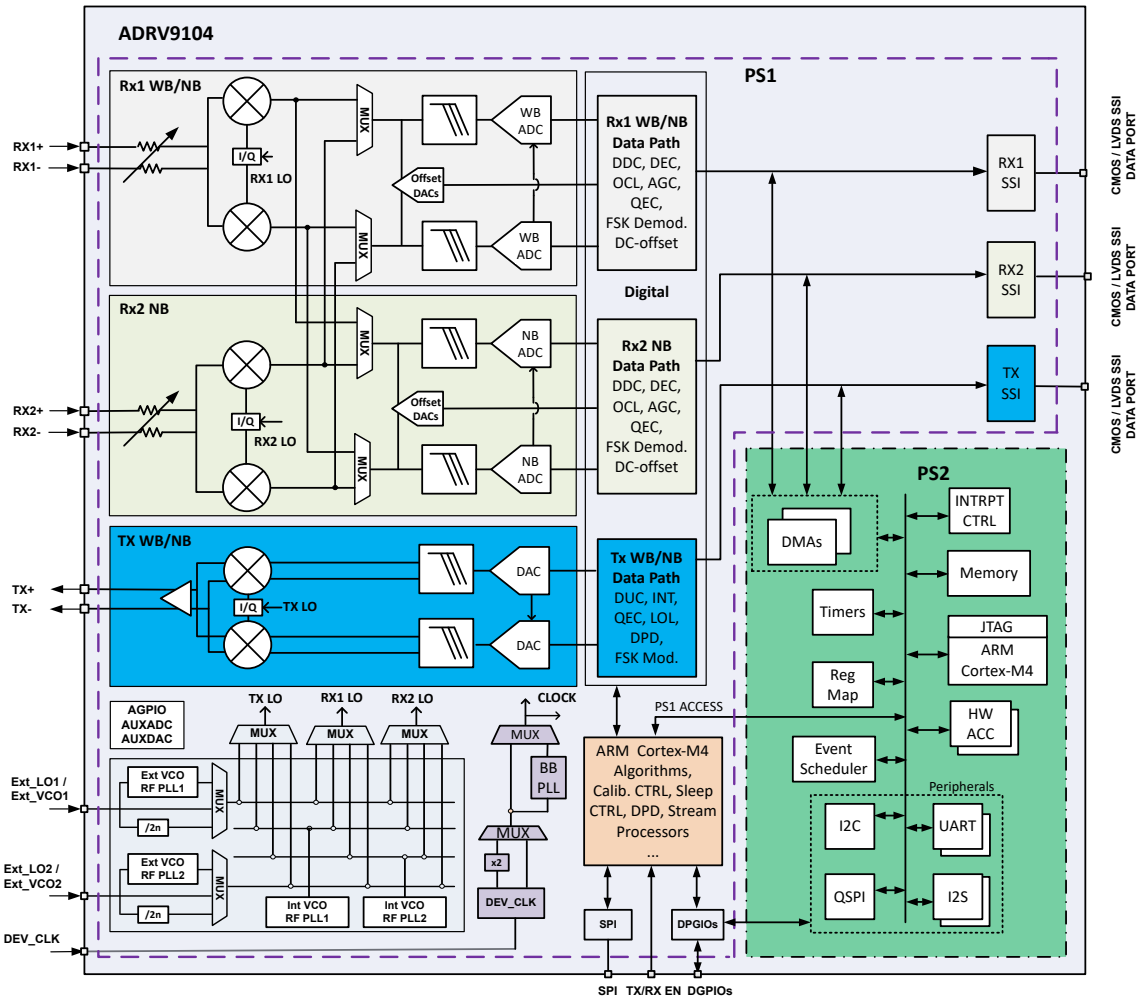

Figure 1. Functional Block Diagram

THEORY OF OPERATION

The ADRV9104 is a general-purpose Software Defined Radio (SDR) with extended capabilities for modem functionalities that can be configured for a wide range of applications. The device integrates all RF, mixed-signal, and digital blocks necessary to provide transmit and receive functions in a single device. Programmability allows the transmitter channel and two receiver channels to be used in TDD and FDD systems for mobile radio and cellular standards. The ADRV9104 contains serial interface links that consist of LVDS and a CMOS synchronous serial interface (LSSI/CSSI). Both receiver and transmitter channels provide a low pin count and reliable data interface to a field-programmable gate array (FPGA) or other integrated baseband solutions.

TRANSMITTER

The ADRV9104 uses a direct conversion transmitter architecture that provides digital processing, mixed signals, PLL, and RF blocks necessary to implement a direct conversion system.

The ADRV9104 has an optional, fully programmable, 128-tap FIR. The FIR output is sent to a series of interpolation filters that provide additional filtering and data rate interpolation prior to reaching the DAC. Each DAC has an adjustable sample rate and is linear up to full scale. The configurable digital datapath design allows the transmitter to support narrow band or wide band applications.

The DAC output produces baseband analog signals. The I and Q signals are first filtered to remove sampling artifacts and then fed to the up conversion mixers. At the mixer stage, the I and Q signals are recombined and upconverted to the carrier frequency for transmission to the output stage. The transmit chain provides a wide attenuation adjustment range with fine granularity to help designers optimize the signal-to-noise ratio (SNR).

RECEIVER

ADRV9104 contains two receiver paths: Rx1 WB/NB is a wide to narrow band path with up to 40 MHz RF bandwidth; Rx2 NB is a dedicated low power narrow band path with up to 2 MHz RF bandwidth. Both receivers, Rx1 WB/NB and Rx2 NB, are a fully integrated, direct conversion receiver signal chains with digital NCOs enabling support for low IF mode. The receiver subsystems consist of a resistive input network for gain control followed by a current mode passive mixer. The output current of the mixer is converted to a voltage by a transimpedance amplifier and then digitized by the ADC. There is a wide band, high performance Σ-Δ ADC on Rx channel 1 and a narrow band, high performance Σ-Δ ADC on Rx channel 2. The digital baseband that provides the required filtering and decimation follows these ADCs. The mixer architecture is linear and inherently wideband, which facilitates impedance matching. The differential input impedance of the receiver inputs is 100 Ω. To achieve gain control, a programmed gain index map is implemented. This gain map distributes attenuation among the various receiver blocks for optimal performance at each power level. The gain range is 34 dB. The ADRV9104 is a wideband architecture transceiver that relies on the ADC high dynamic range to receive signals and interference at the same time. Filtering provided by the receive LPF attenuates ADC alias images.

The receive LPF characteristic is flat and not intended to provide rejection of close in blockers.

The ADC output can be conditioned further by a series of decimation filters and a fully programmable, FIR filter with additional decimation settings. The sample rate of each digital filter block automatically adjusts with each change of the decimation factors to produce the desired output data rate.

For standards that demand low phase noise performance, the receiver supports Intermediate Frequency (IF) receive architecture where the LO frequency is offset by that of the receive carrier frequency. The IF signal at the mixer and LPF output is digitalized by ADC, the digital down converter with the NCO down converts the IF signal to baseband. The ADRV9104 makes no assumptions about high-side or low-side injection.

CLOCK INPUT

The reference clock inputs provide a low frequency clock from which all internal ADRV9104 clocks are derived. The ADRV9104 offers multiple reference input clocking options. The reference input clock pins on the device are labeled DEV_CLK_IN±. If a differential input clock is provided, the clock signal must be ac-coupled with the input range limited from 10 MHz to 307.2MHz. The ADRV9104 can also accept an external crystal (XTAL) as a clock source. The frequency range of the supported crystal is between 20 MHz to 80 MHz. The external crystal connection must be dc-coupled. If a differential clock is not available, a single-ended, ac-coupled, 1 V p-p (maximum) CMOS signal can be applied to the DEV_CLK_IN+ pin with the DEV_CLK_IN− pin unconnected. The maximum clock frequency in this mode is limited to 80 MHz.

SYNTHESIZERS

The ADRV9104 offers two distinct PLL paths, an RF PLL for the high frequency RF path and a baseband PLL for the digital and sampling clocks of the data converters.

THEORY OF OPERATION

RF PLL

The PLL structure in the ADRV9104 is unique as it includes two internal RF PLLs with fully integrated on-chip VCOs and two internal RF PLLs fit for external VCOs. The RF PLL supports the use of internal LO signals, external LO signals and external VCO signals. Any of these sources can be routed to any or all the RF channels. This flexibility enables the ADRV9104 to meet various applications that require versatility.

The internal LO is generated by an on-chip VCO, which is tunable over a frequency range of 6.5 GHz to 13 GHz. The output of the VCO is phase-locked to an external reference clock through a fractional-N PLL that is programmable. The VCO outputs are steered through a combination of frequency dividers to produce in-phase and quadrature phase LO signals in the 70 MHz to 6 GHz frequency range.

An external LO signal can be applied to the external LO inputs of the ADRV9104 to generate the LO signals in quadrature for the RF path. If the external LO path is chosen, the input frequency range is between 60 MHz and 12 GHz.

Alternatively, the ADRV9104 internal PLLs can interface with external VCO design, the external VCO outputs are applied to the ADRV9104 external LO inputs and are phase locked to the reference clock through the internal programmable factional-N PLLs. This allows integration of custom VCO designs for maximum versatility in LO generation.

BASEBAND PLL

The ADRV9104 contains a baseband PLL synthesizer that generates all baseband and data port related clocks. The ADRV9104 has the option to disable the baseband PLL and utilizes the reference clock input, or reference clock input with doubler, to generate all baseband and data port related clocks.

THEORY OF OPERATION

PROCESSOR SUBSYSTEM 2 (PS2)

The ADRV9104 enables users to jump start designs for a flexible wireless connectivity by implementing various protocol stack layers from physical (PHY) to upper layers (L1/L2/L3). The ADRV9104 PS2 contains dedicated hardware accelerators to support all major PHY layer functions, enabling development for a wide range of wireless applications.

The ADRV9104 PS2 block diagram is shown in Figure 1, which consists of the transceiver component (ADRV9104 PS1) and the extended open ARM Cortex-M4 processor-based PS2 for the functions of the modem upper protocol stack layer.

By bringing an ARM Cortex-M4 subsystem with 928 kB of memory, a variety of peripherals, and flexible and scalable hardware accelerators for protocol stack functions together, the ADRV9104 PS2 gives developers more design choices for rapid deployment of applications requiring wireless connectivity.

The ADRV9104 PS2 main features include the following:

- An ARM processor Cortex-M4 subsystem
- 928 kB of useable memory
- Direct memory access (DMA) controllers to transfer data between PS2 memory, SSI, the PS1 data path and peripherals
- A variety of peripherals: SPI-M, SPI-S, I^2C, I^2S, Q-SPI, UART
- Timers and system event scheduler
- Dedicated PHY hardware accelerators (DSP and communication)

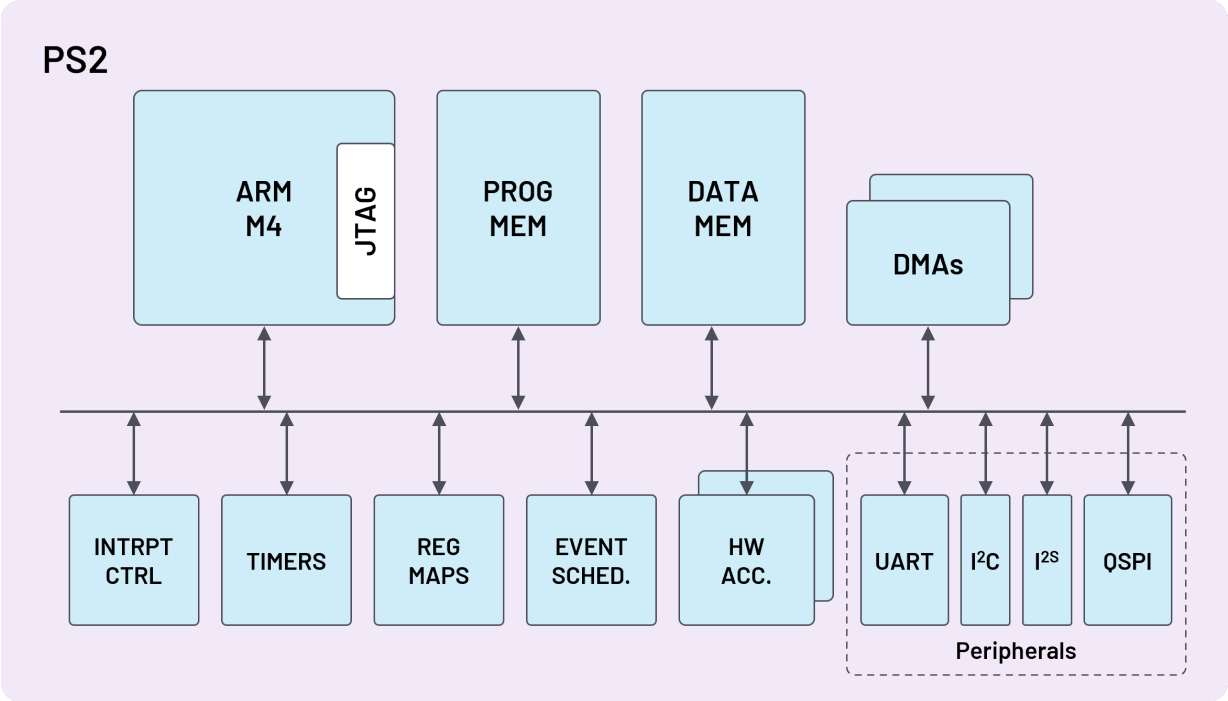

Figure 2. PS2 Block Diagram

OUTLINE DIMENSIONS

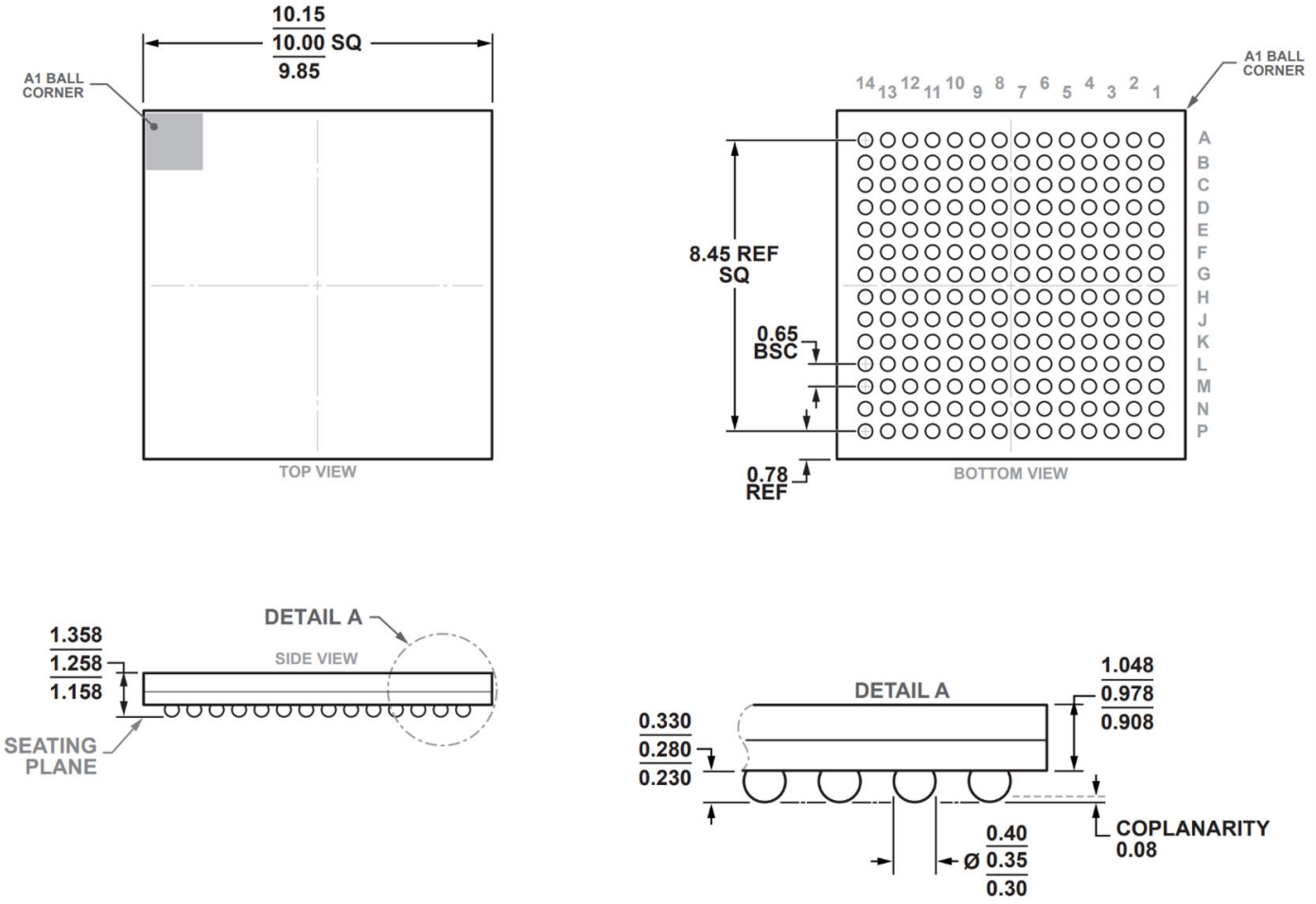

Figure 3. 196-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-196-16)
Dimensions shown in millimeters