REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 21-03-04	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** JAMES R. ESCHMEYER	TITLE MICROCIRCUIT, DIGITAL, LOW POWER, PRECISION ANALOG MICROCONTROLLER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/21606**
	REV	**PAGE** 1 **OF** 22

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AMSC N/A

5962-V029-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low power, precision analog microcontroller microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/21606	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADUCM362-EP	Low power, precision analog microcontroller

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MO-220-WKKD-4	Lead frame chip scale package (LFCSP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

AVDD to AGND	-0.3 V to +3.96 V
IOVDD to DGND	-0.3 V to +3.96 V 2/
Digital input voltage to DGND	-0.3 V to +3.96 V 2/
Digital output voltage to DGND	-0.3 V to +3.96 V 2/
Analog inputs to AGND	-0.3 V to +3.96 V
Temperature:	
Operating range	-55°C to +125°C
Storage range	-65°C to +150°C
Junction (T_J)	+150°C
Peak solder reflow:	
Tin Lead (SnPb) assemblies (10 seconds to 30 seconds)	240°C
Nickel (Ni), Palladium (Pd), Gold (Au) assemblies (20 seconds to 40 seconds)	260°C
Thermal resistance, junction to case (θ_{JC})	9.5°C/W
Thermal resistance, junction to ambient (θ_{JA})	28°C/W
Electrostatic discharge (ESD) rating:	
Human body model (HBM) per JEDEC JS-001	±2 kV
Field induced charged device model (FICDM) per JEDEC JS-002	±1000 V

1.4 Recommended operating conditions. 3/

AVDD/IOVDD	1.8 V to 3.6 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ DGND is the digital system ground reference.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JEDEC JS-002	–	Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM)
JESD22-A117	–	Electrically Eraseable Programmable Rom (EEPROM) Program/Erase Endurance and Data Retention Test
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
ADC specifications section.		ADC0 and ADC1					
Conversion rate 3/		Chop off	-55°C to +125°C	01	3.5	3906	Hz
		Chop on			3.5	1302	
No missing codes 3/		Chop off, ADC frequency (fADC) ≤ 500 Hz	-55°C to +125°C	01	24		Bits
		Chop on, fADC ≤ 250 Hz			24		
Integral nonlinearity 3/		Gain = 1, input buffer off	-55°C to +125°C	01	±10 typical		ppm of FSR
		Gain = 2, 4, 8, or 16			±15 typical		
		Gain = 32, 64, or 128			±20 typical		
Offset error 4/ 5/ 6/ 7/ 8/		Chop off, and the offset error is in the order of the noise for the programmed gain and update rate following calibration	-55°C to +125°C	01	±230/gain typical		μV
		Chop on 3/			±1.0		
Offset error drift versus temperature 3/ 6/ 7/		Chop off, gain ≤ 4	-55°C to +125°C	01	1/gain typical		μV/°C
		Chop off, gain ≥ 8			230 typical		
		Chop on			10 typical		
Offset error lifetime 9/ stability		Gain = 128	-55°C to +125°C	01	1 typical		μV / 1000 Hr
Full scale error 3/ 6/ 7/ 8/ 10/			-55°C to +125°C	01	±0.5/gain typical		mV
Full scale error 9/ lifetime stability		Gain = 128	-55°C to +125°C	01	70 typical		μV / 1000 Hr
Gain error drift versus temperature 3/ 6/ 7/		Gain = 1, 2, 4, 8, or 16, External reference	-55°C to +125°C	01	±3 typical		ppm/°C
		Gain = 32, 64, or 128, External reference			±6 typical		
PGA gain mismatch error			-55°C to +125°C	01	±0.15 typical		%

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
ADC specifications section – continued. ADC0 and ADC1							
Power supply rejection 3/		Chop on, ADC input = 0.25 V, gain = 4, external reference	-55°C to +125°C	01	95		dB
		Chop off, ADC input = 0.78 V, gain = 128, external reference			80		
		Chop off, ADC input = 1 V, gain = 1, external reference			90		
Absolute input voltage range, unbuffered mode			-55°C to +125°C	01	AGND	AVDD	V
Absolute input voltage range, buffered mode		Available for all gain settings, G = 1 to 128	-55°C to +125°C	01	AGND + 0.1	AVDD – 0.1	V
Differential input voltage ranges 3/		Gain = 1	-55°C to +125°C	01		±VREF	V
		Gain = 2				±500	mV
		Gain = 4				±250	
		Gain = 8				±125	
		Gain = 16				±62.5	
Common mode voltage 3/	V_{CM}	Ideally, V_{CM} = ((AIN+) + (AIN−))/2 and gain = 2 to 128, where AIN+ or AIN− refers to any ADC input pin in which the sign indicates a positive or negative voltage input, respectively	-55°C to +125°C	01	AGND	AVDD	V
Input current, buffered mode 11/		Gain > 1 (excluding AIN4, AIN5, AIN6, and AIN7 pins)	-55°C to +125°C	01	1 typical		nA
		Gain > 1 (AIN4, AIN5, AIN6, and AIN7 pins)			2 typical		
Input current, unbuffered mode 11/		Input current varies with input voltage	-55°C to +125°C	01	860 typical		nA/V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
ADC specification section – continued. ADC0 and ADC1							
Average input current drift, buffered mode 3/		AIN1, AIN3, AIN5, AIN7, and AIN11	-55°C to +125°C	01	±5 typical		pA/°C
		AIN0, AIN4, AIN9, and AIN10			±9 typical		
		AIN2, AIN6, and AIN8			±15 typical		
Average input current drift, unbuffered mode 3/			-55°C to +125°C	01	±250 typical		pA/V/°C
Common mode rejection, dc 3/	CMR	On ADC input, ADC gain = 1, AVDD < 2 V	-55°C to +125°C	01	100 typical		dB
					65		
		On ADC input, ADC gain = 1, AVDD > 2 V			100 typical		
					80		
		On ADC input, ADC gain = 2 to 128			80		
Common mode rejection, 50 Hz/60Hz 3/	CMR	ADC gain = 1, 50 Hz/60 Hz ± 1 Hz, f_{ADC} = 16.67 Hz with chop on, and f_{ADC} = 50 Hz with chop off	-55°C to +125°C	01	97		dB
		ADC gain = 2 to 128, 50 Hz/60 Hz ± 1 Hz, f_{ADC} = 16.67 Hz with chop on, and f_{ADC} = 50 Hz with chop off			90		
Normal mode rejection, 50 Hz/60Hz 3/	NMR	On ADC input, 50 Hz/60 Hz ± 1 Hz, f_{ADC} = 16.67 Hz with chop on, and f_{ADC} = 50 Hz with chop off	-55°C to +125°C	01	80 typical		dB
					60		
Temperature sensor section. 3/							
Voltage output		After use calibration, processor powered down or in standby mode before measurements	+25°C	01	82.1 typical		mV
Voltage temperature coefficient			-55°C to +125°C	01	250 typical		µV/°C
Accuracy			-55°C to +125°C	01	6 typical		°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Ground switch section.							
On resistance	R_{ON}		-55°C to +125°C	01	10 typical		Ω
					3.7	19	
Allowable current 3/		20 kΩ resistor off, direct short to ground	-55°C to +125°C	01		20	mA
Voltage reference section.		ADC internal reference					
Internal reference voltage	V_{REF}		-55°C to +125°C	01	1.2 typical		V
Initial accuracy			+25°C	01	-0.1	+0.1	%
Reference 3/ 12/ temperature coefficient			-55°C to +125°C	01	±5 typical		ppm/°C
					-15	+15	
Power supply 3/ rejection	PSR		-55°C to +125°C	01	90 typical		dB
					82		
External reference inputs section.							
Input range, buffered model		Minimum differential voltage between VREF+ and VREF− pins is 400 mV	-55°C to +125°C	01	AGND + 0.1	AVDD – 0.1	V
Input range, unbuffered model			-55°C to +125°C	01	0	AVDD	V
Input current, buffered mode		Minimum differential voltage between VREF+ and VREF− pins is 400 mV	-55°C to +125°C	01	+10 typical		nA
					-20	+27	
Input current, unbuffered mode			-55°C to +125°C	01	500 typical		nA/V
Normal mode 3/ rejection			-55°C to +125°C	01	80 typical		dB
Common mode 3/ rejection			-55°C to +125°C	01	100 typical		dB
					85		
Reference detect 3/ levels			-55°C to +125°C	01	400 typical		mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Excitation current sources section.							
Output current		Available from each current source, value programmable from 10 µA to 1 mA	-55°C to +125°C	01	10	1000	µA
Initial tolerance		Output current (I_{OUT}) ≥ 50 µA	+25°C	01	±5 typical		%
Drift 3/		Using internal reference resistor	-55°C to +125°C	01	100 typical		ppm/°C
						400	
		Using external 150 kΩ reference resistor between IREF pin and AGND, and the resistor must have a drift specification of 5 ppm/°C			75 typical		
						400	
Initial current matching 3/		Matching between both current sources	+25°C	01	±0.5 typical		%
Drift matching 3/			-55°C to +125°C	01	50 typical		ppm/°C
Load regulation, AVDD 3/		AVDD = 3.3 V	-55°C to +125°C	01	0.2 typical		%/V
Output compliance 3/		I_{OUT} = 10 µA to 210 µA	-55°C to +125°C	01	AGND – 0.03	AVDD – 0.85	V
		I_{OUT} > 210 µA			AGND – 0.03	AVDD – 1.1	
DAC channel specifications section. Load resistance (RL) = 5 kΩ and load capacitance (CL) = 100 pF							
Voltage range		Internal reference	-55°C to +125°C	01	0	V_{REF}	V
		External reference			0	1.8	
DC specifications 13/							
Resolution			-55°C to +125°C	01	12		Bits
Relative accuracy			-55°C to +125°C	01	±3 typical		LSB
Differential nonlinearity		Guaranteed monotonic	-55°C to +125°C	01	±0.5 typical		LSB
						±1	
Offset error	OE	1.2 V internal reference	-55°C to +125°C	01	±2 typical		mV
						±10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DAC channel specifications section - continued. Load resistance (RL) = 5 kΩ and load capacitance (CL) = 100 pF							
DC specifications – continued. 13/							
Gain error		VREF range (reference = 1.2 V)	-55°C to +125°C	01		±0.5	%
NPN mode. 3/							
Resolution			-55°C to +125°C	01	12		Bits
Relative accuracy			-55°C to +125°C	01	±3 typical		LSB
Differential nonlinearity			-55°C to +125°C	01	±0.5 typical		LSB
Offset error			-55°C to +125°C	01	±0.35 typical		mA
Gain error			-55°C to +125°C	01	±0.75 typical		mA
Output current range			-55°C to +125°C	01	0.008	23.6	mA
Interpolation mode. 3/ 14/		Only monotonic to 14 bits					
Resolution			-55°C to +125°C	01	14 typical		Bits
Relative accuracy		For 14 bits resolution	-55°C to +125°C	01	±6 typical		LSB
Differential nonlinearity		Monotonic (14 bits)	-55°C to +125°C	01	±0.6 typical		LSB
Offset error		1.2 V internal reference	-55°C to +125°C	01	±2 typical		mA
Gain error		V_{REF} range (reference = 1.2 V)	-55°C to +125°C	01	±1 typical		%
		AVDD range			±1 typical		
DAC AC characteristics section. 3/							
Voltage output settling time			-55°C to +125°C	01	10 typical		μs
Digital to analog glitch energy		1 LSB change at major carry (maximum number of bits changes simultaneously in the DACDAT register)	-55°C to +125°C	01	±20 typical		nV-sec
Power on reset (POR) section.							
POR trip level		Voltage at IOVDD pin, power on levels	-55°C to +125°C	01	1.65 typical		V
		Voltage at IOVDD pin, power down levels			1.65 typical		
Timeout from POR 3/			-55°C to +125°C	01	50 typical		ms

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Watchdog timer (WDT) section. 3/							
Timeout period			-55°C to +125°C	01	0.00003	8192	sec
Timeout step size		Register T3CON, bits[3:2] (PRE) = 10	-55°C to +125°C	01	7.8125 typical		ms
Flash/EE memory section. 3/							
Endurance 15/			-40°C to +125°C	01	10,000		Cycles
Read			-55°C to +125°C	01	10,000		Cycles
Write			-55°C to -40°C	01	1000		Cycles
Data Retention 16/			T_J = +85°C	01	10		Years
Digital inputs section.		All digital inputs					
Input leakage current.		Digital inputs except for the $\overline{\text{RESET}}$, SWCLK, and SWDIO pins					
Logic 1		High input voltage (V_{INH}) = IOVDD or V_{INH} = 1.8 V	-55°C to +125°C	01	140 typical		µA
		Internal pull-up disabled			1 typical		nA
Logic 0		Low input voltage (VINL) = 0 V	-55°C to +125°C	01	160 typical		µA
		Internal pull up disabled			10 typical		nA
Input leakage current.		$\overline{\text{RESET}}$, SWCLK, and SWDIO pins					
Logic 1			-55°C to +125°C	01	140 typical		µA
Logic 0			-55°C to +125°C	01	160 typical		µA
Input capacitance 3/	C_{IN}		-55°C to +125°C	01	10 typical		pF
Logic input voltage, low	V_{INL}		-55°C to +125°C	01		0.2 x IOVDD	V
Logic input voltage, high	V_{INH}		-55°C to +125°C	01	0.7 x IOVDD		V
Logic output voltage, high	V_{OH}	Source current (I_{SOURCE}) = 1 mA	-55°C to +125°C	01	IOVDD – 0.4		V
Logic output voltage, low	V_{OL}	Sink current (I_{SINK}) = 1 mA	-55°C to +125°C	01		0.4	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Crystal oscillator section. 3/		32.768 kHz crystal inputs					
Logic input 17/ voltage, XTALI only	V_{INL}		-55°C to +125°C	01		0.8	V
	V_{INH}				1.7		
XTALI capacitance			-55°C to +125°C	01	6 typical		pF
XTALO capacitance			-55°C to +125°C	01	6 typical		pF
On chip low power oscillator section.							
Oscillator frequency			-55°C to +125°C	01	32.768 typical		kHz
Accuracy			-55°C to +125°C	01	±10 typical		%
					-30	+30	
On chip high frequency oscillator section.							
Oscillator frequency			-55°C to +125°C	01	16 typical		MHz
Accuracy			-55°C to +125°C	01	-1.8	+1.4	%
Long term stability 9/			-55°C to +125°C	01	0.8 typical		°C / 1000 Hr
Processor clock rate 3/ section		Nine programmable core clock selections within specified range	-55°C to +125°C	01	0.5 typical		MHz
					0.0625	16	
Using an external clock			-55°C to +125°C	01	0.032768	16	MHz
Processor start up time section. 3/							
At power on		Includes kernel power on execution time	-55°C to +125°C	01	41 typical		ms
After reset event			-55°C to +125°C	01	1.44 typical		ms
From processor power down (mode 1, mode 2, and mode 3)		Clock frequency (f_{CLK}) is the Cortex-M3 core clock	-55°C to +125°C	01	3 to 5 typical		f_{CLK}
From total halt or hibernate mode (mode 4 or mode 5)		Clock frequency (f_{CLK}) is the Cortex-M3 core clock	-55°C to +125°C	01	30.8 typical		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power requirements section.							
Power supply voltage range	VDD	AVDD, IOVDD	-55°C to +125°C	01	1.8	3.6	V
Power consumption.							
I_{DD} (microcontroller unit (MCU) active mode 18/ 19/		Processor clock rate = 16 MHz, all peripherals on (CLKSYSDIV = 0)	-55°C to +125°C	01	5.5 typical		mA
		Processor clock rate = 8 MHz, all peripherals on (CLKSYSDIV = 1)			3 typical		
		Processor clock rate = 500 kHz, both ADCs on (input buffers off) with PGA gain = 4, 1 × SPI port on, and all timers on			1 typical		
I_{DD} (MCU powered down)		Total halt mode (mode 4)	-55°C to +125°C	01	4 typical		µA
I_{DD}, total (ADC0) 19/		PGA enabled, gain ≥ 32	-55°C to +125°C	01	320 typical		µA
PGA		Gain = 4, 8, or 16, PGA only	-55°C to +125°C	01	130 typical		µA
		Gain = 32, 64, 0r 128, PGA only			180 typical		
Input buffers		2 x input buffers = 70 µA	-55°C to +125°C	01	70 typical		µA
Digital interface and modulator			-55°C to +125°C	01	70 typical		µA
I_{DD} (ADC1)		Input buffers off, gain = 4, 8, or 16 only	-55°C to +125°C	01	200 typical		µA
External reference input buffers		60 µA each	-55°C to +125°C	01	120 typical		µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, AVDD/IOVDD = 1.8 V to 3.6 V, internal 1.2 V reference, core frequency (f_{CORE}) = 16 MHz, and all specifications at T_A = -55°C to +125°C.

3/ These numbers are not production tested but are guaranteed by design and/or characterization data at production release.

4/ Tested at gain = 4 after initial offset calibration

5/ Measured with an internal short. A system zero-scale calibration removes this error

6/ A recalibration at any temperature removes these errors

7/ These numbers do not include internal reference temperature drift

8/ Factory calibrated at gain = 1.

9/ The long term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

10/ System calibration at a specific gain removes the error at this gain.

11/ Input current is measured with one ADC measuring a channel. If both ADCs measure the same input channel, the input current increases (approximately doubles).

12/ Measured using the box method.

13/ Reference DAC linearity is calculated using a reduced code range of 0x0AB to 0xF30.

14/ Measured using a low-pass filter with resistance = 1 kΩ and capacitance = 100 nF.

.

15/ Endurance is qualified to 10,000 cycles as per JEDEC Standard 22, Method A117 and is measured at −40°C, +25°C, and +125°C. Typical endurance at 25°C is 170,000 cycles.

16/ Retention lifetime equivalent at T_J = 85°C as per JEDEC Standard 22, Method A117. Retention lifetime derates with junction temperature.

17/ Voltage input levels are relevant only if driving the crystal input from a voltage source. If a crystal is connected directly, the internal crystal interface determines the common-mode voltage.

18/ Typical additional supply current (I_{DD}) consumed during Flash/EE memory program and erase cycles are 7 mA.

19/ Total I_{DD} for ADC includes figures for PGA ≥ 32, input buffers, digital interface, and the Σ-Δ modulator.

Case X

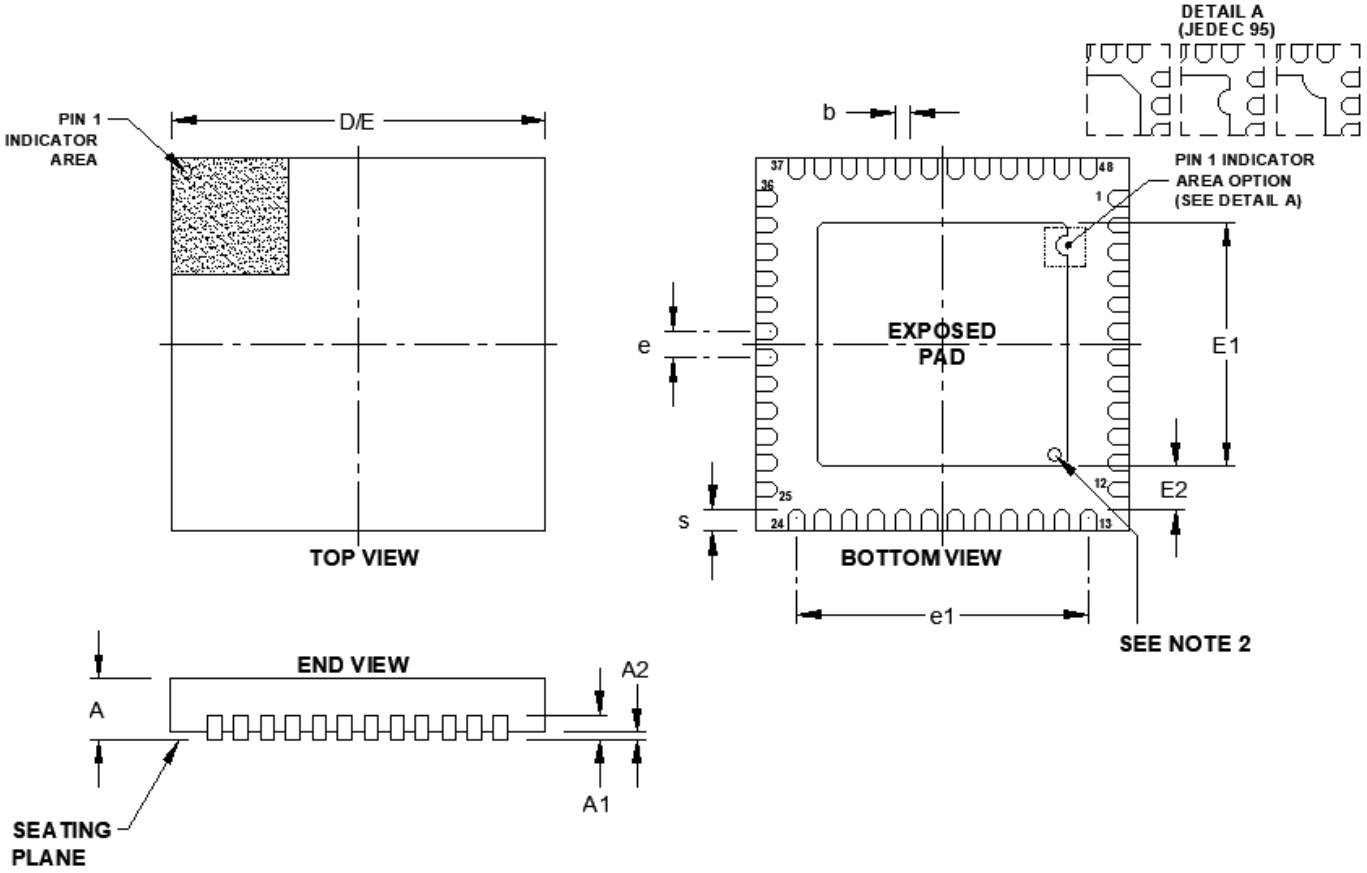

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/21606
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Case X - continued

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.027	.029	.031	0.70	0.75	0.80
A1	.008 REF			0.203 REF		
A2	.001	---	.002	0.02	---	0.05
COPLANARITY	.003	---	---	0.08	---	---
b	.007	.009	.011	0.18	0.23	0.30
D/E	.272	.275	.279	6.90	7.00	7.10
E1	.197	.201	.205	5.00	5.10	5.20
E2	.008	---	---	0.20	---	---
e	.020 BSC			0.50 BSC		
e1	.216 REF			5.50 REF		
s	.014	.016	.018	0.35	0.40	0.45

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	$\overline{\text{RESET}}$	Reset Pin, Active Low Input. An internal pull-up is provided.
2	P2.1/SDA/ UART1DCD/ UARTDCD	General-Purpose Input/Output P2.1/I^2C Serial Data Pin/UART1 Data Carrier Detect Pin/UART Data Carrier Detect Pin.
3	P2.2/BM	General-Purpose Input/Output P2.2/Boot Mode Input Select Pin. When the P2.2/BM pin is held low during and for a short time after any reset sequence, the device enters UART download mode.
4	XTALO	External Crystal Oscillator Output Pin. Optional 32.768 kHz source for real-time clock.
5	XTALI	External Crystal Oscillator Input Pin. Optional 32.768 kHz source for real-time clock.
6	IOVDD	Digital System Supply Pin. IOVDD must be connected to the digital system ground reference (DGND) via a 0.1 µF capacitor.
7	DVDD_REG	Digital Regulator Supply. DVDD_REG must be connected to DGND via a 470 nF capacitor and to AVDD_REG (Pin 18).
8	AIN0	ADC Analog Input 0. AIN0 can be configured as a positive or negative input to either ADC in differential or single-ended mode.
9	AIN1	ADC Analog Input 1. AIN1 can be configured as a positive or negative input to either ADC in differential or single-ended mode.
10	AIN2	ADC Analog Input 2. AIN2 can be configured as a positive or negative input to either ADC in differential or single-ended mode.
11	AIN3	ADC Analog Input 3. AIN3 can be configured as a positive or negative input to either ADC in differential or single-ended mode.
12	AIN4/IEXC	ADC Analog Input 4/Excitation Current Source. AIN4 can be configured as a positive or negative input to either ADC in differential or single-ended mode. IEXC can be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1.

FIGURE 2. Terminal connections.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
13	GND_SW	Sensor Power Switch to Analog Ground Reference.
14	VREF+	External Reference Positive Input. An external reference can be applied between the VREF+ and VREF− pins.
15	VREF−	External Reference Negative Input. An external reference can be applied between the VREF+ and VREF− pins.
16	AGND	Analog System Ground Reference Pin.
17	AVDD	Analog System Supply Pin. AVDD must be connected to AGND via a 0.1 µF capacitor.
18	AVDD_REG	Internal Analog Regulator Supply Output. AVDD_REG must be connected to AGND via a 470 nF capacitor and to DVDD_REG (Pin 7).
19	DAC	DAC Voltage Output.
20	INT_REF	Internal Reference. INT_REF must be connected to ground via a 470 nF decoupling capacitor.
21	IREF	Optional Reference Current Resistor Connection for the Excitation Current Sources. The reference current used for the excitation current sources is set by a low drift (5 ppm/°C) external resistor connected to IREF.
22	AIN5/IEXC	ADC Analog Input 5/Excitation Current Source. AIN5 can be configured as a positive or negative input to either ADC in differential or single-ended mode. IEXC can also be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1.
23	AIN6/IEXC	ADC Analog Input 6/Excitation Current Source. AIN6 can be configured as a positive or negative input to either ADC in differential or single-ended mode. IEXC can also be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1.
24	AIN7/VBIAS0/ IEXC/ EXTREF2IN+	ADC Analog Input 7/Bias Voltage Output/Excitation Current Source/External Reference 2 Positive Input. AIN7 can be configured as a positive or negative input to either an ADC in differential or single-ended mode. VBIAS0 can be configured as an analog output pin to generate the bias voltage, VBIAS0, of AVDD_REG/2. IEXC can be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1. EXTREF2IN+ can be configured as the positive input for External Reference 2.

FIGURE 2. Terminal connections - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
25	AIN8/ EXTREF2IN−	ADC Analog Input 8/External Reference 2 Negative Input. AIN8 can be configured as a positive or negative input to either an ADC in differential or single-ended mode. EXTREF2IN− can be configured as the negative input for External Reference 2.
26	AIN9/ DACBUFF+	ADC Analog Input 9/Noninverting Input to the DAC Output Buffer. AIN9 can be configured as a positive or negative input to either an ADC in differential or single-ended mode. DACBUFF+ can be configured as the noninverting input to the DAC output buffer when the DAC is configured for NPN mode.
27	AIN10	ADC Analog Input 10. AIN10 can be configured as a positive or negative input to either ADC in differential or single-ended mode.
28	AIN11/VBIAS1	ADC Analog Input 11/Bias Voltage Output. AIN11 can be configured as a positive or negative input to either an ADC in differential or single-ended mode. VBIAS1 can be configured as an analog output pin to generate the bias voltage, VBIAS1, of AVDD_REG/2.
29	P0.0/MISO1/ UART1DCD/ UARTDCD	General-Purpose Input/Output P0.0/SPI1 Master Input, Slave Output Pin/UART1 Data Carrier Detect Pin/UART Data Carrier Detect Pin.
30	P0.1/SCLK1/ SCL/RxD	General-Purpose Input/Output P0.1/SPI1 Serial Clock Pin/I^2C Serial Clock Pin/UART Serial Input (Data Input for the UART Downloader).
31	P0.2/MOSI1/ SDA/TxD	General-Purpose Input/Output P0.2/SPI1 Master Output, Slave Input Pin/I^2C Serial Data Pin/ UART Serial Output (Data Output for the UART Downloader).
32	P0.3/IRQ0/ CS1/RTS1/RTS	General-Purpose Input/Output P0.3/External Interrupt Request 0/SPI1 Chip Select Pin, Active Low (When Using SPI1, Configure as CS1)/UART1 Request to Send Signal/UART Request to Send Signal.
33	P0.4/RTS/ECLKO/ RTS1	General-Purpose Input/Output P0.4/UART Request to Send Signal/External Clock Output Pin for Test Purposes/UART1 Request to Send Signal.
34	P0.5/IRQ1/CTS	General-Purpose Input/Output P0.5/External Interrupt Request 1/UART Clear to Send Signal.
35	P0.6/IRQ2/RxD1	General-Purpose Input/Output P0.6/External Interrupt Request 2/UART1 Serial Input.
36	P0.7/POR/TxD1	General-Purpose Input/Output P0.7/Power-On Reset Pin (Active High)/UART1 Serial Output.

FIGURE 2. Terminal connections - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
37	IOVDD	Digital System Supply Pin. IOVDD must be connected to DGND via a 0.1 µF capacitor.
38	P1.0/IRQ3/ PWMSYNC/ EXTCLK	General-Purpose Input/Output P1.0/External Interrupt Request 3/PWM External Synchronization Input/External Clock Input Pin.
39	P1.1/IRQ4/PWMTRIP/ DTR	General-Purpose Input/Output P1.1/External Interrupt Request 4/PWM External Trip Input/ UART Data Terminal Ready Pin.
40	P1.2/PWM0/RI	General-Purpose Input/Output P1.2/PWM0 Output/UART Ring Indicator Pin.
41	P1.3/PWM1/DSR	General-Purpose Input/Output P1.3/PWM1 Output/UART Data Set Ready Pin.
42	P1.4/PWM2/MISO0/ SDA	General-Purpose Input/Output P1.4/PWM2 Output/SPI0 Master Input, Slave Output Pin/I^2C Serial Data Pin.
43	P1.5/IRQ5/PWM3/ SCLK0	General-Purpose Input/Output P1.5/External Interrupt Request 5/PWM3 Output/SPI0 Serial Clock Pin.
44	P1.6/IRQ6/PWM4/ MOSI0	General-Purpose Input/Output P1.6/External Interrupt Request 6/PWM4 Output/SPI0 Master Output, Slave Input Pin.
45	P1.7/IRQ7/PWM5/CS0	General-Purpose Input/Output P1.7/External Interrupt Request 7/PWM5 Output/SPI0 Chip Select Pin, Active Low (When Using SPI0, Configure as CS0).
46	P2.0/SCL/UARTCLK	General-Purpose Input/Output P2.0/I^2C Serial Clock Pin/Input Clock Pin for UART Block Only.
47	SWCLK	Serial Wire Debug Clock Input Pin.
48	SWDIO	Serial Wire Debug Data Input/Output Pin.
	EP	Exposed Pad. The exposed pad must be soldered to a metal plate on the PCB and to DGND for mechanical reasons.

FIGURE 2. Terminal connections - Continued.

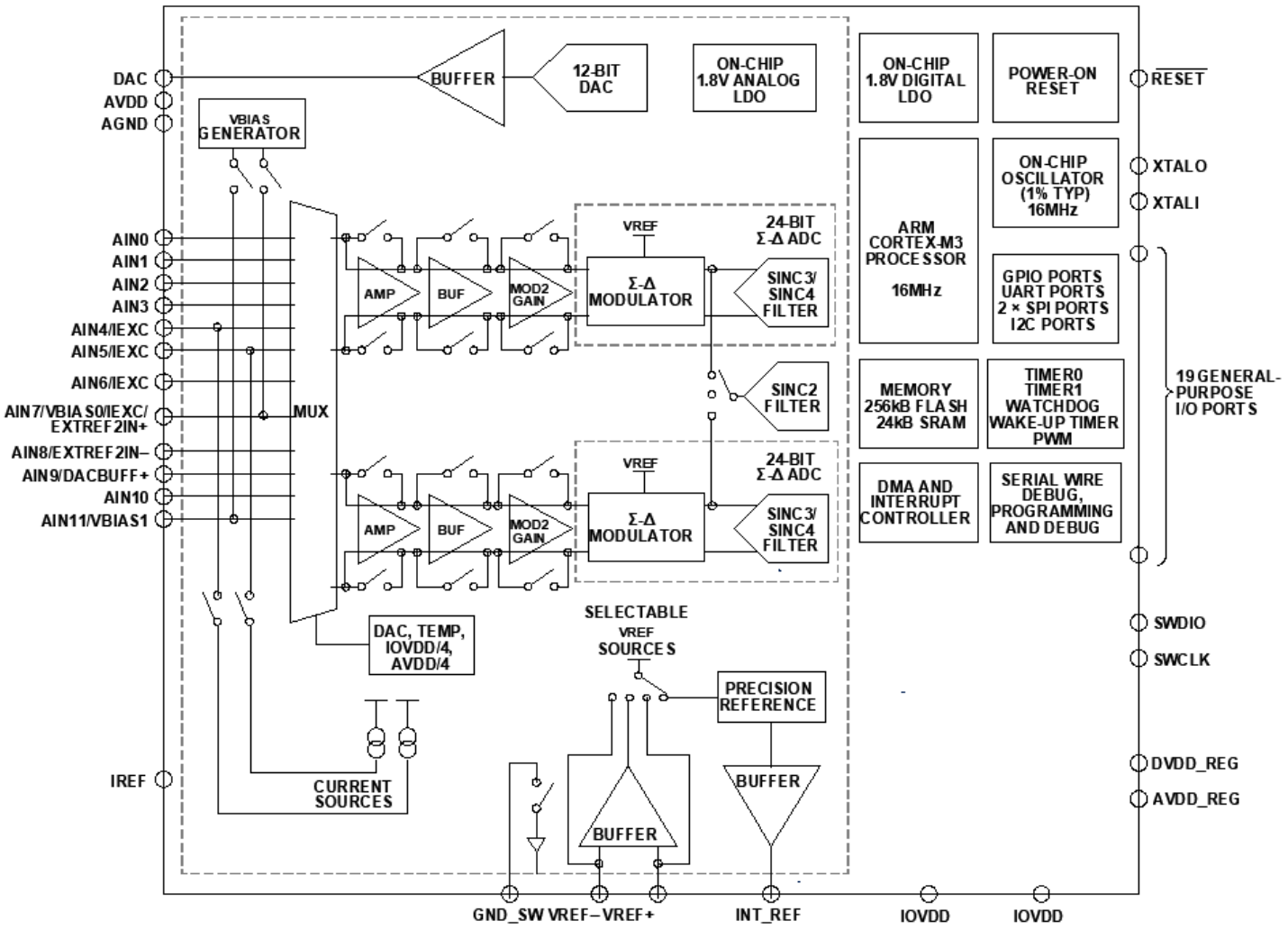

FIGURE 3. Functional block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/21606-01XE	24355	Reel, 750 units	ADUCM362TCPZ56EPR7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123