Data Sheet

ADuM320N/ADuM321N

5.7 kV RMS/3.0 kV RMS Dual Digital Isolators

FEATURES

- High common-mode transient immunity: 180 kV/µs typical
- High robustness to radiated and conducted noise
- Low propagation delay
  - 6.2 ns typical (10 ns maximum) for 5 V operation
- Low dynamic power consumption, <1.65 mA/ch at 1 Mbps
- 2.25 V to 5.5 V level translation
- 150 Mbps maximum guaranteed data rate
- High temperature operation: 125°C
- Safety and regulatory approvals
  - UL recognition per UL1577
    - V_{ISO} = 5700 V rms (SOIC_IC)
    - V_{ISO} = 3000 V rms (SOIC_N)
  - VDE certificate of conformity (pending)
    - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 1173 V_{PEAK} (SOIC_IC)
    - V_{IORM} = 636 V_{PEAK} (SOIC_N)
    - 10,000 V peak reinforced surge isolation voltage (SOIC_IC)
    - 6250 V peak reinforced surge isolation voltage (SOIC_N)
  - CSA component certification per IEC 62368-1, IEC60601-1, and IEC 61010-1 (pending)
  - TÜV SÜD component certification per EN 62368-1 (pending)
  - CQC component certification per GB4943.1-2022 (pending)
- ±8 kV IEC 61000-4-2 ESD protection across isolation barrier
- ±4 kV HBM ESD protection on input/output pins
- Fail-safe high (N1) or low (N0) options
- SOIC_N Backward compatibility with
  - ADuM1200/ADuM1201/ADuM1210/ADuM1211
  - ADuM3200/ADuM3201/ADuM3210/ADuM3211
  - ADuM120N/ADuM121N
- AEC-Q100 qualified for automotive applications
- Operating temperature range: −40°C to +125°C
- Available in 8-lead, narrow-body, RoHS-compliant, standard small outline SOIC_N package and 8-lead, wide-body, RoHS-compliant, standard small outline SOIC_IC package

APPLICATIONS

- Inverters
- Power supplies
- Industrial field bus isolation
- PWM controller signal isolation
- General-purpose multichannel isolation

GENERAL DESCRIPTION

The ADuM320N/ADuM321N[1] are dual-channel digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed, complementary metal-oxide semiconductor (CMOS) and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics and meet CISPR 32/EN 55032 Class B limits at 5 Mbps. The maximum propagation delay is 10 ns with a pulse width distortion of less than 3 ns at 5 V operation. Channel matching is hard at 3.0 ns maximum.

The ADuM320N/ADuM321N data channels are independent and are available in a variety of configurations with a withstand voltage rating of 5.7 kV RMS and 3.0 kV RMS (for more information, see the Ordering Guide section). The devices operate with the supply voltage on either side ranging from 2.25 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

Two different fail-safe options are available, by which the outputs transition to a predetermined state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS

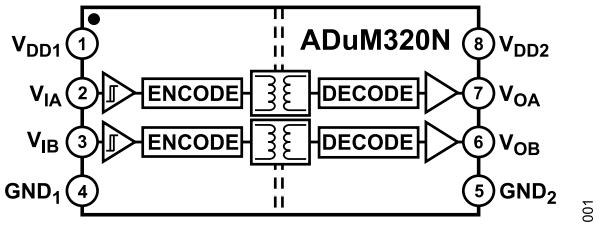

Figure 1. ADuM320N Functional Block Diagram

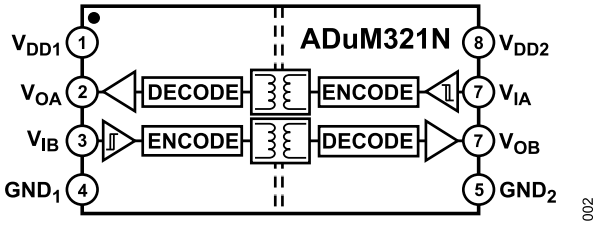

Figure 2. ADuM321N Functional Block Diagram

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

TABLE OF CONTENTS

REVISION HISTORY

2/2024—Rev. B to Rev. C

Changes to Features Section ... 1
Changes to Table 11 and Table 12 ... 10

12/2023—Rev. A to Rev. B

Change to Features Section ... 1
Changes to Propagation Delay Parameter and Note 12, Table 3 ... 5
Change to Note 12, Table 5 ... 7
Changes to Table 11 and Table 12 ... 10
Changes to Table 13 ... 11
Changes to Table 17 ... 14
Changes to Table 18 ... 15
Changes to Ordering Guide ... 22

9/2023—Rev. 0 to Rev. A

Change to Minimum External Air Gap (Clearance) Parameter, Table 7 ... 9
Changes to Ordering Guide ... 22

7/2023—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (5 V OPERATION)

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 1. Electrical Characteristics (5 V Operation)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within pulse width distortion (PWD) limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		6.2	10	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.3	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.1	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.3	3.0	ns	
Opposing Direction	t_{PSKOD}		0.3	3.0	ns	
Jitter[1]						For more information, see the Jitter Measurement section
Random Jitter, RMS (1σ)[2]	$t_{JIT(RJ)}$		4.6		ps	1 MHz clock input, all channels switching
Deterministic Jitter, Peak-to-Peak[3, 4]	$t_{JIT(DJ)}$		96		ps	100 Mbps, 2^{15} − 1 PRBS
Total Jitter, Peak-to-Peak, at Bit Error Rate (BER) 1 x 10^{-12}	$t_{JIT(TJ)}$					100 Mbps, 2^{15} − 1 PRBS input[5]
Without Crosstalk			149		ps	Single channel switching
With Crosstalk			238		ps	All channels switching
DC SPECIFICATIONS						
Input Threshold Voltage						V_{Ix}, V_{Ex}
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{HYS}		0.85		V	V_{IH} − V_{IL}
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[6] = −20 μA, V_{Ix} = V_{IxH}[7]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[6] = −4 mA, V_{Ix} = V_{IxH}[7]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[6] = 20 μA, V_{Ix} = V_{IxL}[8]
			0.2	0.4	V	I_{Ox}[6] = 4 mA, V_{Ix} = V_{IxL}[8]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}, 0 V ≤ V_{Ex} ≤ V_{DDx}
Quiescent Supply Current						
ADuM320N						
	$I_{DD1 (Q)}$		0.41	0.6	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD2 (Q)}$		0.84	1.4	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD1 (Q)}$		3.62	5.3	mA	V_I[9] = 1 (N0), 0 (N1)[10]
	$I_{DD2 (Q)}$		1.65	2.5	mA	V_I[9] = 1 (N0), 0 (N1)[10]
ADuM321N						
	$I_{DD1 (Q)}$		0.63	1.0	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD2 (Q)}$		0.63	1.0	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD1 (Q)}$		2.66	3.8	mA	V_I[9] = 1 (N0), 0 (N1)[10]
	$I_{DD2 (Q)}$		2.68	3.8	mA	V_I[9] = 1 (N0), 0 (N1)[10]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.011		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.029		mA/Mbps	Inputs switching, 50% duty cycle

SPECIFICATIONS

Table 1. Electrical Characteristics (5 V Operation) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		2.0	2.2	V	Rising supply voltage enable threshold
Negative V_{DDx} Threshold	V_{DDxUV-}	1.7	1.8		V	Falling supply voltage lockout threshold
V_{DDx} Hysteresis	V_{DDxUVH}		0.2		V	UVLO hysteresis
UVLO Recovery Time[11]	t_{UVLO}			60	µs	UVLO release delay after V_{UVLO+} threshold
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[12]	$\|CM_H\|$	100	180		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	100	180		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

1 Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter.

2 This specification is measured over a population of ~100,000 edges.

3 Peak-to-peak jitter specifications include jitter due to PWD.

4 This specification is measured over a population of ~300,000 edges.

5 Using the following formula: $t_{JIT(TJ)} = 14 \times t_{JIT(RJ)} + t_{JIT(DJ)}$.

6 I_{Ox} is the channel x output current, where x = A, or B.

7 V_{IxH} is the input side logic high.

8 V_{IxL} is the input side logic low.

9 V_I is the voltage input.

10 N0 is the ADuM320N0/ADuM321N0 models, and N1 is the ADuM320N1/ADuM321N1 models. For more information, see the Ordering Guide section.

11 Guaranteed by design and not subject to production test.

12 $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage-output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
ADuM320N						
1 Mbps						
Supply Current Side 1	I_{DD1}		2.0	2.9	mA	
Supply Current Side 2	I_{DD2}		1.3	1.9	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		2.2	3.2	mA	
Supply Current Side 2	I_{DD2}		2.0	3.0	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		3.1	4.2	mA	
Supply Current Side 2	I_{DD2}		4.2	6.7	mA	C_L = 0 nF
ADuM321N						
1 Mbps						
Supply Current Side 1	I_{DD1}		1.6	2.3	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		1.6	2.3	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		2.1	3.0	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		2.1	3.0	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		3.7	5.5	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		3.7	5.5	mA	C_L = 0 nF

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (3.3 V OPERATION)

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 3. Electrical Characteristics (3.3 V Operation)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate		100			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		6.6	10	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.5	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.5	3.0	ns	
Opposing Direction	t_{PSKOD}		0.5	3.0	ns	
Jitter[1]						For more information, see the Jitter Measurement section
Random Jitter, RMS (1σ)[2]	$t_{JIT(RJ)}$		5		ps	1 MHz clock input, All channels switching
Deterministic Jitter, Peak-to-Peak[3, 4]	$t_{JIT(DJ)}$		93		ps	100 Mbps, 2^{15} − 1 PRBS input
Total Jitter, Peak-to-Peak, at Bit Error Rate (BER) 1 x 10^{-12}	$t_{JIT(TJ)}$					100 Mbps, 2^{15} − 1 PRBS input[5]
Without Crosstalk			149			Single channel switching
With Crosstalk			229			All channels switching
DC SPECIFICATIONS						
Input Threshold Voltage						V_{Ix}, V_{Ex}
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{HYS}		0.7		V	V_{IH} − V_{IL}
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[6] = −20 µA, V_{Ix} = V_{IxH}[7]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[6] = −2 mA, V_{Ix} = V_{IxH}[7]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[6] = 20 µA, V_{Ix} = V_{IxL}[8]
			0.2	0.4	V	I_{Ox}[6] = 2 mA, V_{Ix} = V_{IxL}[8]
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}, 0 V ≤ V_{Ex} ≤ V_{DDx}
Quiescent Supply Current						
ADuM320N						
	$I_{DD1 (Q)}$		0.4	0.6	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD2 (Q)}$		0.8	1.3	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD1 (Q)}$		3.6	5.2	mA	V_I[9] = 1 (N0), 0 (N1)[10]
	$I_{DD2 (Q)}$		1.6	2.3	mA	V_I[9] = 1 (N0), 0 (N1)[10]
ADuM321N						
	$I_{DD1 (Q)}$		0.61	0.9	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD2 (Q)}$		0.61	0.9	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD1 (Q)}$		2.6	3.7	mA	V_I[9] = 1 (N0), 0 (N1)[10]
	$I_{DD2 (Q)}$		2.6	3.7	mA	V_I[9] = 1 (N0), 0 (N1)[10]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.009		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.019		mA/Mbps	Inputs switching, 50% duty cycle

SPECIFICATIONS

Table 3. Electrical Characteristics (3.3 V Operation) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{UVLO+}		2.0	2.2	V	Rising supply voltage enable threshold
Negative V_{DDx} Threshold	V_{UVLO-}	1.7	1.8		V	Falling supply voltage lockout threshold
V_{DDx} Hysteresis	V_{UVLO_HYS}		0.2		V	UVLO hysteresis
UVLO Release Time[11]	t_{UVLO}			60	µs	UVLO release delay after V_{UVLO+} threshold
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[12]	$\|CM_H\|$	100	180		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	100	180		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter.

[2] This specification is measured over a population of ~100,000 edges.

[3] Peak-to-peak jitter specifications include jitter due to PWD.

[4] This specification is measured over a population of ~300,000 edges.

[5] Using the following formula: $t_{JIT(TJ)} = 14 \times t_{JIT(RJ)} + t_{JIT(DJ)}$.

[6] I_{Ox} is the Channel x output current, where x = A or B.

[7] V_{IxH} is the input side logic high.

[8] V_{IxL} is the input side logic low.

[9] V_I is the voltage input.

[10] N0 refers to ADuM320N0/ADuM321N0 models, and N1 refers to ADuM320N1/ADuM321N1 models. For more information, see the Ordering Guide section.

[11] Guaranteed by design and not subject to production test.

[12] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage-output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
ADuM320N						
1 Mbps						
Supply Current Side 1	I_{DD1}		2.0	2.9	mA	
Supply Current Side 2	I_{DD2}		1.3	1.8	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		2.2	3.0	mA	
Supply Current Side 2	I_{DD2}		1.73	2.5	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		2.9	3.8	mA	
Supply Current Side 2	I_{DD2}		3.2	4.9	mA	C_L = 0 nF
ADuM321N						
1 Mbps						
Supply Current Side 1	I_{DD1}		1.62	2.3	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		1.62	2.3	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		2.0	2.7	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		2.0	2.7	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		3.1	4.4	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		3.1	4.4	mA	C_L = 0 nF

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (2.5 V OPERATION)

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operation range of 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 5. Electrical Characteristics (2.5 V Operation)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate		100			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		7.2	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.3	4.5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			8.9	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.4	5.0	ns	
Opposing Direction	t_{PSKOD}		0.4	5.0	ns	
Jitter[1]						For more information, see the Jitter Measurement section
Random Jitter, RMS (1σ)[2]	$t_{JIT(RJ)}$		5.2		ps	1 MHz clock input, All channels switching
Deterministic Jitter, Peak-to-Peak[3, 4]	$t_{JIT(DJ)}$		120		ps	100 Mbps, 2^{15} − 1 PRBS input
Total Jitter, Peak-to-Peak, at Bit Error Rate (BER) 1 x 10^{-12}	$t_{JIT(TJ)}$					100 Mbps, 2^{15} − 1 PRBS input[5]
Without Crosstalk			181		ps	Single channel switching
With Crosstalk			247		ps	All channels switching
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{HYS}		0.65		V	$V_{IH} - V_{IL}$
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[6] = −20 μA, V_{Ix} = V_{IxH}[7]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[6] = −2 mA, V_{Ix} = V_{IxH}[7]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[6] = 20 μA, V_{Ix} = V_{IxL}[8]
			0.2	0.4	V	I_{Ox}[6] = 2 mA, V_{Ix} = V_{IxL}[8]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM320N						
	$I_{DD1 (Q)}$		0.4	0.6	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD2 (Q)}$		0.8	1.3	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD1 (Q)}$		3.6	5.2	mA	V_I[9] = 1 (N0), 0 (N1)[10]
	$I_{DD2 (Q)}$		1.6	2.3	mA	V_I[9] = 1 (N0), 0 (N1)[10]
ADuM321N						
	$I_{DD1 (Q)}$		0.6	0.9	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD2 (Q)}$		0.6	0.9	mA	V_I[9] = 0 (N0), 1 (N1)[10]
	$I_{DD1 (Q)}$		2.6	3.7	mA	V_I[9] = 1 (N0), 0 (N1)[10]
	$I_{DD2 (Q)}$		2.6	3.7	mA	V_I[9] = 1 (N0), 0 (N1)[10]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.008		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.0015		mA/Mbps	Inputs switching, 50% duty cycle

SPECIFICATIONS

Table 5. Electrical Characteristics (2.5 V Operation) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		2.0	2.2	V	
Negative V_{DDx} Threshold	V_{DDxUV-}	1.7	1.8		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.2		V	
UVLO Release Time[11]				60	µs	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[12]	$\|CM_H\|$	100	180		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	100	180		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

1 Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter.

2 This specification is measured over a population of ~100,000 edges.

3 Peak-to-peak jitter specifications include jitter due to PWD.

4 This specification is measured over a population of ~300,000 edges.

5 Using the following formula: $t_{JIT(TJ)} = 14 \times t_{JIT(RJ)} + t_{JIT(DJ)}$.

6 I_{Ox} is the Channel x output current, where x = A or B.

7 V_{IxH} is the input side logic high.

8 V_{IxL} is the input side logic low.

9 V_I is the voltage input.

10 N0 refers to ADuM320N0/ADuM321N0 models, and N1 refers to ADuM320N1/ADuM321N1 models. For more information, see the Ordering Guide section.

11 Guaranteed by design and not subject to production test.

12 $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage-output (V_O) < 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 6. Total Supply Current vs. Data Throughput

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
ADuM320N						
1 Mbps						
Supply Current Side 1	I_{DD1}		2.0	2.9	mA	
Supply Current Side 2	I_{DD2}		1.3	1.8	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		2.2	3.0	mA	
Supply Current Side 2	I_{DD2}		1.6	2.3	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		2.8	3.7	mA	
Supply Current Side 2	I_{DD2}		2.8	4.2	mA	C_L = 0 nF
ADuM321N						
1 Mbps						
Supply Current Side 1	I_{DD1}		1.6	2.3	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		1.6	2.3	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		1.9	2.6	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		1.9	2.6	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		2.8	3.9	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		2.8	3.9	mA	C_L = 0 nF

SPECIFICATIONS

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 7. R-8 Narrow-Body [SOIC_N] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	3.5	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	3.5	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	4.0	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Distance through insulation	DTI	34	µm	Minimum internal clearance
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	Tested in accordance to IEC 60112
Material Group		I		Material Group per IEC 60664-1

Table 8. RI-8-1 Wide-Body, with Increased Creepage [SOIC_IC] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5700	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Distance through insulation	DTI	34	µm	Minimum internal clearance
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	Tested in accordance to IEC 60112
Material Group		I		Material Group per IEC 60664-1

PACKAGE CHARACTERISTICS

Table 9. R-8 Narrow-Body [SOIC_N] Package

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Insulation Resistance[1]	R_{I-O}		10^{13}		Ω	V_{I-O} = 500 VDC
Insulation Capacitance[1]	C_{I-O}		0.5		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		93		°C/W	Simulated per JEDEC JESD-51

[1] The device is considered a 2-terminal device: Pin 1 through Pin 4 and Pin 5 through Pin 8 are shorted together.

[2] Input capacitance is from any input data pin to the respective ground.

Table 10. RI-8-1 Wide-Body, with Increased Creepage [SOIC_IC] Package

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Insulation Resistance[1]	R_{I-O}		10^{13}		Ω	V_{I-O} = 500 VDC
Insulation Capacitance[1]	C_{I-O}		0.5		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		89		°C/W	Simulated per JEDEC JESD-51

[1] The device is considered a 2-terminal device: Pin 1 through Pin 4 and Pin 5 through Pin 8 are shorted together.

[2] Input capacitance is from any input data pin to the respective ground.

SPECIFICATIONS

REGULATORY INFORMATION

For details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels, see Table 17. Certifications available at Safety and Regulatory Certification for Digital Isolators.

Table 11. R-8 Narrow-Body [SOIC_N] Package

Regulatory Agency	Standard Certification/Approval	File
UL[1]	Recognized Under 1577 Component Recognition Program Single Protection, 3000 V rms Isolation Voltage	File E214100
VDE[2] (Pending)	Certified according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01 Reinforced insulation, V_{IORM} = 636 V_{PEAK}, V_{IOSM} = 6250 V_{PEAK} Certified according to DIN EN IEC 60747-17 Reinforced insulation, V_{IORM} = 636 V_{PEAK}, V_{IOSM} = 6250 V_{PEAK}	Pending Pending
CSA (Pending)	Approved under CSA Component Acceptance CSA 62368-1-19, EN 62368-1:2020 and IEC 62368-1:2018 third edition Basic insulation at 350 V rms Reinforced insulation at 175 V rms IEC 60601-1:2005 Ed 3.0+A1+A2 Basic insulation (1 means of patient protection (1 MOPP)), 187.5 V rms CSA 61010-1-12 and IEC 61010-1 third edition: Basic insulation at 300 V rms mains Reinforced insulation at 150 V rms Mains	Pending
TÜV Süd (Pending)	Component Certification EN 62368-1: 2020+A11:2020	Pending
CQC (Pending)	Certified by CQC11-471543-2012, GB4943.1-2022 Basic insulation at 350 V rms (495 V_{PEAK})	Pending

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.

[2] In accordance with DIN V VDE V 0884-11, each product is proof tested by applying an insulation test voltage ≥ 1194 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC).

Table 12. RI-8-1 Wide-Body, with Increased Creepage [SOIC_IC] Package

Regulatory Agency	Standard Certification/Approval	File
UL[1]	Recognized Under 1577 Component Recognition Program Single Protection, 5700 V rms Isolation Voltage	File E214100
VDE[2] (Pending)	Certified according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01 Reinforced insulation, V_{IORM} = 1173 V_{PEAK}, V_{IOSM} = 10000 V_{PEAK} Certified according to DIN EN IEC 60747-17 Reinforced insulation, V_{IORM} = 1173 V_{PEAK}, V_{IOSM} = 10000 V_{PEAK}	
CSA (Pending)	Approved under CSA Component Acceptance CSA 62368-1-19, EN 62368-1:2020 and IEC 62368-1:2018 third edition Basic insulation at 830 V rms Reinforced insulation at 415 V rms IEC 60601-1:2005 Ed 3.0+A1+A2: Basic insulation (1 means of patient protection (1 MOPP)), 500 V rms Reinforced insulation (2 MOPP), 250 V rms CSA 61010-1-12 and IEC 61010-1 third edition: Basic insulation at 600 V rms mains Reinforced insulation at 300 V rms Mains	Pending
TÜV Süd (Pending)	Component Certification EN 62368-1: 2020+A11:2020	Pending

SPECIFICATIONS

Table 12. RI-8-1 Wide-Body, with Increased Creepage [SOIC_IC] Package (Continued)

Regulatory Agency	Standard Certification/Approval	File
CQC (Pending)	Certified by CQC11-471543-2012, GB4943.1-2022 Basic insulation at 830 V rms (1174 V_{PEAK}) Reinforced insulation at 415 V rms (587 V_{PEAK}), tropical climate, altitude ≤5000 meters	Pending

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec.

[2] In accordance with DIN V VDE V 0884-11, each product is proof tested by applying an insulation test voltage ≥ 2199 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC).

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS (PENDING)

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The asterisk (*) marking on packages denotes DIN V VDE V 0884-11 approval (pending).

Table 13. ADuM320N/ADuM321N R-8 Narrow-Body [SOIC_N] Package

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 450 V rms			I to II	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	636	V_{PEAK}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	1194	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{pd\ (m)}$		
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		955	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		764	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	4242	V_{PEAK}
Surge Isolation Voltage Reinforced	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6250	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.34	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

SPECIFICATIONS

Table 14. ADuM320N/ADuM321N RI-8-1 Wide-Body, with Increased Creepage [SOIC_IC] Package

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	1173	V_{PEAK}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	2199	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{pd\ (m)}$		
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1759	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1407	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	8061	V_{PEAK}
Surge Isolation Voltage Reinforced	V_{PEAK} = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	10000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.40	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

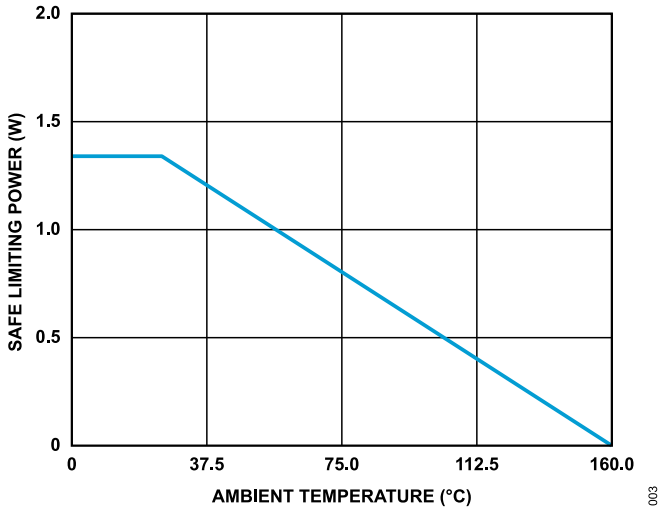

Figure 3. ADuM320N/ADuM321N R-8 SOIC Narrow [SOIC_N] Package Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature Per DIN V VDE V 0884-11

SPECIFICATIONS

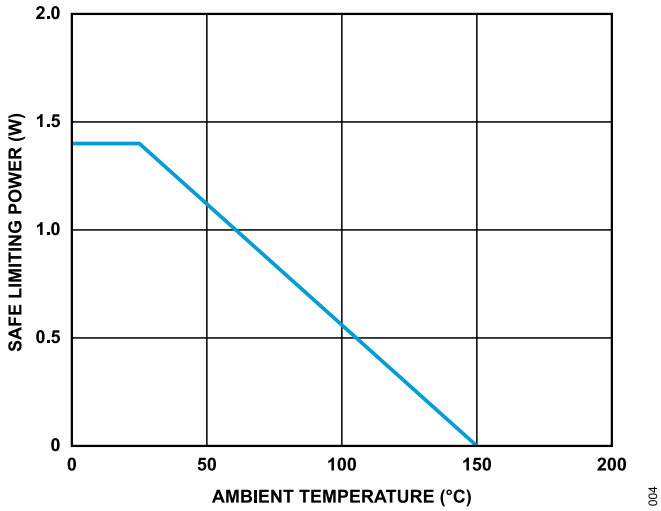

Figure 4. ADuM320N/ADuM321N RI-8-1 Wide-Body, with Increased Creepage [SOIC_IC] Package Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature Per DIN V VDE V 0884-11

RECOMMENDED OPERATING CONDITIONS

Table 15. Recommended Operating Conditions

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +125°C
Supply Voltages		
V_{DD1}		2.25 V to 5.5 V
V_{DD2}		2.25 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 16. Absolute Maximum Ratings

Parameter	Rating
Supply Voltages	
V_{DD1} to GND_1	−0.5 V to +7.0 V
V_{DD2} to GND_2	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})	−0.5 V to V_{DDI}[1] + 0.5 V
Output Voltages (V_{OA}, V_{OB})	−0.5 V to V_{DDO}[2] + 0.5 V
Average Output Current per Pin[3]	
Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4]	−300 kV/µs to +300 kV/µs
Temperature	
Storage Range (T_{ST})	−65°C to +150°C
Ambient Operating Range (T_A)	−40°C to +125°C
Moisture Sensitivity Level	MSL3

[1] V_{DDI} is the input side supply voltage.

[2] V_{DDO} is the output side supply voltage.

[3] For the maximum rated current values for various ambient temperatures, see Figure 3 and Figure 4.

[4] Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latchup or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 17. Maximum Continuous Working Voltage[1] R-8 Narrow-Body [SOIC_N] Package

Parameter	Rating	Constraint
AC VOLTAGE		
Bipolar Waveform		
Basic Insulation	450 V rms	Rating limited by V_{IOWM}[2] (reinforced) per IEC60747-17
Reinforced Insulation	347 V rms	Rating limited by package creepage per IEC 60664-1:2020 in pollution degree 2 environment
DC VOLTAGE		
Basic Insulation	636 VDC	Rating limited by V_{IORM}[3] (reinforced) per IEC60747-17
Reinforced Insulation	347 VDC	Rating limited by package creepage per IEC 60664-1:2020 in pollution degree 2 environment

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier in pollution degree 2 environment. For more information, see the Insulation Lifetime section.

[2] V_{IOWM} is the RMS or equivalent DC voltage characterizing the specified long-term withstand capability of its isolation.

[3] V_{IORM} is the maximum repetitive peak isolation voltage.

ABSOLUTE MAXIMUM RATINGS

Table 18. Maximum Continuous Working Voltage[1] RI-8-1 Wide-Body [SOIC_IC] Package

Parameter	Rating	Constraint
AC VOLTAGE		
Bipolar Waveform		
Basic Insulation	1000 V rms	Basic insulation rating per IEC60747-17. Accumulative failure rate over lifetime (FROL) ≤ 1000 ppm at 20 years.
Reinforced Insulation	830 V rms	Rating limited by package creepage per IEC 60664-1:2020 in pollution degree 2 environment
DC VOLTAGE		
Basic Insulation	1414 VDC	Basic insulation rating per IEC60747-17. Accumulative failure rate over lifetime (FROL) ≤ 1000 ppm at 20 years
Reinforced Insulation	830 VDC	Rating limited by package creepage per IEC 60664-1:2020 in pollution degree 2 environment

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier in pollution degree 2 environment. For more information, see the Insulation Lifetime section.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD Ratings for ADuM320N/ADuM321N

Table 19. ADuM320N/ADuM321N, 8-Lead SOIC_N and SOIC_IC

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±5500 (ADuM320N) ±4500 (ADuM321N)	3A
CDM[1]	±1500	C3
IEC[2]	±8kV (across isolation barrier with respect to GNDx)	Level 4

[1] With respect to local VDDx and GNDx pins.

[2] Across the isolation barrier between GND_1 and GND_2.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

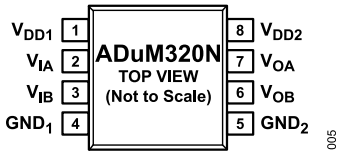

Figure 5. ADuM320N Pin Configuration

Table 20. ADuM320N Pin Function Descriptions

Pin Number	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1. This pin requires a 0.1 µF bypass capacitor.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground Reference for Isolator Side 1.
5	GND_2	Ground Reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2. This pin requires a 0.1 µF bypass capacitor.

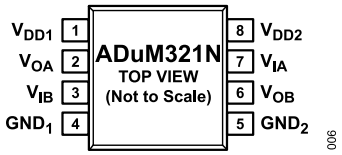

Figure 6. ADuM321N Pin Configuration

Table 21. ADuM321N Pin Function Descriptions

Pin Number	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1. This pin requires a 0.1 µF bypass capacitor.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground Reference for Isolator Side 1.
5	GND_2	Ground Reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2. This pin requires a 0.1 µF bypass capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

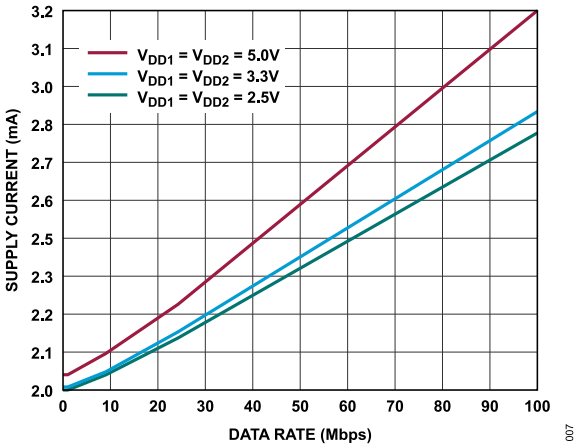

Figure 7. I_{DD1} Supply Current vs. Data Rate at Various Voltages

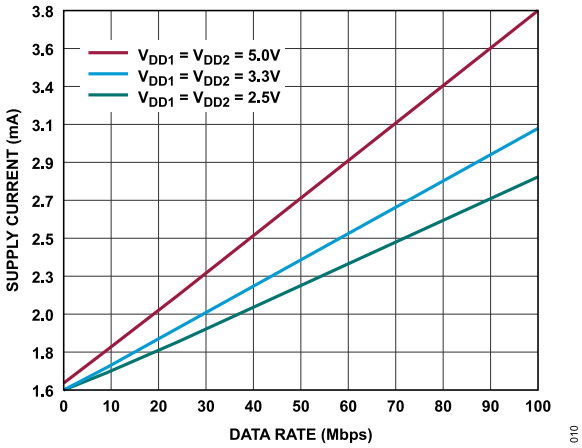

Figure 10. I_{DD2} Supply Current vs. Data Rate at Various Voltages

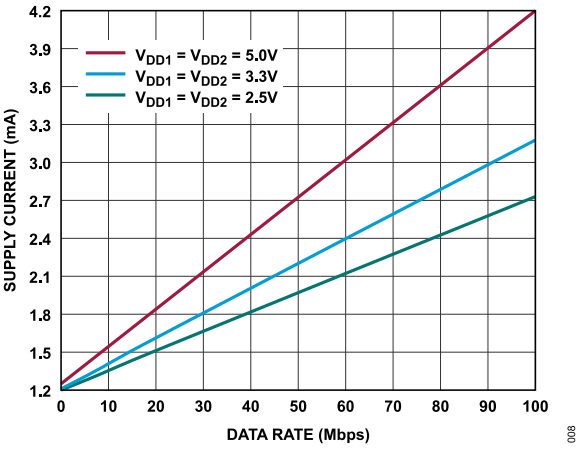

Figure 8. I_{DD2} Supply Current vs. Data Rate at Various Voltages

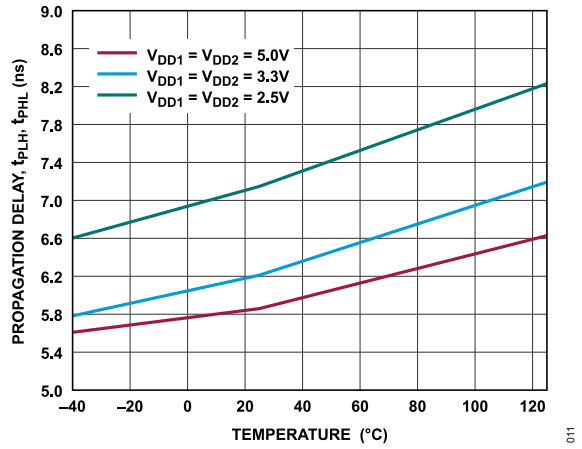

Figure 11. Propagation Delay, t_{PLH}, t_{PHL} vs. Temperature at Various Voltages

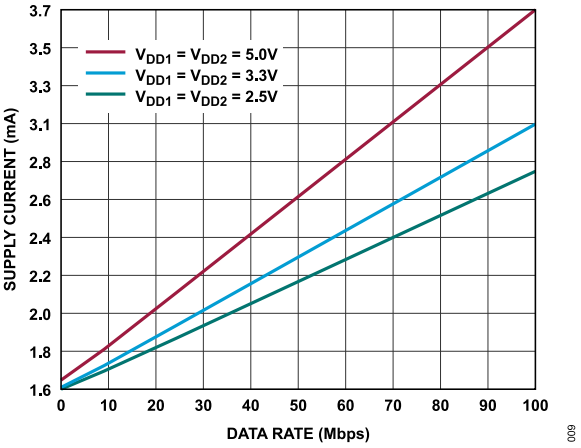

Figure 9. I_{DD1} Supply Current vs. Data Rate at Various Voltages

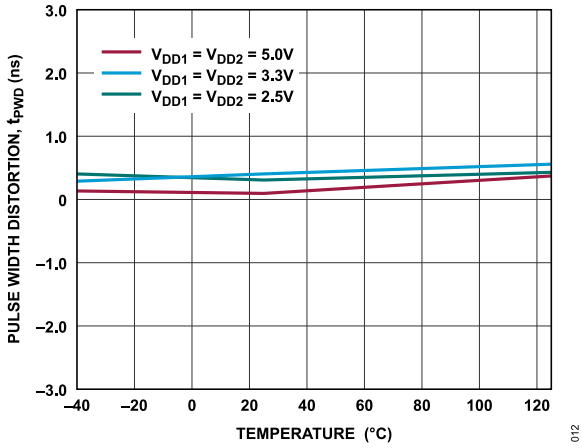

Figure 12. Pulse Width Distortion, t_{PWD} vs. Temperature at Various Voltages

THEORY OF OPERATION

The ADuM320N/ADuM321N use a high-frequency carrier to transmit data across the isolation barrier using *i*Coupler chip-scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture shown in Figure 13 and Figure 14, the ADuM320N/ADuM321N have very low propagation delay and high speed.

There is no interdependency between V_{DD1} and V_{DD2} supplies. They can simultaneously operate at any voltage within their specified operating ranges and may sequence in any order. This enables the isolator to perform voltage translation of 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient (CMTI) immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 13 shows the waveforms for models of the ADuM320N/ADuM321N that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the low fail-safe output state (ADuM320N0/ADuM321N0) sets the output to low. For the ADuM320N/ADuM321N that have a high fail-safe output state, Figure 14 shows the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the high fail-safe output state (ADuM320N1/ADuM321N1) sets the output to high. For the model numbers that have the fail-safe output state of low or the fail-safe output state of high, see the Ordering Guide section.

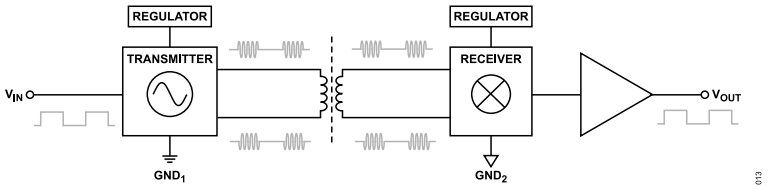

Figure 13. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State

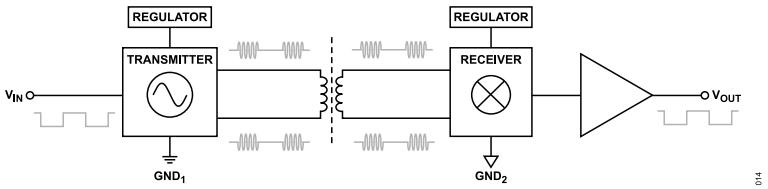

Figure 14. Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

THEORY OF OPERATION

TRUTH TABLE

Table 22. ADuM320N/ADuM321N Truth Table (Positive Logic)

V_{Ix} Input[1, 2]	V_{DDI} State[3]	V_{DDO} State[4]	Default Low (N0), V_{Ox} Output[1, 5, 6]	Default High (N1), V_{Ox} Output[1, 5, 7]	Test Conditions/ Comments
L	Powered	Powered	L	L	Normal operation
H	Powered	Powered	H	H	Normal operation
L	Undervoltage	Powered	L	H	Fail-safe output
X[8]	Undervoltage	Powered	Z	Z	Outputs disabled
X	Powered	Undervoltage	Indeterminate	Indeterminate	

[1] L means low, H means high, X means don't care, NC means not connected, and Z means high impedance within one diode drop of GNDx.

[2] V_{Ix} refers to the input signals of a given channel (A or B).

[3] V_{DDI} refers to the supply voltages on the input sides of the given channel.

[4] V_{DDO} refers to the supply voltages on the output sides of the given channel.

[5] V_{Ox} refers to the output signals of a given channel (A or B).

[6] N0 refers to the ADuM320N0/ADuM321N0 models. For more information, see the Ordering Guide section.

[7] N1 refers to the ADuM320N1/ADuM321N1 models. For more information, see the Ordering Guide section.

[8] Input pins (V_{Ix} and V_{Ex}) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

INPUT/OUTPUT SCHEMATICS

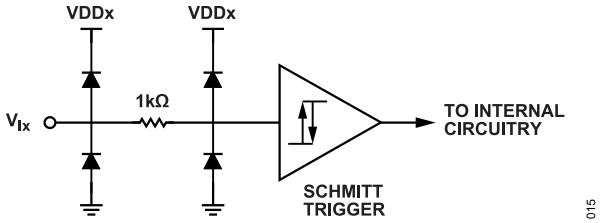

Figure 15. V_{IA} and V_{IB} Input Schematics

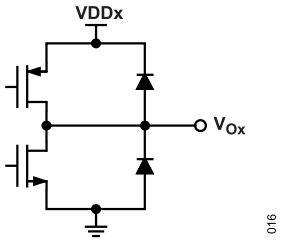

Figure 16. V_{OA} and V_{OB} Output Schematics

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM320N/ADuM321N digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 17). Bypass capacitors are to be connected between Pin 1 and Pin 4 for V_{DD1} and between Pin 8 and Pin 5 for V_{DD2}. The required bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm.

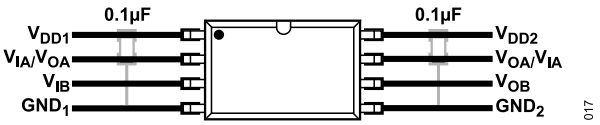

Figure 17. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, so leading to latchup or permanent damage.

For board layout guidelines, refer to the AN-1109 Application Note, *Recommendations for Control of Radiated Emissions with iCoupler Devices*.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time required for a logic signal to propagate through a component. The propagation delay to a Logic 0 output can differ from the propagation delay to a Logic 1 output.

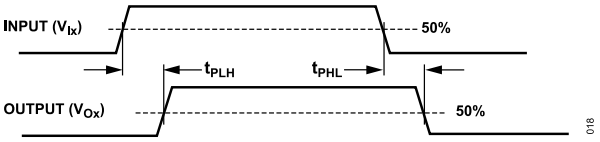

Figure 18. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount that the propagation delay differs between channels within a single ADuM320N/ADuM321N component.

Propagation delay skew is the maximum amount that the propagation delay differs between multiple ADuM320N/ADuM321N components operating under the same conditions.

JITTER MEASUREMENT

Figure 19 shows the resulting eye diagram for the ADuM321N. The measurement is taken using a Keysight 81160A pulse pattern generator at 100 Mbps with pseudorandom bit sequences (PRBS15) 2^{15}-1 input. Jitter is measured using the Tektronix 6 Series B mixed-signal oscilloscope, with a TAP1500 probe and using the Tektronix jitter and analysis software. The 10% to 90% rise and fall times of the input signal from the generator approximately equals 1.2 ns. The result shows a typical output eye diagram measured on the ADuM321N. Figure 19 shows random and deterministic jitter characteristics for a PRBS input.

Total Jitter is evaluated at a BER of $1x10^{-12}$ and calculated for a PRBS input with and without the effects of crosstalk. The total jitter measurement without crosstalk consists of examining one channels input, while the adjacent channels inputs are grounded. The jitter measurement with crosstalk consists of all channels switching simultaneously at the same rate.

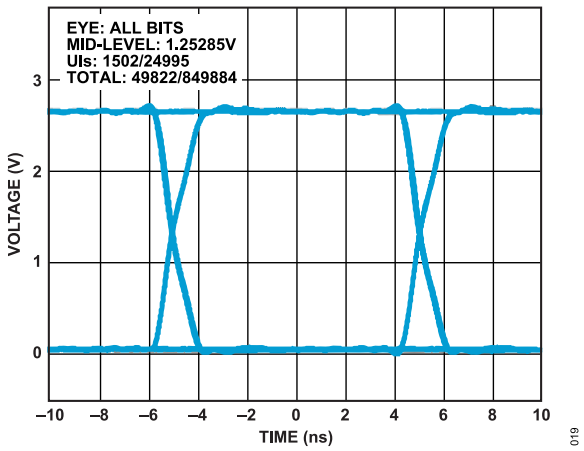

Figure 19. ADuM321N Eye Diagram

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking, and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

APPLICATIONS INFORMATION

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total RMS voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM320N/ADuM321N isolators are shown in Table 7.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out cannot be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as DC stress, which causes very little wear out because there is no displacement current, and an AC component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz AC and DC across the barrier as shown in Equation 1. Because only the AC portion of the stress causes wear out, the equation can be rearranged to solve for the AC RMS voltage, as is shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the AC RMS voltage determines the product lifetime.

$$V_{RMS} = \sqrt{{V_{AC\ RMS}}^2 + {V_{DC}}^2} \quad (1)$$

Or

$$V_{AC\ RMS} = \sqrt{{V_{RMS}}^2 - {V_{DC}}^2} \quad (2)$$

Where:
V_{RMS} is the total RMS working voltage.
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{DC} is the DC offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power-conversion applications. Assume that the line voltage on one side of the isolation is 240 V AC RMS and a 400 V DC bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 20 and the following equations.

The working voltage across the barrier from Equation 1 is:

$$V_{RMS} = \sqrt{{V_{AC\ RMS}}^2 + {V_{DC}}^2}$$
$$V_{RMS} = \sqrt{240^2 + 400^2} \quad (3)$$
$$V_{RMS} = 466\ V$$

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the AC RMS voltage, use Equation 2.

$$V_{AC\ RMS} = \sqrt{{V_{RMS}}^2 - {V_{DC}}^2}$$
$$V_{AC\ RMS} = \sqrt{466^2 - 400^2} \quad (4)$$
$$V_{AC\ RMS} = 240\ V\ rms$$

In this case, the AC RMS voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 17 for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the DC working voltage limit in Table 17 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

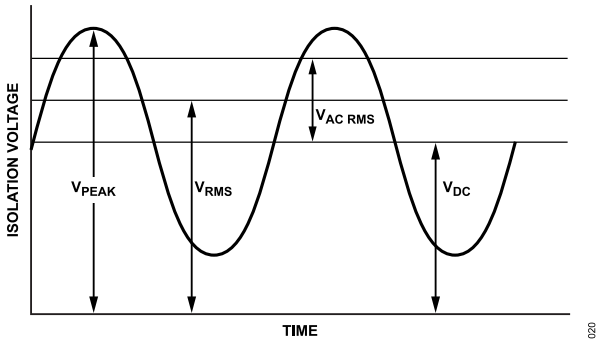

Figure 20. Critical Voltage Example

OUTLINE DIMENSIONS

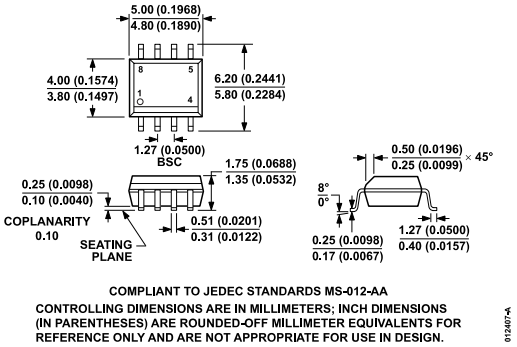

Figure 21. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow-Body
(R-8)
Dimensions Shown in millimeters and (inches)

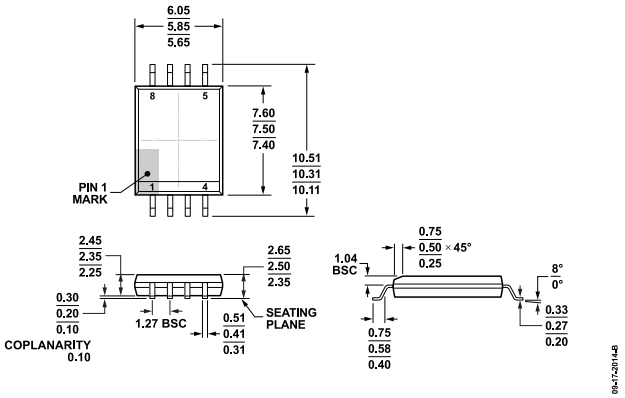

Figure 22. 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide-Body
(RI-8-1)
Dimensions Shown in millimeters

Updated: November 22, 2023

ORDERING GUIDE

Table 23. Ordering Guide

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADUM320N0BRIZ	-40°C to +125°C	8-Lead SOIC (Increased Creepage)		RI-8-1
ADUM320N0BRIZ-RL	-40°C to +125°C	8-Lead SOIC (Increased Creepage)	Reel, 1500	RI-8-1
ADUM320N0BRZ	-40°C to +125°C	8-Lead SOIC		R-8
ADUM320N0BRZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8
ADUM320N0WBRIZ	-40°C to +125°C	8-Lead SOIC (Increased Creepage)		RI-8-1
ADUM320N0WBRIZ-RL	-40°C to +125°C	8-Lead SOIC (Increased Creepage)	Reel, 1500	RI-8-1
ADUM320N0WBRZ	-40°C to +125°C	8-Lead SOIC		R-8
ADUM320N0WBRZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8
ADUM320N1BRIZ	-40°C to +125°C	8-Lead SOIC (Increased Creepage)		RI-8-1
ADUM320N1BRIZ-RL	-40°C to +125°C	8-Lead SOIC (Increased Creepage)	Reel, 1500	RI-8-1
ADUM320N1BRZ	-40°C to +125°C	8-Lead SOIC		R-8
ADUM320N1BRZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8
ADUM320N1WBRIZ	-40°C to +125°C	8-Lead SOIC (Increased Creepage)		RI-8-1
ADUM320N1WBRIZ-RL	-40°C to +125°C	8-Lead SOIC (Increased Creepage)	Reel, 1500	RI-8-1

OUTLINE DIMENSIONS

Table 23. Ordering Guide (Continued)

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADUM320N1WBRZ	-40°C to +125°C	8-Lead SOIC		R-8
ADUM320N1WBRZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8
ADUM321N0BRIZ	-40°C to +125°C	8-Lead SOIC (Increased Creepage)		RI-8-1
ADUM321N0BRIZ-RL	-40°C to +125°C	8-Lead SOIC (Increased Creepage)	Reel, 1500	RI-8-1
ADUM321N0BRZ	-40°C to +125°C	8-Lead SOIC		R-8
ADUM321N0BRZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8
ADUM321N0WBRIZ	-40°C to +125°C	8-Lead SOIC (Increased Creepage)		RI-8-1
ADUM321N0WBRIZ-RL	-40°C to +125°C	8-Lead SOIC (Increased Creepage)	Reel, 1500	RI-8-1
ADUM321N0WBRZ	-40°C to +125°C	8-Lead SOIC		R-8
ADUM321N0WBRZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8
ADUM321N1BRIZ	-40°C to +125°C	8-Lead SOIC (Increased Creepage)		RI-8-1
ADUM321N1BRIZ-RL	-40°C to +125°C	8-Lead SOIC (Increased Creepage)	Reel, 1500	RI-8-1
ADUM321N1BRZ	-40°C to +125°C	8-Lead SOIC		R-8
ADUM321N1BRZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8
ADUM321N1WBRIZ	-40°C to +125°C	8-Lead SOIC (Increased Creepage)		RI-8-1
ADUM321N1WBRIZ-RL	-40°C to +125°C	8-Lead SOIC (Increased Creepage)	Reel, 1500	RI-8-1
ADUM321N1WBRZ	-40°C to +125°C	8-Lead SOIC		R-8
ADUM321N1WBRZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8

[1] Z = RoHS Compliant Part.

[2] W = Qualified for Automotive Applications.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADuM32XNEBZ	Evaluation Board

[1] Z = RoHS Compliant Part.

AUTOMOTIVE PRODUCTS

The ADuM320NW/ADuM321NW models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial model, therefore, designers must review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact the local Analog Devices, Inc., account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.