Data Sheet

LTC2668

16-Channel 16-/12-Bit ±10 V V_{OUT} SoftSpan DACs with 10 ppm/°C Max Reference

FEATURES

- Precision Reference 10 ppm/°C Max
- Independently Programmable Output Ranges: 0 V to 5 V, 0 V to 10 V, ±2.5 V, ±5 V, ±10 V
- Full 16-Bit/12-Bit Resolution at All Ranges
- Maximum INL Error: ±5 LSB at 16 Bits
- A/B Toggle via Software or Dedicated Pin
- 16:1 Analog Multiplexer
- Guaranteed Monotonic Over Temperature
- Internal or External Reference
- Outputs Drive ±10 mA Guaranteed
- 1.8 V to 5 V SPI Serial interface
- 6mm × 6mm 40-Lead QFN Package

APPLICATIONS

- Optical Networking
- Instrumentation
- Data Acquisition
- Automatic Test Equipment
- Process Control and Industrial Automation

GENERAL DESCRIPTION

The LTC2668 is a family of 16-channel, 16-/12-bit ±10 V digital-to-analog converters with integrated precision references. They are guaranteed monotonic and have built-in rail-to-rail output buffers. These SoftSpan™ DACs offer five output ranges up to ±10 V. The range of each channel is independently programmable, or the part can be hardware-configured for operation in a fixed range.

The integrated 2.5 V reference is buffered separately to each channel; an external reference can be used for additional range options. The LTC2668 also includes A/B toggle capability via a dedicated pin or software toggle command.

The serial port interface (SPI)/MICROWIRE™-compatible 3-wire serial interface operates on logic levels as low as 1.71 V at clock rates up to 50 MHz.

FUNCTIONAL BLOCK DIAGRAM

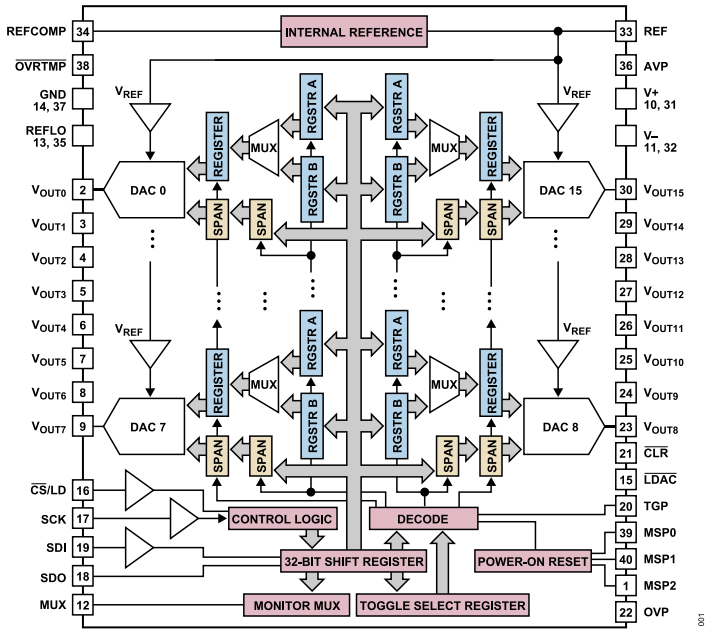

Figure 1.

Rev. B

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8/2023—Rev. A to Rev. B

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

The specifications apply over the full operating temperature range, unless otherwise specified. T_A = 25°C for the typical values. AVP = 5 V, OVP = 5 V, V^+ = 15 V, V^- = –15 V, V_{REF} = 2.5 V, V_{OUT} unloaded, unless otherwise specified.

Table 1.

			LTC2668-12			LTC2668-16			
Parameter	**Symbol**	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DC PERFORMANCE									
Resolution			12			16			Bits
Monotonicity		All ranges[1]	12			16			Bits
Differential Nonlinearity	DNL	All ranges[1]		±0.05	±0.5		±0.2	±1	LSB
Integral Nonlinearity	INL	V^+/V^- = ±15 V		±0.2	±1		±2.2	±5	LSB
All Ranges[1]		V^- = GND[1]							
C Grade, I Grade				±0.2	±1		±2.2	±5	LSB
H Grade				±0.2	±1		±2.2	±6	LSB
Unipolar Offset Error	V_{OS}	0 V to 5 V range		±1	±2		±1	±2	mV
		0 V to 10 V range		±2	±4		±2	±4	mV
V_{OS} Temperature Coefficient		All unipolar ranges, T_A = 25°C		1			1		ppm/°C
Single-Supply Zero-Scale Error	ZSE	All unipolar ranges, V^- = GND		2	4		2	4	mV
Bipolar Zero Error	BZE	All bipolar ranges		±0.02	±0.08		±0.02	±0.08	%FSR
BZE Temperature Coefficient		All bipolar ranges, T_A = 25°C		1			1		ppm/°C
Gain Error	GE	All ranges, external reference		±0.02	±0.08		±0.02	±0.08	%FSR
Gain Temperature Coefficient		T_A = 25°C		2			2		ppm/°C
Power Supply Rejection	PSR	AVP = 5 V, ±10%, T_A = 25°C		0.1			1		LSB/V
All Ranges		V^+/V^- = ±15 V, ±5%, T_A = 25°C		0.001			0.01		LSB/V

[1] For V^- = GND, linearity is defined from Code k_L to Code 2^N – 1, where N is the resolution and k_L is the lower end code for which no output limiting occurs. For V_{REF} = 2.5 V and N = 16, k_L = 128 and linearity is defined from Code 128 to Code 65,535. For V_{REF} = 2.5 V and N = 12, k_L = 8 and linearity is defined from Code 8 to Code 4095.

Table 2.

Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
OUTPUT VOLTAGE SWING	V_{OUT}	To V^- (unloaded, V^- = GND), T_A = 25°C		V^- + 0.004		V
		To V^+ (unloaded, V^+ = 5 V) , T_A = 25°C		V^+ – 0.004		V
		To V^- (–10 mA ≤ I_{OUT} ≤ 10 mA)			V^- + 1.4	V
		To V^+ (–10 mA ≤ I_{OUT} ≤ 10 mA)	V^+ – 1.4			V
LOAD REGULATION		–10 mA ≤ I_{OUT} ≤ 10 mA[1]		78	150	µV/mA
DC OUTPUT IMPEDANCE	R_{OUT}	–10 mA ≤ I_{OUT} ≤ 10 mA[1]		0.078	0.15	Ω
DC CROSSTALK[2]		Due to full-scale output change, T_A = 25°C		±1		µV
0 V to 5 V Range		Due to load current change, T_A = 25°C		±2		µV/mA
		Due to powering down (per channel), T_A = 25°C		±4		µV
V^+/V^- SHORT-CIRCUIT OUTPUT CURRENT[3]	I_{SC}	AVP = 5.5 V, V^+/V^- = ±15.75 V, V_{REF} = 2.5 V, ±10 V output range				
		Code: zero scale; forcing output to GND	16		42	mA
		Code: full scale; forcing output to GND	–40		–4.5	mA
REFERENCE						
Reference Output Voltage			2.495	2.5	2.505	V
Reference Temperature Coefficient[4]		T_A = 25°C		±2	±10	ppm/°C
Reference Line Regulation		AVP ± 10%, T_A = 25°C		50		µV/V
Reference Short-Circuit Current		AVP = 5.5 V, forcing output to GND			5	mA
REFCOMP Pin Short-Circuit Current		AVP = 5.5 V, forcing output to GND			200	µA

SPECIFICATIONS

Table 2. (Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Load Regulation		AVP = 5 V ± 10%, I_{OUT} = 100 µA sourcing, T_A = 25°C		140		mV/mA
Reference Output Voltage Noise Density		$C_{REFCOMP}$ = C_{REF} = 0.1 µF, at f = 10 kHz, T_A = 25°C		32		nV/√Hz
Reference Input Range		External reference mode[5]	0.5		AVP – 1.75	V
Reference Input Current		External reference		0.001	1	µA
Reference Input Capacitance[6]				40		pF
POWER SUPPLY						
Analog Supply Voltage	AVP		4.5		5.5	V
Analog Positive Supply	V^+		4.5		15.75	V
Analog Negative Supply	$V^–$	$V^–$ not tied to GND	–15.75		–4.5	V
		$V^–$ tied to GND, T_A = 25°C		0		V
Digital I/O Supply Voltage	OVP		1.71		AVP + 0.3	V
Supply Current AVP	I_{AVP}	AVP = 5 V, unipolar ranges[7]		5.4	6.5	mA
		AVP = 5 V, bipolar ranges[7]		9.4	12	mA
Supply Current $V^+/V^–$	I_S	Unipolar ranges (code = 0)		4.6	6.5	mA
		Bipolar ranges[8]		8	9.5	mA
Supply Current OVP[9]	I_{OVP}	OVP = 5 V		0.02	1	µA
AVP Shutdown Supply Current		OVP = AVP = 5 V, $V^+/V^–$ = ±15 V		1	3	µA
V^+ Shutdown Supply Current		OVP = AVP = 5 V, $V^+/V^–$ = ±15 V		35	70	µA
$V^–$ Shutdown Supply Current		OVP = AVP = 5 V, $V^+/V^–$ = ±15 V	–60	–27		µA
MONITOR MUX						
Monitor Mux DC Output Impedance		T_A = 25°C		2.2		kΩ
Monitor Mux Leakage Current		Monitor mux disabled (high impedance)		0.02	1	µA
Monitor Mux Output Voltage Range		Monitor mux selected to DAC channel	$V^–$		V^+ – 1.4	V
Monitor Mux Continuous Current[6]					±1	mA
AC PERFORMANCE						
Settlig Time[6, 10]						
0 V to 5 V or ±2.5 V Span, ±5 V Step		±0.024% (±1 LSB at 12 bits), T_A = 25°C		4.5		µs
		±0.0015% (±1 LSB at 16 bits), T_A = 25°C		9		µs
0 V to 10 V or ±5 V Span, ±10 V Step		±0.024% (±1 LSB at 12 bits), T_A = 25°C		8		µs
		±0.0015% (±1 LSB at 16 bits), T_A = 25°C		9		µs
±10 V Span, ±20 V Step	t_{SET}	±0.024% (±1 LSB at 12 bits), T_A = 25°C		15.5		µs
		±0.0015% (±1 LSB at 16 bits), T_A = 25°C		20.5		µs
Voltage Output Slew Rate	SR	T_A = 25°C		5		V/µs
Capacitive Load Driving		T_A = 25°C		1000		pF
Glitch Impulse[11]		At midscale transition, 0 V to 5 V range, T_A = 25°C		8		nV × sec
DAC-to-DAC Crosstalk[12]		Due to full-scale output change, T_A = 25°C		6		nV × sec
Output Voltage Noise	e_n	Density at f = 1 kHz, T_A = 25°C		90		nV/√Hz
0 V to 5 V Output Span, Internal Reference		Density at f = 10 kHz, T_A = 25°C		80		nV/√Hz
		0.1 Hz to 10 Hz, internal reference, T_A = 25°C		1.7		μV_{RMS}
		0.1 Hz to 200 kHz, internal reference, T_A = 25°C		55		μV_{RMS}
DIGITAL I/O						
Digital Output High Voltage	V_{OH}	SDO pin, load current = –100 µA	OVP – 0.2			V
Digital Output Low Voltage	V_{OL}	SDO pin, load current = 100 µA			0.2	V
		$\overline{OVRTMP}$ pin, load current = 100 µA			0.2	V
Digital High-Z Output Leakage	I_{OZ}	SDO pin leakage current ($\overline{CS}$/LD high)			±1	µA
		$\overline{OVRTMP}$ pin leakage current (not asserted)			1	µA
Digital Input Leakage	I_{LK}	V_{IN} = GND to OVP			±1	µA
Digital Input Capacitance[6]	C_{IN}				8	pF

SPECIFICATIONS

Table 2. (Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital Input High Voltage	V_{IH}	OVP = 2.7 V to AVP	0.8 × OVP			V
Digital Input Low Voltage	V_{IL}	OVP = 2.7 V to AVP			0.5	V
Digital Input High Voltage	V_{IH}	OVP = 1.71 V to 2.7 V	0.8 × OVP			V
Digital Input Low Voltage	V_{IL}	OVP = 1.71 V to 2.7 V			0.3	V

[1] 4.5 V ≤ V^+ ≤ 16.5 V; −16.5 V ≤ V^- ≤ –4.5 V or V^- = GND. V_{OUT} is at least 1.4 V below V^+ and 1.4 V above V^-.

[2] DC crosstalk is measured with AVP = 5 V, using the internal reference. The conditions of one DAC channel are changed as specified, and the output of an adjacent channel (at midscale) is measured before and after the change.

[3] This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

[4] Temperature coefficient is calculated by first computing the ratio of the maximum change in output voltage to the nominal output voltage. The ratio is then divided by the specified temperature range.

[5] Gain error and bipolar zero error specifications may be degraded for reference input voltages less than 1.25 V. See Figure 4 and Figure 5 curves in the Typical Performance Characteristics section.

[6] Guaranteed by design and not production tested.

[7] Internal reference on.

[8] I(V^+) measured in ±10 V span; outputs unloaded; all channels at full scale. I(V^-) measured in ±10 V span; outputs unloaded; all channels at negative full scale. Each DAC amplifier is internally loaded by a 40 kΩ feedback network. Thus, supply currents increase as output voltages diverge from 0 V.

[9] Digital inputs at 0 V or OVP.

[10] Internal reference mode. Load is 2k in parallel with 100 pF to GND.

[11] AVP = 5 V, 0 V to 5 V range, internal reference mode. DAC is stepped ±1 LSB between half-scale and half-scale – 1LSB. Load is 2k in parallel with 200 pF to GND.

[12] DAC-to-DAC crosstalk is the glitch that appears at the output of one DAC due to full-scale change at the output of another DAC. 0 V to 10 V range with internal reference. The measured DAC is at midscale.

TIMING CHARACTERISTICS

The specifications apply over the full operating temperature range, unless otherwise specified. T_A = 25°C for the typical values. AVP = 5 V, OVP = 5 V, V+ = 15 V, V– = –15 V, V_{REF} = 2.5 V, V_{OUT} unloaded, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AVP = 4.5 V to 5.5 V, OVP = 2.7 V to AVP						
SDI Valid to SCK Setup	t_1		6			ns
SDI Valid to SCK Hold	t_2		6			ns
SCK High Time	t_3		9			ns
SCK Low Time	t_4		9			ns
$\overline{CS}$/LD Pulse Width	t_5		10			ns
LSB SCK High to $\overline{CS}$/LD High	t_6		7			ns
$\overline{CS}$/LD Low to SCK High	t_7		7			ns
SDO Propagation Delay from SCK Falling Edge	t_8	C_{LOAD} = 10 pF				nsns
		OVP = 4.5 V to AVP			20	
		OVP = 2.7 V to 4.5 V			30	
$\overline{CLR}$ Pulse Width	t_9		20			ns
$\overline{CS}$/LD High to SCK Positive Edge	t_{10}		7			ns
$\overline{LDAC}$ Pulse Width	t_{12}		15			ns
$\overline{CS}$/LD High to $\overline{LDAC}$ High or Low Transition	t_{13}		15			ns
SCK Frequency		50% duty cycle			50	MHz
TGP High Time[1]	t_{14}		1			µs
TGP Low Time[1]	t_{15}		1			µs

SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AVP = 4.5 V to 5.5 V, OVP = 1.71 V to 2.7 V						
SDI Valid to SCK Setup	t_1		7			ns
SDI Valid to SCK Hold	t_2		7			ns
SCK High Time	t_3		30			ns
SCK Low Time	t_4		30			ns
$\overline{CS}$/LD Pulse Width	t_5		15			ns
LSB SCK High to $\overline{CS}$/LD High	t_6		7			ns
$\overline{CS}$/LD Low to SCK High	t_7		7			ns
SDO Propagation Delay from SCK Falling Edge	t_8	C_{LOAD} = 10 pF			60	ns
$\overline{CLR}$ Pulse Width	t_9		30			ns
$\overline{CS}$/LD High to SCK Positive Edge	t_{10}		7			ns
$\overline{LDAC}$ Pulse Width	t_{12}		15			ns
$\overline{CS}$/LD High to $\overline{LDAC}$ High or Low Transition	t_{13}		15			ns
SCK Frequency		50% duty cycle			15	MHz
TGP High Time[1]	t_{14}		1			µs
TGP Low Time[1]	t_{15}		1			µs

[1] Guaranteed by design and not production tested.

Timing Diagram

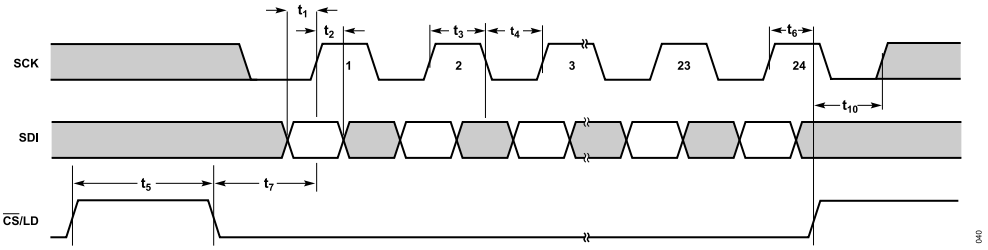

Figure 2. Serial Interface Timing

ABSOLUTE MAXIMUM RATINGS

All voltages are with respect to GND.

Table 4.

Parameter	Rating
Analog Supply Voltage (AVP)	–0.3 V to +6 V
Digital I/O Voltage (OVP)	–0.3 V to +6 V
REFLO	–0.3 V to +0.3 V
V+	–0.3 V to +16.5 V
V–	–16.5 V to +0.3 V
$\overline{CS}$/LD, SCK, SDI, $\overline{LDAC}$, CLR, TGP	−0.3 V to +6 V
MSP0, MSP1, MSP2	–0.3 V to Min (AVP + 0.3 V, 6 V)
V_{OUT0} to V_{OUT15}, MUX	V^- – 0.3 V to V^+ + 0.3 V (Max ±16.5 V)
REF, REFCOMP	–0.3 V to Min (AVP + 0.3 V, 6 V)
SDO	–0.3 V to Min (OVP + 0.3 V, 6 V)
$\overline{OVRTMP}$	–0.3 V to +6 V
Operating Temperature Range	
LTC2668C	0°C to 70°C
LTC2668I	–40°C to +85°C
LTC2668H	–40°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	–65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

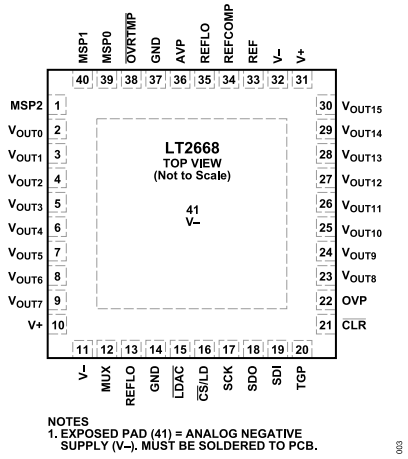

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MSP2	MSPAN Bit 2. Tie this pin to AVP or GND to select the power-on span and power-on-reset code for all 16 channels (see Table 9).
2 to 9, 23 to 30	V_{OUT0} to V_{OUT15}	DAC Analog Voltage Outputs.
10, 31	V^+	Analog Positive Supply. Typically 15 V; 4.5 V to 15.75 V range. Bypass to GND with a 1 µF capacitor.
11, 32, 41	V^-	Analog Negative Supply. Typically –15 V; –4.5 V to –15.75 V range, or can be tied to GND. Bypass to GND with a 1 µF capacitor unless V^- is connected to GND.
12	MUX	Analog Multiplexer Output. Any of the 16 DAC outputs can be internally routed to the MUX pin. When the mux is disabled, this pin becomes high impedance.
13, 35	REFLO	Reference Low Pins. Signal ground for all DAC channels and internal reference. These pins should be tied to GND.
14, 37	GND	Analog Ground. Tie to a clean analog ground plane.
15	$\overline{\text{LDAC}}$	Active-low Asynchronous DAC Update Pin. If $\overline{\text{CS}}$/LD is high, a falling edge on $\overline{\text{LDAC}}$ immediately updates all DAC registers with the contents of the input registers (similar to a software update). If $\overline{\text{CS}}$/LD is low when $\overline{\text{LDAC}}$ goes low, the DAC registers are updated after $\overline{\text{CS}}$/LD returns high. A low on the $\overline{\text{LDAC}}$ pin powers up the DACs. A software power-down command is ignored if $\overline{\text{LDAC}}$ is low. Logic levels are determined by OVP. Tie $\overline{\text{LDAC}}$ high (to OVP) if not used. Updates can then be performed through SPI commands. See Table 6.
16	$\overline{\text{CS}}$/LD	Serial Interface Chip Select/Load Input. When $\overline{\text{CS}}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{\text{CS}}$/LD is taken high, SCK is disabled and the specified command (see Table 6) is executed. Logic levels are determined by OVP.
17	SCK	Serial Interface Clock Input. Logic levels are determined by OVP.
18	SDO	Serial Interface Data Output. The serial output of the 32-bit shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. Can be used for data echo readback or daisy-chain operation (pull-up/down resistor required). The SDO pin becomes high impedance when $\overline{\text{CS}}$/LD is high. Logic levels are determined by OVP.
19	SDI	Serial Interface Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2668 accepts input word lengths of either 24 or 32 bits. Logic levels are determined by OVP.
20	TGP	Asynchronous Toggle Pin. A falling edge updates the DAC register with data from input register A. A rising edge updates the DAC register with data from Input Register B. Toggle operations only affect those DAC channels with their toggle select bit (Tx) set to 1. Tie the TGP pin to OVP if toggle operations are to be done through software. Tie the TGP pin to GND if not using toggle operations. Logic levels are determined by OVP.
21	CLR	Active-low Asynchronous Clear Input. A logic low at this level-triggered input clears the part to the reset code and range determined by the hardwired option chosen using the MSPAN pins and specified in Table 9. The control registers are cleared to zero. Logic levels are determined by OVP.
22	OVP	Digital Input/Output Supply Voltage. 1.71 V ≤ OVP ≤ AVP + 0.3 V. Bypass to GND with a 0.1 µF capacitor.
33	REF	Reference In/Out. The voltage at the REF pin sets the full-scale range of all channels. By default, the internal reference is routed to this pin. Must be buffered when driving external DC load currents. If the reference is disabled (see the Reference Modes section in the Theory of Operation section), its output is disconnected and the REF pin becomes a high impedance

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
		input to which a precision external reference can be applied. For low noise and reference stability, tie a capacitor from this pin to GND. The value must be ≤$C_{REFCOMP}$, where $C_{REFCOMP}$ is the capacitance tied to the REFCOMP pin. The allowable external reference input voltage range is 0.5 V to V_{AVP} – 1.75 V.
34	REFCOMP	Internal Reference Compensation Pin. For low noise and reference stability, tie a 0.1 µF capacitor to GND. Tying REFCOMP to GND causes the part to power up with the internal reference disabled, allowing the use of an external reference at start-up.
36	AVP	Analog Supply Voltage Input. 4.5 V ≤ AVP ≤ 5.5 V. Bypass to GND with a 1 µF capacitor.
38	$\overline{\text{OVRTMP}}$	Thermal Protection Interrupt Pin. This open-drain N-channel output pulls low when chip temperature exceeds 160°C. This pin is released on the next $\overline{\text{CS}}$/LD rising edge. A pull-up resistor is required.
39	MSP0	MSPAN Bit 0. Tie this pin to AVP or GND to select the power-on span and power-on-reset code for all 16 channels (see Table 9).
40	MSP1	MSPAN Bit 1. Tie this pin to AVP or GND to select the power-on span and power-on-reset code for all 16 channels (see Table 9).
41	EPAD	Exposed Pad, Analog Negative Supply (V^-). Must be soldered to PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

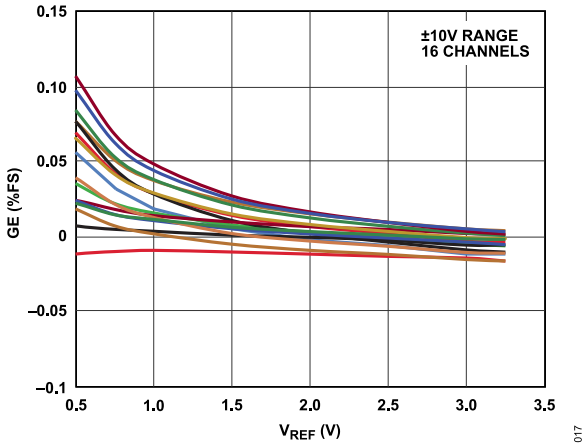

Figure 4. Gain Error vs. Reference Input

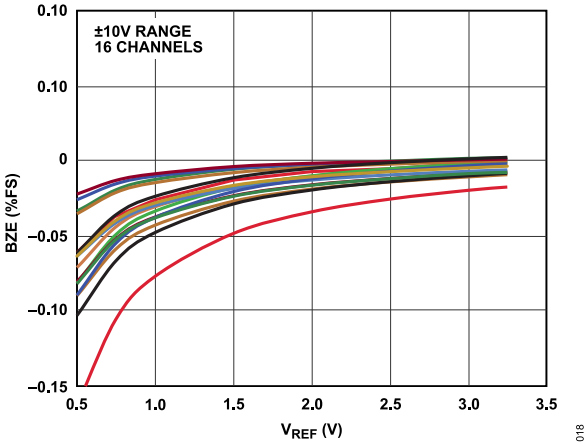

Figure 5. Bipolar Zero Error vs. Reference Input

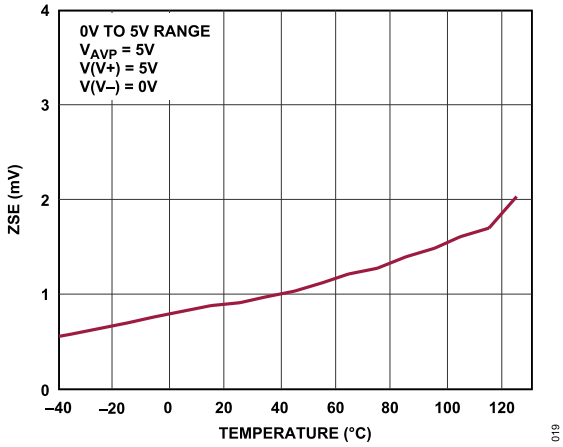

Figure 6. Single-Supply Zero-Scale Error vs. Temperature

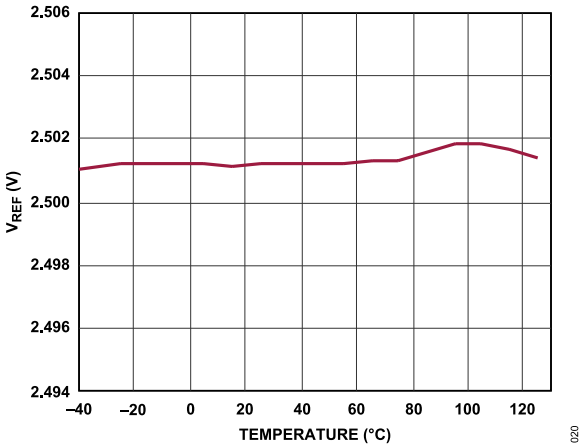

Figure 7. Reference Output vs. Temperature

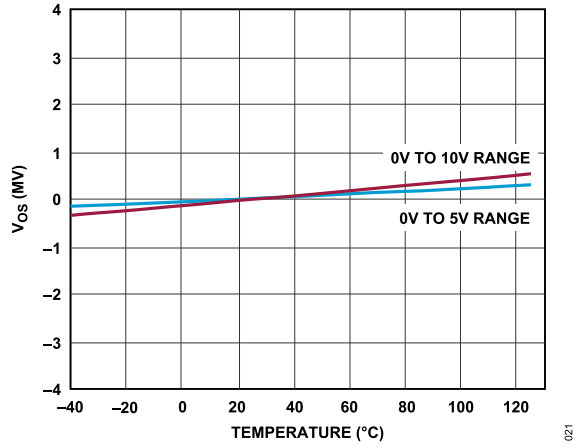

Figure 8. Unipolar Offset vs. Temperature

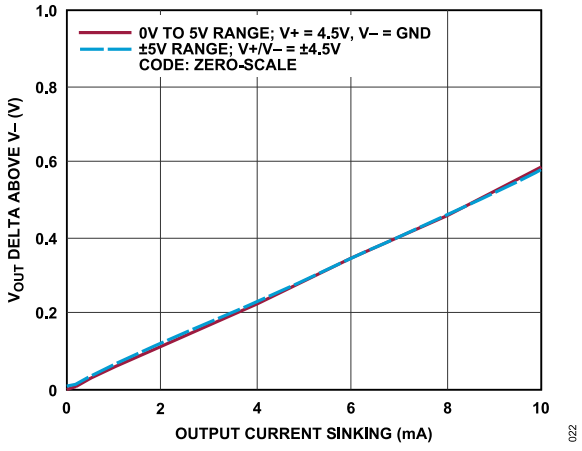

Figure 9. Headroom to V⁻ Rail vs. Output Current

TYPICAL PERFORMANCE CHARACTERISTICS

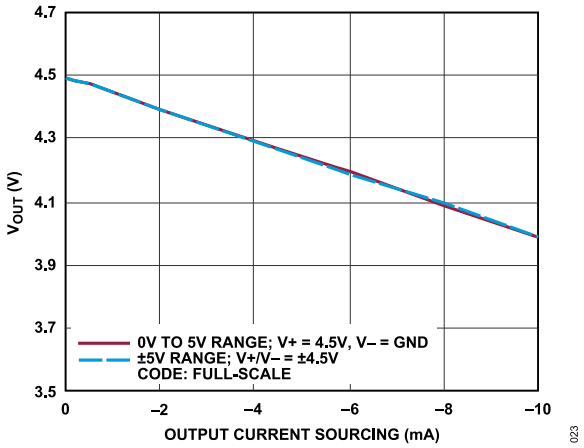

Figure 10. Headroom to V+ Rail vs. Output Current

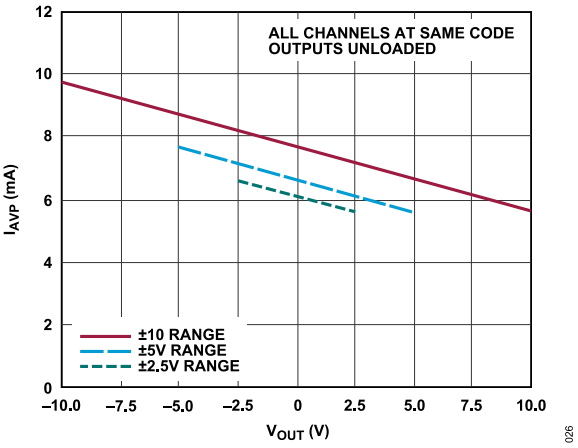

Figure 13. AVP Supply Current vs. Bipolar Output Voltage

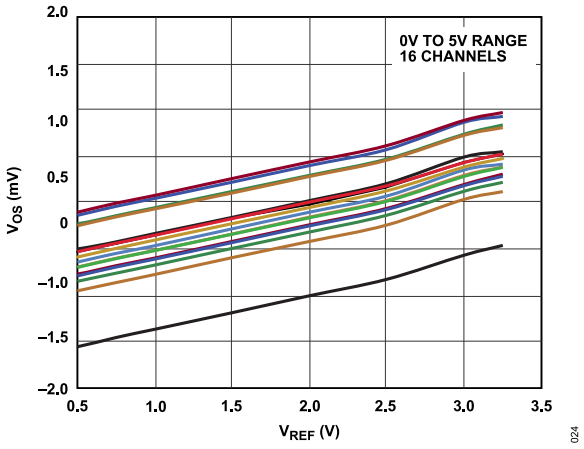

Figure 11. Unipolar Offset vs. Reference Input

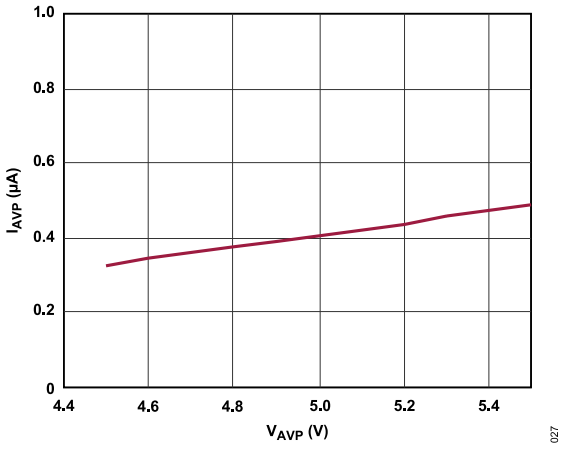

Figure 14. AVP Shutdown Current vs. AVP

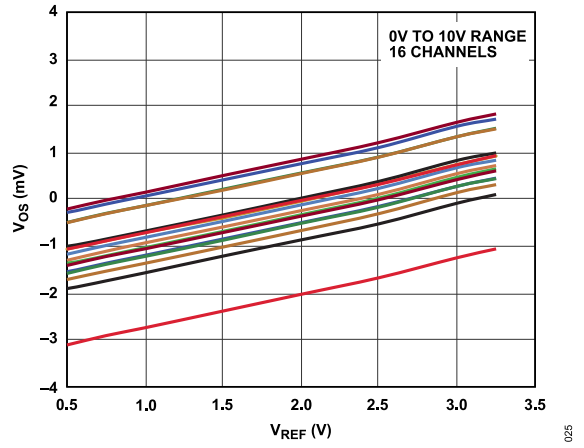

Figure 12. Unipolar Offset vs. Reference Input

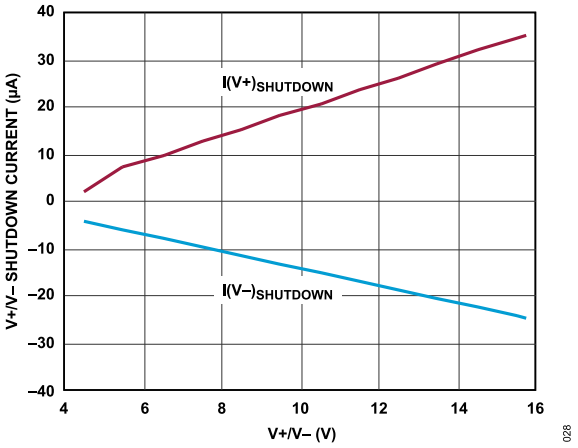

Figure 15. V+/V– Shutdown Current vs. Symmetric Supplies

TYPICAL PERFORMANCE CHARACTERISTICS

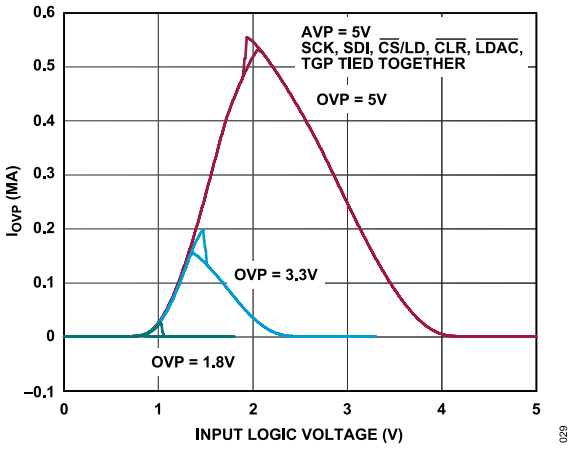

Figure 16. I_{OVP} Supply Current vs. Logic Voltage

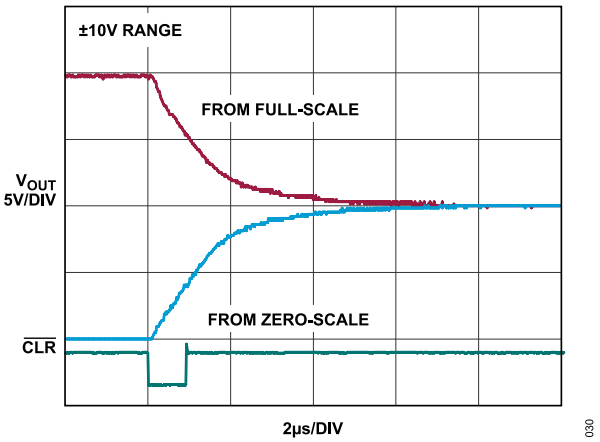

Figure 17. Hardware $\overline{CLR}$ to Midscale

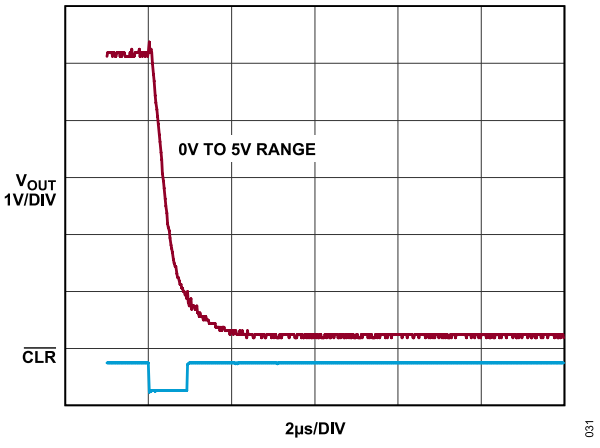

Figure 18. Hardware $\overline{CLR}$ to Zero Scale

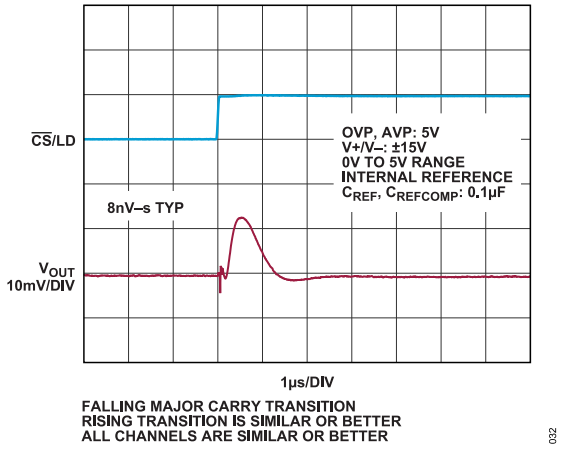

Figure 19. Midscale Glitch Impulse

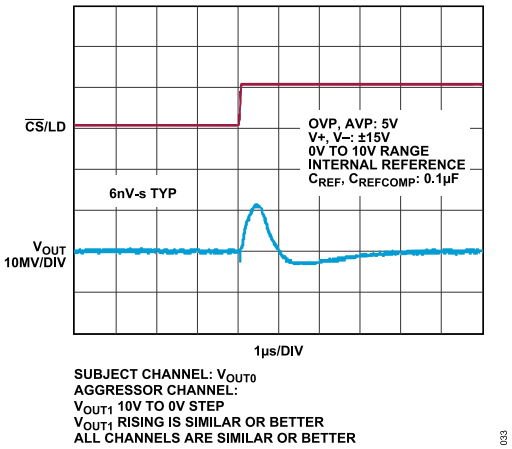

Figure 20. DAC-to-DAC Crosstalk

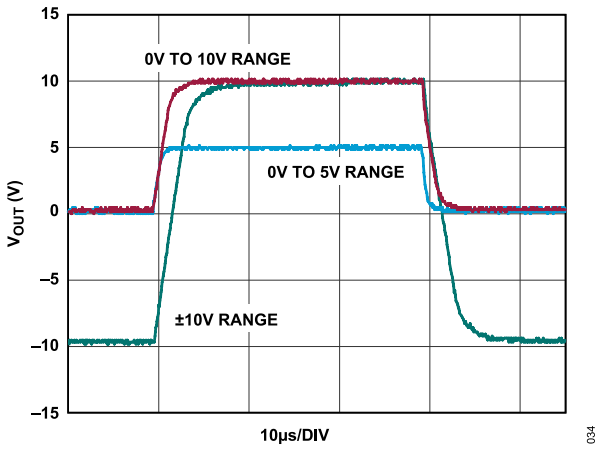

Figure 21. Large Signal Response

TYPICAL PERFORMANCE CHARACTERISTICS

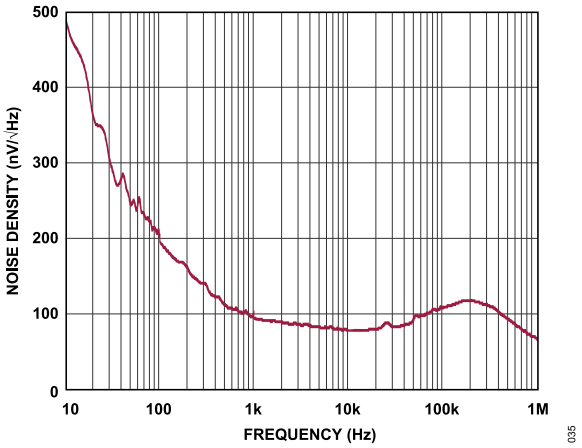

Figure 22. Noise Density vs. Frequency

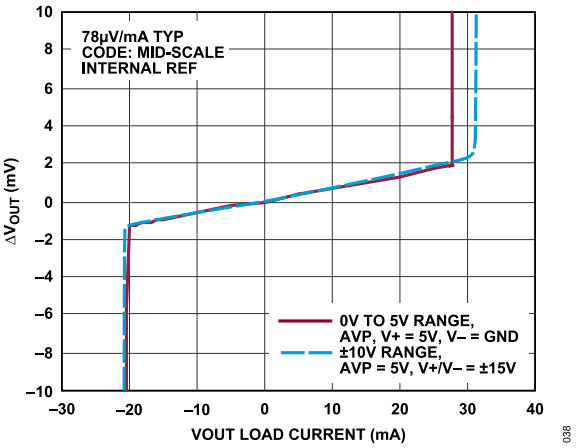

Figure 25. Load Regulation

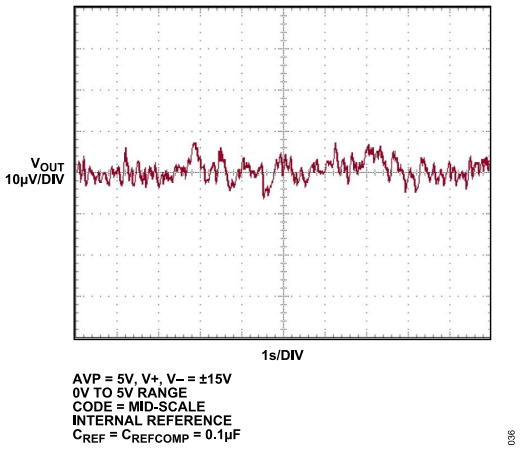

Figure 23. Output 0.1 Hz to 10 Hz Voltage Noise

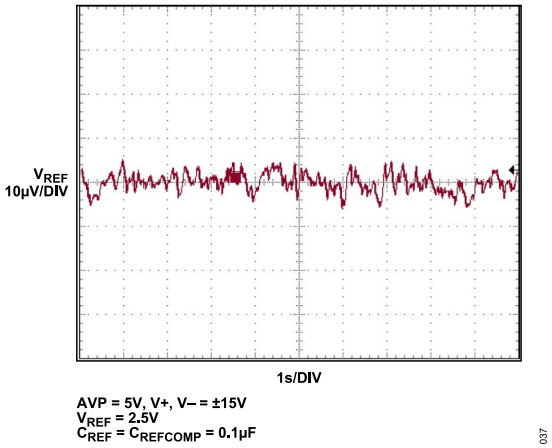

Figure 24. Reference 0.1 Hz to 10 Hz Voltage Noise

TYPICAL PERFORMANCE CHARACTERISTICS

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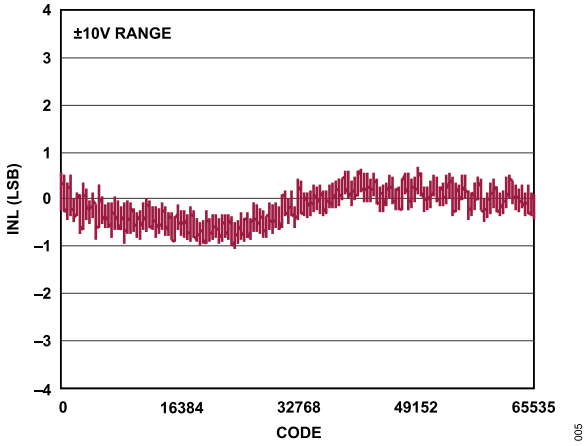

Figure 26. Integral Nonlinearity (INL)

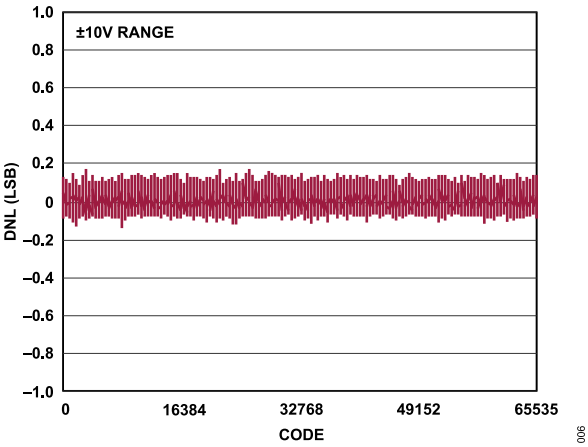

Figure 27. Differential Nonlinearity (DNL)

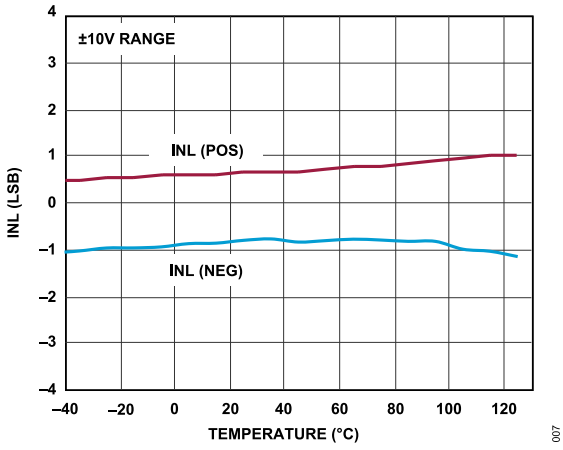

Figure 28. INL vs. Temperature

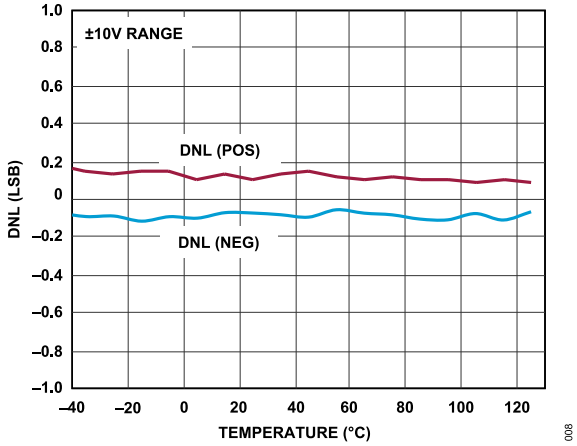

Figure 29. DNL vs. Temperature

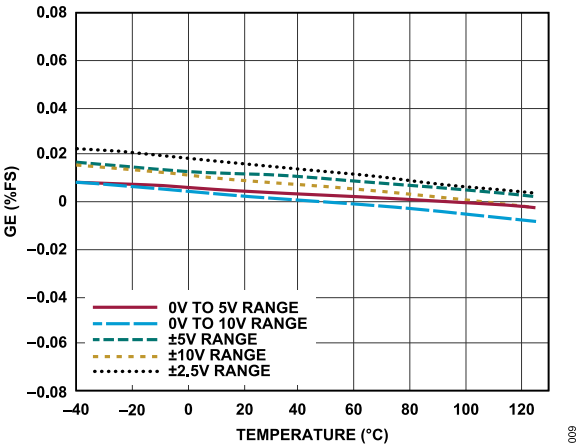

Figure 30. Gain Error vs. Temperature

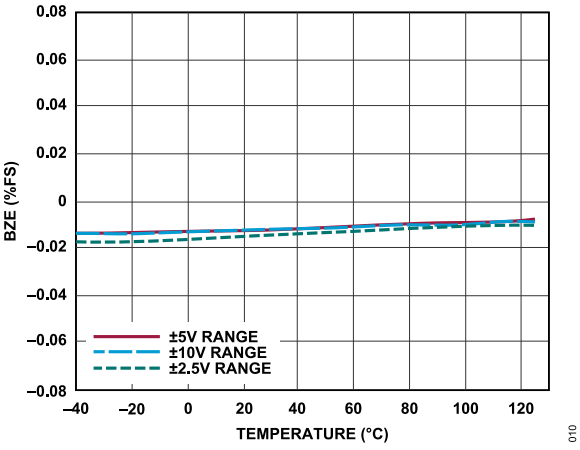

Figure 31. Bipolar Zero Error vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

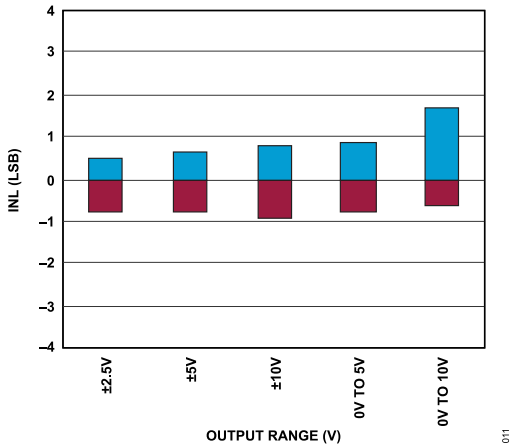

Figure 32. INL vs. Output Range

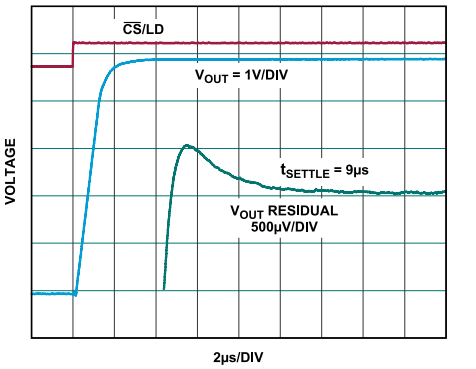

Figure 33. Settling 5 V Step

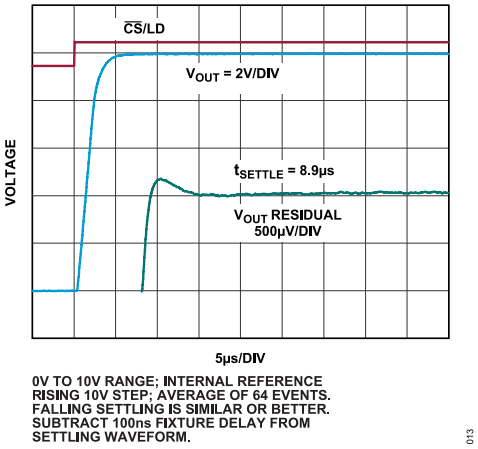

Figure 34. Settling 10 V Step

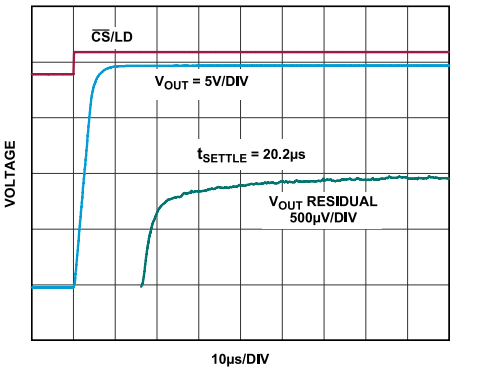

Figure 35. Settling 20 V Step

TYPICAL PERFORMANCE CHARACTERISTICS

LTC2668-12

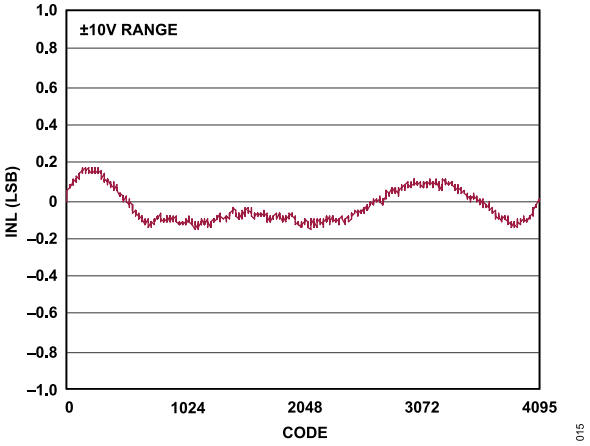

Figure 36. Integral Nonlinearity (INL)

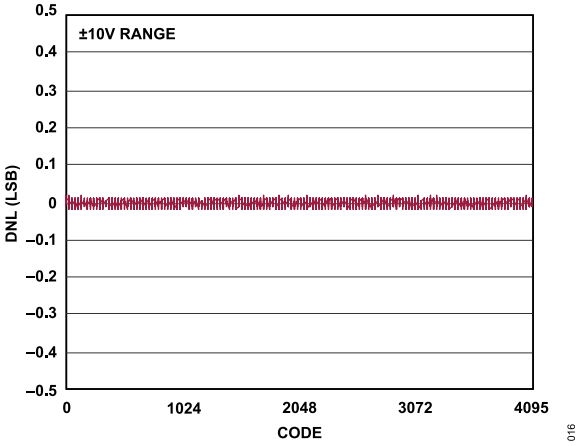

Figure 37. Differential Nonlinearity (DNL)

THEORY OF OPERATION

The LTC2668 is a family of 16-channel, ±10 V digital-to-analog converters with selectable output ranges and an integrated precision reference. The DACs operate on positive 5 V and bipolar ±15 V supplies. The bipolar supplies can operate as low as ±4.5 V, and need not be symmetrical. In addition, the negative V^- supply can be operated at ground, making the parts compatible with single-supply systems. The outputs are driven by the bipolar supply rails.

The output amplifiers offer true rail-to-rail operation. When drawing a load current from the V^+ or V^- rail, the output voltage headroom with respect to that rail is limited by the 60 Ω typical channel resistance of the output devices. See Figure 9 and Figure 10 in the Typical Performance Characteristics section.

The LTC2668 is controlled using a cascadable 3-wire SPI/MICROWIRE-compatible interface with echo readback.

POWER-ON RESET

The outputs reset when power is first applied, making system initialization consistent and repeatable. By tying the MSPAN pins (MSP2, MSP1, MSP0) to GND and/or AVP, the user can select the initial output range and reset code (zero scale or midscale), as well as selecting between a manual (fixed) range and SoftSpan operation. See Table 9 for pin configurations and available options.

POWER SUPPLY SEQUENCING AND START-UP

The supplies (AVP, OVP, V^+, and V^-) can be powered up in any convenient order.

If an external reference is used, the voltage at REF should be kept within the range $-0.3V \le V_{REF} \le AVP + 0.3$ V (see the Absolute Maximum Ratings section). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences when the voltage at AVP is in transition.

Supply bypassing is critical to achieving the best possible performance. At least 1 µF to ground on the AVP, V^+, and V– supplies, and at least 0.1 µF of low ESR capacitance for each supply, as close to the device as possible, is recommended. The larger capacitor can be omitted for OVP.

Hot-plugging or hard switching of supplies is not recommended, as power supply cable or trace inductances combined with bypass capacitances can cause supply voltage transients beyond absolute maximum ratings, even if the bench supply has been carefully current-/voltage-limited. During start-up, limit the supply inrush currents to no more than 5 A and supply slew rates to no more than 5V/µs. Internal protection circuitry can be damaged and long-term reliability adversely affected if these requirements are not met.

Table 6. Command Codes

Command				
C3	C2	C1	C0	
0	0	0	0	Write code to n
1	0	0	0	Write code to all

Table 6. Command Codes (Continued)

Command				
C3	C2	C1	C0	
0	1	1	0	Write span to n
1	1	1	0	Write span to All
0	0	0	1	Update n (power up)
1	0	0	1	Update all (power up)
0	0	1	1	Write code to n, update n (power up)
0	0	1	0	Write code to n, update all (power up)
1	0	1	0	Write code to all, update all (power up)
0	1	0	0	Power down n
0	1	0	1	Power down chip (all DACs, mux and reference)
1	0	1	1	Monitor mux
1	1	0	0	Toggle select
1	1	0	1	Global toggle
0	1	1	1	Config
1	1	1	1	No operation

Table 7. DAC Addresses, n

Address				
A3	A2	A1	A0	
0	0	0	0	DAC 0
0	0	0	1	DAC 1
0	0	1	0	DAC 2
0	0	1	1	DAC 3
0	1	0	0	DAC 4
0	1	0	1	DAC 5
0	1	1	0	DAC 6
0	1	1	1	DAC 7
1	0	0	0	DAC 8
1	0	0	1	DAC 9
1	0	1	0	DAC 10
1	0	1	1	DAC 11
1	1	0	0	DAC 12
1	1	0	1	DAC 13
1	1	1	0	DAC 14
1	1	1	1	DAC 15

DATA TRANSFER FUNCTIONS

The DAC input-to-output transfer functions for all output ranges and resolutions are shown in Figure 38 and Figure 39. The input code is in straight binary format for all ranges.

SERIAL INTERFACE

When the $\overline{CS}$/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (SCK pin). The 4-bit command, C3-C0, is loaded first, followed by the 4-bit DAC address, A3 to A0, and finally the 16-bit data-word in straight binary format. For the LTC2668-16, the data-word comprises the 16-bit input code, ordered MSB-to-LSB. For the LTC2668-12, the data-word comprises the 12-bit input code, ordered MSB to LSB,

THEORY OF OPERATION

followed by four don't care bits. Data can only be transferred to the LTC2668 when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word. The complete sequence is shown in Figure 40.

While the minimum input word is 24 bits, it may optionally be extended to 32 bits. To use the 32-bit word width, 8 don't care bits must be transferred to the device first, followed by the 24-bit word, as just described. Figure 41 shows the 32-bit sequence. The 32-bit word is required for echo readback and daisy-chain operation, and is also available to accommodate processors that have a minimum word width of 16 or more bits.

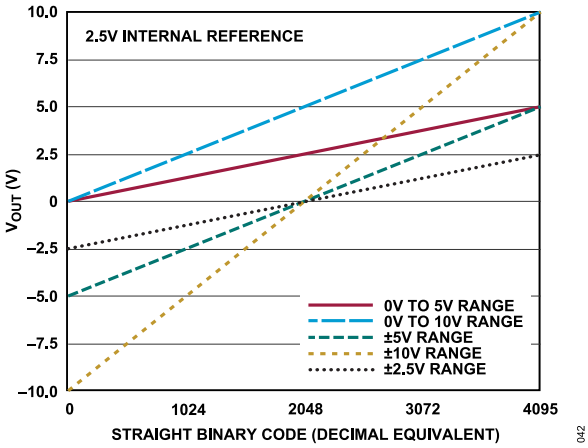

Figure 39. LTC2668-12 Transfer Function

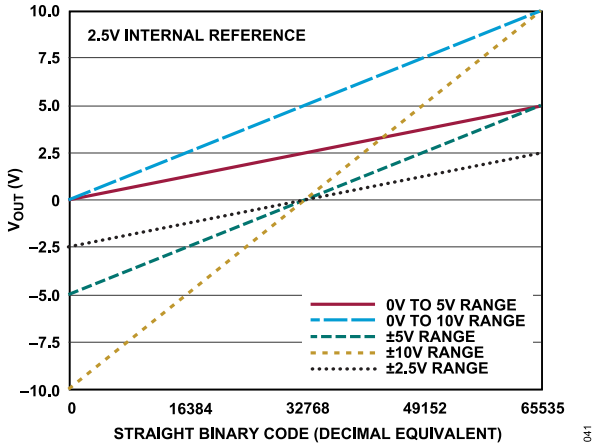

Figure 38. LTC2668-16 Transfer Function

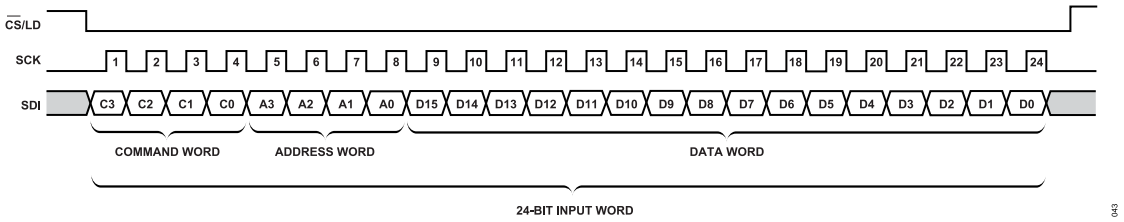

Figure 40. LTC2668-16 24-Bit Load Sequence (Minimum Input Word), LTC2668-12 SDI Data-Word Is 12-Bit Input Code + 4 Don't Care Bits

THEORY OF OPERATION

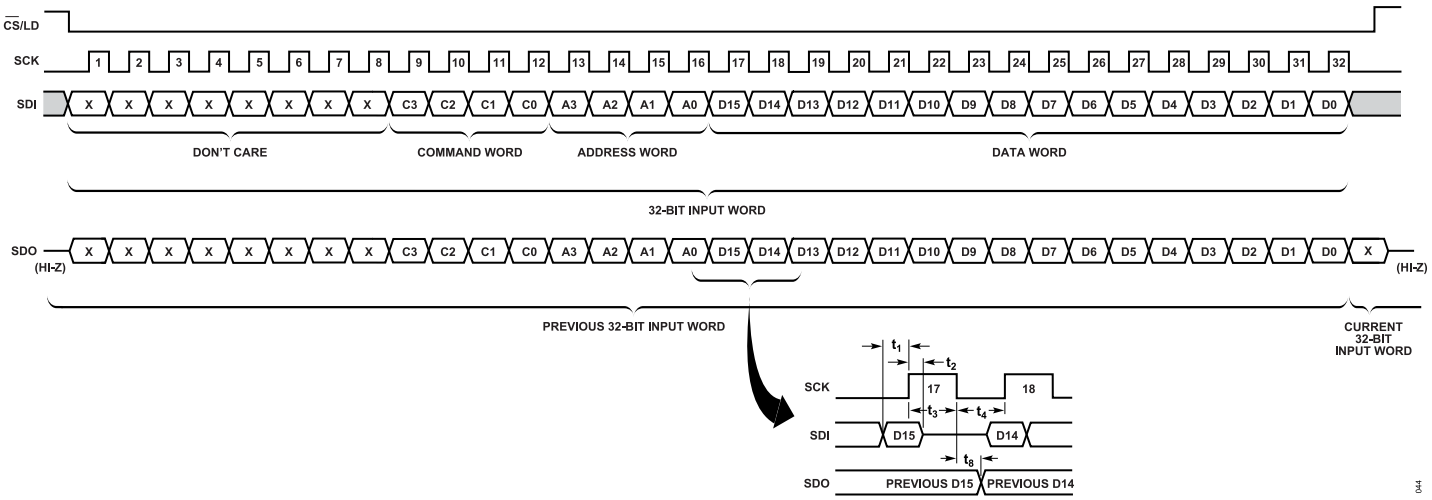

Figure 41. LTC2668-16 32-Bit Load Sequence, LTC2668-12 SDI/SDO Data-Word Is 12-Bit Input Code + 4 Don't Care Bits

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INPUT AND DAC REGISTERS

The LTC2668 has five internal registers for each DAC, in addition to the main shift register (see Figure 1). Each DAC channel has two sets of double-buffered registers: one set for the code data, and one set for the span (output range) of the DAC. Double buffering provides the capability to simultaneously update the span and code, which allows smooth voltage transitions when changing output ranges. It also permits the simultaneous updating of multiple DACs.

Each set of double-buffered registers comprises an input register and a DAC register, as follows:

- Input register: The write operation shifts data from the SDI pin into a chosen input register. The input registers are holding buffers; write operations do not affect the DAC outputs.

  In the code data path, there are two input registers, A and B, for each DAC register. Register B is an alternate input register used only in the toggle operation, while Register A is the default input register (see Figure 1).
- DAC register: The update operation copies the contents of an input register to its associated DAC register. The content of a DAC register directly controls the DAC output voltage or range. The update operation also powers up the selected DAC if it had been in power-down mode. The data path and registers are shown in Figure 1.

  Note that updates always refresh both code and span data, but the values held in the DAC registers remain unchanged unless the associated input register values have been changed via a write operation. For example, if the user writes a new code and updates the channel, the code is updated, while the span is refreshed unchanged. A channel update can come from a serial update command, an $\overline{\text{LDAC}}$ negative pulse, or a toggle operation.

Table 8. Write Span Code

			Output Range	
S2	S1	S0	Internal Reference	External Reference
0	0	0	0 V to 5 V	0 V to 2 V_{REF}
0	0	1	0 V to 10 V	0 V to 4 V_{REF}
0	1	0	±5 V	±2 V_{REF}
0	1	1	±10 V	±4 V_{REF}
1	0	0	±2.5 V	±V_{REF}

OUTPUT RANGES

The LTC2668 is a 16-channel DAC with selectable output ranges. Ranges can either be programmed in software or hardwired through pin strapping.

SOFTSPAN OPERATION

SoftSpan operation (ranges controlled through the serial interface) is invoked by tying all three MSPAN pins (MSP2, MSP1, and MSP0) to AVP (see Table 9). In SoftSpan configuration, all channels initialize to zero -scale in 0 V to 5 V range at power-on. The range and code of each channel are then fully programmable.

Each channel has a set of double-buffered registers for range information (see Figure 1). Program the span input register using the write span n or write span all commands (0110b and 1110b, respectively). Figure 42 shows the syntax, and Table 8 shows the span codes and ranges.

As with the double-buffered code registers, update operations copy the span input registers to the associated span DAC registers.

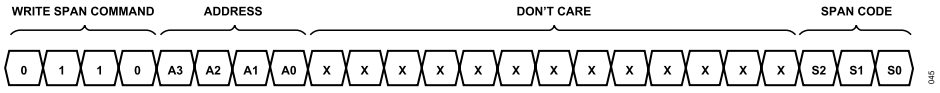

Figure 42. Write Span Syntax

THEORY OF OPERATION

MANUAL SPAN OPERATION

Multiple output ranges are not needed in all applications. By tying the MSPAN pins (MSP2, MSP1, and MSP0) to GND and/or AVP, any output range can be hardware configured without additional operational overhead. Zero-scale and midscale reset options are also available for the unipolar modes (see Table 9).

Table 9. MSPAN Pin Configurations

MSP2	MSP1	MSP0	Output Range	Reset Code	Manual Span[1]	SoftSpan[1]
0	0	0	±10 V	Midscale	X	
0	0	AVP	±5 V	Midscale	X	
0	AVP	0	±2.5 V	Midscale	X	
0	AVP	AVP	0 to 10 V	Zero scale	X	
AVP	0	0	0 V to 10 V	Midscale	X	
AVP	0	AVP	0 V to 5 V	Zero scale	X	
AVP	AVP	0	0 V to 5 V	Midscale	X	
AVP	AVP	AVP	0 V to 5 V	Zero scale		X

[1] X means don't care.

MONITOR MUX

The LTC2668 includes a high voltage multiplexer (mux) for surveying the channel outputs.

The MUX pin is intended for use with high impedance inputs only; the output impedance of the multiplexer is 2.2 kΩ. Continuous DC output current at the MUX pin must be limited to ±1 mA to avoid damaging internal circuits.

The output voltage range of the multiplexer is from V^- to V^+ – 1.4 V. The output is disabled (high impedance) at power-up.

The syntax and codes for the Mux command are shown in Figure 43 and Table 10.

Table 10. Monitor Mux Control Codes

M4	M3	M2	M1	M0	MUX Pin Output
0	0	0	0	0	Disabled (high-Z)
1	0	0	0	0	V_{OUT0}
1	0	0	0	1	V_{OUT1}
1	0	0	1	0	V_{OUT2}
1	0	0	1	1	V_{OUT3}
1	0	1	0	0	V_{OUT4}
1	0	1	0	1	V_{OUT5}
1	0	1	1	0	V_{OUT6}
1	0	1	1	1	V_{OUT7}
1	1	0	0	0	V_{OUT8}
1	1	0	0	1	V_{OUT9}
1	1	0	1	0	V_{OUT10}
1	1	0	1	1	V_{OUT11}
1	1	1	0	0	V_{OUT12}
1	1	1	0	1	V_{OUT13}
1	1	1	1	0	V_{OUT14}
1	1	1	1	1	V_{OUT15}

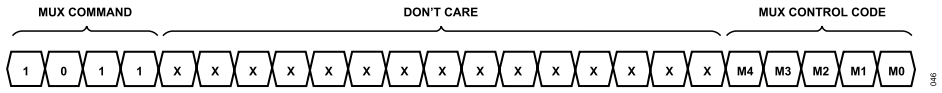

Figure 43. Mux Command

THEORY OF OPERATION

TOGGLE OPERATIONS

Some systems require that DAC outputs switch repetitively between two voltage levels. Examples include introducing a small AC bias, or independently switching between the on and off states. The LTC2668 toggle function facilitates these kinds of operations by providing two input registers (A and B) per DAC channel.

Toggling between A and B is controlled by three signals. The first of these is the toggle select command, which acts on a data field of 16 bits, each of which controls a single channel (see Figure 44). The second is the global toggle command, which controls all selected channels using the global toggle bit TGB (see Figure 45). Finally, the TGP pin allows the use of an external clock or logic signal to toggle the DAC outputs between A and B. The signals from these controls are combined as shown in Figure 46.

If the toggle function is not needed, tie TGP (Pin 20) to ground and leave the toggle select register in its power-on reset state (cleared to zero). Input Registers A then function as the sole input registers, and Registers B are not used.

TOGGLE SELECT REGISTER (TSR)

The toggle select command (1100b) syntax is shown in Figure 44. Each bit in the 16-bit TSR data field controls the DAC channel of the same name: T0 controls Channel 0, T1 controls Channel 1,..., and Tx controls Channel x.

The toggle select bits (T0, T1,..., T15) have a dual function. First, each toggle select bit controls which input register (A or B) receives data from a write-code operation. When the toggle select bit of a given channel is high, write-code operations are directed to Input Register B of the addressed channel. When the bit is low, write-code operations are directed to Input Register A.

Secondly, each toggle select bit enables the corresponding channel for a toggle operation.

WRITING TO INPUT REGISTER A AND INPUT REGISTER B

Having chosen channels to toggle, write the desired codes to Input Registers A for the chosen channels. Then set the channels' toggle select bits using the toggle select command. Finally, write the desired codes to Input Registers B. Once these steps are completed, the channels are ready to toggle. For example, to set up Channel 3 to toggle between Code 4096 and Code 4200,

1. Write Code Channel 3 (code = 4096) to Register A.

   00000011 00010000 00000000
2. Toggle select (set Bit T3).

   11000000 00000000 00001000
3. Write Code Channel 3 (code = 4200) to Register B.

   00000011 00010000 01101000

The write code of Step 3 is directed to Register B because in Step 2, Bit T3 was set to 1. Channel 3 now has Input Register A and Input Register B holding the two desired codes, and is prepared for the toggle operation.

TOGGLING BETWEEN REGISTER A AND REGISTER B

Once Input Register A and Register B have been written to for all desired channels and the corresponding toggle select bits are set high, as in the previous example, the channels are ready for toggling.

The LTC2668 supports three types of toggle operations: a first in which all selected channels are toggled together using the SPI port; a second in which all selected channels are toggled together using an external clock or logic signal; and a third in which any combination of channels can be instructed to update from either Input Register A or Input Register B.

The internal toggle-update circuit is edge triggered, so only transitions (of TGB or TGP) trigger an update from the respective input register.

To toggle all selected channels together using the SPI port, ensure the TGP pin is high and that the bits in the toggle select register corresponding to the desired channels are also high. Use the global toggle command (1101b) to alternate codes, sequentially changing the global toggle bit TGB (see Figure 45). Changing TGB from 1 to 0 updates the DAC registers from their respective Input Registers A. Changing TGB from 0 to 1 updates the DAC registers from their respective input registers B. Note that in this way up to 16 channels may be toggled with just one serial command.

To toggle all selected channels using an external logic signal, ensure that the TGB bit in the global toggle register is high and that in the toggle select register, the bits corresponding to the desired channels are also high. Apply a clock or logic signal to the TGP pin to alternate codes. TGP falling edges update the DAC registers from their associated Input Registers A. TGP rising edges update the DAC registers from their associated Input Registers B. Note that once the input registers are set up, all toggling is triggered by the signal applied to the TGP pin, with no further SPI instructions needed.

To cause any combination of channels to update from either Input Register A or Input Register B, ensure the TGP pin is high and that the TGB bit in the global toggle register is also high. Using the toggle select command, set the toggle select bits as needed to select the input register (A or B) with which each channel is to be updated. Then update all channels, either by using the serial command (1001b) or by applying a negative pulse to the LDAC pin. Any channels whose toggle select bits are 0 update from Input Register A, while channels whose toggle select bits are 1 update from Input Register B (see Figure 46). By alternating toggle-select and update operations, up to 16 channels can be simultaneously switched to A or B as needed.

THEORY OF OPERATION

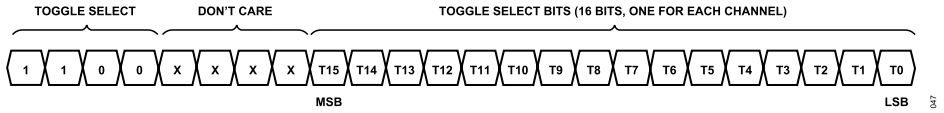

Figure 44. Toggle Select Syntax

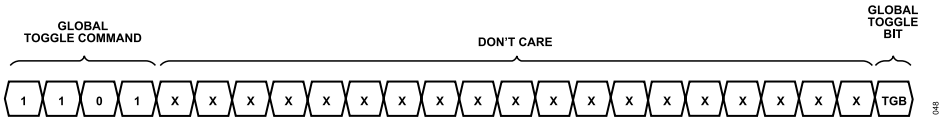

Figure 45. Global Toggle Syntax

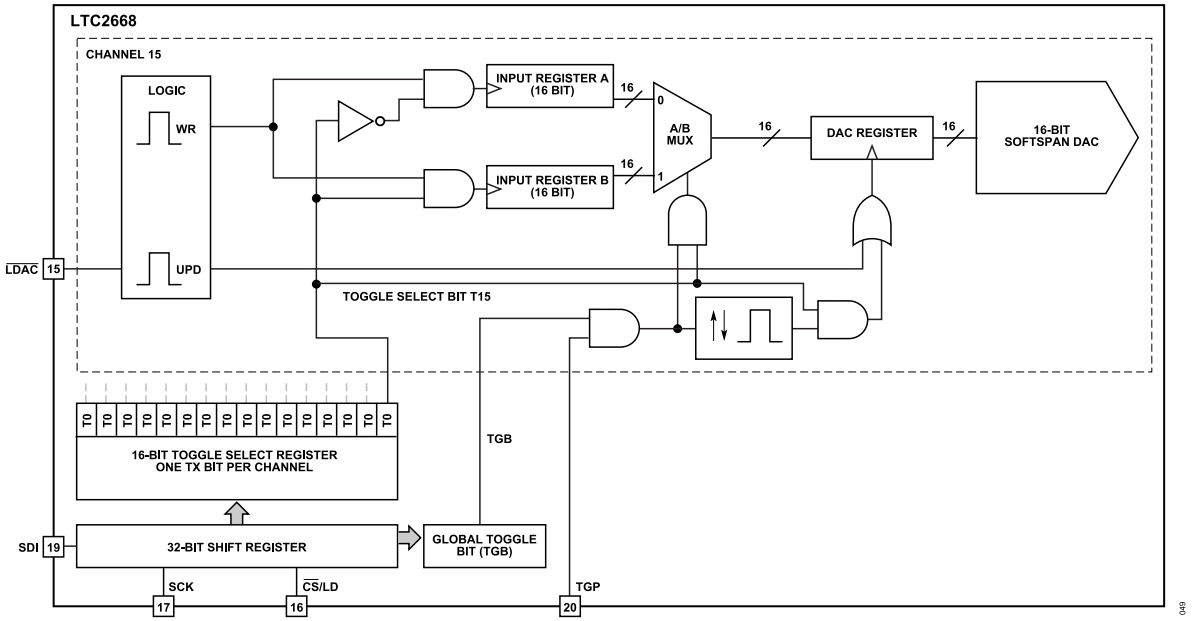

Figure 46. Simplified Toggle Block Diagram—Conceptual Only, Actual Circuit May Differ

THEORY OF OPERATION

DAISY-CHAIN OPERATION

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge, suitable for clocking into the microprocessor on the next 32 SCK rising edges.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (that is, SCK, SDI, and $\overline{CS}$/LD). Such a daisy-chain series is configured by connecting the SDO of each upstream device to the SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register that extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then, the concatenated input data is transferred to the chain, using the SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the no-operation command (1111) for all other devices in the chain.

When $\overline{CS}$/LD is taken high, the SDO pin presents a high impedance output, so a pull-up resistor is required at the SDO of each device (except the last) for daisy-chain operation.

ECHO READBACK

The SDO pin can be used to verify data transfer to the device. During each 32-bit instruction cycle, SDO outputs the previous 32-bit instruction for verification.

When $\overline{CS}$/LD is high, SDO presents a high impedance output, releasing the bus for use by other SPI devices.

POWER-DOWN MODE

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than 16 DAC outputs are needed. When in power-down, the output amplifiers and reference buffers are disabled. The DAC outputs are put into a high impedance state, and the output pins are passively pulled to ground through individual 42 kΩ (minimum) resistors. Register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using Command 0100b in combination with the appropriate DAC address. In addition, all the DAC channels and the integrated reference together can be put into power-down mode using the power-down chip command, 0101b. The 16-bit data word is ignored for all power-down commands.

Normal operation resumes by executing any command which includes a DAC update—either in software, as shown in Table 6, by taking the asynchronous $\overline{LDAC}$ pin low, or by toggling (see the Toggling Between Register A and Register B section). The selected DAC is powered up as its voltage output is updated. When updating a powered-down DAC, add a wait time to accommodate the extra power-up delay. If the channels have been powered down (command 0100b) prior to the update command, the power-up delay time is 30 µs. If, on the other hand, the chip has been powered down (Command 0101b), the power-up delay time is 35 µs.

ASYNCHRONOUS DAC UPDATE USING $\overline{LDAC}$

In addition to the update commands shown in Table 6, the asynchronous, active-low $\overline{LDAC}$ pin updates all 16 DAC registers with the contents of the input registers.

If $\overline{CS}$/LD is high, a low on the $\overline{LDAC}$ pin causes all DAC registers to be updated with the contents of the input registers.

If $\overline{CS}$/LD is low, a low going pulse on the $\overline{LDAC}$ pin before the rising edge of $\overline{CS}$/LD powers up all DAC outputs, but does not cause the outputs to be updated. If $\overline{LDAC}$ remains low after the rising edge of $\overline{CS}$/LD, then $\overline{LDAC}$ is recognized, the command specified in the 24-bit word is executed and the DAC outputs are updated.

The DAC outputs are powered up when $\overline{LDAC}$ is taken low, independent of the state of $\overline{CS}$/LD.

If $\overline{LDAC}$ is low at the time $\overline{CS}$/LD goes high, any software power-down command (power down n, power-down chip, config/select external reference) that was specified in the input word is inhibited.

REFERENCE MODES

The LTC2668 has two reference modes (internal and external) with which the reference source can be selected. In either mode, the voltage at the REF pin and the output range settings determine the full-scale voltage of each of the channels.

The device has a precision 2.5 V integrated reference with a typical temperature drift of 2 ppm/°C. To use the internal reference, the REFCOMP pin should be left floating (no DC path to ground). In addition, the RD bit in the config register must have a value of 0. This value is reset to 0 at power-up, or it can be reset using the config command, 0111b. Figure 47 shows the command syntax.

A buffer is needed if the internal reference is to drive external circuitry. For reference stability and low noise, a 0.1 µF capacitor should be tied between REFCOMP and GND. In this configuration, the internal reference can drive up to 0.1 µF with excellent stability. In order to ensure stable operation, the capacitive load on the REF pin should not exceed that on the REFCOMP pin.

To use an external reference, tie the REFCOMP pin to ground. This disables the output of the internal reference at startup, so that the REF pin becomes a high impedance input. Apply the desired reference voltage at the REF pin after powering up, and set the RD bit to 1 using the config command (0111b). This reduces AVP supply current by approximately 200 µA.

THEORY OF OPERATION

The acceptable external reference voltage range is: 0.5 V ≤ V_{REF} ≤ AVP – 1.75 V.

INTEGRATED REFERENCE BUFFERS

Each channel has its own integrated high performance reference buffer. The buffers have very high input impedance and do not load the reference voltage source. These buffers shield the reference voltage from glitches caused by DAC switching and, thus, minimize DAC-to-DAC dynamic crosstalk. Typically DAC-to-DAC crosstalk is less than 6 nV × s (0 V to 10 V range). See Figure 20 in the Typical Performance Characteristics section.

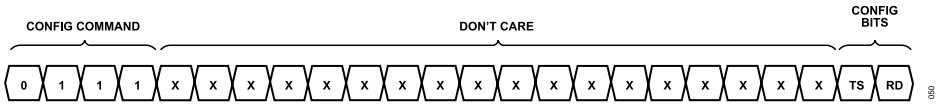

Figure 47. Config Command Syntax—Thermal Shutdown (TS) and Reference Disable (RD)

THEORY OF OPERATION

VOLTAGE OUTPUTS

An amplifier's ability to maintain its rated voltage accuracy over a wide range of load conditions is characterized in its load regulation specification. The change in output voltage is measured per milliampere of forced load current change. Each of the LTC2668 high voltage, rail-to-rail output amplifiers has guaranteed load regulation when sourcing or sinking up to 10 mA with supply headroom as low as 1.4 V. Additionally, the amplifiers can drive up to ±14 mA if available headroom is increased to 2.2 V or more.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from µV/mA to ohms. The amplifier's DC output impedance is typically 0.08 Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 60 Ω typical channel resistance of the output devices—for example, when sinking 1 mA, the minimum output voltage (above V^-) is 60 Ω × 1 mA = 60 mV. See Figure 9 and Figure 10 in the Typical Performance Characteristics section.

The amplifiers are stable driving capacitive loads of up to 1000 pF.

THERMAL OVERLOAD PROTECTION

The LTC2668 protects itself if the die temperature exceeds 160°C. All channels power down, and the open-drain $\overline{\text{OVRTMP}}$ interrupt pin pulls low. The reference and bias circuits stay powered on. Once triggered, the device stays in shutdown even after the die cools.

The temperature of the die must fall to approximately 150°C before the channels can be returned to normal operation. Once the part has cooled sufficiently, the shutdown can be cleared with any valid update operation, including $\overline{\text{LDAC}}$ or a toggle operation. A $\overline{\text{CS}}$/LD rising edge releases the $\overline{\text{OVRTMP}}$ pin regardless of the die temperature.

Since the total load current of the device can easily exceed 100 mA, die heating potential of the system design should be evaluated carefully. Grounded loads as low as 1 k can be used and does not result in excessive heat.

Thermal protection can be disabled by using the config command to set the TS bit (see Figure 47).

BOARD LAYOUT

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by minimizing common-mode resistance of signal and power grounds.

As with any high resolution converter, clean board grounding is important. A low impedance analog ground plane is necessary, as are star-grounding techniques. Keep the board layer used for star ground continuous to minimize ground resistances; that is, use the star-ground concept without using separate star traces. Resistance from the REFLO pin to the star point should be as low as possible.

For best performance, stitch the ground plane with arrays of vias on 150 to 200 mil centers connecting it with the ground pours from the other board layers. This reduces overall ground resistance and minimizes ground loop area.

USING THE LTC2668 IN 5 V SINGLE-SUPPLY SYSTEMS

The LTC2668 can be used in single-supply systems simply by connecting the V– pins to ground along with REFLO and GND, while V^+ and AVP are connected to a 5 V supply. OVP can be connected to the 5 V supply or to the logic supply voltage if lower than 5 V.

With the internal reference, use the 0 V to 5 V output range. As with any rail-to-rail device, the output is limited to voltages within the supply range. Since the outputs of the device cannot go below ground, they may limit at the lowest codes, as shown in Figure 49. Similarly, limiting can occur near full scale if full-scale error (FSE = V_{OS} + GE) is positive, or if $V^+ < 2 \times V_{REF}$. See Figure 50.

The multiplexer can be used and is fully functional. It can pull all the way to ground, but the upper headroom limitation means that it is useful for output voltages of 3.6 V or below only (V^+ = 5 V).

More flexibility can be afforded by using an external reference. For example, by using a 1.25 V reference such as the LTC6655, we can now select between the 0× to 2× and 0× to 4× ranges, which give full-scale voltages of 2.5 V and 5 V, respectively. Furthermore, the part can be configured for reset to zero- or mid-scale codes (see the Output Ranges section).

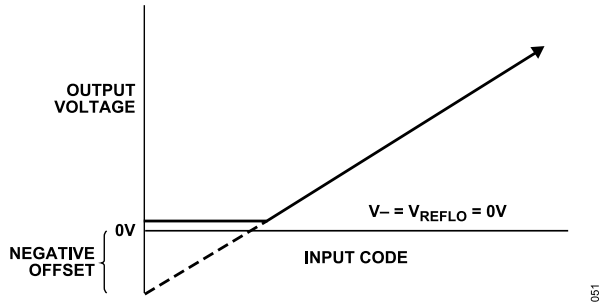

Figure 48. Effects of 0 V to 5 V Output Range for Single-Supply Operation—Overall Transfer Function

THEORY OF OPERATION

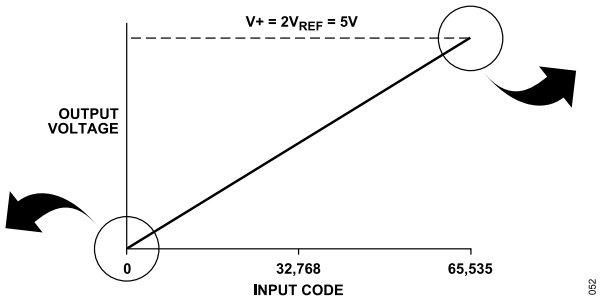

Figure 49. Effects of 0 V to 5 V Output Range for Single-Supply Operation—Effect of Negative Offset for Codes Near Zero Scale

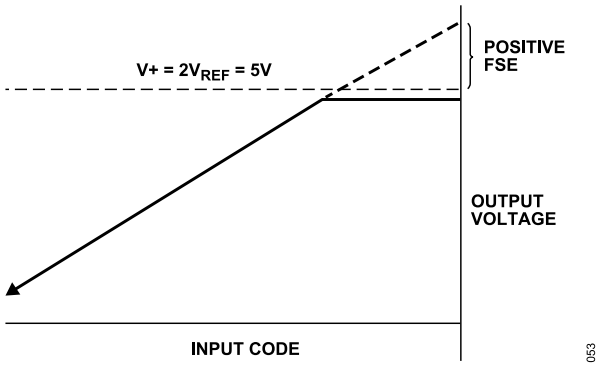

Figure 50. Effects of 0 V to 5 V Output Range for Single-Supply Operation—Effect of Positive Full-Scale Error for Codes Near Full Scale

THEORY OF OPERATION

TYPICAL APPLICATION

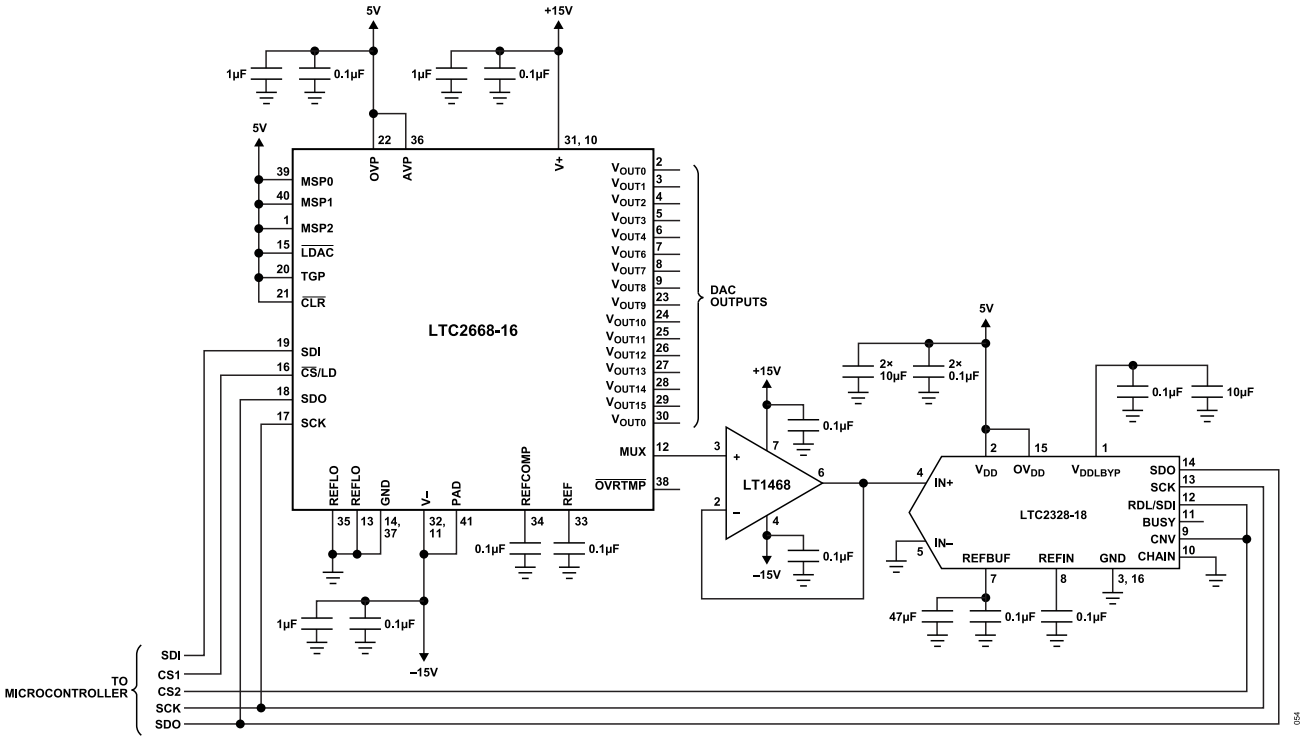

Figure 51. Using the Analog Multiplexer to Measure DAC Output Voltages Up to ±10.24 V; Independent ADC Reference Cross-Checks LTC2668 Internal Reference

RELATED PARTS

Table 11. Related Parts

Part Number	Description	Comments
DACs		
LTC2704	Quad serial 16-/14-/12-bit V_{OUT} SoftSpan DACs with ±2 LSB INL, ±1 LSB DNL	Software programmable output ranges up to ±10 V, SPI interface, no external amps needed
LTC2754	Quad serial 16-/12-bit I_{OUT} SoftSpan DACs with ±1 LSB INL, ±1 LSB DNL	Software programmable output ranges up to ±10 V, SPI interface, 7 mm × 8 mm QFN package
LTC2656	Octal serial 16-/12- bit V_{OUT} DACs with internal reference	±10 ppm/°C internal reference, 4 mm × 5 mm QFN Package
LTC2636	Octal 12-/10-/8-bit SPI V_{OUT} DACs with internal reference	±10 ppm/°C internal reference, 4 mm × 3 mm DFN and 16-Lead MSOP packages
References		
LTC6655A	Low drift precision buffered reference	0.025% max tolerance, 2 ppm/°C Max, 0.25 ppm_{P-P} 0.1 Hz to 10 Hz noise

OUTLINE DIMENSIONS

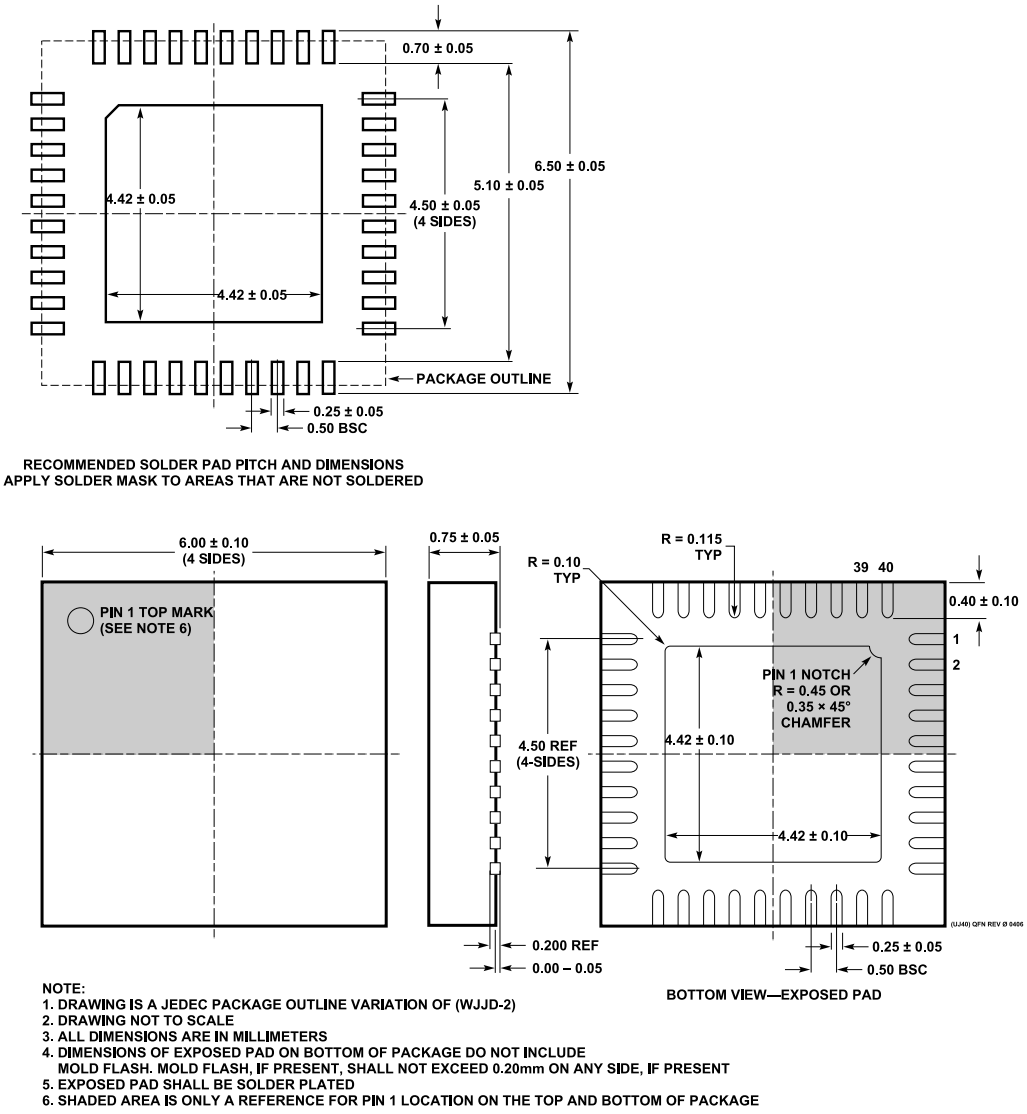

Figure 52. 40-Lead Plastic QFN
(6 mm × 6 mm)
UJ Package

Updated: August 14, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
LTC2668CUJ-12#PBF	0°C to +70°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)		05-08-1728
LTC2668CUJ-12#TRPBF	0°C to +70°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)	Reel, 2000	05-08-1728
LTC2668CUJ-16#PBF	0°C to +70°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)		05-08-1728
LTC2668CUJ-16#TRPBF	0°C to +70°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)	Reel, 2000	05-08-1728
LTC2668HUJ-12#PBF	-40°C to +125°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)		05-08-1728
LTC2668HUJ-12#TRPBF	-40°C to +125°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)	Reel, 2000	05-08-1728
LTC2668HUJ-16#PBF	-40°C to +125°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)		05-08-1728
LTC2668HUJ-16#TRPBF	-40°C to +125°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)	Reel, 2000	05-08-1728
LTC2668IUJ-12#PBF	-40°C to +85°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)		05-08-1728

OUTLINE DIMENSIONS

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
LTC2668IUJ-12#TRPBF	-40°C to +85°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)	Reel, 2000	05-08-1728
LTC2668IUJ-16#PBF	-40°C to +85°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)		05-08-1728
LTC2668IUJ-16#TRPBF	-40°C to +85°C	40-Lead QFN (6mm x 6mm x 0.75mm w/ EP)	Reel, 2000	05-08-1728

[1] All models are RoHS compliant.

EVALUATION BOARDS

Model[1]	Description
DC2025A-B	LTC2668-12 Demo Board
DC2025A-A	LTC2668-16 Demo Board

[1] All models are RoHS compliant.