*Click **here** to ask an associate for production status of specific part numbers.*

MAX20029/MAX20029B/ MAX20029C/MAX20029D

Automotive Quad/Triple Low-Voltage Step-Down DC-DC Converters

General Description

The MAX20029/MAX20029B/MAX20029C/MAX20029D power-management ICs (PMICs) integrate four low-voltage, high-efficiency, step-down DC-DC converters. Each of the four outputs is factory or resistor programmable between 1V to 4.0V (MAX20029/MAX20029B) or 0.7V to 3.8V (MAX20029C/MAX20029D). The MAX20029/MAX20029C has two 0.5A/1A/1.5A channels and two 0.5A/1.5A channels, while the MAX20029B/MAX20029D has two 0.5A/1.5A channels and by combining channels 1 and 2, a single 2A/3A channel. The PMICs operate from 3.0V to 5.5V, making them ideal for automotive point-of-load and post-regulation applications.

The PMICs feature fixed-frequency PWM-mode operation with a switching frequency of 2.2MHz. High-frequency operation allows for an all-ceramic capacitor design and small-size external components. The low-resistance on-chip switches ensure high efficiency at heavy loads while minimizing critical inductances, making the layout a much simpler task with respect to discrete solutions. Internal current sensing and loop compensation reduce board space and system cost.

The PMICs offer a spread-spectrum option to reduce radiated emissions. Two of the four buck converters operate 180° out-of-phase with the internal clock. This feature reduces the necessary input capacitance and improves EMI as well. All four buck converters operate in constant PWM mode outside the AM band. The PMICs offer a SYNC input to synchronize to an external clock.

The PMICs provide individual enable inputs and power-good/ reset outputs, as well as factory-programmable PG times.

The PMICs offer several important protection features including: input overvoltage protection, input undervoltage lockout, cycle-by-cycle current limiting, and overtemperature shutdown.

The MAX20029/MAX20029B/MAX20029C/MAX20029D PMICs are available in a 28-pin TQFN package with an exposed pad and are specified for operation over the -40°C to +125°C automotive temperature range.

Applications

- Automotive
- Industrial

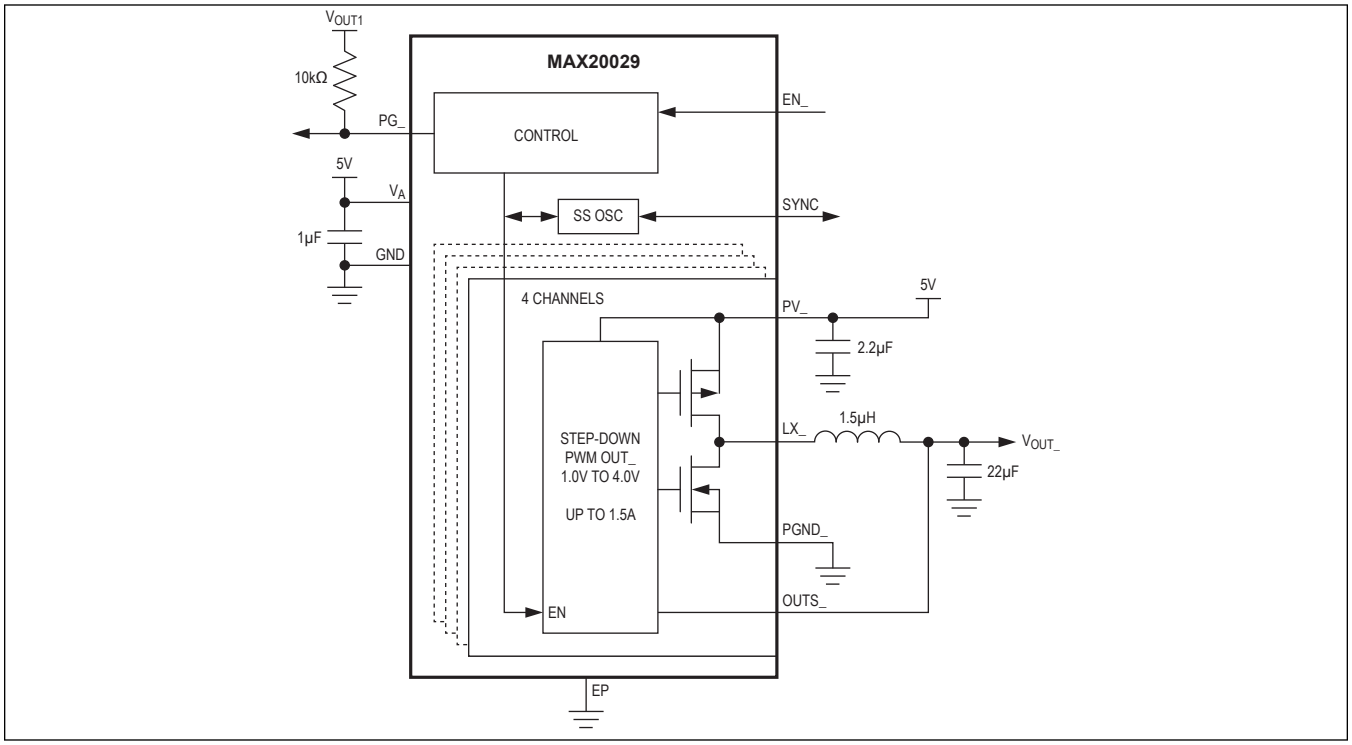
Benefits and Features

- Quad Step-Down DC-DC Converters with Integrated FETs
- Operate from 3.0V to 5.5V Supply Voltage
- 0.7V to 4.0V Fixed or Adjustable Output Voltage
- 2.2MHz Switching Frequency
- MAX20029/MAX20029C: Up to Four 1.5A Channels
- MAX20029B/MAX20029D: Up to One 3A + Two 1.5A Channels
- Designed to Improve Automotive EMI Performance
  - Forced-PWM Operation
  - Two Channels 180° Out-of-Phase
  - SYNC Input
  - Spread-Spectrum Option
- Soft-Start and Supply Sequencing Reduces Inrush Current
- Individual Enable Inputs and Power-Good Outputs Simplify Sequencing
- OV Input-Voltage Monitoring
- Overtemperature and Short-Circuit Protection
- 28-Pin (5mm x 5mm x 0.8mm) TQFN-EP Package
- -40°C to +125°C Operating Temperature Range

Ordering Information appears at end of data sheet.

19-100083; Rev 13; 5/24

Simplified Block Diagram



Absolute Maximum Ratings

PV_ to PGND_ ..... -0.3V to +6.0V
V_A to GND ..... -0.3V to +6.0V
OUTS_, EN_, PG_, SYNC to GND .....-0.3V to V_A + 0.3V
PV_ to PV_ ..... -0.3V to +0.3V
PGND_ to GND ..... -0.3V to +0.3V
LX_ to PGND..... -1.0V to PV_ + 0.3V
LX_ Continuous RMS Current..... 2.0A
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
28-pin TQFN (derate 28.6mW/°C above +70°C).....2285mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28 TQFN-EP

Package Code	T2855+5
Outline Number	21-0140
Land Pattern Number	90-0027
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	35°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to *analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html*.

Electrical Characteristics

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Supply Voltage Range	$V_{PV\_}$	Fully operational		3.0		5.5	V
Supply Current	I_{PV0}	No load, no switching, V_{EN1} = V_{EN2} = V_{EN3} = V_{EN4} = $V_{PV\_}$		2.5	3.8	5	mA
Shut-Off Current	I_{VPSD}	V_{EN1} = V_{EN2} = V_{EN3} = V_{EN4} = V_{GND}	T_A = +25°C		0.1	2	µA
			T_A = +125°C		2		
Overvoltage Threshold		Rising		5.6	5.8	6	V
		Hysteresis			0.1		
UVLO Threshold		$V_{PV\_}$ falling		2.68			V
		$V_{PV\_}$ falling (MAX20029D)		2.6			
		$V_{PV\_}$ rising				3.0	
PWM Switching Frequency	f_{SW}			2.0	2.2	2.4	MHz

Electrical Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Spread Spectrum	Df/f	Spread-spectrum option = enabled (see the *Selector Guide*)		+3		%
SYNC Input Frequency Range	f_{SYNC}		1.7		2.5	MHz
SYNCHRONOUS STEP-DOWN DC-DC CONVERTERS (OUT1–OUT4)						
Fixed DC Output Accuracy		I_{LOAD} = 0mA		+1.5		%
		I_{LOAD} = 0mA to I_{MAX}	-3		+3	
		I_{LOAD} = 0mA to 1.0A (MAX20029C/MAX20029D)	-3		+3	
		I_{LOAD} = 0mA to 1.0A at +125°C (MAX20029C/MAX20029D)	-3		+3.2	
		I_{LOAD} = 0mA to 1.5A (MAX20029C/MAX20029D)	-3.75		+3	
		I_{LOAD} = 0mA to 1.5A at +125°C (MAX20029C/MAX20029D)	-3.75		+3.2	
		I_{LOAD} = 0mA to 750mA (MAX20029BATIH)	-2		3	
FB DC Set-Point Accuracy	$V_{SFB\_}$	I_{LOAD} = 0mA (MAX20029/MAX20029B)		1015		mV
		I_{LOAD} = 0mA to I_{MAX} (MAX20029/MAX20029B)	970		1030	
Load Regulation		MAX20029 MAX20029B/ MAX20029D (OUT3, OUT4) MAX20029C — Per 1A of load		-1.5		%
		MAX20029B/ MAX20029D (OUT1) — Per 2A of load		-1.5		
Line Regulation		I_{LOAD} = I_{MAX}/2, $V_{PV\_}$ = 4.5V to 5.5V		+0.3		%
pMOS On-Resistance		$V_{PV\_}$ = 5.0V, $I_{LX\_}$ = 0.2A		125	250	mΩ
nMOS On-Resistance		$V_{PV\_}$ = 5.0V, $I_{LX\_}$ = 0.2A		100	200	mΩ

Electrical Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
pMOS Current-Limit Threshold		MAX20029 MAX20029C	OUT1/OUT2, Opt 1 (0.5A channel)	0.8	1.1	1.5	A
		OUT1/OUT2, Opt 2 (1A channel)		1.4	1.65	2	
		OUT1/OUT2, Opt 3 (1.5A channel)		1.85	2.2	2.75	
		MAX20029B/ MAX20029D (OUT1, 2A channel, per LX_ pin)	(see *Selector Guide*)	1.4	1.65	2	
		MAX20029B/ MAX20029D (OUT1, 3A channel, per LX_) pin	(see *Selector Guide*)	1.85	2.2	2.75	
		OUT3/OUT4 (0.5A channel)	(see *Selector Guide*)	0.8	1.1	1.5	
		OUT3/OUT4 (1.5A channel)	(see *Selector Guide*)	1.85	2.2	2.75	
Soft-Start Ramp Time					3272		Cycles
OUTS Leakage Current	$I_{B\_OUTS\_}$	Externally adjustable output			20		nA
OUTS Bias Current		Factory-preset output voltage (MAX20029BATIH)		19.8	22	24.2	µA
LX Leakage Current		$V_{PV\_}$ = 5.0V, LX_ = $V_{PGND\_}$ or $V_{PV\_}$			0.1		µA
Minimum On-Time					45	66	ns
LX Rise/Fall Time					4		ns
Duty-Cycle Range						100	%
OUTS_ Discharge Resistance		$V_{EN\_}$ = V_{GND}			35		Ω
OUT1, OUT2 Phasing		(*Note 2*)			0		Degrees
OUT3, OUT4 Phasing		(*Note 2*)			180		Degrees
THERMAL OVERLOAD							
Thermal-Shutdown Temperature		T_J rising (*Note 3*)			+185		°C
Hysteresis		(*Note 3*)			15		°C
OUTPUT POWER-GOOD INDICATORS (PG1–PG4)							
Output Overvoltage Threshold		V_{OUT} rising (percentage of nominal output)		106	110	114	%

Electrical Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Undervoltage Threshold		V_{OUT} falling (percentage of nominal output)	92.5	94	96	%
		V_{OUT} rising (percentage of nominal output)	93.5	95	97	
		V_{OUT} falling (percentage of nominal output), MAX20029C/MAX20029D	90	94	96	
		V_{OUT} rising (percentage of nominal output), MAX20029C/MAX20029D	90.5	95	96.5	
UV/OV Propagation Delay				15		µs
PG_ Output High Leakage Current				0.1		µA
PG_ Output Low Level		$V_{PV\_}$ = 3.0V, sinking 3mA			0.22	V
Active Timeout Period		Option 1		256		Cycles
		Option 2		20,480		
ENABLE INPUTS (EN1–EN4)						
Input High Level		$V_{PV\_}$ = 5.0V, $V_{EN\_}$ rising	0.7	1.0	1.3	V
Hysteresis		$V_{PV\_}$ = 5.0V, $V_{EN\_}$ falling		50		mV
Pull-Down Resistance				100		kΩ
DIGITAL INTERFACE (SYNC)						
Input Voltage High	V_{INH}		1.5			V
Input Voltage Low	V_{INL}				0.5	V
Input Voltage Hysteresis				70		mV
Pull-Down Resistance				100		kΩ

Note 1: All units are 100% production tested at +25ºC. All temperature limits are guaranteed by design.

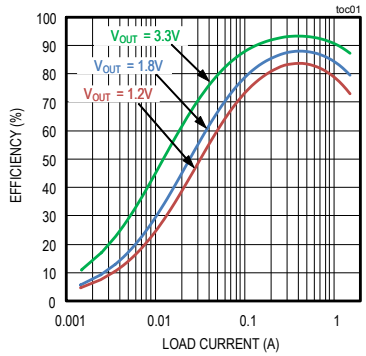
Note 2: Phase measurement is in relation to the rising edge of $V_{LX\_}$.

Note 3: Guaranteed by design. Not production tested.

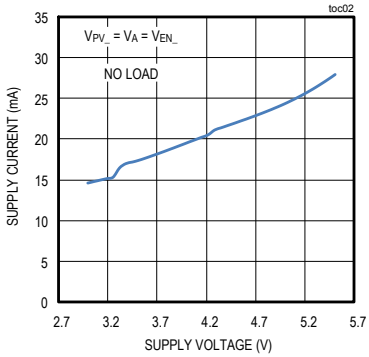
Typical Operating Characteristics

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V; T_A = +25°C, unless otherwise noted.)

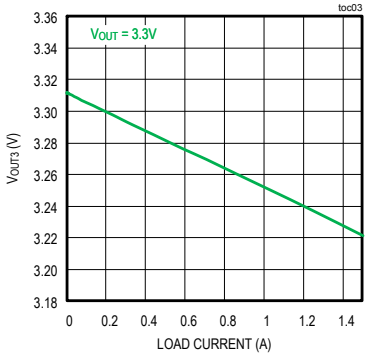
EFFICIENCY CURVE



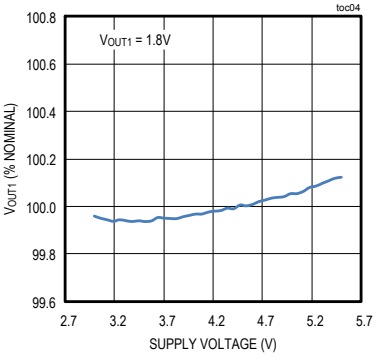
SUPPLY CURRENT



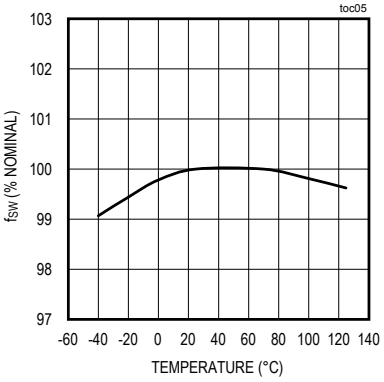
LOAD REGULATION



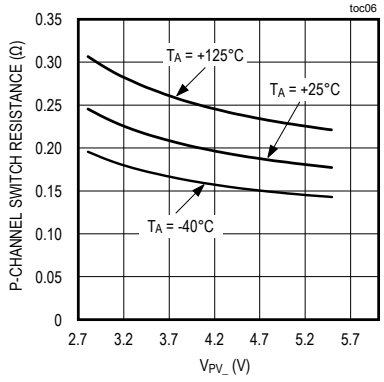
LINE REGULATION



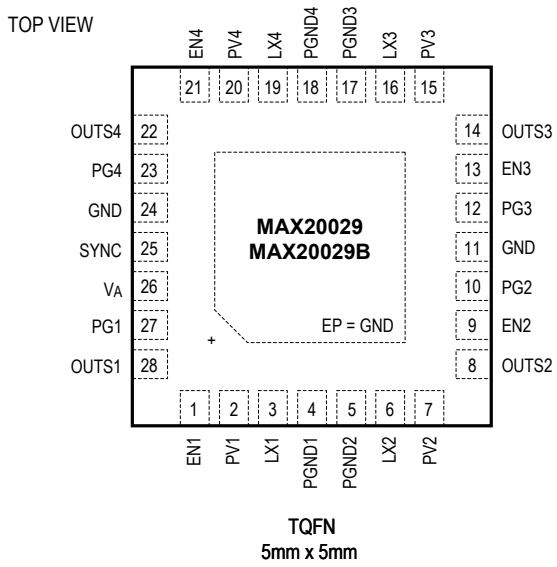
SWITCHING FREQUENCY
vs. TEMPERATURE



P-CHANNEL SWITCH RESISTANCE
vs. SUPPLY VOLTAGE



Pin Configuration



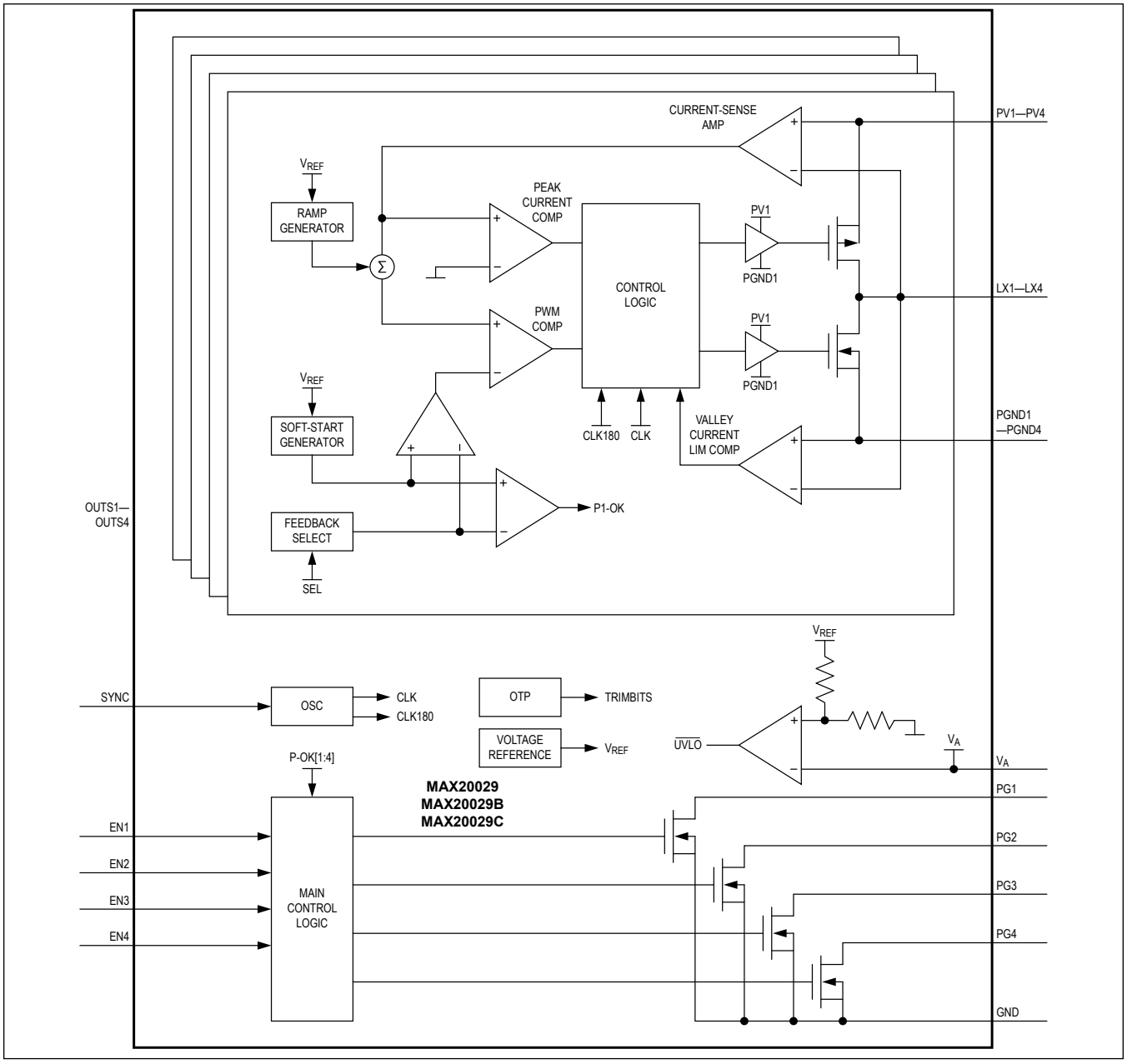
Pin Description

PIN	NAME	FUNCTION
1	EN1	Active-High Digital Enable Input for Buck 1. Driving EN1 high enables Buck 1.
2	PV1	Buck 1 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV1 to PGND1 as close as possible to the device.
3	LX1	Buck 1 Switching Node. LX1 is high impedance when the device is off.
4	PGND1	Power Ground for Buck 1
5	PGND2	Power Ground for Buck 2
6	LX2	Buck 2 Switching Node. LX2 is high impedance when the device is off. Connect to LX1 for the MAX20029B/MAX20029D.
7	PV2	Buck 2 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV2 to PGND2 as close as possible to the device.
8	OUTS2	Buck 2 Voltage-Sense Input. Connect to output capacitor. Connect to ground for the MAX20029B/ MAX20029D.
9	EN2	Active-High Digital Enable Input for Buck 2. Driving EN2 high enables Buck 2. Connect to ground for the MAX20029B/MAX20029D.
10	PG2	Open-Drain, Active-High, Power-Good Output for Buck 2. To obtain a logic signal, pull up PG2 with an external resistor connected to a positive voltage equal to or lower than V_A. Connect to ground for the MAX20029B/MAX20029D.
11	GND	Ground
12	PG3	Open-Drain, Active-High, Power-Good Output for Buck 3. To obtain a logic signal, pull up PG3 with an external resistor connected to a positive voltage equal to or lower than V_A.
13	EN3	Active-High Digital Enable Input for Buck 3. Driving EN3 high enables Buck 3.
14	OUTS3	Buck 3 Voltage Sense Input
15	PV3	Buck 3 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV3 to PGND3 as close as possible to the device.

Pin Description (continued)

PIN	NAME	FUNCTION
16	LX3	Buck 3 Switching Node. LX3 is high impedance when the device is off.
17	PGND3	Power Ground for Buck 3
18	PGND4	Power Ground for Buck 4
19	LX4	Buck 4 Switching Node. LX4 is high impedance when the device is off.
20	PV4	Buck 4 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV4 to PGND4 as close as possible to the device.
21	EN4	Active-High Digital Enable Input for Buck 4. Driving EN4 high enables Buck 4.
22	OUTS4	Buck 4 Voltage Sense Input
23	PG4	Open-Drain, Active-High, Power-Good Output for Buck 4. To obtain a logic signal, pull up PG4 with an external resistor connected to a positive voltage equal to or lower than V_A.
24	GND	Analog Ground
25	SYNC	SYNC Input. Supply an external clock to control the switching frequency. Connect SYNC to PGND_ to use the default switching frequency.
26	V_A	Analog Voltage Supply. Connect a 1µF or larger ceramic capacitor from V_A to GND as close as possible to the device. Connect to the same supply as PV_ inputs.
27	PG1	Open-Drain, Active-High, Power-Good Output for Buck 1. To obtain a logic signal, pull up PG1 with an external resistor connected to a positive voltage equal to or lower than V_A.
28	OUTS1	Buck 1 Voltage Sense Input
—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND1–PGND4 and GND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Internal Block Diagram



Detailed Description

The MAX20029/MAX20029B/MAX20029C/MAX20029D PMICs offer four high-efficiency, synchronous step-down converters that operate with a 3.0V to 5.5V input voltage range and provide a 0.7V to 4.0V output voltage range. The PMICs deliver up to 1.5A of load current per output, and achieve ±3% output error over load, line, and temperature ranges.

The PMICs feature fixed-frequency PWM-mode operation with a 2.2MHz switching frequency. An optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency, while a factory-programmable synchronization input (SYNC) allows the device to synchronize to an external clock.

Integrated low $R_{DS(ON)}$ switches help minimize efficiency losses at heavy loads and reduce critical/parasitic inductance, making the layout a much simpler task with respect to discrete solutions.

The PMICs are offered in factory-preset output voltages to allow customers to achieve ±3% output-voltage accuracy, without using expensive 0.1% resistors. In addition, adjustable output-voltage versions can be set to any desired values between 1.0V and 4.0V using an external resistive divider. See the *Selector Guide* for available options.

Additionally, each converter features soft-start, PG_ output, overcurrent, and overtemperature protections (see the *Internal Block Diagram*).

Control Scheme

The PMICs use peak current-mode control, and feature internal slope compensation and loop compensation, both of which reduce board space and allow a very compact solution.

Hybrid Load-Line Architecture

The PMICs feature hybrid load-line architecture to reduce the output capacitance needed, potentially saving system cost and size. This results in a measurable load-transient response (see Figure 1).

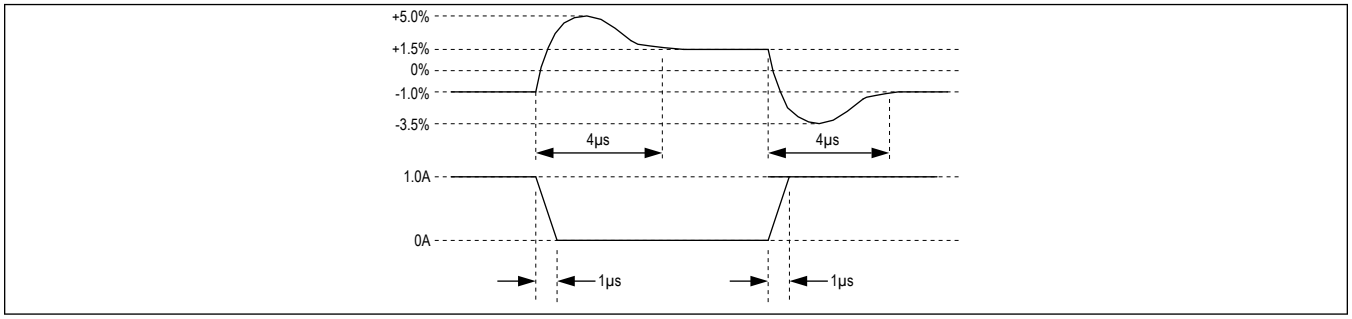


Figure 1. Load-Transient Response

Input Overvoltage Monitoring (OV)

The PMICs feature an input overvoltage-monitoring circuit on the input supply. When the input exceeds 5.8V (typ) all power-good indicators (PG_) go low. When the input supply returns to within the operating range of 5.7V (typ) or less during the timeout period, the power-good indicators go high.

Input Undervoltage Lockout (UVLO)

The PMICs feature an undervoltage lockout on the PV_ inputs set at 2.77V (typ) falling. This prevents loss of control of the device by shutting down all outputs. This circuit is only active when at least one buck converter is enabled.

Power-Good Outputs (PG_)

The PMICs feature an open-drain power-good output for each of the four buck regulators. PG_ asserts low when the output voltage drops 6% below the regulated voltage or 10% above the regulated voltage for approximately 15µs. PG_ remains asserted for a fixed number of switching cycles after the output returns to its regulated voltage. See the *Selector*

Guide for available options. PG_ asserts low during soft-start and in shutdown. PG_becomes high impedance when Buck_ is in regulation. Connect PG_ to a logic supply with a 10kΩ resistor.

Soft-Start

The soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point. During soft-start, the converters operate in skip mode to prevent the outputs from discharging. Expected soft-start time for MAX20029 and MAX20029B is approximately 1.5ms, and approximately 1ms for MAX20029C/MAX20029D (a scaling factor is applied due to the internal voltage reference difference).

Spread-Spectrum Option

The PMICs feature a linear spread-spectrum (SS) operation, which varies the internal operating frequency between f_{SW} and (f_{SW} + 3%). The internal oscillator is frequency modulated at a rate of 1.5kHz with a frequency deviation of 3% (see Figure 2). This function does not apply to an oscillation frequency applied externally through the SYNC pin. Spread spectrum is a factory-selectable option. See the *Selector Guide* for available options.

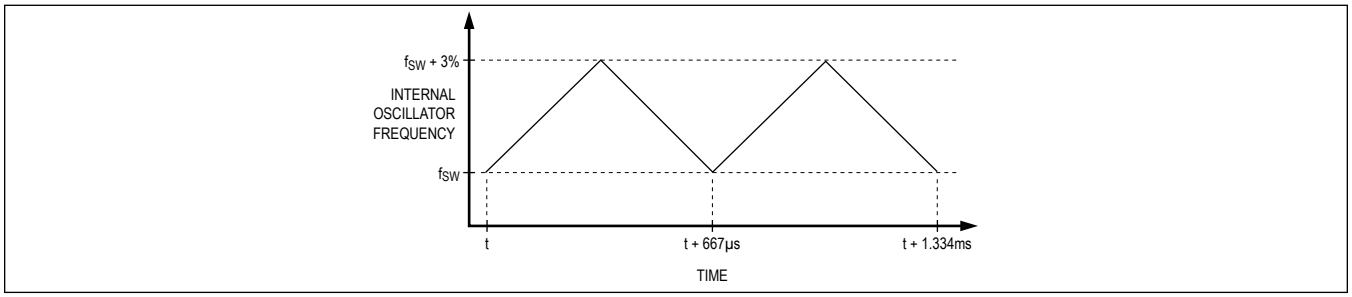


Figure 2. Effect of Spread Spectrum on Internal Oscillator

Synchronization (SYNC)

The PMICs feature a SYNC input to allow the internal oscillator to synchronize with an external clock. SYNC accepts signal frequencies in the range of 1.7MHz < f_{SYNC} < 2.5MHz. Connect to PGND_ if the SYNC feature is not used.

Current-Limit/Short-Circuit Protection

The PMICs offer a current-limit feature that protects the devices against short-circuit and overload conditions on each output. In the event of a short-circuit or overload condition at an output, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET and the inductor current ramps down. The converter allows the high-side MOSFET to turn on only when the inductor current ramps down to the low-side MOSFET's current threshold. This cycle repeats until the short or overload condition is removed.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the PMICs. When the junction temperature exceeds +185°C (typ), an internal thermal sensor shuts down the step-down converters, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C. The IC goes through a standard power-up sequence as defined in the *Soft-Start* section.

Applications Information

Adjustable Output-Voltage Option

The MAX20029/MAX20029B PMICs feature adjustable output voltages (see the *Selector Guide* for more details), which allows the customer to set the outputs to any voltage between 1.0V and $V_{PV\_}$ - 0.5V (up to 4.0V). Connect a resistive divider from output ($V_{OUT\_}$) to OUTS_ to GND to set the output voltage (see Figure 3). Select R2 (OUTS_ to the GND resistor) ≤ 100kΩ. Calculate R1 ($V_{OUT\_}$ to the OUTS_ resistor) with the following equation:

$$R1 = R2[(\frac{V_{OUT\_}}{V_{OUTS\_}}) - 1]$$

where $V_{OUTS\_}$ = 1.0V (see the *Electrical Characteristics* table). The output voltage is nominal at 50% load current.

The external feedback resistive divider must be frequency compensated for proper operation. Place a capacitor across R1 in the resistive divider network. Use the following equation to determine the value of the capacitor:

$$If \frac{R2}{R1} > 1,\ C1 = C(\frac{R2}{R1})$$

else C1 = C, where C = 15pF.

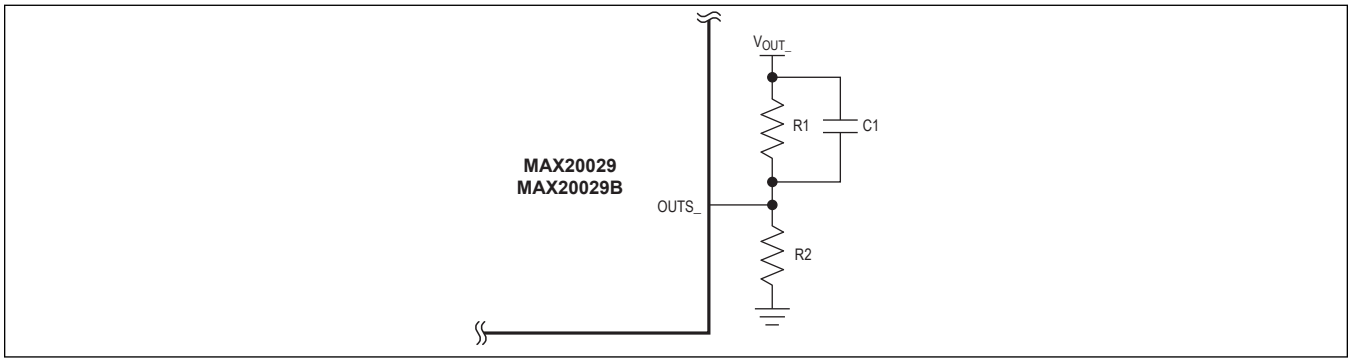


Figure 3. Adjustable Output-Voltage Configuration

Connect OUTS_ to $V_{OUT\_}$ for a fixed 1.0V output voltage.

Inductor Selection

The PMICs are optimized for use with a 1.5µH inductor on outputs configured for 0.5A, 1A, or 1.5A, and a 1.0µH inductor for an output configured for 2A or 3A. For output voltages less than 0.9V, 0.47µH is recommended.

Input Capacitor

The PMICs are designed to operate with a single 2.2µF ceramic bypass capacitor on each PV_ input. Phase interleaving of the four buck converters contributes to a lower required input capacitance by canceling input ripple currents. Place the bypass capacitors as close as possible to their corresponding PV_ input to ensure the best EMI and jitter performance.

Output Capacitor

All outputs of the PMICs are optimized for use with ceramic capacitors.

For $\frac{V_{OUT}}{V_{IN}} > 0.2$:

$$C_{OUT\_MIN} = \frac{20}{V_{OUT}}\mu F$$

$$C_{OUT\_NOM} = \frac{33}{V_{OUT}}\mu F$$

For $\frac{V_{OUT}}{V_{IN}} \le 0.2$:

$$C_{OUT\_MIN} = \frac{40}{V_{OUT}}\mu F$$

$$C_{OUT\_NOM} = \frac{60}{V_{OUT}}\mu F$$

Additional output capacitance can be used if better voltage ripple or load-transient response is required (see Figure 1). To guarantee stability, it is recommended that the phase margin be measured under the worst-case deration of the output capacitor(s). Due to the soft-start sequence, the PMICs are unable to drive arbitrarily large output capacitors.

Thermal Considerations

How much power the package can dissipate strongly depends on the mounting method of the IC to the PCB and the copper area for cooling. Using the JEDEC test standard, the maximum power dissipation allowed is 2285mW in the TQFN package. More power dissipation can be handled by the package if great attention is given during PCB layout. For example, using the top and bottom copper as a heatsink and connecting the thermal vias to one of the middle layers (GND) transfers the heat from the package into the board more efficiently, resulting in lower junction temperature at high power dissipation in some PMIC applications. Furthermore, the solder mask around the IC area on both top and bottom layers can be removed to radiate the heat directly into the air. The maximum allowable power dissipation in the IC is as follows:

$$P_{MAX} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JC} + \theta_{CA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature (+150°C), T_A is the ambient air temperature, θ_{JC} (3°C/W for the 28-pin TQFN) is the thermal resistance from the junction to the case, and θ_{CA} is the thermal resistance from the case to the surrounding air through the PCB, copper traces, and the package materials. θ_{CA} is directly related to system-level variables and can be modified to increase the maximum power dissipation.

The TQFN package has an exposed thermal pad on its underside. This pad provides a low thermal-resistance path for heat transfer into the PCB. This low thermally resistive path carries a majority of the heat away from the IC. The PCB is effectively a heatsink for the IC. The exposed pad should be connected to a large ground plane for proper thermal and electrical performance. The minimum size of the ground plane is dependent upon many system variables. To create an efficient path, the exposed pad should be soldered to a thermal landing, which is connected to the ground plane by thermal vias. The thermal landing should be at least as large as the exposed pad and can be made larger depending on the amount of free space from the exposed pad to the other pin landings. A sample layout is available on the evaluation kit to speed designs.

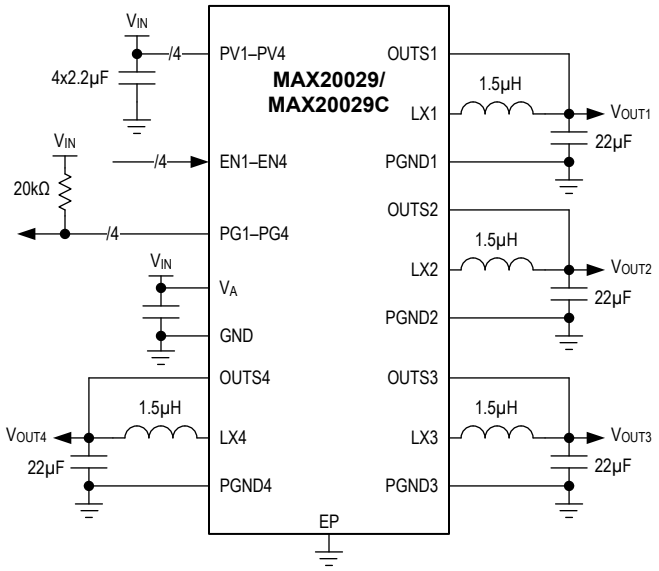
PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

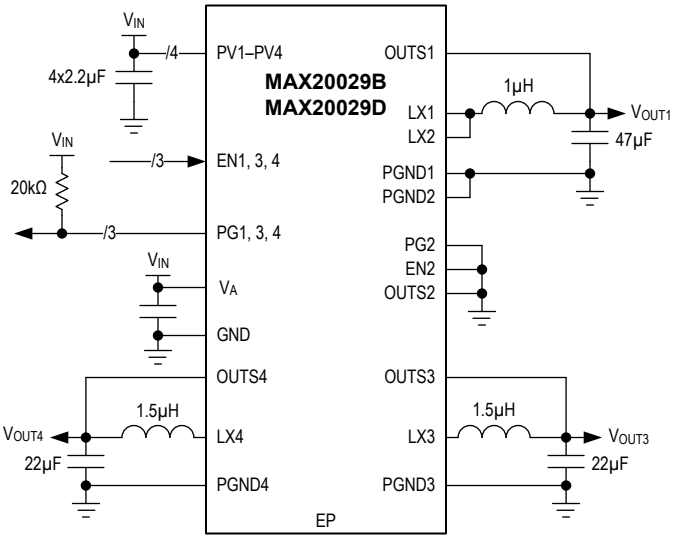
1. Use a large contiguous copper plane under the PMIC packages. Ensure that all heat-dissipating components have adequate cooling.
2. Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, inductor, and the output capacitor should be as short as possible.
3. Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
4. Use a single ground plane to reduce the chance of ground potential differences. With a single ground plane, enough isolation between analog return signals and high-power signals must be maintained.

Typical Operating Circuits

MAX20029/MAX20029C



MAX20029B/MAX20029D



Typical Operating Circuits (continued)

Selector Guide

PART	I_{OUT} (A)				V_{OUT} (V)				SPREAD SPECTRUM	PG_ TIMEOUT (CYCLES)
	CH1	CH2	CH3	CH4	CH1	CH2	CH3	CH4		
MAX20029										
MAX20029ATIA/V+	1.5	1.5	1.5	1.5	ADJ	ADJ	ADJ	ADJ	Off	256
MAX20029ATIB/V+	1.0	1.0	1.5	1.5	1.5	1.8	1.15	1.4	+3%	256
MAX20029ATIC/V+	1.0	1.0	1.5	1.5	1.8	1.35	3.3	1.2	+3%	256
MAX20029ATID/V+	1.0	1.0	1.5	0.5	1.0	1.8	ADJ	3.3	+3%	256
MAX20029ATIF/V+	1.5	1.5	1.5	1.5	1.0	1.8	ADJ	3.3	+3%	256
MAX20029B										
MAX20029BATIA/V+	3.0	—	1.5	1.5	ADJ	—	ADJ	ADJ	Off	20,480
MAX20029BATIB/V+	3.0	—	1.5	1.5	1	—	1.8	1.5	+3%	20,480
MAX20029BATIC/V+	3.0	—	1.5	1.5	1.1	—	1.8	1.0	Off	256
MAX20029BATID/V+	3.0	—	1.5	0.5	1.0	—	1.8	1.2	+3%	256
MAX20029BATIE/V+**	3.0	—	1.5	1.5	1.5	—	1.8	3.3	+3%	256
MAX20029BATIF/V+	3.0	—	1.5	1.5	ADJ	—	ADJ	ADJ	+3%	20,480
MAX20029BATIH/V+	3.0	—	1.5	1.5	1.15	—	3.3	1.8	+3%	20,480
MAX20029C										
MAX20029CATIA/V+	1.5	1.5	1.5	1.5	3.3	1.8	1.0	0.7	Off	256
MAX20029CATIB/V+	1.0	1.0	0.5	1.5	1.5	0.9	1.1	0.7	+3%	256
MAX20029CATIC/V+	1.5	1.5	1.5	1.5	1.8	3.3	0.85	1.8	+3%	256
MAX20029D										
MAX20029DATIA/V+	3.0	—	1.5	1.5	1.1	—	0.7	1.8	Off	20,480

Note: *Contact factory for custom configuration. Factory-selectable features include:*

CH1/CH2 Current Configuration: 0.5A, 1.0A, or 1.5A (both channels have the same current level)
CH3, CH4 Current Configuration: 0.5A or 1.5A
DC-DC Voltages:

- *(MAX20029/MAX20029B) Adjustable, or a fixed voltage between 1.0V and 4.0V in 50mV steps*
- *(MAX20029C) Fixed voltages between 0.7V and 3.8V in 50mV steps*

Spread Spectrum: Off, +3%, or +6%
PG_ Active Timeout Period: 256 or 20,480 clock cycles
CH1 Current Configuration: 2.0A or 3.0A
***Future product—contact factory for availability.*
See the Ordering Information table for other options.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20029ATI_/V+	-40°C to +125°C	28 TQFN-EP*
MAX20029BATI_/V+	-40°C to +125°C	28 TQFN-EP*
MAX20029CATI_/V+	-40°C to +125°C	28 TQFN-EP*
MAX20029DATI_/V+	-40°C to +125°C	28 TQFN-EP*

Note: Insert the desired suffix letter (from the Selector Guide) into the blank area "_" to indicate factory-selectable features.

/V denotes an automotive-qualified part that conforms to AEC-Q100.

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	9/17	Replaced TOCs 1, 2, 3, 4 deleted TOCs 6–9, and renumbered TOC10 to TOC05 and TOC12 to TOC06; added MAX20029ATIC/V+ (as a future product) and MAX20029BATIB/V+ to the Selector Guide	6, 7, 16
2	10/17	Removed future product status from MAX20029ATIC/V+ and added future product status on MAX20029BATIB/V+ in the Selector Guide	15
3	7/18	Updated title, General Description, Benefits and Features, and Detailed Description; updated Electrical Characteristic table, Figure 1, Typical Operating Circuits; added MAX20029BATIC/V+ and MAX20029CATIA/V+ to the Selector Guide and Ordering Information tables as future parts	1–16
4	9/18	Updated General Description, Electrical Characteristics table, Soft-Start, and Output Capacitor. Added MAX20029ATID/V+**, MAX20029BATID/V+**, MAX20029CATIB/ V+** with the accompanying ordering information to the Selector Guide	1, 4, 5, 10, 12, 15
5	9/18	Updated Electrical Characteristics table	4
5.1		Replaced missing rows from bottom of Electrical Characteristics table and future product and Ordering Information footnotes under the Selector Guide, which were omitted in error	5, 16
6	10/18	Added MAX20029BATIE/V+** with the accompanying ordering information and removed future product status from MAX20029CATIA/V+ in the Selector Guide	16
7	1/19	Removed future product status from MAX20029BATID/V+ and MAX20029CATIB/V+, updated CH1 for MAX20029CATIB/V+, and corrected DC-DC Voltages note in the Selector Guide	16
8	2/19	Removed future product status from MAX20029ATID/V+, MAX20029BATIB/V+ and MAX20029BATIC/V+ in the Selector Guide	16
9	3/19	Added MAX20029ATIF/V+ in the Selector Guide	16
10	12/19	Added MAX20029D in the General Description and Benefits and Features, updated Electrical Characteristics table, added MAX20029D in the Pin Description table, Detailed Description and Soft-Start section, updated Inductor Selection, added MAX20029D in the Typical Operating Circuits diagram, Updated Selector Guide and Ordering Information tables by adding new row for MAX20029D	1, 3–6, 8, 11, 13, 15-16
11	2/20	Added MAX20029CATIC/V+** and updated MAX20029DATIA/V+ in Selector Guide	16
12	4/22	Added MAX20029BATIF/V+ and removed ** from MAX20029CATIC/V+ in the Selector Guide	16
13	5/24	Added MAX20029BATIH/V+ in the Selector Guide, updated Electrical Characteristics table, updated land pattern	3, 4, 5, 17