

MAX22193

Product Highlights

- High-Speed, Industrial Digital Inputs
 - 300ns Maximum Propagation Delay
 - · 40ns Maximum Channel-to-Channel Skew
 - · Parallel Output for Simultaneous Signal Delivery
- High Integration Reduces BOM and Space
 - Operates Directly from Field Supply (7V to 65V)
 - Compatible with 3.3V or 5V Logic
 - 4mm x 4mm, 20-TQFN Package
- Low Power and Low Heat Dissipation
 - 1.2mA (max) Quiescent Current with 3.3V Supply
 - Accurate Input Current-Limiters
 - Energyless Field-Side LED Drivers
- Fault Tolerant with Built-In Diagnostics
 - Integrated Field-Side Supply Monitor
 - Integrated Overtemperature Monitor
 - Current-Setting Resistor Monitor
- Configurability Enables Wide Range of Applications
 - Configurable IEC 61131-2 Type 1, 2, and 3 Inputs
 - Input Current Limiting from 1.18mA to 7.01mA
 - Robust Design for Industrial Environments
 - ±2kV Surge Tolerant using 470Ω Resistor (min)
 - ±8kV Contact ESD and ±15kV Air Gap Electrostatic Discharge (ESD) Using 470Ω Resistor (min)
 - -40°C to +125°C Ambient Operating Temperature

Key Applications

- Programmable Logic Controllers (PLC)
- Distributed Control System (DCS)
- Motor Control
- Industrial Automation
- Process Automation

The MAX22193 translates four 24V industrial digital inputs to four CMOS-logic-compatible, parallel outputs. Propagation delay from input-to-output is less than 300ns for all four channels. Current-limiter on each digital input greatly reduces power dissipation compared to traditional resistive input. The accuracy of these current-limiters minimizes power dissipation while ensures compliance with the IEC 61131-2 standard. A current-setting resistor allows the MAX22193 to be configured for Type 1, Type 2 or Type 3 digital inputs. Additionally, the MAX22193 has energyless field-side LED drivers to meet the indicator light requirement of IEC 61131-2 with no additional power dissipation.

Simplified Application Diagram



Pin Configuration



The MAX22193 provides a 3.3V integrated voltage regulator. The internal LDO accepts the field supply V_{DD24} from 7V to 65V. The internal LDO output can supply up to 25mA of current in addition to powering the basic MAX22193 requirements. This LDO can be used to power digital isolators and other field-side circuits. Alternatively, the MAX22193 can be powered from an external 3.0V to 5.5V supply at V_{DD3} .

The MAX22193 includes an open-drain READY output that asserts high to indicate the MAX22193 is functional. If the V_{DD24} field-side supply voltage is too low, or a fault in the current-setting resistor is detected, or the device reaches an over-temperature condition, the READY signal is set to high-impedance.

Ordering Information appears at end of data sheet.

Absolute Maximum Ratings

V _{DD3} to GND	-0.3V to +6V		
V _{DD24} to GND	0.3V to +70V		
OP1-OP4 to GND	0.3V to (V _{DD3} +0.3)V		
IN1-IN4 to GND	40V to +40V		
REFDI to GND	0.3V to (V _{DD3} +0.3)V		
READY, RDYEN to GND	0.3V to +6V		
EXTVM to GND	0.3V to +6V		
LED1-LED4 to GND	0.3V to +6V		
Continuous Power Dissipation (T _A = +70°C)			

Single-layer Board (derate 16.90mW/°C above T _A = +70°C)
Multilayer Board (derate 25.60mW/°C above T _A = +70°C)
Temperature Ratings
Operating Temperature Range40°C to +125°C
Maximum Junction Temperature+150°C
Storage Temperature Range65°C to +150°C
Lead Temperature (soldering, 10s)+300°C
Soldering Temperature (reflow)+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

20-TQFN

Package Code	T2044+3C
Outline Number	<u>21-0139</u>
Land Pattern Number	<u>90-0037</u>
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	59°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	6°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	39°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	6°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to <u>www.maximintegrated.com/thermal-tutorial</u>.

For the latest package outline information and land patterns (footprints), go to <u>www.maximintegrated.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

 $(V_{DD3} = +3.0V \text{ to } +5.5V, C_L \text{ on OP}_ = 15\text{pF}, T_A = -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}, \text{ unless otherwise noted}. Typical values are at V_{DD24} = +24V$, field inputs $V_{IN} = +24V$, $T_A = +25^{\circ}\text{C}$, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
	V _{DD24}	Normal Operation	7		65	
Supply Voltage	V _{DD3}	Powered from an external power supply	3.0		5.5	V
Supply Current Powered from V _{DD24}	I _{DD24}	$V_{DD24} = 24V, V_{IN} = 0V, LED = GND,$ no load on OP		0.6	1.2	mA
Supply Current Powered from V _{DD3}	I _{DD3}	V_{DD3} = 3.3V, V_{DD24} floating, V_{IN} = 0V, LED_ = GND, no load on OP_		0.6	1.2	mA
V _{DD3} Undervoltage- Lockout Threshold	V _{UVLO3}	Powered from V _{DD3} , V _{DD3} rising, V _{DD24} floating	2.4		2.9	V
V _{DD3} Undervoltage- Lockout Threshold Hysteresis	V _{UVHYST3}			0.07		V
V _{DD24} READY	V _{READY_24VR}	V _{DD24} rising, EXTVM = GND	13.8	14.6	15.4	Ň
Threshold	V _{READY_24VF}	V _{DD24} falling, EXTVM = GND	13.3	14.1	15.0	V
V _{DD24} Undervoltage- Lockout Threshold	V _{UVLO24}	V _{DD24} rising	6.0		6.8	V
V _{DD24} Undervoltage- Lockout Threshold Hysteresis	V _{UVHYST24}			0.45		V
Regulator Output Voltage	V _{DD3}	I _{LOAD} = 1mA, V _{DD24} = 7V to 65V	3.0	3.3	3.6	V
Line Regulation	dV _{DDLINE}	I_{LOAD} = 1mA, V_{DD24} = 12V to 24V		0		mV
Load Regulation	dV _{DDLOAD}	I_{LOAD} = 1mA to 10mA, V_{DD24} = 12V		1		mV
Short-Circuit Current Limit	I _{DD24_SC}	I_{DD24} when V_{DD3} short to GND, V_{DD24} = 12V	28	37.5	50	mA
EXTVM MONITOR						
EXTVM Glitch Filter				3		μs
EXTVM Threshold Off- to-On	V _{24TH_OFF_O} N	V _{DD24} rising	0.77	0.81	0.84	V
EXTVM Threshold On- to-Off	V _{24TH_ON_OF} F	V _{DD24} falling	0.74	0.79	0.82	V
External EXTVM Selection Threshold	EXTVM_SEL			0.3		V
External EXTVM Selectable V _{DD24} Threshold	EXTVM_VDD2 4		10		30	v
EXTVM Leakage Current	IEXTVM_L		-1		+1	μA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T _{SHDN}	V _{DD3} internal regulator off		165		°C
Thermal Shutdown Threshold Hysteresis	T _{SHDN_HYS}			10		°C
REFDI SETTINGS						
REFDI Voltage	V _{REFDI}			0.61		V

$(V_{DD3} = +3.0V \text{ to } +5.5V, C_{L} \text{ on } OP_{} = 15pF$, $T_A = -40^{\circ}C$ to +125°C, unless otherwise noted.	Typical values are at V _{DD24} = +24V,	, field
inputs V_{IN} = +24V, T_A = +25°C, unless oth	erwise noted.) (<u>Note 1</u>))		

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Setting Resistance	R _{REFDI}		6	18	36	kΩ
		Increasing current at REFDI pin		550		
REFUI PIN Short	REFDI_5	Decreasing current at REFDI pin		548		μΑ
IC INPUTS (TYPE 1, 2, a	nd 3)	·				
Negative Input Current		$-40V < V_{IN} < 0V$, VIN_ at the pin		100		μA
LED On-State Current	ILED_ON	$R_{REFDI} = 18k\Omega, V_{LED} = 3V$	1.5			mA
DI Leakage, Current Sources Disabled	I _{DI_LEAK}	V _{IN} _= 28V, REFDI floating	40	58	84	μA
Input Threshold Low-to- High	V _{THP+}	V_{IN} at the pin, R_{REFDI} = 18k Ω	5.2	5.6	6	V
Input Threshold High-to- Low	V _{THP-}	V_{IN} at the pin, R_{REFDI} = 18k Ω	4.4	4.7	5.0	V
Input Threshold Hysteresis	VINPHYST	V_{IN} at the pin, R_{REFDI} = 18k Ω		0.9		V
FIELD INPUTS TYPE 1, 3	3: (EXTERNAL S	ERIES RESISOR R _{IN} = 1.5kΩ, R _{REFDI} = 18	3kΩ)			1
Field Input Current Limit	I _{INLIM}	6V (V _{THP+} MAX) ≤ V _{IN} _ at the pin ≤ 28V, LED on, R _{REFDI} = 18kΩ	2.05	2.39	2.75	mA
Field Input Threshold Low-to-High	V _{INF+}	R_{REFDI} = 18kΩ, 1.5kΩ external series resistor			10	V
Field Input Threshold High-to-Low	V _{INF-}	R_{REFDI} = 18kΩ, 1.5kΩ external series resistor	8			V
FIELD INPUTS TYPE 2: (EXTERNAL SERIES RESISOR R_{IN} = 470 Ω , R_{REFDI} = 6k Ω)						
Field Input Current Limit	I _{INLIM}	6V (V _{THP+} MAX) ≤ V _{IN} at the pin ≤ 28V, LED on, R _{REFDI} = 6kΩ	6	7	8.9	mA
Field Input Threshold Low-to-High	V _{INF+}	$R_{REFDI} = 6k\Omega$, 470 Ω external series resistor			10.2	V
Field Input Threshold High-to-Low	V _{INF-}	R_{REFDI} = 6kΩ, 470Ω external series resistor	7.2			V
LOGIC INPUT (RDYEN)						
Input Logic-High Voltage	V _{IH}		0.7 x V _{DD3}			V
Input Logic-Low Voltage	V _{IL}				0.3 x V _{DD3}	V
Input Pulldown Resistance	R _{PD}			199		kΩ
LOGIC OUTPUTS (OP_,	READY)	1				I
Output Logic-High Voltage	V _{OH}	I _{OUT} = -4mA Source	V _{DD3} – 0.4			V
Output Logic-Low Voltage	V _{OL}	I _{OUT} = 4mA Sink			0.4	V
Output Leakage Current	I _{OL}		-1		+1	μA
DYNAMIC CHARACTER	ISTICS (OP_)					
Propagation Delay Low-	ton u	IN_to OP_, $R_{IN} = 470\Omega$, $V_{INF} = 1\overline{1V}$ (<i>Note 2</i>)		85	280	ne
to-High (<u><i>Figure 1</i></u>)		IN_ to OP_, R _{IN} = 470Ω, V _{INF} _ = 36V (<i>Note 2</i>)		85	280	115

High-Speed, Quad, Industrial Digital Input with Parallel Output

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay High-	too	IN_ to OP_, R _{IN} = 470Ω, V _{INF} _ = 11V (<u>Note 2</u>)		150	235	
to-Low (<u>Figure 1</u>)	PDHL	IN_ to OP_, R _{IN} = 470Ω, V _{INF} _ = 36V (<u>Note 2</u>)		150	235	ns
Propagation Delay	topowow ou	IN_ to OP_, R _{IN} = 470Ω, V _{INF} _ = 11V (<u>Note 2</u>)	-20		+20	
Skew Channel-to- Channel (<u>Figure 1</u>)	^{IPDSKEW_CH}	IN_ to OP_, R _{IN} = 470Ω, V _{INF} _ = 36V (<u>Note 2</u>)	-20		+20	ns
Propagation Delay Skew Part-to-Part ^t PDSKEW (<u>Figure 1</u>)	topovou pr	IN_ to OP_, $R_{IN} = 470\Omega$, $V_{INF} = 11V$, all conditions are the same between parts (<i>Note 2</i>)	-200		+200	20
	PDSKEW_PT	IN_ to OP_, $R_{IN} = 470\Omega$, $V_{INF} = 36V$, all conditions are the same between parts (<i>Note 2</i>)	-200		+200	ns
Detectable Pulse Width	tow	IN_ to OP_, R _{IN} = 470Ω, V _{INF} _ = 11V (<u>Note 2</u>)			200	
(<u>Figure 1</u>)	ΨW	IN_ to OP_, R _{IN} = 470Ω, V _{INF} _ = 36V (<u>Note 2</u>)			200	ns
	PWD	t _{PDLH} - t _{PDHL} , V _{INF} = 11V (<u>Note 2</u>)	0	65	180	
Pulse wight Distortion		t _{PDLH} - t _{PDHL} , V _{INF} = 36V (<u>Note 2</u>)	0	65	180	ris

 $(V_{DD3} = +3.0V \text{ to } +5.5V, C_L \text{ on OP}_ = 15pF, T_A = -40^{\circ}C \text{ to } +125^{\circ}C, \text{ unless otherwise noted}. Typical values are at V_{DD24} = +24V$, field inputs $V_{IN} = +24V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (*Note 1*)

Note 1: All parts are production tested at $T_A = +25^{\circ}C$. Specifications over temperature are guaranteed by design.

Note 2: V_{INF} is the voltage measured at the field input; V_{IN} is the voltage measured at the pin.

EMC Characteristics

PARAMETER	SYMBOL	COND	ITIONS	MIN	TYP	MAX	UNITS
		IEC 61000-4-5,	Line-to-Line		±2		
		1.2/50µs pulse,	Line-to-Ground		±2		
Surge minimum 47 resistor in se with IN1–IN4	minimum 470Ω resistor in series with IN1–IN4	V _{DD24}		±1		kV	
ESD		All pins	Human Body Model		±2		
		IEC 61000-4-2, minimum 470Ω resistor in series with IN1–IN4	Contact Discharge		±8		kV
			Air-Gap Discharge		±15		

Timing Diagram



Figure 1. Test Circuit (A) and Timing Diagram (B)

Typical Operating Characteristics

 $(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25^{\circ}C, R_{REFDI} = 18k\Omega \text{ or } 6k\Omega, R_{IN} = 1.5k \text{ or } 470\Omega, unless otherwise noted.})$





 $(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25^{\circ}C, R_{REFDI} = 18k\Omega \text{ or } 6k\Omega, R_{IN} = 1.5k \text{ or } 470\Omega, \text{ unless otherwise noted.})$



 $(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25^{\circ}C, R_{REFDI} = 18k\Omega \text{ or } 6k\Omega, R_{IN} = 1.5k \text{ or } 470\Omega, \text{ unless otherwise noted.})$

High-Speed, Quad, Industrial Digital Input with Parallel Output



 $(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25^{\circ}C, R_{REFDI} = 18k\Omega \text{ or } 6k\Omega, R_{IN} = 1.5k \text{ or } 470\Omega, \text{ unless otherwise noted.})$

Pin Configuration



High-Speed, Quad, Industrial Digital Input with Parallel Output

Pin Description

PIN	NAME	FUNCTION		
20	V _{DD24}	24V Field Supply. Bypass to GND with 0.1 μ F capacitor in parallel with 1 μ F capacitor. If powering V _{DD3} from an external supply, leave V _{DD24} floating.		
2	V _{DD3}	3.3V output from integrated LDO when powered from V _{DD24} , or 3.0 to 5.5V supply input when V _{DD24} not driven. Bypass to GND with a 0.1 μ F capacitor in parallel with a 1 μ F capacitor. If powering V _{DD3} from an external supply, leave V _{DD24} floating. V _{DD3} output is turned off during thermal shutdown.		
1, 15	GND	Ground Return for All Signals and the Power Supplies.		
EP		Exposed Pad. Connect to GND. Solder entire exposed pad area to ground plane with multiple vias for best thermal performance.		
17	EXTVM	Connect EXTVM to GND to use internal thresholds (14V, typ) for V _{DD24} voltage monitoring. Connect EXTVM to external resistive divider to set external thresholds for V _{DD24} voltage monitoring. Connect EXTVM to V _{DD3} to disable V _{DD24} voltage monitoring at the READY pin if the device is powered by V _{DD3} .		
16	REFDI	Digital Input Current Limiting Reference Resistor. For 24V type 1/3 inputs, place an $18k\Omega$ resistor to GND. For type 2 inputs, place a $6k\Omega$ resistor.		
3, 5, 12, 14	IN1 to IN4, respectively	Field Inputs. For 24V type 1/3 inputs, place a $1.5k\Omega$ resistor between the field input and the IN_ pin. For type 2 inputs, place a 470 Ω resistor. Capacitors for filtering should not be connected to the IN_ pins. See the <u>Surge Protection of Field Inputs section</u> for more information.		
4, 6, 11, 13	LED1 to LED4, respectively	Energyless LED Driver Outputs. Connect to GND if LEDs are not used.		
7, 8, 9, 10	OP1 to OP4, respectively OP4. GND. If thermal shutdown is triggered, OP1 to OP4 are high-impedance.			
18	RDYEN	Ready Enable. Has a weak internal pulldown. Assert high to enable the READY output. Cascade the READY signal of multiple devices through a single isolator or a microcontroller input pin by connecting the READY output of each device to the RDYEN input of the next device in the chain. READY from the last device in the chain drives the isolator input or the microcontroller GPI.		
19	READY	 Open-drain Output. Connect a pulldown resistor between READY and GND pin. Assert high to indicate that the device is functional and the outputs are valid. The following conditions must be met for READY to assert high: V_{DD3} is above the UVLO threshold. REFDI is not shorted to GND. MAX22193 is not in thermal shutdown. RDYEN is high. VDD24 is valid if the device is powered by VDD24 and EXTVM is not connected to VDD3. 		

Functional Diagram



Detailed Description

The MAX22193 senses the state (on, high or off, low) of each input (IN1 to IN4). The voltages at the IN_ input pins are compared against internal references to determine whether the sensor is on (logic 1) or off (logic 0). Placing an $18k\Omega$ current-setting resistor between REFDI and GND and a $1.5k\Omega$ resistor in series with each input ensures that the current at the on and off trip points as well as the voltage at the trip points satisfy the requirements of IEC 61131-2 for Type 1/3 inputs (*Figure 2*). The current sunk by each input pin rises linearly with input voltage until the level set by the current-limiter is reached; any voltage increase beyond this point does not increase the input current. Limiting the input current ensures compliance with IEC 61131-2 while significantly reducing power dissipation compared to traditional resistive inputs.

The current-setting resistor R_{REFDI} can be calculated using this equation:

 R_{REFDI} (k Ω , typ) = 42/(I_{INLIM} (mA) - V_{IN} /517 (V/k Ω))

where V_{IN} is 5.6V at the input pin during production test for the typical value of Type 1/3, and Type 2 current limits.

RDYEN and READY Monitor

The READY output is used to signal a logic-side controller that the field-side circuit is working. This allows the controller to distinguish from a valid reading of four low inputs or an invalid reading caused by a field-side fault such as loss of power. The READY output is asserted high when the following five conditions are met: the UVLO voltage threshold for V_{DD3} is exceeded, the V_{DD24} field supply requirement is met as set by internal thresholds or EXTVM external thresholds if enabled, the device is not in thermal shutdown, the current through the REFDI pin is in a normal range, and the RDYEN is high.

Ready Enable RDYEN is used to cascade other READY signals through to a single digital isolation channel or a microcontroller GPI pin. Connect the READY output of one device to the RDYEN input of the next device in the chain. Connect the final READY output to a digital isolator or a microcontroller GPI pin. All READY signals must be high for the final READY signal to go high. READY is an open-drain output, driven to V_{DD3} for a high output and set at high-impedance for a low output. See the <u>Typical Application Circuits</u> section for details.

Outputs OP1 to OP4 are high-impedance only when thermal shutdown is triggered.



Figure 2. Switching Characteristics for IEC 61131-2 Type 1, 2, and 3 24VDC Digital Inputs

External VDD24 Voltage Monitor

The EXTVM input controls how the V_{DD24} field supply affects the READY output. When EXTVM is connected to V_{DD3}, the status of the V_{DD24} field supply becomes a don't-care in the decision to assert READY. This is useful when the MAX22193 is being powered directly from a 3.3V supply on V_{DD3} and V_{DD24} is not in use. When EXTVM is connected to GND, the V_{DD24} must be above the nominal 14V threshold before READY is asserted high. To use a user-defined V_{DD24} supply voltage threshold, use an external resistive divider to apply an analog voltage directly to EXTVM. The voltage at EXTVM must be greater than the threshold, 0.81V (V_{24TH_OFF_ON}) nominal, before READY is asserted high. *Figure 3* shows an example of the V_{DD24} being monitored with the use of external resistive divider to set a nominal threshold before READY is asserted high. Use the following equation to determine the threshold:



 $V_{DD24} = V_{REF} x (1 + (R2/R1))$

Figure 3. User-Defined V_{DD24} Threshold Set by EXTVM and External Resistive Divider

Short Detection at REFDI Pin

Short detection at REFDI pin is implemented by monitoring the current set by the resistor at the REFDI pin. When more than 550µA (typ) current is detected (meaning a short at REFDI), the 2mA minimum input current is not guaranteed; field input low-to-high and high-to-low thresholds are changed, and the READY pin is not asserted.

Energyless LED Drivers

When IN_ is determined to be on, its input current is diverted to the LED_ pin and flows from that pin to GND. Placing a LED between LED_ and GND provides an indication of the input state without increasing overall power dissipation. If the indicator LEDs are not used, connect LED_ to GND.

Type 2 Sensor Inputs

Each channel of the MAX22193 supports the higher current of Type 2 inputs (6mA, min) and the associated power dissipation. The current of the input channel is set to a nominal 7mA by placing a $6k\Omega$ resistor from REFDI to GND. The proper voltage drop across the input resistor is maintained by reducing the resistance from 1.5k Ω to 470 Ω (*Figure 4*).



Figure 4. Implementing Type 2 Digital Inputs with the MAX22193

Thermal Considerations

The MAX22193 operates at an ambient temperature of 125°C on a properly designed multilayer PC board. Operating at higher voltages or with heavy output loads such as optical isolators increases power dissipation and reduces the maximum allowable operating temperature. See <u>Package Information</u> and <u>Absolute Maximum Ratings</u> for safety operation temperature and maximum power dissipation.

The MAX22193 is in thermal shutdown when the thermal shutdown temperature threshold is exceeded. During thermal shutdown, the internal voltage regulator, input channels, REFDI circuitry are all turned off, and outputs OP1 to OP4 are high-impedance.

Applications Information

Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DD24} and V_{DD3} with a 0.1µF low-ESR ceramic capacitor in parallel with 1µF ceramic capacitor to GND, respectively. Place the bypass capacitors as close as possible to the power supply input pins.

Powering MAX22193 with VDD3

The MAX22193 can alternatively be powered using a 3.0V to 5.5V supply connected to the V_{DD3} pin. In this case, a 24V supply is no longer needed, so the V_{DD24} pin must be left unconnected and EXTVM pin connected to V_{DD3} to disable the V_{DD24} voltage monitoring (see the <u>Typical Application Circuits</u> section for details). This configuration has lower power consumption and heat dissipation since the on-chip LDO voltage regulator is disabled (the V_{DD24} undervoltage lockout is below threshold and automatically disables the LDO).

PCB Layout Recommendations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. Avoid using vias on the signals to make low-inductance paths.
- Have a solid ground plane underneath the entire exposed pad (EP) area with multiple thermal vias for best thermal performance.
- In order to achieve the highest EFT performance, it is recommended to have the GND plane around the REFDI traces, and isolate the REFDI traces from all input traces (especially IN4) as much as possible. For example, route input traces and REFDI traces on two different layers and have a GND plane on the inner layers in between.

IEC 61131-2 EMC Requirements

The MAX22193 is required to operate reliably in harsh industrial environments. The device can meet the transient immunity requirements as specified in IEC 61131-2, including electrostatic discharge (ESD) per IEC 61000-4-2 and surge immunity per IEC 61000-4-5. Analog Devices proprietary process technology provides robust input channels and field supply with internal ESD structures and high <u>Absolute Maximum Ratings</u>, but external components are also required to absorb excessive energy from ESD and surge transients. The circuit with external components shown in <u>Figure 5</u> allows the device to meet and exceed the transient immunity requirements as specified in IEC 61131-2 and related IEC 61000-4-x standards. The system shown in <u>Figure 5</u> (using the components shown in <u>Table 1</u>) is designed to be robust against ESD and surge specifications as listed in <u>Table 2</u>. In all these tests, the part or DUT is soldered onto a properly designed application board (e.g., the MAX22193EVKIT#) with necessary external components.

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED
C1	1µF, 100V ceramic capacitor	Required
C2	0.1µF, 100V low-ESR ceramic capacitor	Required
C3	1µF, 10V ceramic capacitor	Required
C4	0.1µF, 10V low-ESR ceramic capacitor	Required
C5	3.3nF, safety rated Y capacitor (2220)	Recommended
D1	Bi-directional TVS diode SMAJ33CA (42Ω) or SM30T39CAY (2Ω)	Recommended
D2	Bi-directional TVS diode SMAJ33CA (42Ω) or SM30T39CAY (2Ω)	Required to pair with R4
D3	Low forward voltage Schottky diode	Recommended
R1	Minimum 470Ω, 2512, 2W pulse withstanding resistor	Required
R2	Minimum 470Ω, 0603, 0.1W resistor	Required
All other resistors	0603, 0.1W resistors	Required
All LEDs	LEDs for visual input status indication	Recommended

Table 1. Recommended Components for EMC Compliance



Figure 5. Typical EMC Protection Circuit for the MAX22193

ESD Protection of Field Inputs

The input resistor limits the energy into the MAX22193 IN_ pins and protects the internal ESD structure from excessive transient energy. An input series resistor is required and should be rated to withstand such ESD levels. The MAX22193 input channels can withstand up to $\pm 8kV$ ESD contact discharge and $\pm 15kV$ ESD air-gap discharge with an input series resistor of 470 Ω or larger. The input resistor value shifts the field voltage switching threshold scaled by the input current; thus, it determines the input characteristics of the application. The package of the resistor should be large enough to prevent the arcing across the two resistor pads. Arcing depends on the ESD level applied to the field input and the application pollution degree.

Surge Protection of Field Inputs

There are two options in order to protect the IN_ pins against $\pm 2kV/42\Omega$, 1.2/50µs surges (*Figure 6* and *Figure 7*). The first option is to use a series pulse-withstanding resistor as shown in the various application diagrams in the data sheet. The pulse resistor should support dissipation of the surge energy. For Type 1/3 digital inputs with 1.5k Ω series resistors, it is recommended to use a CRCW-IF or CRCW-HP thick film resistor or similar to protect against up to $\pm 2kV$ surges. For Type 2 digital inputs with 470 Ω series resistors, it is recommended to use a CRCW-IF or CRCW-HP thick film resistor or similar to protect against up to $\pm 2kV$ surges. For Type 2 digital inputs with 470 Ω series resistors, it is recommended to use a CRCW-IF or CRCW-HP thick film resistor or similar to protect against up to $\pm 2kV$ surges. For Type 2 digital inputs with 470 Ω series resistors, it is recommended to use a CRCW-IF or CRCW-HP thick film resistor or similar to protect against up to $\pm 2kV$ surges.

High-Speed, Quad, Industrial Digital Input with Parallel Output

similar to protect against up to $\pm 1kV$ surge. Use the CMB0207 MELF resistor for $\pm 2kV$ surge protections. Capacitors for filtering should not be connected to the IN_ pins.

The second option, which can result in a smaller overall footprint, is to use a bidirectional TVS to GND at the field input with a low-power series resistor greater than or equal to 470Ω . The TVS must be able to absorb the surge energy and has the function of limiting the peak voltage so that the resistor only sees a low differential voltage. Suitable TVS with a small footprint are SMAJ33CA, offering protection against ±2kV /42\Omega surges.

Surge Protection of 24V Supply

In order to protect the V_{DD24} pin against \pm 1kV/42 Ω , 1.2/50µs surges (*Figure 6*), a SMAJ33CA TVS can be applied to the V_{DD24} pin, along with a series Schottky diode for reverse current protection. To protect against \pm 1kV/2 Ω , 1.2µs/50µs surges, a SM30T39CAY TVS can be applied to the V_{DD24} pin.



Figure 6. 1.2/50µs Surge Voltage Waveform



Figure 7. Surge Testing Method

Table 2. Transient Immunity Test Results

TEST	RESULT	
IEC 61000 1 2 Electrostatic Discharge (ESD)	Contact ESD	±8kV
IEC 61000-4-2 Electrostatic Discharge (ESD)	Air-Gap ESD	±15kV
	Line-to-Ground	±2kV
IEC 61000-4-5 Surge Immunity	Line-to-Line	±2kV
	Power Supply	±1kV

Typical Application Circuits





Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22193ATP+	-40°C to +125°C	20-TQFN
MAX22193ATP+T	-40°C to +125°C	20-TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BICMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/22	Release for Market Intro	_
1	10/23	Updated Product Highlights section, Electrical Characteristics table, Typical Operating Characteristics 13 and 15, Pin Description table, RDYEN and READY Monitor section, External VDD24 Voltage Monitor, Energyless LED Drivers, Thermal Considerations section, Powering MAX22193 with VDD3, IEC 61131-2 EMC Requirements, Surge Protection of Field Inputs.	1, 3–5, 8,12, 14–18,



Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.