*Click **here** to ask an associate for production status of specific part numbers.*

MAX32670

High-Reliability, Ultra-Low-Power Microcontroller Powered by Arm Cortex-M4 Processor with FPU for Industrial and IoT

General Description

In the Darwin family, the MAX32670 is an ultra-low-power, cost-effective, high-reliability 32-bit microcontroller enabling designs with complex sensor processing without compromising battery life. It combines a flexible and versatile power management unit with the powerful Arm® Cortex®-M4 processor with a floating point unit (FPU). It also offers legacy designs an easy and cost-optimal upgrade path from 8- or 16-bit microcontrollers.

The device integrates 384KB (376KB user) of flash memory and 160KB of SRAM to accommodate application and sensor code. Additional features, such as the two windowed watchdog timers with fully flexible and independent clocking, have been added to further enhance reliable operation. Brown-out detection ensures proper operation during power-down/power-up events and unexpected supply transients.

Multiple high-speed peripherals such as 3.4MHz I^2C, 50MHz SPI, and UARTs maximize communication bandwidth. In addition, a low-power UART is available for operation in the lowest-power sleep modes to facilitate wake-up on activity without any loss of data. A total of six timers with I/O capability are provided, including two low-power timers to enable pulse counting, capture/compare, and PWM generation in the lowest-power sleep modes. All of this capability is packaged in a tiny form factor: 5mm x 5mm, 40-pin TQFN-EP or 1.75mm x 2.50mm, 24-bump WLP.

Applications

- Smart Sensor Controller
- Industrial Sensors
- Optical Communication Modules
- Secure Radio Modem Controller
- Battery-Powered Medical Devices
- System Housekeeping Controller
- Algorithm Coprocessor

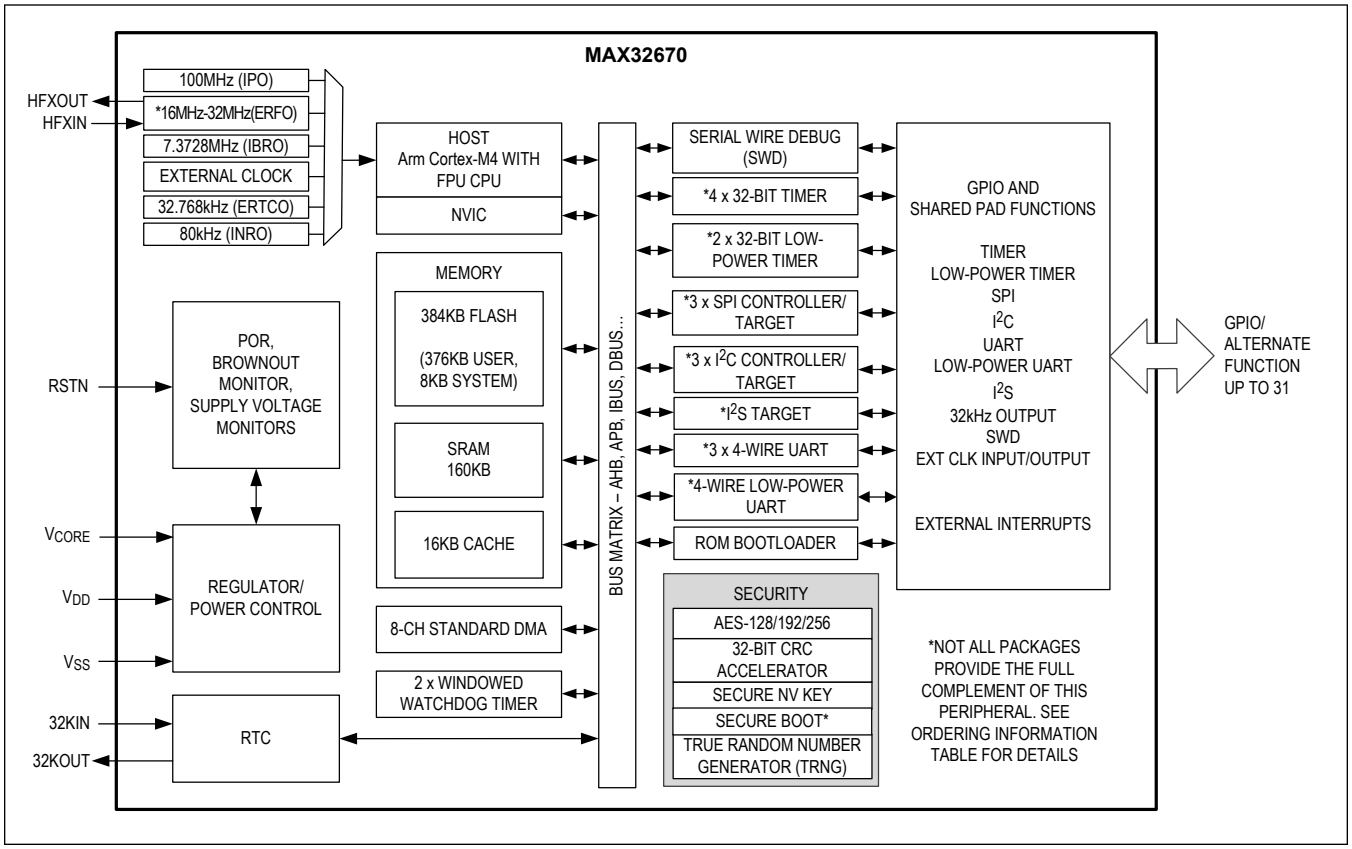
Ordering Information appears at end of data sheet.

Benefits and Features

- High-Efficiency Microcontroller for Low-Power, High-Reliability Devices
  - Arm Cortex-M4 Core with FPU up to 100MHz
  - 384KB (376KB User) of Flash Memory
  - 160KB SRAM, Optionally Preserved in Lowest Power Modes
  - 16KB Unified Cache
  - Dual- or Single-Supply Operation
    - Ultra-Low 0.9V to 1.1V V_{CORE} Supply Voltage
    - Internal LDO Operation from 1.7V to 3.6V Single Supply
- Flexible Clocking Schemes
  - Internal High-Speed 100MHz Oscillator
  - Internal Low-Power 7.3728MHz and Ultra-Low-Power 80kHz Oscillators
  - 16MHz to 32MHz Oscillator (External Crystal Required)
  - 32.768kHz Oscillator (External Crystal Required)
  - External Clock Input for the Core
  - External Clock Input for the LPUART and LPTMR
- Power Management Maximizes Uptime for Battery Applications
  - 44µA/MHz ACTIVE Mode at 0.9V up to 12MHz
  - 50µA/MHz ACTIVE Mode at 1.1V up to 100MHz
  - 2.6µA Maximum Memory Retention Current in BACKUP Mode at V_{DD} = 1.8V
  - 350nA Ultra-Low-Power RTC at V_{DD} = 1.8V
  - Wake from LPUART or LPTMR
- Optimal Peripheral Mix Provides Platform Scalability
  - Up to 31 General-Purpose I/O Pins
  - Up to Three SPI Controller/Target (up to 50MHz)
  - Up to Three 4-Wire UART
  - Up to One Low-Power UART (LPUART)
  - Up to Three I^2C Controller/Target 3.4Mbps High Speed
  - 8-Channel Standard DMA Controller
  - Up to Four 32-Bit Timers (TMR)
  - Up to Two Low-Power 32-Bit Timers (LPTMR)
  - Two Windowed Watchdog Timers
  - Up to One I^2S Controller/Target for Digital Audio
- Robust Security and Reliability
  - UART ROM Bootloader
  - True Random Number Generator (TRNG)
  - AES 128/192/256 Hardware Acceleration Engine
  - Secure Nonvolatile Key Storage
  - 32-Bit CRC Acceleration Engine
  - Wide, -40°C to +105°C Operating Temp Range

19-100782; Rev 5; 4/24

Simplified Block Diagram



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Absolute Maximum Ratings

(All voltages with respect to V_{SS}, unless otherwise noted.).....
V_{CORE} ..... -0.3V to +1.21V
V_{DD} ..... -0.3V to +3.63V
HFXIN, HFXOUT ..... -0.2V to V_{CORE}V
32KIN, 32KOUT, RSTN, GPIO ..... -0.3V to V_{DD} + 0.3V
Total Current into All GPIO Combined (sink) 100mA
V_{SS} 100mA
Output Current (sink) by Any GPIO Pin 25mA
Output Current (source) by Any GPIO Pin ..... -25mA

Continuous Package Power Dissipation 40 TQFN-EP (multilayer board) T_A = +70°C (derate 35.7mW/°C above +70°C) 2857.10mW
Continuous Package Power Dissipation 24 WLP (multilayer board) T_A = +70°C (derate 18.85mW/°C above +70°C) ..1.51mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +125°C
Soldering Temperature (reflow) ..... +260°C

Note: No device pin can exceed +3.6V. All voltages with respect to V_{SS}, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 WLP

Package Code	W241A2+1
Outline Number	21-100625
Land Pattern Number	Refer to *Wafer-Level Packaging (WLP) and Its Applications*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	53.04°C/W
Junction to Case (θ_{JC})	N/A

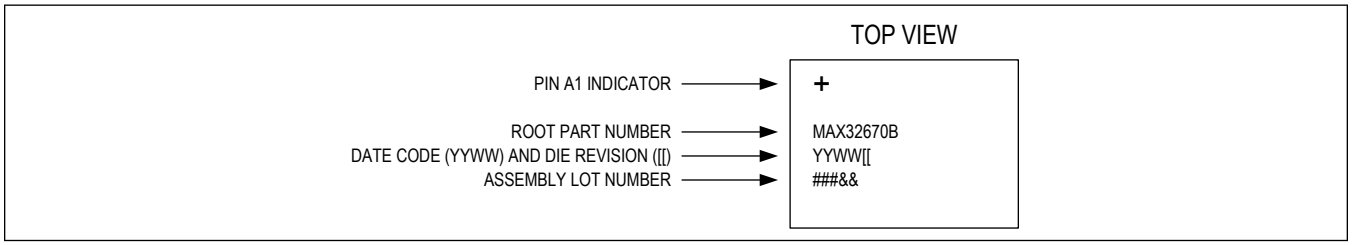


Figure 1. Example 24 WLP Top Marking

40 TQFN-EP

Package Code	T4055+1
Outline Number	21-0140
Land Pattern Number	90-0016
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	45°C/W
Junction to Case (θ_{JC})	2°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	2°C/W

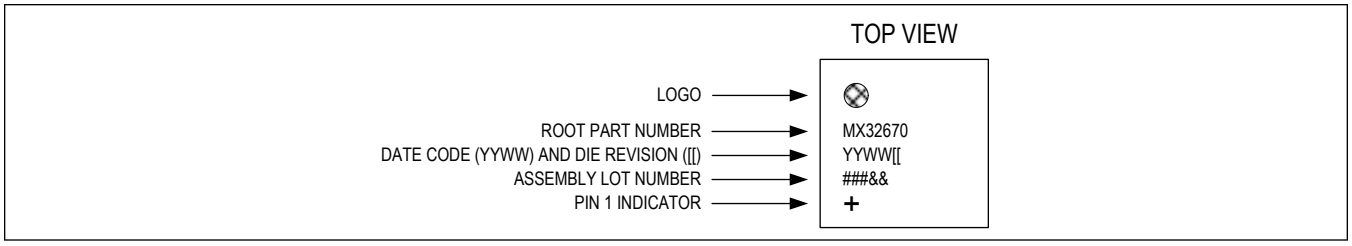


Figure 2. Example 40 TQFN-EP Top Marking

For the latest package outline information and land patterns (footprints), go to the Package Index on the Analog Devices website. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to Thermal Characterization of IC Packages.

Electrical Characteristics

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER / BOTH SINGLE-SUPPLY OPERATION AND DUAL-SUPPLY OPERATION (See *Bypass Capacitor Recommendations*.)							
Supply Voltage	V_{DD}	Decay time of the V_{DD} supply from $V_{DD\_RST(MIN)}$ to 1.47V must be greater than 100µs		1.71	1.8	3.63	V
Supply Voltage, Core	V_{CORE}	Dual-supply operation	OVR = [00]	0.855	0.9	0.945	V
			OVR = [01]	0.95	1.0	1.05	
			Default OVR = [10]	1.045	1.1	1.155	
		No power supply connection for single-supply operation			—		
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD}		1.58		1.71	V
		Monitors V_{CORE} during dual-supply operation		0.77		0.845	
Power-on-Reset Voltage	V_{POR}	Monitors V_{DD}			1.4		V
		Monitors V_{CORE} during dual-supply operation			0.58		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER / SINGLE-SUPPLY OPERATION (V_{DD} ONLY) (See *Bypass Capacitor Recommendations*.)							
V_{DD} Current ACTIVE Mode	I_{DD_DACTS}	Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing CoreMark®, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		57.5		µA/MHz
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		55.7		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		52.2		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		56.9		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		55.3		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		52		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing while(1), inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		43		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		40.7		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		37.5		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing while(1), inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		42.4		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		40.5		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		38.2		
	I_{DD_FACTS}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V. See *Temperature Variance*.		735		µA
			OVR = [01], internal regulator set to 1.0V. See *Temperature Variance*.		659		
			OVR = [00], internal regulator set to 0.9V. See *Temperature Variance*.		563		
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V. See *Temperature Variance*.		754		
			OVR = [01], internal regulator set to 1.0V. See *Temperature Variance*.		663		
			OVR = [00], internal regulator set to 0.9V. See *Temperature Variance*.		538		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Current SLEEP Mode	I_{DD_DSLPS}	Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		30		µA/MHz
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		28.8		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		28.0		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		36.4		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		28.5		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		28.1		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, DMA disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		13.4		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		11.8		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		10.6		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, DMA disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		14.6		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		11.7		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		10.5		
	I_{DD_FSLPS}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V. See *Temperature Variance*.		735		µA
			OVR = [01], internal regulator set to 1.0V. See *Temperature Variance*.		659		
			OVR = [00], internal regulator set to 0.9V. See *Temperature Variance*.		563		
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V. See *Temperature Variance*.		754		
			OVR = [01], internal regulator set to 1.0V. See *Temperature Variance*.		633		
			OVR = [00], internal regulator set to 0.9V. See *Temperature Variance*.		538		
V_{DD} Fixed Current, DEEPSLEEP Mode	I_{DD_FDSLPS}	Standby state with full data retention and 160KB SRAM retained	V_{DD} = 3.3V. See *Temperature Variance*.		4.0		µA
			V_{DD} = 1.8V. See *Temperature Variance*.		3.7		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Fixed Current, BACKUP Mode	I_{DD_FBKUS}	V_{DD} = 3.3V, RTC disabled	0KB SRAM retained, retention regulator disabled. See *Temperature Variance*.		0.38		µA
			20KB SRAM retained. See *Temperature Variance*.		1.08		
			40KB SRAM retained. See *Temperature Variance*.		1.4		
			80KB SRAM retained. See *Temperature Variance*.		1.9		
			160KB SRAM retained. See *Temperature Variance*.		2.8		
		V_{DD} = 1.8V, RTC disabled	0KB SRAM retained, retention regulator disabled. See *Temperature Variance*.		0.15		
			20KB SRAM retained. See *Temperature Variance*.		0.86		
			40KB SRAM retained. See *Temperature Variance*.		1.2		
			80KB SRAM retained. See *Temperature Variance*.		1.7		
			160KB SRAM retained. See *Temperature Variance*.		2.58		
V_{DD} Fixed Current, STORAGE Mode	I_{DD_FSTOS}	V_{DD} = 3.3V. See *Temperature Variance*.			0.3		µA
		V_{DD} = 1.8V. See *Temperature Variance*.			0.11		
SLEEP Mode Resume Time	t_{SLP_ONS}	Time from power mode exit to execution of first instruction			2.1		µs

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DEEPSLEEP Mode Resume Time	t_{DSL_ONS}	fast_wk_en = 1, time from power mode exit to execution of first instruction		89		µs
		fast_wk_en = 0, time from power mode exit to execution of first instruction		129		
BACKUP Mode Resume Time	t_{BKU_ONS}	Time from power mode exit to execution of first instruction		1.25		ms
STORAGE Mode Resume Time	t_{STO_ONS}	Time from power mode exit to execution of first instruction		1.5		ms

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER / DUAL-SUPPLY OPERATION (V_{DD} AND V_{CORE}) (See *Bypass Capacitor Recommendations*.)							
V_{CORE} Current, ACTIVE Mode	I_{CORE_DACTD}	Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		56.7		µA/MHz
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		55.3		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		48.9		
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing while(1), inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		42.2		
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		40.5		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		35.7		
	I_{CORE_FACTD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V. See *Temperature Variance*.		311		µA
			OVR = [01], V_{CORE} = 1.0V. See *Temperature Variance*.		209		
			OVR = [00], V_{CORE} = 0.9V. See *Temperature Variance*.		106		
	I_{DD_DACTD}	Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 100MHz		0.449		µA/MHz
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 50MHz		0.457		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 12MHz		0.473		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing CoreMark, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 100MHz		0.209		
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 50MHz		0.214		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 12MHz		0.233		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing while(1), inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 100MHz		0.448		
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 50MHz		0.456		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 12MHz		0.474		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing while(1), inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 100MHz		0.207		
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 50MHz		0.214		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 12MHz		0.226		
	I_{DD_FACTD}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V. See *Temperature Variance*.		391		µA
			OVR = [01], V_{CORE} = 1.0V. See *Temperature Variance*.		390		
			OVR = [00], V_{CORE} = 0.9V. See *Temperature Variance*.		387		
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V. See *Temperature Variance*.		372		
			OVR = [01], V_{CORE} = 1.0V. See *Temperature Variance*.		372		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			OVR = [00], V_{CORE} = 0.9V. See *Temperature Variance*		369		
V_{CORE} Current, SLEEP Mode	I_{CORE_DSLPD}	Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		29.8		µA/MHz
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		28.7		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		26.3		
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, DMA disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		13.0		
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		11.7		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		9.0		
	I_{CORE_FSLPD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR [10], V_{CORE} = 1.1V. See *Temperature Variance*.		311		µA
			OVR [01], V_{CORE} = 1.0V. See *Temperature Variance*.		209		
			OVR [00], V_{CORE} = 0.9V. See *Temperature Variance*.		106		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Current, SLEEP Mode	I_{DD_DSLPD}	Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		0.001		µA/MHz
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		0.001		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		0.001		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		0.001		
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		0.001		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		0.001		
	I_{DD_FSLPD}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V. See *Temperature Variance*.		391		µA
			OVR = [01], V_{CORE} = 1.0V. See *Temperature Variance*.		390		
			OVR = [00], V_{CORE} = 0.9V. See *Temperature Variance*.		387		
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V. See *Temperature Variance*.		372		
			OVR = [01], V_{CORE} = 1.0V. See *Temperature Variance*.		372		
			OVR = [00], V_{CORE} = 0.9V. See *Temperature Variance*.		369		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CORE} Fixed Current, DEEPSLEEP Mode	I_{CORE_FDSLPD}	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		10.5		µA
		V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		4		
		V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		10.5		
		V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		4		
V_{DD} Fixed Current, DEEPSLEEP Mode	I_{DD_FDSLPD}	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.36		µA
		V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.36		
		V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.149		
		V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.149		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CORE} Fixed Current, BACKUP Mode	I_{CORE_FBKUD}	0KB SRAM retained, RTC disabled, retention regulator disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.3		μA
			V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.19		
			V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.297		
			V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.187		
		20KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		1.37		
			V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.6		
			V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		1.37		
			V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.6		
		40KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		2.39		
			V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.99		
			V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		2.39		
			V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.99		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		80KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		4.15		
			V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		1.6		
			V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		4.15		
			V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		1.6		
		160KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		7.4		
			V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		2.7		
			V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		7.4		
			V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		2.7		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Fixed Current, BACKUP Mode	I_{DD_FBKUD}	0KB SRAM retained with RTC disabled, retention regulator disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.36		µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.36		
			V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.15		
			V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.15		
		20KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.36		
			V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.36		
			V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.15		
			V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.15		
		40KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.36		
			V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.36		
			V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.15		
			V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.15		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		80KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.36		
			V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.36		
			V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.15		
			V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.15		
		160KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.36		
			V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.36		
			V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.		0.15		
			V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.		0.15		
V_{CORE} Fixed Current, STORAGE Mode	I_{CORE_FSTOD}	V_{DD} = 3.3V, V_{CORE} = 1.1V. See *Temperature Variance*.			0.25		µA
		V_{DD} = 3.3V, V_{CORE} = 0.855V. See *Temperature Variance*.			0.14		
		V_{DD} = 1.8V, V_{CORE} = 1.1V. See *Temperature Variance*.			0.25		
		V_{DD} = 1.8V, V_{CORE} = 0.855V. See *Temperature Variance*.			0.14		
V_{DD} Fixed Current, STORAGE Mode	I_{DD_FSTOD}	V_{DD} = 3.3V; V_{CORE} = 1.1V. See *Temperature Variance*.			0.32		µA
		V_{DD} = 3.3V; V_{CORE} = 0.855V. See *Temperature Variance*.			0.31		
		V_{DD} = 1.8V; V_{CORE} = 1.1V. See *Temperature Variance*.			0.11		
		V_{DD} = 1.8V; V_{CORE} = 0.855V. See *Temperature Variance*.			0.11		

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SLEEP Mode Resume Time	t_{SLP_OND}			2.1		µs
DEEPSLEEP Mode Resume Time	t_{DSL_OND}	fast_wk_en = 1, time from power mode exit to execution of first instruction		81		µs
		fast_wk_en = 0, time from power mode exit to execution of first instruction		129		
BACKUP Mode Resume Time	t_{BKU_OND}	Time from power mode exit to execution of first instruction		1.25		ms
STORAGE Mode Resume Time	t_{STO_OND}	Time from power mode exit to execution of first instruction		1.5		ms
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO, RSTN	V_{IL_GPIO}	Pin configured as GPIO			0.3 × V_{DD}	V
Input High Voltage for All GPIO, RSTN	V_{IH_GPIO}	Pin configured as GPIO	0.7 × V_{DD}			V
Output Low Voltage for All GPIO Except P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V_{OL_GPIO}	V_{DD} = 1.71V, I_{OL} = 1mA, DS[1:0] = 00 (*Note 1*)		0.2	0.4	V
		V_{DD} = 1.71V, I_{OL} = 2mA, DS[1:0] = 10 (*Note 1*)		0.2	0.4	
		V_{DD} = 1.71V, I_{OL} = 4mA, DS[1:0] = 01 (*Note 1*)		0.2	0.4	
		V_{DD} = 1.71V, I_{OL} = 6mA, DS[1:0] = 11 (*Note 1*)		0.2	0.4	
Output Low Voltage for GPIO P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V_{OL_I2C}	V_{DD} = 1.71V, I_{OL} = 2mA, DS = 0 (*Note 1*)		0.2	0.4	V
		V_{DD} = 1.71V, I_{OL} = 10mA, DS = 1 (*Note 1*)		0.2	0.4	
Output High Voltage for All GPIO Except P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V_{OH_GPIO}	V_{DD} = 1.71V, I_{OH} = 1mA, DS[1:0] = 00 (*Note 1*)	V_{DD} - 0.4			V
		V_{DD} = 1.71V, I_{OH} = 2mA, DS[1:0] = 10 (*Note 1*)	V_{DD} - 0.4			
		V_{DD} = 1.71V, I_{OH} = 4mA, DS[1:0] = 01 (*Note 1*)	V_{DD} - 0.4			
		V_{DD} = 1.71V, I_{OH} = 6mA, DS[1:0] = 11 (*Note 1*)	V_{DD} - 0.4			
Output High Voltage for GPIO P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V_{OH_I2C}	V_{DD} = 1.71V, I_{OH} = 2mA, DS = 0 (*Note 1*)	V_{DD} - 0.4			V
		V_{DD} = 1.71V, I_{OH} = 10mA, DS = 1 (*Note 1*)	V_{DD} - 0.4			
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				100	mA
Combined I_{OH}, All GPIO	I_{OH_TOTAL}		-100			mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input/Output Pin Capacitance for All Pins	C_{IO}			4		pF

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current Low	I_{IL}	V_{IN} = 0V, internal pull-up disabled	-500		+500	nA
Input Leakage Current High	I_{IH}	V_{IN} = 3.6V, internal pull-down disabled	-500		+500	nA
Input Pull-Up Resistor to RSTN	R_{PU_VDD}	Pull up to V_{DD} = V_{RST}, RSTN at V_{IH}		18.7		kΩ
		Pull up to V_{DD} = 3.63V, RSTN at V_{IH}		10.0		
Input Pull-Up Resistor for All GPIO	R_{PU}	Device pin configured as GPIO, pull up to V_{DD} = V_{RST}, device pin at V_{IH}		18.7		kΩ
		Device pin configured as GPIO, pull up to V_{DD} = 3.63V, device pin at V_{IH}		10.0		
Input Pull-Down Resistor for All GPIO	R_{PD}	Device pin configured as GPIO, pull down to V_{SS}, V_{DD} = V_{RST}, device pin at V_{IL}		17.6		kΩ
		Device pin configured as GPIO, pull down to V_{SS}, V_{DD} = 3.63V, device pin at V_{IL}		8.8		
RSTN Assertion Time	t_{RSTN}	Device in ACTIVE mode, RSTN device pin assertion duration to entry into device reset state.		6 x t_{SYS_CLK}		µs
CLOCKS						
System Clock Frequency	f_{SYS_CLK}				100	MHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS\_CLK}$		µs
IPO Frequency	f_{IPO}	PWRSEQ_LPCN.ovr = 0b10 (default)		100		MHz
IBRO Frequency	f_{IBRO}			7.3728		MHz
INRO Frequency	f_{INRO}	Measured at V_{DD} = 1.8V		80		kHz
ERFO Frequency	f_{ERFO}	The oscillator supports a crystal or external square-wave input between 16 and 32MHz. Required crystal characteristics: C_{L_XTAL} = 12pF, ESR ≤ 50Ω, C_0 ≤ 7pF, crystal maximum power dissipation ≥ 100µW, refer to the *MAX32670 User Guide* for calculating the load capacitors		16–32		MHz
ERTCO Frequency	f_{ERTCO}	32.768kHz watch crystal or external square-wave input. Required crystal characteristics: C_{L_XTAL}= 6pF, ESR < 90kΩ, C_0 < 2pF, crystal maximum power dissipation ≥ 0.5µW, see *RTC Crystal Guidelines*, no load capacitors required		32.768		kHz
External Clock Input Frequency	f_{EXT_CLK}	External square-wave input on P0.12, EXT_CLK1 (AF4) selected			50	MHz
		External square-wave input on P0.12, EXT_CLK2 (AF2) selected			1	
RTC Operating Current	I_{RTC}	Measured on V_{DD}, V_{DD} = 1.8V, ERTCO enabled with external crystal, RTC_CTRL.en = 1, all power modes, both single- and dual-supply operation		0.35		µA

Electrical Characteristics (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ERTCO Startup Time	$t_{RTC\_ ON}$	PWRSEQ_LPCN.ertco_en = 1 to GCR_CLKCTRL.ertco_rdy = 1		250		ms
Input Low Voltage 32KIN	V_{IL_32K}	External square-wave input on 32KIN pin, crystal bypass mode		0.3 x V_{DD}		V
Input High Voltage 32KIN	V_{IH_32K}	External square-wave input on 32KIN pin, crystal bypass mode		0.7 x V_{DD}		V
Input Low Voltage EXT_CLK1, EXT_CLK2	$V_{IL\_EXT\_CLK}$	External square-wave input on P0.12, EXT_CLK1 (AF4) or EXT_CLK2 (AF2) selected			V_{IL_GPIO}	V
Input High Voltage EXT_CLK1, EXT_CLK2	$V_{IH\_EXT\_CLK}$	External square-wave input on P0.12, EXT_CLK1 (AF4) or EXT_CLK2 (AF2) selected	V_{IH_GPIO}			V
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		30		ms
	t_{P_ERASE}	Page erase		30		
Flash Programming Time per Word	t_{PROG}	32-bit programming mode, f_{FLC_CLK} = 1MHz		42		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +125°C	10			years
Current Consumption During Flash Programming	I_{PROG}	Measured on V_{DD}, current required for flash write/erase		6.5		mA

Electrical Characteristics—SPI

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROLLER MODE						
SPI Controller Operating Frequency	f_{MCK}	f_{SYS_CLK} = 100MHz, $f_{MCK(MAX)} = f_{SYS\_CLK}/2$			50	MHz
SPI Controller SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCK}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns

Electrical Characteristics—SPI (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TARGET MODE						
SPI Target Operating Frequency	f_{SCK}				50	MHz
SPI Target SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs
MISO Hold Time After SSx Deassertion	t_{SLH}			10		ns

Electrical Characteristics—I²C

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD-MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns

Electrical Characteristics—I²C (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$				3.45	µs
Data Valid Acknowledge Time	$t_{VD;ACK}$				3.45	µs
FAST-MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$				0.9	µs
Data Valid Acknowledge Time	$t_{VD;ACK}$				0.9	µs
FAST-MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs

Electrical Characteristics—I²C (continued)

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$				0.45	µs
Data Valid Acknowledge Time	$t_{VD;ACK}$				0.45	µs

Electrical Characteristics—I²S Target

(All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Clock Frequency	f_{BCLK}	96kHz LRCLK frequency			3.072	MHz
BCLK High Time	t_{WBCLKH}			0.5		$1/f_{BCLK}$
BCLK Low Time				0.5		$1/f_{BCLK}$
LRCLK Setup Time	t_{LRCLK_BLCK}			25		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDO}			12		ns
Setup Time for SD (Input)	t_{SU_SDI}			6		ns
Hold Time SD (Input)	t_{HD_SDI}			3		ns

GPIO Drive Strength: **Note 1:** When using a GPIO bias voltage of 2.97V, the drive current capability of the GPIO is 2x that of its drive strength when using a GPIO bias voltage of 1.71V.

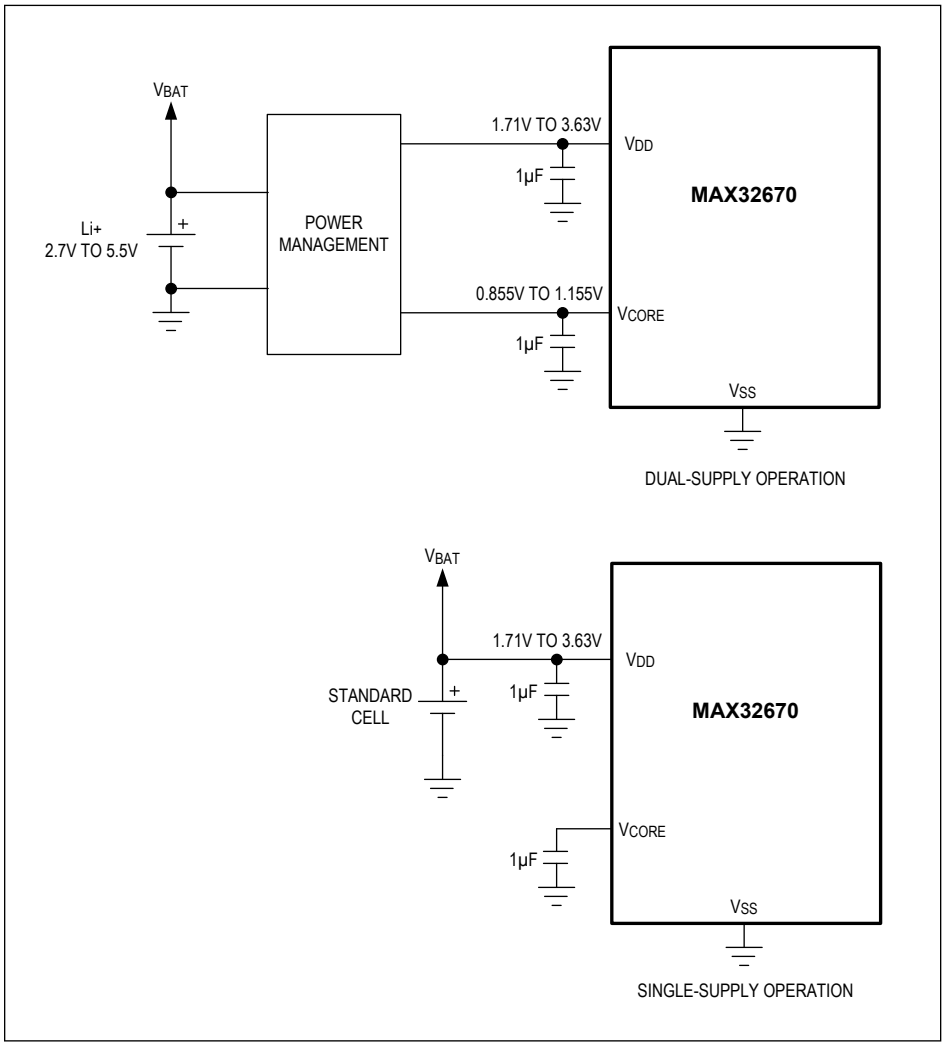


Figure 3. Power-Supply Operational Modes

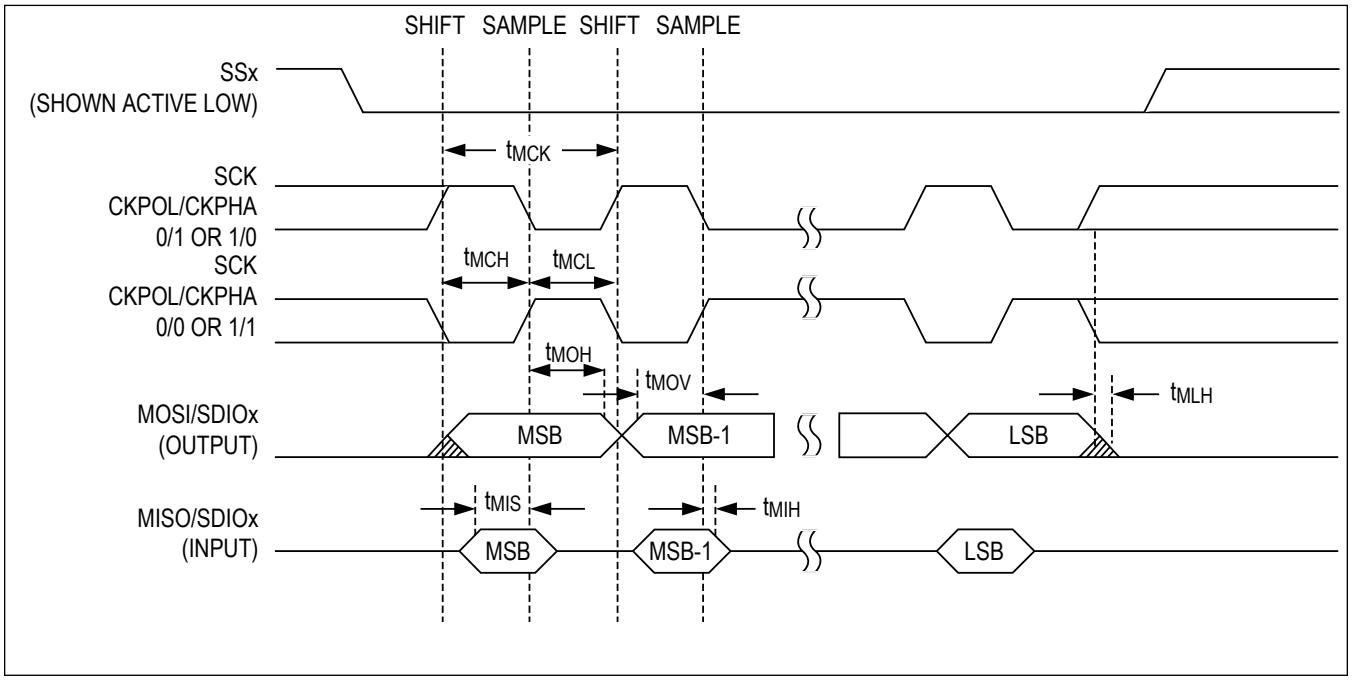


Figure 4. SPI Controller Mode Timing Diagram

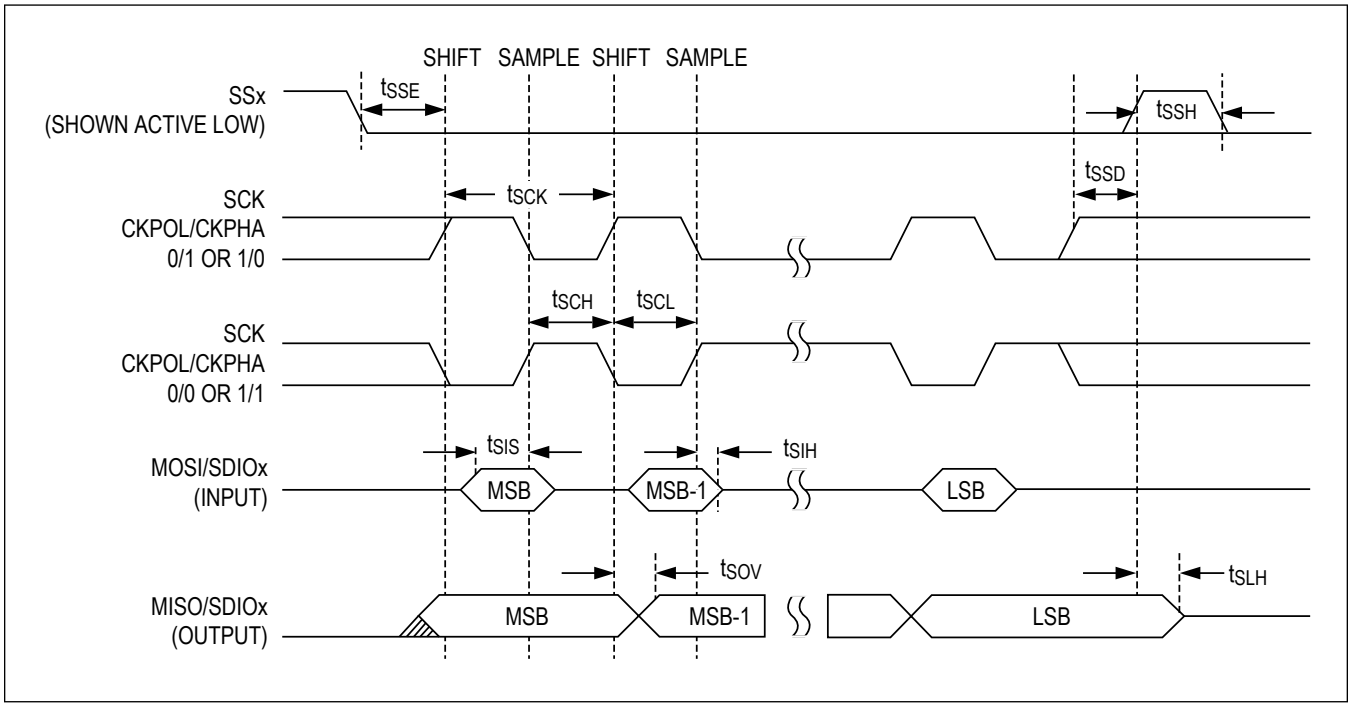


Figure 5. SPI Target Mode Timing Diagram

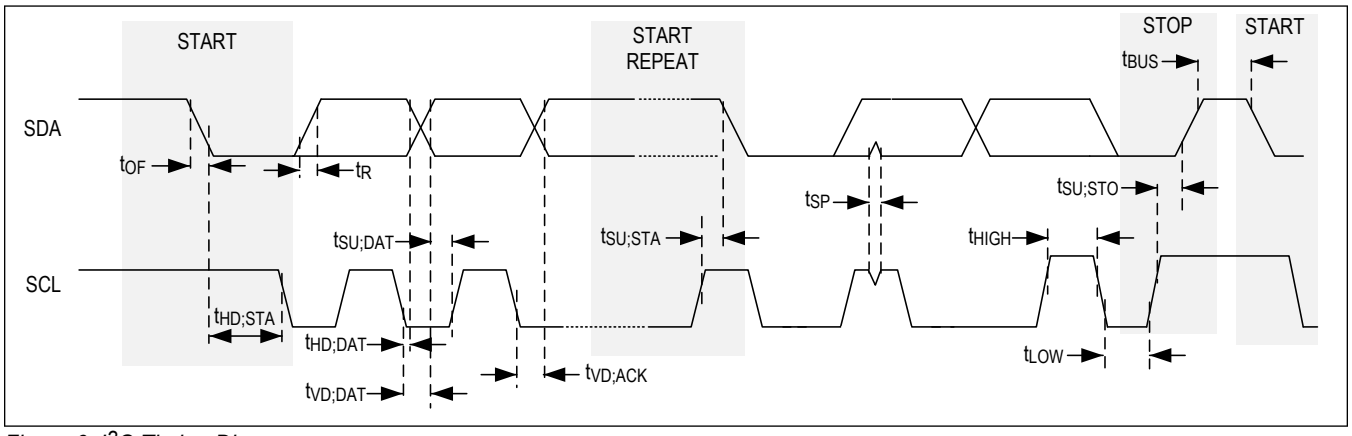


Figure 6. I²C Timing Diagram

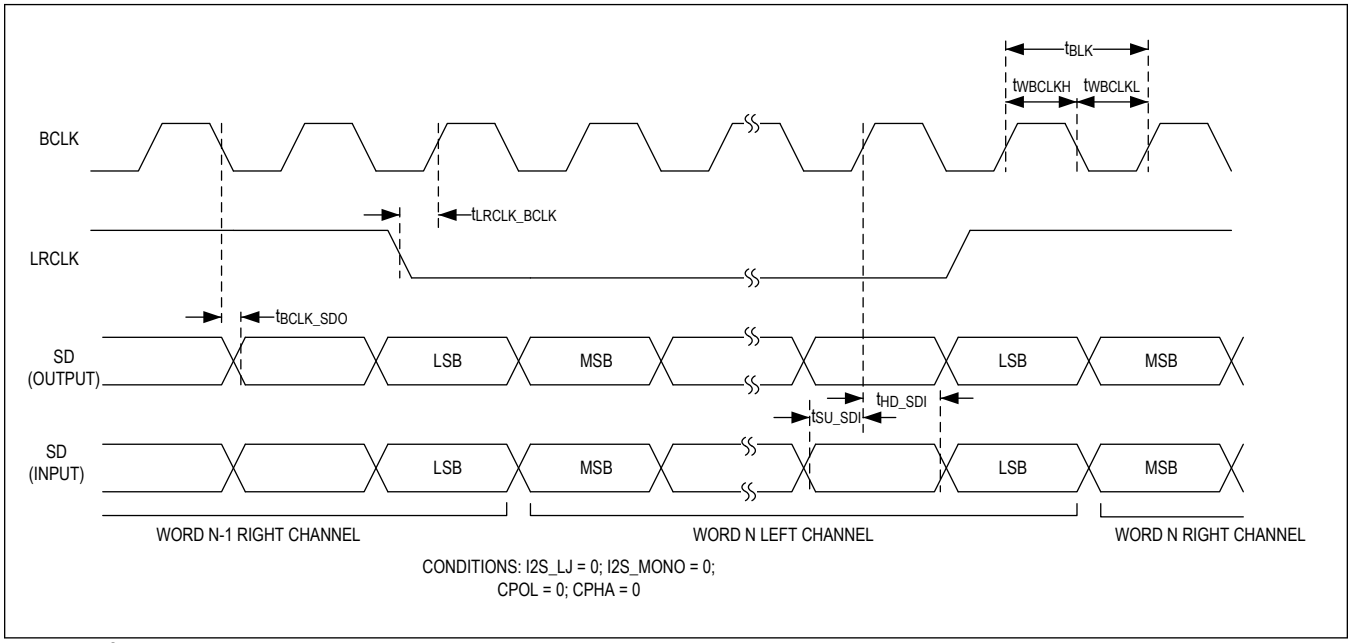
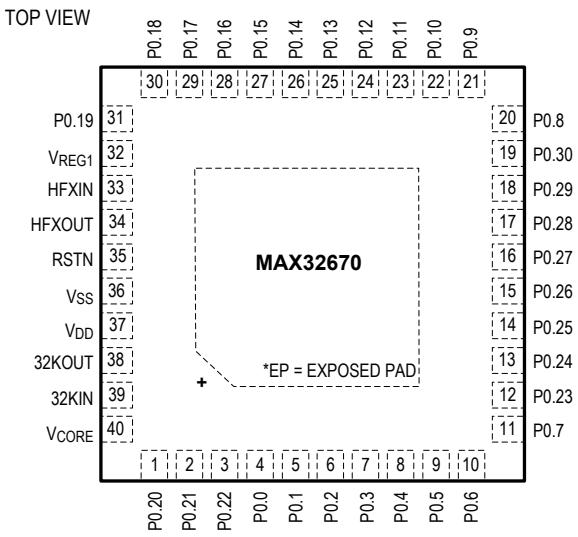


Figure 7. I²S Timing Diagram

Pin Configuration

40 TQFN-EP



40 TQFN-EP
5mm x 5mm

Pin Description

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
POWER (See the *Applications Information* section for bypass capacitor recommendations.)							
40	V_{CORE}	—	—	—	—	—	Digital Power-Supply Input. Bypass with 100nF to V_{SS} and 1µF with 10mΩ to 150mΩ ESR to V_{SS}.
32	V_{REG1}	—	—	—	—	—	Bypass with 4.7nF to V_{SS}. Do not connect this device pin to any other external circuitry.
37	V_{DD}	—	—	—	—	—	Power-Supply Input. Bypass with 100nF to V_{SS} and 1µF with 10mΩ to 150mΩ ESR to V_{SS}.
36	V_{SS}	—	—	—	—	—	Digital Ground

40 TQFN-EP

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
RESET AND CONTROL							
35	RSTN	—	—	—	—	—	External System Reset Input (Active-Low). The device remains in reset while this pin is low. When the pin transitions high, the device performs a system reset and begins execution. This pin has an internal pull-up to the V_{DD} supply.
CLOCKS							
38	32KOUT	—	—	—	—	—	32kHz Crystal Oscillator Output. Connect a 32.768kHz crystal between 32KIN and 32KOUT. If a crystal is not used or if 32KIN is unused, do not connect.
39	32KIN	—	—	—	—	—	32kHz Crystal Oscillator Input. Connect a 32.768kHz crystal between 32KIN and 32KOUT. Load capacitors are not required. See f_{ERTCO} in the *Electrical Characteristics* table for the crystal requirements. Optionally, this pin can be configured as the input for an external CMOS-level clock source. Alternately, if this pin is unused, connect it to V_{SS} through a 1kΩ resistor.
33	HFXIN	—	—	—	—	—	16MHz-32MHz Crystal Oscillator Input. Connect a crystal between HFXIN and HFXOUT. See f_{ERFO} in the *Electrical Characteristics* table for the crystal requirements. Refer to the *MAX32670 User Guide* for calculating the load capacitors. Alternately, if this pin is unused, connect it to V_{SS} through a 10kΩ resistor.
34	HFXOUT	—	—	—	—	—	16MHz-32MHz Crystal Oscillator Output. Connect a crystal between HFXIN and HFXOUT. If a crystal is not used or if HFXIN is unused, do not connect.
GPIO AND ALTERNATE FUNCTION							
4	P0.0	SWDIO	SWDIO	—	TMR0C_IA	—	Serial Wire Debug I/O; Timer0 Port Map C Input.

40 TQFN-EP

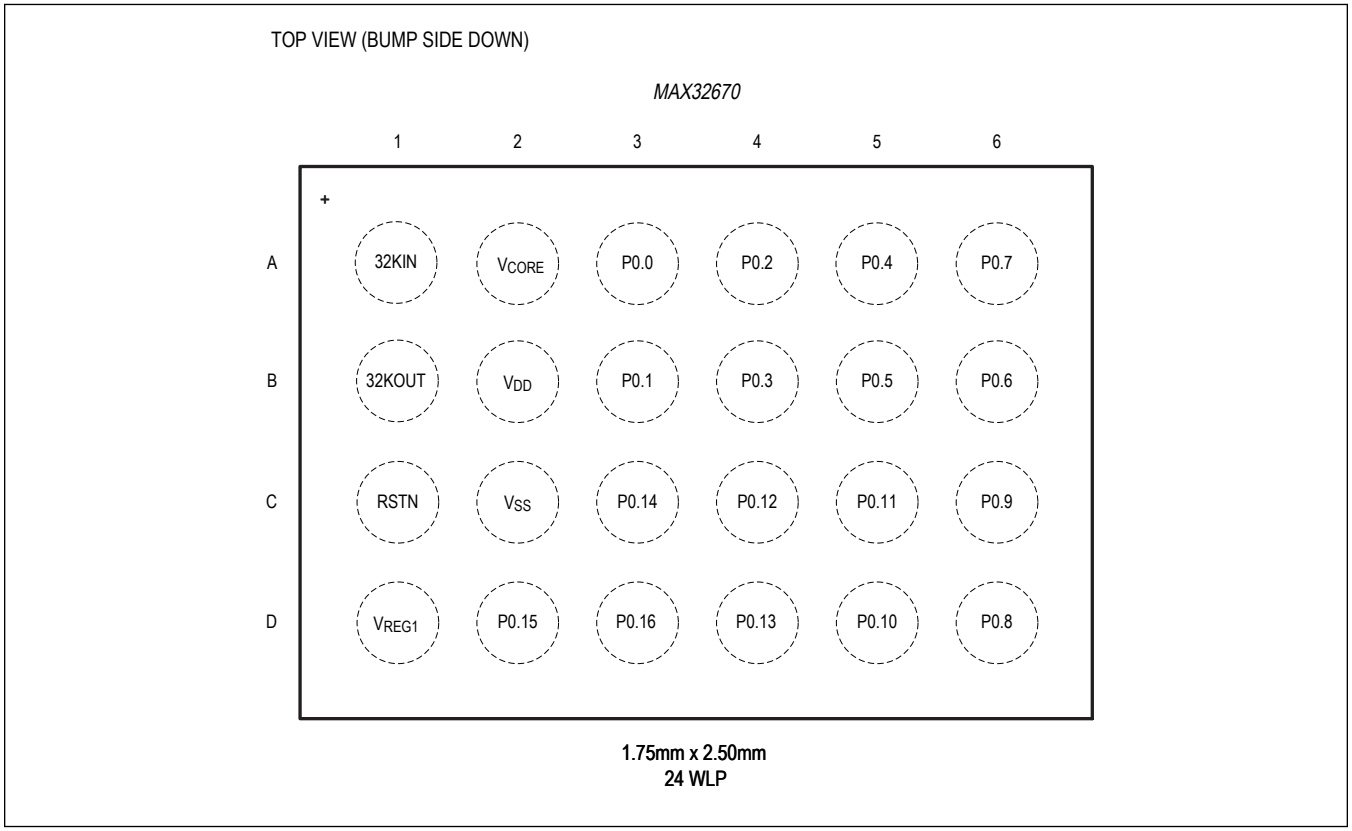
PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
5	P0.1	SWDCLK	SWDCLK	—	TMR0C_O	—	Serial Wire Debug Clock; Timer0 Port Map C Output. This device pin also controls the behavior of the device when exiting a reset event. See *Debug and Development Interface (SWD)*.
6	P0.2	P0.2	SPI0_MISO	UART1B_RX	TMR1C_IA	—	SPI0 Controller In Target Out; UART1 Port Map B Rx; Timer1 Port Map C Input
7	P0.3	P0.3	SPI0_MOSI	UART1B_TX	TMR1C_OA	—	SPI0 Controller Out Target In; UART1 Port Map B Tx; Timer1 Port Map C Output
8	P0.4	P0.4	SPI0_SCK	UART1B_CTS	TMR2C_IA	—	SPI0 Serial Clock; UART1 Port Map B CTS; Timer2 Port Map C Input
9	P0.5	P0.5	SPI0_SS0	UART1B_RTS	TMR2C_OA	DIV_CLK_OUTA	SPI0 Target Select 0; UART1 Port Map B RTS; Timer2 Port Map C Output; Divided Clock Output Port Map A
10	P0.6	P0.6	I2C0_SCL	LPTMR0B_IA	TMR3C_IA	—	I2C0 Serial Clock; Low-Power Timer0 Port Map B Input; Timer3 Port Map C Input
11	P0.7	P0.7	I2C0_SDA	LPTMR0B_OA	TMR3C_OA	—	I2C0 Serial Data; Low-Power Timer0 Port Map B Output; Timer3 Port Map C Output
20	P0.8	P0.8	UART0A_RX	I2S0_SDO	TMR0C_IA	—	UART0 Port Map A Rx; I2S0 Serial Data Output; Timer0 Port Map C Input. This device pin also controls the behavior of the device when exiting a reset event. See *ROM Bootloader Activation* for details.
21	P0.9	P0.9	UART0A_TX	I2S0_LRCLK	TMR0C_OA	—	UART0 Port Map A Tx; I2S0 Left/ Right Clock; Timer0 Port Map C Output
22	P0.10	P0.10	UART0A_CTS	I2S0_BCLK	TMR1C_IA	DIV_CLK_OUTB	UART0 Port Map A CTS; I2S0 Bit Clock; Timer1 Port Map C Input; Divided Clock Output Port Map B
23	P0.11	P0.11	UART0A_RTS	I2S0_SDI	TMR1C_OA	—	UART0 Port Map A RTS; I2S0 Serial Data Input; Timer1 Port Map C Output
24	P0.12	P0.12	I2C1_SCL	EXT_CLK2	TMR2C_IA	EXT_CLK1	I2C1 Serial Clock; Low-Power External Clock Input; Timer2 Port Map C Input; External Clock Input
25	P0.13	P0.13	I2C1_SDA	32KCAL	TMR2C_OA	SPI1_SS0	I2C1 Serial Data; 32.768kHz Calibration Output; Timer2 Port Map C Output; SPI1 Target Select 0
26	P0.14	P0.14	SPI1_MISO	UART2B_RX	TMR3C_IA	—	SPI1 Controller In Target Out; UART2 Port Map B Rx; Timer3 Port Map C Input

40 TQFN-EP

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
27	P0.15	P0.15	SPI1_MOSI	UART2B_TX	TMR3C_OA	—	SPI1 Controller Out Target In; UART2 Port Map B Tx; Timer3 Port Map C Output
28	P0.16	P0.16	SPI1_SCK	UART2B_CTS	TMR0C_IA	—	SPI1 Serial Clock; UART2 Port Map B CTS; Timer0 Port Map C Input
29	P0.17	P0.17	SPI1_SS0	UART2B_RTS	TMR0C_OA	—	SPI1 Target Select 0; UART2 Port Map B RTS; Timer0 Port Map C Output
30	P0.18	P0.18	I2C2_SCL	—	TMR1C_IA	—	I2C2 Serial Clock; Timer1 Port Map C Input
31	P0.19	P0.19	I2C2_SDA	—	TMR1C_OA	—	I2C2 Serial Data; Timer1 Port Map C Output
1	P0.20	P0.20	CM4_RX	—	TMR2C_IA	SWDCLKB	CM4 Rx Event Input; Timer2 Port Map C Input; Serial Wire Debug Clock Port Map B
2	P0.21	P0.21	CM4_TX	—	TMR2C_OA	—	CM4 Tx Event Output; Timer2 Port Map C Output
3	P0.22	P0.22	LPTMR1A_IA	—	TMR3C_IA	SWDIOB	Low-Power Timer1 Port Map A Input; Timer3 Port Map C Input; Single-Wire Debug Port Map B I/O
12	P0.23	P0.23	LPTMR1A_OA	—	TMR3C_OA	—	Low-Power Timer1 Port Map A Output; Timer3 Port Map C Output
13	P0.24	P0.24	LPUART0_CTS	UART0B_RX	TMR0C_IA	—	Low-Power UART0 CTS; UART0 Port Map B Rx; Timer0 Port Map C Input
14	P0.25	P0.25	LPUART0_RTS	UART0B_TX	TMR0C_OA	—	Low-Power UART0 RTS; UART0 Port Map B Tx; Timer0 Port Map C Output
15	P0.26	P0.26	LPUART0_RX	UART0B_CTS	TMR1C_IA	—	Low-Power UART0 Rx; UART0 Port Map B CTS; Timer1 Port Map C Input
16	P0.27	P0.27	LPUART0_TX	UART0B_RTS	TMR1C_OA	—	Low-Power UART0 Tx; UART0 Port Map B RTS; Timer1 Port Map C Output
17	P0.28	P0.28	UART1A_RX	—	TMR2C_IA	—	UART1 Port Map A Rx; Timer2 Port Map C Input
18	P0.29	P0.29	UART1A_TX	—	TMR2C_OA	—	UART1 Port Map A Tx; Timer2 Port Map C Output
19	P0.30	P0.30	UART1A_CTS	—	TMR3C_IA	—	UART1 Port Map A CTS; Timer3 Port Map C Input

Pin Configuration

24 WLP



Pin Description

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
POWER (See the *Applications Information* section for bypass capacitor recommendations.)							
A2	V_{CORE}	—	—	—	—	—	Digital Power-Supply Input. Bypass with 100nF to V_{SS} and 1µF with 10mΩ to 150mΩ ESR to V_{SS}.
D1	V_{REG1}	—	—	—	—	—	Bypass with 4.7nF to V_{SS}. Do not connect this device pin to any other external circuitry.
B2	V_{DD}	—	—	—	—	—	Power-Supply Input. Bypass with 100nF to V_{SS} and 1µF with 10mΩ to 150mΩ ESR to V_{SS}.
C2	V_{SS}	—	—	—	—	—	Digital Ground

24 WLP

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
RESET AND CONTROL							
C1	RSTN	—	—	—	—	—	External System Reset Input (Active-Low). The device remains in reset while this pin is low. When the pin transitions high, the device performs a system reset and begins execution. This pin has an internal pull-up to the V_{DD} supply.
CLOCKS							
B1	32KOUT	—	—	—	—	—	32kHz Crystal Oscillator Output. Connect a 32.768kHz crystal between 32KIN and 32KOUT. If a crystal is not used or if 32KIN is unused, do not connect.
A1	32KIN	—	—	—	—	—	32kHz Crystal Oscillator Input. Connect a 32.768kHz crystal between 32KIN and 32KOUT. Load capacitors are not required. See f_{ERTCO} in the *Electrical Characteristics* table for the crystal requirements. Optionally, this pin can be configured as the input for an external CMOS-level clock source. Alternately, if this pin is unused, connect it to V_{SS} through a 1kΩ resistor.
GPIO AND ALTERNATE FUNCTION							
A3	P0.0	SWDIO	SWDIO	—	TMR0C_IA	—	Serial Wire Debug I/O; Timer0 Port Map C Input.
B3	P0.1	SWDCLK	SWDCLK	—	TMR0C_O	—	Serial Wire Debug Clock; Timer0 Port Map C Output. This device pin also controls the behavior of the device when exiting a reset event. See *Debug and Development Interface (SWD)*.
A4	P0.2	P0.2	SPI0_MISO	UART1B_RX	TMR1C_IA	—	SPI0 Controller In Target Out; UART1 Port Map B Rx; Timer1 Port Map C Input
B4	P0.3	P0.3	SPI0_MOSI	UART1B_TX	TMR1C_OA	—	SPI0 Controller Out Target In; UART1 Port Map B Tx; Timer1 Port Map C Output
A5	P0.4	P0.4	SPI0_SCK	UART1B_CTS	TMR2C_IA	—	SPI0 Serial Clock; UART1 Port Map B CTS; Timer2 Port Map C Input
B5	P0.5	P0.5	SPI0_SS0	UART1B_RTS	TMR2C_OA	DIV_CLK_OUTA	SPI0 Target Select 0; UART1 Port Map B RTS; Timer2 Port Map C Output; Divided Clock Output Port Map A

24 WLP

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
B6	P0.6	P0.6	I2C0_SCL	LPTMR0B_IA	TMR3C_IA	—	I2C0 Serial Clock; Low-Power Timer0 Port Map B Input; Timer3 Port Map C Input
A6	P0.7	P0.7	I2C0_SDA	LPTMR0B_OA	TMR3C_OA	—	I2C0 Serial Data; Low-Power Timer0 Port Map B Output; Timer3 Port Map C Output
D6	P0.8	P0.8	UART0A_RX	—	TMR0C_IA	—	UART0 Port Map A Rx; Timer0 Port Map C Input. This device pin also controls the behavior of the device when exiting a reset event. See *ROM Bootloader Activation* for details.
C6	P0.9	P0.9	UART0A_TX	—	TMR0C_OA	—	UART0 Port Map A Tx; Timer0 Port Map C Output
D5	P0.10	P0.10	UART0A_CTS	—	TMR1C_IA	DIV_CLK_OUTB	UART0 Port Map A CTS; Timer1 Port Map C Input; Divided Clock Output Port Map B
C5	P0.11	P0.11	UART0A_RTS	—	TMR1C_OA	—	UART0 Port Map A RTS; Timer1 Port Map C Output
C4	P0.12	P0.12	I2C1_SCL	EXT_CLK2	TMR2C_IA	EXT_CLK1	I2C1 Serial Clock; Low-Power External Clock Input; Timer2 Port Map C Input; External Clock Input
D4	P0.13	P0.13	I2C1_SDA	32KCAL	TMR2C_OA	SPI1_SS0	I2C1 Serial Data; 32.768kHz Calibration Output; Timer2 Port Map C Output; SPI1 Target Select 0
C3	P0.14	P0.14	SPI1_MISO	UART2B_RX	TMR3C_IA	—	SPI1 Controller In Target Out; UART2 Port Map B Rx; Timer3 Port Map C Input
D2	P0.15	P0.15	SPI1_MOSI	UART2B_TX	TMR3C_OA	—	SPI1 Controller Out Target In; UART2 Port Map B Tx; Timer3 Port Map C Output
D3	P0.16	P0.16	SPI1_SCK	UART2B_CTS	TMR0C_IA	—	SPI1 Serial Clock; UART2 Port Map B CTS; Timer0 Port Map C Input

Detailed Description

The MAX32670 is an ultra-low-power, cost-effective, high-reliability 32-bit microcontroller enabling designs with complex sensor processing without compromising battery life. It combines a flexible and versatile power management unit with the powerful Arm Cortex-M4 processor with FPU. It also offers legacy designs an easy and cost-optimal upgrade path from 8- or 16-bit microcontrollers. The device integrates 384KB (376KB user) of flash memory and 160KB of SRAM to accommodate application and sensor code.

The device features five powerful and flexible power modes. It can operate from a single-supply battery or a dual-supply typically provided by a PMIC. The I^2C ports support standard-mode, fast-mode, fast-mode plus, and high-speed mode, operating up to 3400kbps. The SPI ports can run up to 50MHz in both controller and target modes. Four general-purpose 32-bit timers, two low-power 32-bit timers, two windowed watchdog timers, three UARTs, one low-power UART, and a real-time clock (RTC) are also provided. An I^2S interface provides digital audio streaming to a codec.

Arm Cortex-M4 Processor with FPU Engine

The Arm Cortex-M4 processor with FPU combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 processor with FPU supports single instruction multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed or unsigned data, with or without saturation

Memory

Internal Flash Memory

The device provides 384KB of flash memory for nonvolatile program and data storage. 376KB is available for application usage; the last page (8KB) is reserved for system use and must not be modified or erased.

Internal SRAM

The internal 160KB SRAM provides low-power retention of application information in all power modes except STORAGE mode. The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data-retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by only retaining the most essential data.

Clocking Scheme

Multiple system clock sources are available to maximize performance and minimize power consumption:

- 100MHz internal primary oscillator (IPO)
- 80kHz internal nanoring oscillator (INRO)
- 32.768kHz external RTC oscillator (ERTCO) (external crystal or clock source required)
- 7.3728MHz internal baud-rate oscillator (IBRO)
- 16MHz–32MHz external oscillator (ERFO) (external crystal or clock source required)*
- External square-wave clock up to 50MHz
- External square-wave clock up to 1MHz for LPTMR0, LPTMR1, and LPUART

*The ERFO is not available in the 24 WLP package.

The SYS_CLK is the primary clock source for the digital logic and peripherals. Select the IBRO to optimize active power consumption. Wakeup is possible from either the IBRO or the IPO.

An external 32.768kHz time base is required when using the RTC.

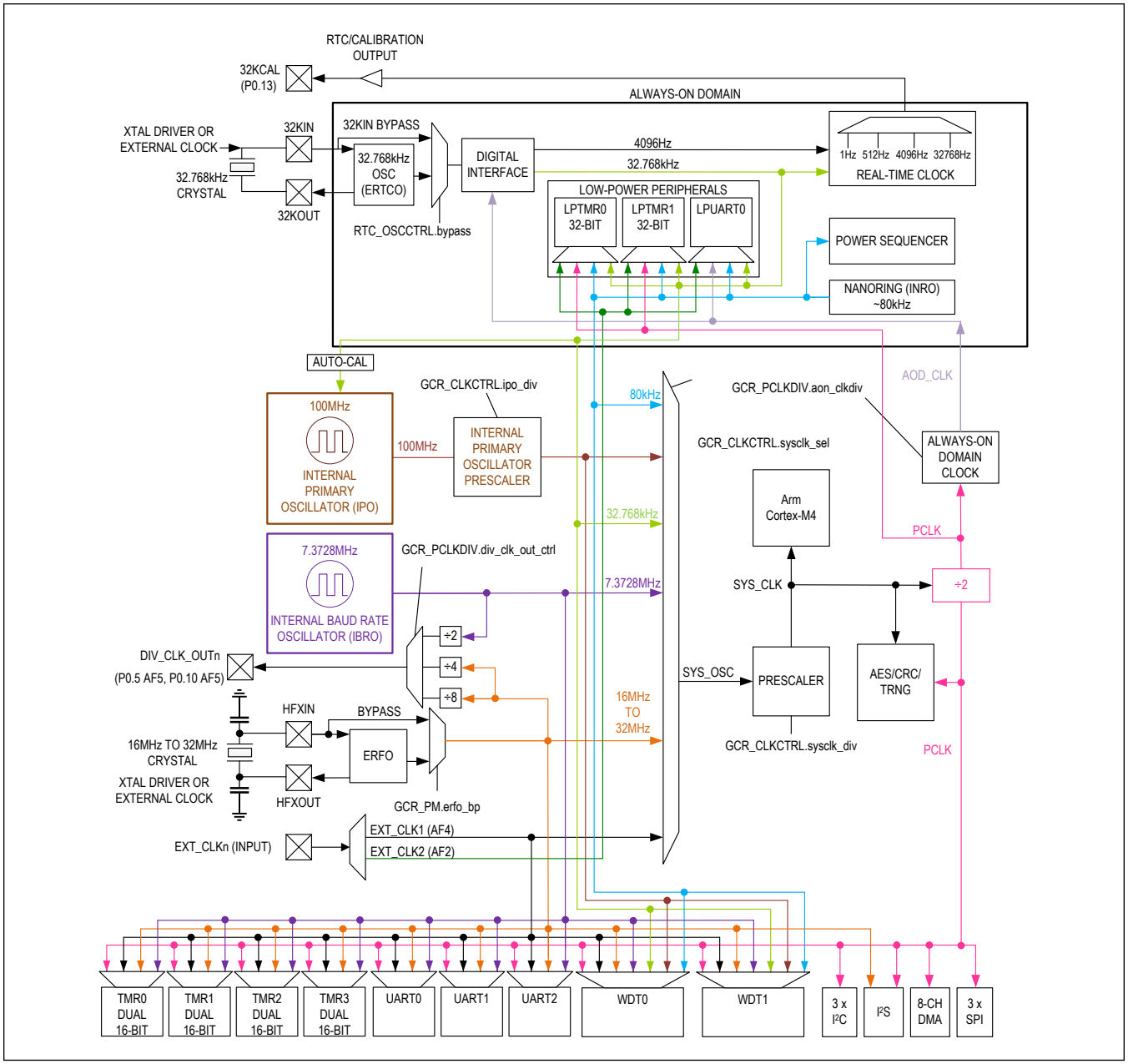


Figure 8. 40 TQFN-EP Clocking Scheme

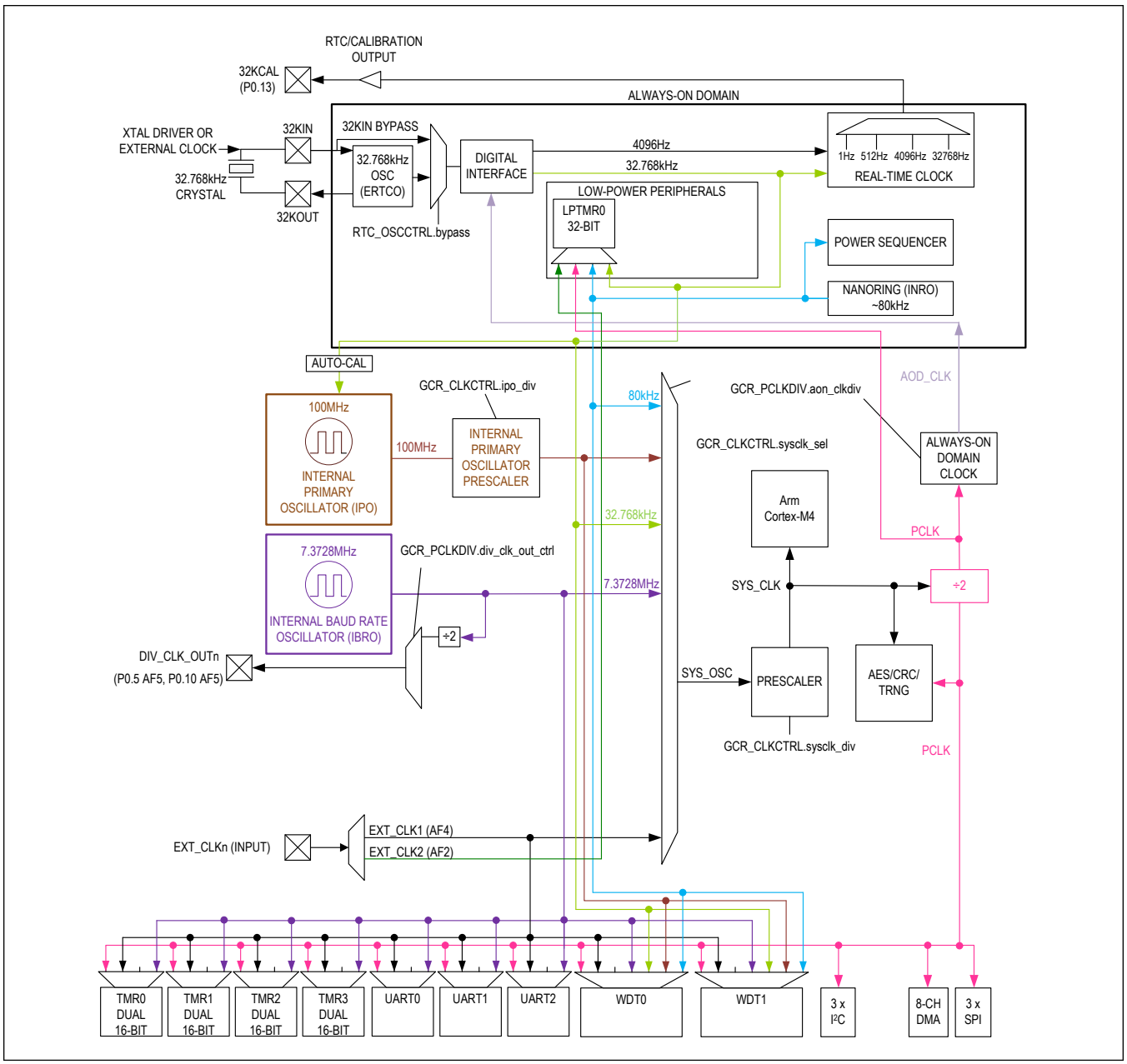


Figure 9. 24 WLP Clocking Scheme

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a firmware-controlled I/O function and one or more special function signals associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a firmware-controlled I/O. Though this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the *Electrical Characteristics* tables.

In GPIO mode, each pin of a port has an interrupt function that can be independently enabled and configured as a level-

or edge-sensitive interrupt. All GPIOs share the same interrupt vector. Some packages do not have all of the GPIOs available. When configured as GPIOs, the following features are provided. These features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high-impedance
- Optional internal pull-up resistor or internal pull-down resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

Table 1. MAX32670 GPIO Instances

PACKAGE	GPIO	INSTANCES
40 TQFN-EP	Up to 31	GPIO0[30:0]
24 WLP	Up to 16	GPIO0[15:0]

Standard DMA Controller

The standard direct memory access (DMA) controller provides a means to offload the CPU for memory/peripheral data transfer leading to a more power-efficient system. It allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 8 channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

Power Management

Power Management Unit

The power management unit (PMU) provides the optimal mix of high-performance and low-power consumption. It exercises intelligent, precise control of power distribution to the CPU and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple clock domains
- Fast wakeup of powered-down peripherals when activity detected

ACTIVE Mode

In this mode, the CPU is executing application code and all digital and analog peripherals are available on demand. Dynamic clocking disables local clocks in peripherals not in use. This mode corresponds to the Arm Cortex-M4 processor with FPU Active mode.

SLEEP Mode

This mode allows for lower power consumption operation than ACTIVE mode. The CPU is asleep, peripherals are on, and the standard DMA block is available. The GPIO or any active peripheral can be configured to interrupt and cause transition to ACTIVE mode. This mode corresponds to the Arm Cortex-M4 processor with FPU Sleep mode.

DEEPSLEEP Mode

In this mode, CPU and critical peripheral configuration settings and all volatile memory are preserved.

The device status is a follows:

- The CPU is powered down. The system state and all SRAM is retained.

- The GPIO pins retain their state.
- The transition from DEEPSLEEP mode to ACTIVE mode is faster than the transition from BACKUP mode because system initialization is not required.
- The system oscillators are all disabled to provide additional power savings over SLEEP mode.
- LPUART0 and LPTMR0/1 can be active and are optional wake-up sources.

This mode corresponds to the Arm Cortex-M4 with FPU DeepSleep mode.

BACKUP Mode

This mode places the CPU in a static, low-power state. BACKUP mode supports the same wake-up sources as DEEPSLEEP mode. The device status is as follows:

- The CPU is powered down.
- SRAM retention as per Table 2. Each of the RAM blocks can be retained.
- LPUART0 and LPTMR0/1 can be active and are optional wake-up sources.

Table 2. BACKUP Mode RAM Retention

RAM BLOCK	RAM SIZE (KB)	RETAINED RAM (KB)
SYSRAM0	20	0
SYSRAM1	20	20
SYSRAM2	40	40
SYSRAM3	80	80

Note: The boot ROM uses certain ranges of SRAM to perform system checks during a system reset, watchdog timer reset, an external reset, and exiting from BACKUP mode. As a result, portions of SRAM may not be retained during an exit from BACKUP mode.

STORAGE Mode

The device status is as follows:

- The CPU is powered off.
- All peripherals are powered off.
- Wake-up from GPIO interrupt.
- RTC can be enabled.
- No SRAM retention.

Real-Time Clock (RTC)

An RTC keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm that can be programmed to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode, but still awaken periodically to perform assigned tasks. A second independent 32-bit 1/4096 subsecond alarm can be programmed between 244µs and 12 days. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low-power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the *Electrical Characteristics* table.

An RTC calibration feature provides the ability for user-software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the 32KCAL alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

Windowed Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One

of the most effective countermeasures is the watchdog timer, which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically reset by the application software using a special timed sequence. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution.

The windowed timeout period feature provides more detailed monitoring of system operation, requiring the WDT to be reset within a specific window of time.

The instances of the peripheral and the clock source options are shown in Table 3. See the *Ordering Information* table for the specific instances available by part number.

Table 3. MAX32670 Watchdog Timer Instances

INSTANCE	WINDOW SUPPORT	OPERATING MODES	CLK0	CLK1	CLK2	CLK3	CLK4	CLK5	CLK6	CLK7
WDT0	YES	ACTIVE SLEEP	PCLK	IPO	IBRO	INRO	ERTCO	EXT_CLK1	ERFO*	—
WDT1	YES	ACTIVE SLEEP	PCLK	IPO	IBRO	INRO	ERTCO	EXT_CLK1	ERFO*	—

**ERFO not available in 24 WLP parts.*

32-Bit Timer/Counter/PWM (TMR, LPTMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals with minimal software interaction. The timer provides the following features:

- 32-bit up counter with autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating or capture
- Timer output pin
- TMR0–TMR3 can be configured as 2 × 16-bit general-purpose timers
- Timer interrupt

Note that the timer function can be multiplexed with other functions on the GPIO pins, so it might not be possible to use all the ports depending on the device configuration.

The instances of the peripheral, operating modes, and clock source options are shown in Table 4. Some instances may not be available in every package configuration; see the *Ordering Information* table for the specific instances available by part number.

Table 4. MAX32670 Timer Instances

INSTANCE	SINGLE 32 BIT	DUAL 16 BIT	OPERATING MODES	CLOCK SOURCE						
				PCLK	IBRO	ERFO*	INRO	ERTCO	EXT_CLK1	EXT_CLK2
TMR0	YES	YES	ACTIVE SLEEP	YES	YES	YES	NO	NO	YES	NO
TMR1	YES	YES	ACTIVE SLEEP	YES	YES	YES	NO	NO	YES	NO
TMR2	YES	YES	ACTIVE SLEEP	YES	YES	YES	NO	NO	YES	NO
TMR3	YES	YES	ACTIVE SLEEP	YES	YES	YES	NO	NO	YES	NO

Table 4. MAX32670 Timer Instances (continued)

INSTANCE	SINGLE 32 BIT	DUAL 16 BIT	OPERATING MODES	CLOCK SOURCE						
				PCLK	IBRO	ERFO*	INRO	ERTCO	EXT_CLK1	EXT_CLK2
LPTMR0	YES	NO	ACTIVE SLEEP	AOD_CLK	NO	NO	YES	YES	NO	YES
			DEEPSLEEP BACKUP	NO						
LPTMR1	YES	NO	ACTIVE SLEEP	AOD_CLK	NO	NO	YES	YES	NO	YES
			DEEPSLEEP BACKUP	NO						

**ERFO not available in 24 WLP parts.*

Serial Peripherals

I²C Interface (I2C)

The I²C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communications medium. These engines support Standard-mode, Fast-mode, Fast-mode Plus, and High-speed mode I²C speeds. It provides the following features:

- Controller or target mode operation
  - Supports up to four different target addresses in target mode
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Transmit FIFO preloading
- Support for clock stretching to allow slower target devices to operate on higher speed busses
- Multiple transfer rates
  - Standard-mode: 100kbps
  - Fast-mode: 400kbps
  - Fast-mode Plus: 1000kbps
  - High-speed mode: 3400kbps
- Internal filter to reject noise spikes
- Receive FIFO depth of 8 bytes
- Transmit FIFO depth of 8 bytes

The MAX32670 provides three instances of the I²C peripheral (I2C0, I2C1, and I2C2).

Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a highly configurable, flexible, and efficient synchronous interface among multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals, and one or more target select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either target or controller mode and provide the following features:

- SPI modes 0, 1, 2, and 3 for single-bit communication
- 3- or 4-wire mode for single-bit target device communication
- Full-duplex operation in single-bit, 4-wire mode
- Multicontroller mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Target select assertion and deassertion timing with respect to leading/trailing SCK edge

The MAX32670 provides multiple instances of the SPI peripheral. See Table 5 for configuration options.

Table 5. SPI Configuration Options

INSTANCE	DATA	TARGET SELECT LINES	
		40 TQFN-EP	24 WLP
SPI0	3 wire, 4 wire	1	1
SPI1	3 wire, 4 wire	1	0
SPI2	N/A	N/A	N/A

I²S Interface (I2S)

The I²S interface is a bidirectional, four-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I²S Bus Specification, June 5, 1996. It provides the following features:

- Controller and target mode operation
- Selectable bits per word from 1 to 32
- Receive and transmit DMA support
- Word-select polarity control
- First bit position selection
- Interrupts generated for FIFO status
- Receiver FIFO depth of 32 bytes
- Transmitter FIFO depth of 32 bytes

The number of instances is shown in Table 6.

Table 6. MAX32670 I²S Instances

PACKAGE	INSTANCES
40 TQFN-EP	1
24 WLP	0

UART (UART, LPUART)

The universal asynchronous receiver-transmitter (UART, LPUART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request to send (RTS) and clear to send (CTS) flow control signaling. Each instance is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for multiple events reduce overhead:
  - Frame error
  - Parity error
  - CTS
  - Receiver FIFO overrun
  - FIFO full
  - FIFO partially full
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Two DMA channels can be connected (read and write FIFOs)

- Programmable word size (5 bits to 8 bits)

The instances of the peripheral, operating modes, and clock source options are shown in Table 7. All instances may not be available in every package configuration; see the *Ordering Information* table for the specific instances available by part number.

Table 7. MAX32670 UART Instances

INSTANCE	OPERATING MODES	CLOCK SOURCE						
		AOD_PCLK	IBRO	ERFO*	INRO	ERTCO	EXT_CLK1	EXT_CLK2
UART0	ACTIVE	YES	YES	YES	NO	NO	YES	NO
UART1	ACTIVE	YES	YES	YES	NO	NO	YES	NO
UART2	ACTIVE	YES	YES	YES	NO	NO	YES	NO
LPUART0	ACTIVE/SLEEP	AOD_CLK	NO	NO	YES	YES	NO	YES
	DEEPSLEEP/BACKUP	NO						

**ERFO not available in 24 WLP parts.*

Security

ROM Bootloader

The bootloader allows the loading and verification of program memory through a serial interface. Features include:

- ROM-based
- Bootloader interface through UART
- Program loading of Motorola® SREC format files
- Permanent lock state prevents altering or erasing program memory through the ROM bootloader
- Access to the USN for device or customer application identification
- Disable SWD interface to block debug access port functionality

The contents of SRAM are not guaranteed following the activation of the bootloader.

Secure Boot

On devices that support the secure boot feature, the device ensures software integrity by automatically comparing program memory against a stored HMAC SHA-256 hash value after every reset. A program that fails the integrity check indicates corrupted or modified program memory and is prevented from executing any instructions.

Devices with the secure boot feature also provide an optional challenge/response that authenticates before executing bootloader commands.

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in dedicated flash to protect against tampering. Key generation and storage is transparent to the user.

True Random Number Generator (TRNG)

Random numbers are a vital part of a secure application, providing random numbers that are useable for cryptographic seeds or strong cryptography keys to ensure data privacy. Software can use random numbers to trigger asynchronous events that result in nondeterministic behavior.

The TRNG is continuously updated by a high-quality, physically-unpredictable entropy source. It generates one random bit per cryptographic clock cycle.

Cyclic Redundancy Check (CRC) Module

A CRC hardware module provides fast calculations and data integrity checks by application software. The CRC polynomial is programmable to support custom CRC algorithms as well as the common algorithms shown in Table 8.

Table 8. Common CRC Polynomials

ALGORITHM	POLYNOMIAL EXPRESSION
CRC-32-ETHERNET	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + x^0$
CRC-CCITT	$x^{16} + x^{12} + x^5 + x^0$
CRC-16	$x^{16} + x^{12} + x^2 + x^0$
USB DATA	$x^{16} + x^{12} + x^2 + x^0$
PARITY	$x^1 + x^0$

Serial Wire Debug (SWD) and Development Interface

The device provides an Arm Debug Access Port (DAP) that supports debugging during application development. The DAP enables an external debugger to access the device. The DAP is a standard Arm CoreSight™ SWD port and uses a two-pin serial interface (SWDCLK and SWDIO).

Applications Information

Bypass Capacitor Recommendations

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The *Pin Descriptions* table indicates which pins should be connected to bypass capacitors, and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the *Pin Descriptions* table shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Capacitors should be placed as close as possible to their corresponding device pins. Pins which recommend more than one value of capacitor per pin should place them in parallel with the lowest value capacitor first, closest to the pin.

RTC Crystal Guidelines

The internal low-power RTC oscillator minimizes power consumption and maximizes battery life. The RTC crystal must be designed to reach its nominal frequency with 6pF (called C_L or C_{L_XTAL} in the *Electrical Characteristics* table) of load capacitance. Crystals designed for values of C_{L_XTAL} greater than 6pF are not supported. Note that crystal load capacitors are electrically in series across the crystal, so the correct value of total pad and trace capacitance for a "6pF crystal" is 12pF per terminal. The RTC in this part includes integrated load capacitors. External load capacitors are not required for RTC operation.

A digital trim feature can compensate for RTC inaccuracies of up to ±127ppm when compared against an external reference clock. Refer to the device User Guide for details.

Although they are not required, customers can also tune the clock using external load capacitors. Final C values must be determined after the PCB layout is complete. However, the low-power design of the RTC oscillator imposes a maximum of 12pF (C_{PAD} + C_{STRAY} + C_{L_XTAL}) total per pin.

If the RTC is unused, the preferred solution is to connect 32KIN to V_{SS} through a 1kΩ resistor. Cost or space-contrained designs can connect 32KIN directly to V_{SS}. The 32KOUT pin should be left unconnected.

ROM Bootloader Activation

The bootloader samples the bootloader stimulus pins during any of the bootloader events shown in Table 9. If any of the stimulus pins are not in their active state during a bootloader activation event, the bootloader is bypassed and the device begins executing the application code.

If all stimulus pins are in their active state during a bootloader activation event, the application software does not execute and instead the ROM bootloader assumes control of the device. The device outputs a status prompt and begins a bootloader session with the host system controlling the programming. While the ROM bootloader is in control, the stimulus pins are ignored and can be driven to any value or used for communication if applicable.

The bootloader session is terminated at any time by performing a POR or asserting RSTN while the stimulus pins are in their inactive state.

Table 9. ROM Bootloader Interface

PART NUMBER	INTERFACE PINS	STIMULUS PINS	BOOTLOADER ACTIVATION EVENTS
All devices	UART0A_RX (P0.8) UART0A_TX (P0.9) SWDCLK (P0.1) RSTN	UART0_RX (P0.8, active low) SWDCLK (P0.1, active low)	POR System Reset (including RSTN and WDT resets) Exit from BACKUP Exit from STORAGE

Typical Fixed Current Consumption Temperature Variance

Single-Supply ACTIVE Mode

Table 10. Single-Supply Operation Fixed V_{DD} Current Consumption ACTIVE Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL	UNITS

Table 10. Single-Supply Operation Fixed V_{DD} Current Consumption ACTIVE Mode (continued)

				-40°C	25°C	55°C	85°C	105°C	
V_{DD} Current ACTIVE Mode	I_{DD_FACTS}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	634	735	863	1127	1477	µA
			OVR = [01], internal regulator set to 1.0V	544	659	760	956	1241	µA
			OVR = [00], internal regulator set to 0.9V	474	563	654	819	1063	µA
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	618	754	847	1099	1435	µA
			OVR = [01], internal regulator set to 1.0V	525	633	734	961	1242	µA
			OVR = [00], internal regulator set to 0.9V	455	538	626	815	1052	µA

Single-Supply SLEEP Mode

Table 11. Single-Supply Operation Fixed V_{DD} Current Consumption SLEEP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DD} Current SLEEP Mode	I_{DD_FSLPS}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	634	735	863	1127	1477	µA
			OVR = [01], internal regulator set to 1.0V	544	659	760	956	1241	µA
			OVR = [00], internal regulator set to 0.9V	474	563	654	819	1063	µA
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	618	754	847	1099	1435	µA
			OVR = [01], internal regulator set to 1.0V	525	633	734	961	1242	µA

Table 11. Single-Supply Operation Fixed V_{DD} Current Consumption SLEEP Mode (continued)

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
			OVR = [00], internal regulator set to 0.9V	455	538	626	815	1052	µA

Single-Supply DEEPSLEEP Mode

Table 12. Single-Supply Operation Fixed V_{DD} Current Consumption DEEPSLEEP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DD} Fixed Current DEEPSLEEP Mode	I_{DD_FDSLPS}	Standby state with full data retention and 160KB SRAM retained	V_{DD} = 3.3V	1.44	4	9.7	24.7	49	µA
			V_{DD} = 1.8V	1.3	3.7	9.3	24.2	48.3	µA

Single-Supply BACKUP Mode

Table 13. Single-Supply Operation Fixed V_{DD} Current Consumption BACKUP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DD} Fixed Current BACKUP Mode	I_{DD_FBKUS}	V_{DD} = 3.3V, RTC disabled	0KB SRAM retained, retention regulator disabled	0.28	0.38	0.57	1	1.75	µA
			20KB SRAM retained	0.64	1.08	1.96	4.3	8.2	µA
			40KB SRAM retained	0.72	1.4	2.84	6.6	12.8	µA
			80KB SRAM retained	0.89	1.9	4.1	9.9	19.5	µA
			160KB SRAM retained	1.2	2.8	6.1	15.2	30.3	µA
		V_{DD} = 1.8V, RTC disabled	0KB SRAM retained, retention regulator disabled	0.13	0.15	0.22	0.48	1	µA
			20KB SRAM retained	0.49	0.86	1.64	3.8	7.5	µA
			40KB SRAM retained	0.58	1.2	2.5	6.1	12.1	µA
			80KB SRAM retained	0.75	1.7	3.7	9.4	18.7	µA
			160KB SRAM retained	1.06	2.58	5.8	14.7	29.7	µA

Single-Supply STORAGE Mode

Table 14. Single-Supply Operation Fixed V_{DD} Current Consumption STORAGE Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V_{DD} Fixed Current STORAGE Mode	I_{DD_FSTOS}	V_{DD} = 3.3V	0.23	0.33	0.51	0.96	1.68	µA
		V_{DD} = 1.8V	0.094	0.11	0.19	0.45	0.94	µA

Dual-Supply ACTIVE Mode

Table 15. Dual-Supply Operation Fixed V_{CORE} Current Consumption ACTIVE Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Current ACTIVE Mode	I_{CORE_FACTD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V	222	311	410	663	996	µA
			OVR = [01], V_{CORE} = 1.0V	131	209	310	483	760	µA
			OVR = [00], V_{CORE} = 0.9V	54	106	171	317	52	µA

Dual-Supply ACTIVE Mode

Table 16. Dual-Supply Operation Fixed V_{DD} Current Consumption ACTIVE Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DD} Current ACTIVE Mode	I_{DD_FACTD}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	360	391	406	424	441	µA
			OVR = [01], internal regulator set to 1.0V	360	390	406	424	441	µA
			OVR = [00], internal regulator set to 0.9V	356	387	402	420	437	µA
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V	341	372	388	406	422	µA
			OVR = [01], internal regulator set to 1.0V	341	372	387	405	421	µA
			OVR = [00], internal regulator set to 0.9V	338	369	384	401	417	µA

Dual-Supply SLEEP Mode

Table 17. Dual-Supply Operation Fixed V_{CORE} Current Consumption SLEEP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Current SLEEP Mode	I_{CORE_FSLPD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V	222	311	410	663	996	µA

Table 17. Dual-Supply Operation Fixed V_{CORE} Current Consumption SLEEP Mode (continued)

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
			OVR = [01], V_{CORE} = 1.0V	131	209	310	483	760	µA
			OVR = [00], V_{CORE} = 0.9V	54	106	171	317	523	µA

Dual-Supply SLEEP Mode

Table 18. Dual-Supply Operation Fixed V_{DD} Current Consumption SLEEP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DD} Current SLEEP Mode	I_{DD_FSLPD}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V	360	391	406	424	441	µA
			OVR = [01], V_{CORE} = 1.0V	360	390	406	424	441	µA
			OVR = [00], V_{CORE} = 0.9V	356	387	402	420	437	µA
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V	341	372	388	406	422	µA
			OVR = [01], V_{CORE} = 1.0V	341	372	387	405	421	µA
			OVR = [00], V_{CORE} = 0.9V	338	369	384	401	417	µA

Dual-Supply DEEPSLEEP Mode

Table 19. Dual-Supply Operation Fixed V_{CORE} Current Consumption DEEPSLEEP Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Fixed-Current, DEEPSLEEP Mode	I_{CORE_FDSLPD}	V_{DD} = 3.3V, V_{CORE} = 1.1V	4.9	10.5	20	43	78	µA
		V_{DD} = 3.3V, V_{CORE} = 0.855V	1.26	4	9.8	25	49	µA
		V_{DD} = 1.8V, V_{CORE} = 1.1V	4.9	10.5	20	43.6	78.9	µA
		V_{DD} = 1.8V, V_{CORE} = 0.855V	1.25	4	9.8	25	49	µA

Dual-Supply DEEPSLEEP Mode

Table 20. Dual-Supply Operation Fixed V_{DD} Current Consumption DEEPSLEEP Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V_{DD} Fixed-Current, DEEPSLEEP Mode	I_{DD_FDSLPD}	V_{DD} = 3.3V, V_{CORE} = 1.1V	0.262	0.36	0.531	0.965	1.67	µA
		V_{DD} = 3.3V, V_{CORE} = 0.855V	0.254	0.36	0.532	0.964	1.69	µA
		V_{DD} = 1.8V, V_{CORE} = 1.1V	0.127	0.149	0.22	0.48	0.99	µA
		V_{DD} = 1.8V, V_{CORE} = 0.855V	0.127	0.149	0.22	0.48	0.99	µA

Dual-Supply BACKUP Mode

Table 21. Dual-Supply Operation Fixed V_{CORE} Current Consumption BACKUP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Fixed-Current, BACKUP Mode	I_{CORE_FBKUD}	0KB SRAM retained with RTC disabled, retention regulator disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V	0.115	0.3	0.856	2.6	5.7	µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V	0.058	0.19	0.626	2.06	4.67	µA
			V_{DD} = 1.8V, V_{CORE} = 1.1V	0.11	0.297	0.86	2.6	5.7	µA
			V_{DD} = 1.8V, V_{CORE} = 0.855V	0.058	0.187	0.623	2.05	4.69	µA
		20KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V	0.595	1.37	2.93	7.1	13.8	µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V	0.177	0.6	1.64	4.6	9.7	µA
			V_{DD} = 1.8V, V_{CORE} = 1.1V	0.59	1.37	2.93	7.1	13.9	µA
			V_{DD} = 1.8V, V_{CORE} = 0.855V	0.179	0.6	1.65	4.6	9.7	µA
		40KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V	1.07	2.39	4.86	11.2	21.1	µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V	0.3	0.99	2.55	6.95	14.2	µA
			V_{DD} = 1.8V, V_{CORE} = 1.1V	1.07	2.39	4.9	11.2	21.3	µA

Table 21. Dual-Supply Operation Fixed V_{CORE} Current Consumption BACKUP Mode (continued)

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
			V_{DD} = 1.8V, V_{CORE} = 0.855V	0.3	0.99	2.56	7	14.3	µA
		80KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V	1.97	4.15	7.9	17.1	31.5	µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V	0.52	1.6	3.9	10.2	20.5	µA
			V_{DD} = 1.8V, V_{CORE} = 1.1V	1.99	4.15	7.9	17.2	31.7	µA
			V_{DD} = 1.8V, V_{CORE} = 0.855V	0.52	1.6	3.9	10.2	20.6	µA
		160KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V	3.7	7.4	13.2	27.2	49	µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V	0.94	2.7	6.2	15.7	31.2	µA
			V_{DD} = 1.8V, V_{CORE} = 1.1V	3.71	7.4	13.3	27.3	49.3	µA
			V_{DD} = 1.8V, V_{CORE} = 0.855V	0.947	2.7	6.3	15.7	31.3	µA

Dual-Supply BACKUP Mode

Table 22. Dual-Supply Operation Fixed V_{DD} Current Consumption BACKUP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
V_{DD} Fixed-Current, BACKUP Mode	I_{DD_FBKUD}	0KB SRAM retained with RTC disabled, retention regulator disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V	0.26	0.36	0.53	0.97	1.7	µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V	0.26	0.36	0.53	0.97	1.7	µA
			V_{DD} = 1.8V, V_{CORE} = 1.1V	0.13	0.15	0.22	0.48	0.99	µA
			V_{DD} = 1.8V, V_{CORE} = 0.855V	0.13	0.15	0.22	0.48	0.99	µA
		20KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V	0.26	0.36	0.53	0.97	1.7	µA

Table 22. Dual-Supply Operation Fixed V_{DD} Current Consumption BACKUP Mode (continued)

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	25°C	55°C	85°C	105°C	
			V_{DD} = 3.3V, V_{CORE} = 0.855V	0.26	0.36	0.53	0.97	1.7	µA
			V_{DD} = 1.8V, V_{CORE} = 1.1V	0.13	0.15	0.22	0.48	0.99	µA
			V_{DD} = 1.8V, V_{CORE} = 0.855V	0.13	0.15	0.22	0.48	0.99	µA
		40KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V	0.26	0.36	0.53	0.97	1.7	µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V	0.26	0.36	0.53	0.97	1.7	µA
			V_{DD} = 1.8V, V_{CORE} = 1.1V	0.13	0.15	0.22	0.48	0.99	µA
			V_{DD} = 1.8V, V_{CORE} = 0.855V	0.13	0.15	0.22	0.48	0.99	µA
		80KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V	0.26	0.36	0.53	0.97	1.7	µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V	0.26	0.36	0.53	0.97	1.7	µA
			V_{DD} = 1.8V, V_{CORE} = 1.1V	0.13	0.15	0.22	0.48	0.99	µA
			V_{DD} = 1.8V, V_{CORE} = 0.855V	0.13	0.15	0.22	0.48	0.99	µA
		160KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V	0.26	0.36	0.53	0.97	1.7	µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V	0.26	0.36	0.53	0.97	1.7	µA
			V_{DD} = 1.8V, V_{CORE} = 1.1V	0.13	0.15	0.22	0.48	0.99	µA
			V_{DD} = 1.8V, V_{CORE} = 0.855V	0.13	0.15	0.22	0.48	0.99	µA

Dual-Supply STORAGE Mode

Table 23. Dual-Supply Operation Fixed V_{CORE} Current Consumption STORAGE Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V_{CORE} Fixed-Current, STORAGE Mode	I_{CORE_FSTOD}	V_{DD} = 3.3V, V_{CORE} = 1.1V	0.064	0.25	0.8	2.58	5.71	µA
		V_{DD} = 3.3V, V_{CORE} = 1.1V	0.009	0.14	0.57	2.02	4.68	µA
		V_{DD} = 1.8V, V_{CORE} = 1.1V	0.064	0.25	0.8	2.57	5.72	µA
		V_{DD} = 1.8V, V_{CORE} = 1.1V	0.007	0.139	0.57	2.03	4.67	µA

Dual-Supply STORAGE Mode

Table 24. Dual-Supply Operation Fixed V_{DD} Current Consumption STORAGE Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	25°C	55°C	85°C	105°C	
V_{DD} Fixed-Current, STORAGE Mode	I_{DD_FSTOD}	V_{DD} = 3.3V, V_{CORE} = 1.1V	0.22	0.32	0.49	0.93	1.66	µA
		V_{DD} = 3.3V, V_{CORE} = 1.1V	0.21	0.31	0.48	0.92	1.64	µA
		V_{DD} = 1.8V, V_{CORE} = 1.1V	0.092	0.11	0.19	0.44	0.95	µA
		V_{DD} = 1.8V, V_{CORE} = 1.1V	0.092	0.11	0.19	0.44	0.95	µA

Ordering Information

PART NUMBER	SPI	I²C	TMR	LPTMR	UART	LPUART	I²S	ROM BOOT LOADER	SECURE BOOT	GPIO	DEFAULT SYS_OSC	PIN-PACKAGE
MAX32670GTL+	2	3	4	2	3	2	1	Yes	No	31	IPO	40 TQFN-EP, 5mm x 5mm, 0.4mm pitch
MAX32670GTL+T	2	3	4	2	3	2	1	Yes	No	31	IPO	40 TQFN-EP 5mm x 5mm, 0.4mm pitch
MAX32670GLL+	2	3	4	2	3	2	1	Yes	No	31	IBRO	40 TQFN-EP, 5mm x 5mm, 0.4mm pitch
MAX32670GLL+T	2	3	4	2	3	2	1	Yes	No	31	IBRO	40 TQFN-EP 5mm x 5mm, 0.4mm pitch
MAX32670BGWG+	2	2	4	1	3	1	0	Yes	No	17	IBRO	24 WLP 1.75mm x 2.50mm, 0.4mm pitch
MAX32670BGWG+T	2	2	4	1	3	1	0	Yes	No	17	IBRO	24 WLP 1.75mm x 2.50mm, 0.4mm pitch

All versions provide 384KB (376KB user) of flash memory, 160KB SRAM, one RTC, CRC and AES accelerators, TRNG, SWD, and two WDT.

I²S = Integrated Inter-IC Sound Bus Interface

SPI = serial peripheral interface

I²C = Inter-Integrated Circuit Interface

TMR = 32-bit timer

LPTMR = low-power 32-bit timer

UART = universal asynchronous receiver-transmitter

LPUART = low-power UART

WDT = watchdog timer

GPIO = general-purpose I/O pins

SYS_OSC = system oscillator

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/20	Initial release	—
1	5/20	Added MAX32671 and updated *Pin Descriptions*.	1–44
2	5/21	Updated *Pin Descriptions*. Updated *Simplified Block Diagram*. Added Bootloader and Secure Boot descriptions. Added new Bootloader Activation description in *Applications Information*. Added ERTCO stability capacitor requirements. Updated the *Clocking Scheme*. Changed the ERFO frequency range.	1, 2, 23, 32–35, 36, 39, 42–44
3	5/22	Updated *Benefits and Features*, the *POWER* section of the *Electrical Characteristics* table, and the *Pin Description* table. Removed *UART* speed indication. Updated the *Bootloader Activation* section in Applications Information. Added temperature variance Table 6 through Table 20 to the *Applications Information* section.	1, 8–14, 16–26, 36-38, 45, 48–55
4	1/24	Removed references to max UART Speed, removed ECC functionality, removed MAX32671, replaced master/slave with controller/target wording, clarified RSTN causes a system reset, clarified the last page of flash memory is reserved for system use, clarified I^2S operates in both controller and target modes, removed requirement for 32KIN/32KOUT capacitors, clarified why some SRAM is not retained in *BACKUP* mode, maximum storage temperature changed from 150°C to 125°C, added *RTC Crystal Guidelines*, added 32KIN V_{IH} and V_{IL} values, clarified TQFN is TQFN-EP package, clarified that 40 TQFN has 2 SPI interfaces, added slew rate requirement to V_{DD} specification in Electrical Conditions, indicated which events test bootloader activation pins, corrected Single-Wire Debug to Serial Wire Debug, added number of peripheral instances and default oscillator to *Ordering Information*	All
5	4/24	Added 24 WLP Pin Configuration drawing and 24WLP Pin Description and 24 WLP package information, updated detailed description and *Ordering Information* with information on 24 WLP, clarified that only 376KB of 384KB flash is available as the last 8KB page of memory is reserved for system use, clarified 32-bit timers do not have down count capability, corrected I^2C $t_{VD;DAT}$ and $t_{VD;ACK}$ from min values to max values, added MAX32670GLL+ and MAX32670GLL+T part numbers, corrected f_{INRO} frequency typical value from 70kHz to 80kHz in *Electrical Characteristics* table.	1, 2, 7, 8, 25, 28-32, 37-48, 52, 54, 55, 59