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MAX77542

16V_{IN}/16A, Quad-Phase High-Efficiency Buck Converter

General Description

The MAX77542 is a high-efficiency step-down converter with four 4A switching phases. It uses an adaptive constant on-time (COT) current-mode control scheme and its flexible architecture supports five phase configurations. Its wide input-voltage range enables a direct conversion for less than 1V outputs from 1 to 3-cell Li+ batteries and USB power delivery (PD) supply rails. The output voltages are preset with resistors and are further adjustable through an I^2C-compatible interface.

Flexible sequencer and programmable soft-start/soft-stop slew rates provide controlled transitions between operating states. Programmable switching frequency, frequency tracking, and spread-spectrum features allow easier system optimization for noise-sensitive applications. Multifunction I/Os allow for flexible control of each output for EN, LPM, FPWM, POK, RSTINB, and RSTOB status. An array of built-in protections ensures safe operation under abnormal operating conditions.

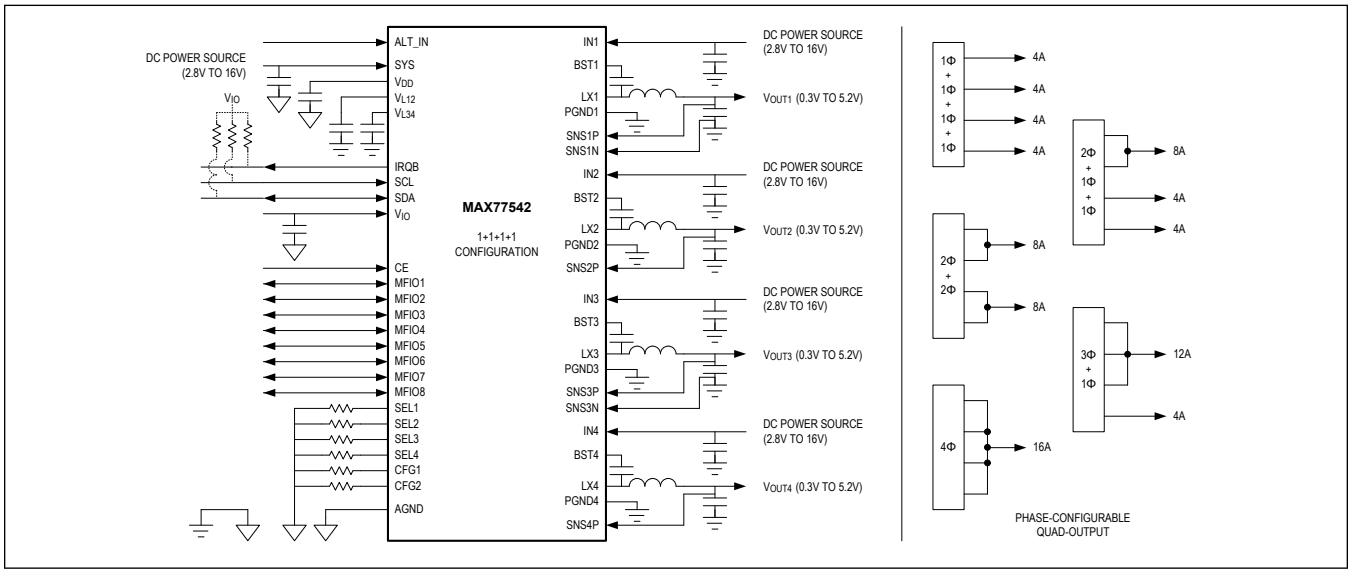
Applications

- 1 to 3-Cell Li+ and USB-C Power Delivery Systems
- Audio/Video Equipment and PCIe/RAID Cards
- Application Processors, FPGAs, DSPs, and ASICs

Benefits and Features

- 2.8V to 16V Input-Voltage Range
- 0.3V to 5.2V Output-Voltage Range
- Max 16A (4A/Φ) with Five Phase Configurations
- ±0.5% V_{OUT} Accuracy (Default V_{OUT} at +25°C)
- 94% Peak Efficiency (7.6V_{IN}, 3.3V_{OUT}, 1MHz)
- Auto Skip/PWM Transition and Low-Power Mode
- Drop-Out Operation with 98% of Max Duty Cycle
- Differential Output-Voltage Sensing
- Flexible Sequencer with Soft-Start/Soft-Stop Slew Rates
- Prebiased Startup and Active Output Discharge
- 0.5MHz/1.0MHz/1.5MHz Nominal Switching Frequency
- Spread-Spectrum Modulation for EMI Reduction
- Internal/External Frequency Tracking
- Default V_{OUT} and Phase Configuration Setting by R_{SELx}
- Multifunction I/Os for EN, LPM, FPWM, and POK
- UVLO, Thermal-Shutdown, and Short-Circuit Protection
- High-Speed, I^2C Serial Interface
- Available in 60-Bump WLP (4.36mm x 2.56mm x 0.65mm)
- Less than 115mm^2 Total Solution Size with 2520 Inductors

Typical Applications Circuit



Typical Application Circuits continued at end of data sheet.
Ordering Information appears at end of data sheet.

19-101666; Rev 1; 5/23

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Absolute Maximum Ratings

SYS to AGND ..... -0.3V to +17.6V
ALT_IN to AGND ..... -0.3V to +6.0V
V_{DD} to AGND ..... -0.3V to +2.2V
V_{L12}, V_{L34} to AGND, PGND ..... -0.3V to +2.2V
CE to AGND ..... -0.3V to min (V_{SYS} + 0.3, +17.6)V
CFGx to AGND ..... -0.3V to min (V_{DD} + 0.3, +2.2)V
SELx to AGND ..... -0.3V to min (V_{DD} + 0.3, +2.2)V
INx to PGNDx, AGND ..... -0.3V to +17.6V
LXx to PGNDx ..... -0.3V to +17.6V
LXx to PGNDx (less than 10ns) ..... (V_{IN} - 22)V to +22V
BSTx to LXx ..... -0.3V to +2.2V
SNSxP to AGND ..... -0.3V to +12.0V
SNSxN to AGND ..... -0.3V to +0.3V
PGNDx to AGND ..... -0.3V to +0.3V
V_{IO} to AGND ..... -0.3V to +2.2V
SCL to AGND ..... -0.3V to +2.2V
SDA to AGND ..... -0.3V to +2.2V
IRQB to AGND ..... -0.3V to +2.2V
MFIOx to AGND ..... -0.3V to min (V_{IO} + 0.3, +2.2)V
Continuous Power Dissipation (JESD51-7, T_A = +70ºC)
60 WLP (derate 25.4mW/°C above +70°C) 2037mW
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: LXx has internal clamp diodes to its corresponding PGNDx and INx. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

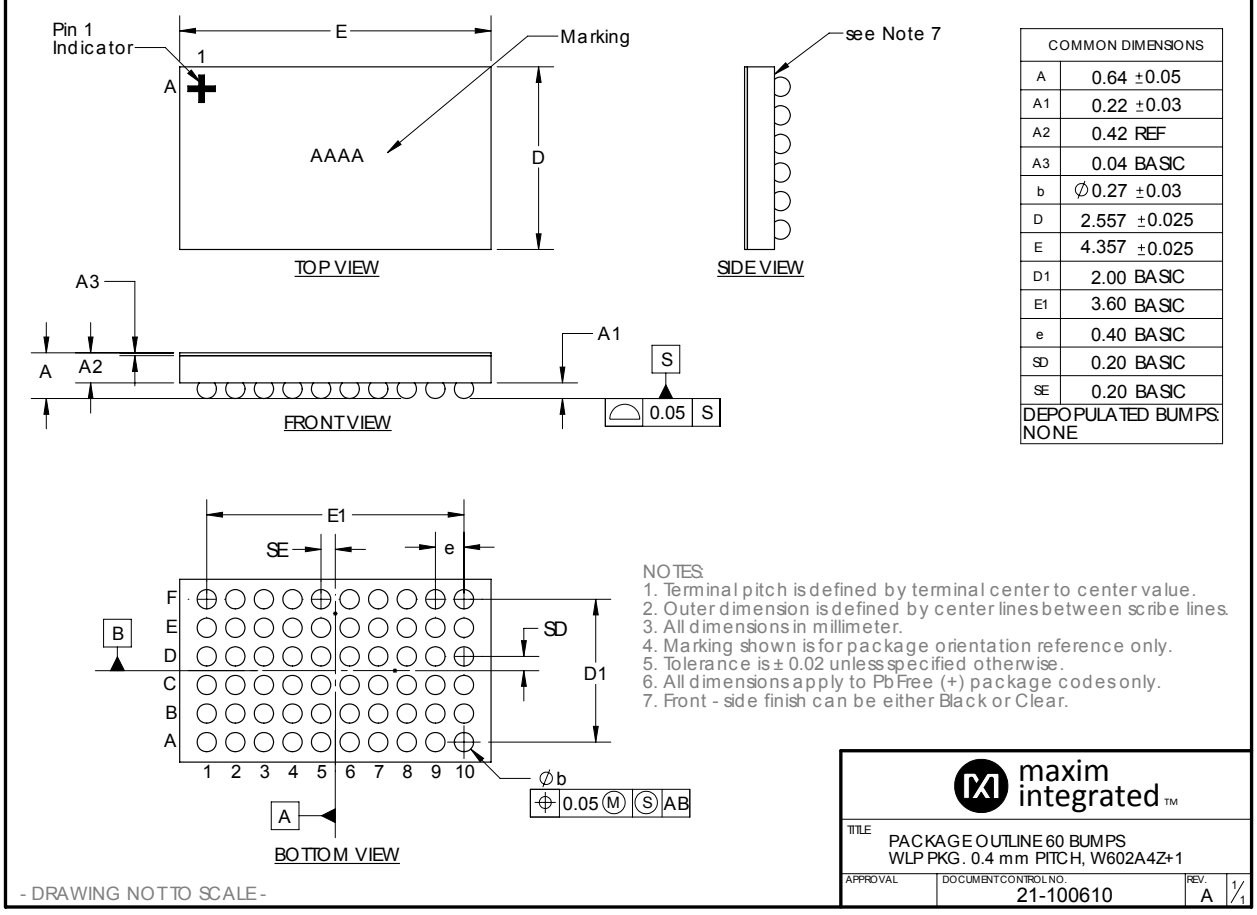
PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Input Voltage Range	V_{IN}		2.8 to 16	V
Output Current Range	I_{OUT}	For continuous operation at 4A, the junction temperature (T_J) is limited to +120ºC; if the junction temperature is higher than +120ºC, the expected lifetime at 4A continuous operation is derated	0 to 4	A
Junction Temperature Range	T_J		-40 to +125	ºC

Note: These limits are not guaranteed.

Package Information

60 WLP (Thick UBM)

Packkage Code	W602A4Z+1
Outline Number	21-100610
Land Pattern Number	*Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	39.27°C/W



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.22 ±0.03
A2	0.42 REF
A3	0.04 BASIC
b	∅0.27 ±0.03
D	2.557 ±0.025
E	4.357 ±0.025
D1	2.00 BASIC
E1	3.60 BASIC
e	0.40 BASIC
SD	0.20 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to Pb Free (+) package codes only.
7. Front - side finish can be either Black or Clear.

maxim integrated™

TITLE: PACKAGE OUTLINE 60 BUMPS WLP PKG. 0.4 mm PITCH, W602A4Z+1

APPROVAL | DOCUMENT CONTROL NO. 21-100610 | REV. A | 1/1

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics—Top-Level

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 0.8V (M1_RNG = 0x0), V_{OUT2} = 1.1V (M2_RNG = 0x1), V_{OUT3} = 1.8V (M3_RNG = 0x1), V_{OUT4} = 3.3V (M4_RNG = 0x2), single-phase configuration, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT VOLTAGE AND SUPPLY CURRENT							
SYS and INx Voltage Range	V_{SYS}, V_{INx}			2.8		16	V
SYS Undervoltage Lock-Out (UVLO)	V_{UVLO_R}	V_{SYS} rising		2.8	2.9	3.0	V
	V_{UVLO_F}	V_{SYS} falling with 200mV of hysteresis		2.6	2.7	2.8	
Power-On Reset (POR) Threshold (Note 7)	V_{POR}	V_{SYS} falling			1.7		V
Shutdown Supply Current (Note 3)	I_{SHDN}	V_{CE} = 0V, T_J = -40°C to +85°C			1.5	15	µA
Standby Supply Current (Note 3)	I_{STBY}	FTMON_EN = 0, all bucks are disabled, T_J = -40°C to +85°C			25	60	µA
Quiescent Supply Current in LP-Skip Mode (Note 3)	$I_{Q\_LP-SKIP}$	V_{ALT_IN} = 0V, V_{OUT} > $V_{OUT(TARGET)}$, no load	Only one buck phase is enabled		270	370	µA
			Two buck phases are enabled		380	480	
			Three buck phases are enabled		505	635	
			All buck phases are enabled		625	755	
Quiescent Supply Current in Skip Mode (Note 3)	I_{Q_SKIP}	V_{ALT_IN} = 0V, V_{OUT} > $V_{OUT(TARGET)}$, no load	Only one buck phase is enabled		300	405	µA
			Two buck phases are enabled		450	555	
			Three buck phases are enabled		620	750	
			All buck phases are enabled		780	910	
INTERNAL BIAS SUPPLY							
V_{DD} Regulator Voltage	V_{DD}				1.9		V
V_{DD} Undervoltage Lock-Out (UVLO)	$V_{DD\_UVLO\_F}$				1.55		V
V_{L12}, V_{L34} Regulator Voltage	V_{Lx}				1.8		V
V_{L12}, V_{L34} Undervoltage Lock-Out (UVLO)	$V_{L\_UVLO\_F}$				1.55		V
ALT_IN Switchover Threshold	V_{SWO}	V_{ALT_IN} rising, 100mV hysteresis, V_L and V_{DD} input switches from SYS to ALT_IN above this threshold		2.7	2.8	2.9	V
ALT_IN Valid Voltage Range	V_{ALT_IN}			V_{SWO}		5.5	V
ALT_IN Shutdown Supply Current	$I_{ALT\_IN\_SHDN}$	V_{CE} = 0V, V_{ALT_IN} = 3.3V			0.2		µA

Electrical Characteristics—Top-Level (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 0.8V (M1_RNG = 0x0), V_{OUT2} = 1.1V (M2_RNG = 0x1), V_{OUT3} = 1.8V (M3_RNG = 0x1), V_{OUT4} = 3.3V (M4_RNG = 0x2), single-phase configuration, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. *Note 2*.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
THERMAL PROTECTION							
Thermal Warning	T_{WARN}	T_J rising, 15°C hysteresis	TWARN_TH[2:0] = 0x0		+95		°C
			TWARN_TH[2:0] = 0x1		+100		
			TWARN_TH[2:0] = 0x2		+105		
			TWARN_TH[2:0] = 0x3		+110		
			TWARN_TH[2:0] = 0x4		+115		
			TWARN_TH[2:0] = 0x5 (default)		+120		
			TWARN_TH[2:0] = 0x6		+125		
			TWARN_TH[2:0] = 0x7		+130		
Thermal Shutdown (TSHDN)	T_{SHDN}	T_J rising, 15°C hysteresis			+165		°C
FLEXIBLE POWER SEQUENCER (FPS)							
Sequence Start Delay	t_{DLY_SEQ}	Delay from rising edge of FPS_EN signal to V_{OUTx} ramping start-off in the 1st time slot	V_{Lx} is enabled		100		µs
Time Slot Delay Step	t_{DLY_STEP}	DLY_STEP[1:0] = 0x0			0.5		ms
		DLY_STEP[1:0] = 0x1			1.0		
		DLY_STEP[1:0] = 0x2			2.0		
		DLY_STEP[1:0] = 0x3			4.0		
Time Slot Accuracy	f_{OSC_ACC}	Root oscillator accuracy		-5		+5	%
LOGIC INPUT AND OUTPUT							
CE Input Logic High Threshold	V_{IH_CE}	CE_PD_EN = 0		1.1			V
		CE_PD_EN = 1		1.5			
CE Input Logic Low Threshold	V_{IL_CE}					0.4	V
IRQB Output Logic Low Threshold	V_{OL_IRQB}	Sinking 2mA				0.2	V
CE Pull-Down Current	I_{PD_CE}	CE_PD_EN = 1	1.1V ≤ V_{CE} ≤ 16V	0.5	1.7	4.0	µA
			V_{CE} ≤ 0.4V		100	200	nA
CE Leakage Current	I_{LKG_CE}	V_{SYS} = 16V, V_{CE} = 0V and 16V, CE_PD_EN = 0	T_J = +25°C		±0.1		µA
			T_J = +85°C (*Note 5*)		±0.5		

Electrical Characteristics—Top-Level (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 0.8V (M1_RNG = 0x0), V_{OUT2} = 1.1V (M2_RNG = 0x1), V_{OUT3} = 1.8V (M3_RNG = 0x1), V_{OUT4} = 3.3V (M4_RNG = 0x2), single-phase configuration, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. *Note 2*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IRQB Leakage Current	I_{LKG_IRQB}	IRQB set to high impedance (i.e., no interrupt pending), V_{IRQB} = 0V and 2.0V	-1		+1	µA

Electrical Characteristics—Quad-Phase Configurable Buck Converter

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 0.8V (M1_RNG = 0x0), V_{OUT2} = 1.1V (M2_RNG = 0x1), V_{OUT3} = 1.8V (M3_RNG = 0x1), V_{OUT4} = 3.3V (M4_RNG = 0x2), single-phase configuration, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input-Voltage Range	V_{INx}		2.8		16	V
DC OUTPUT VOLTAGE AND ACCURACY						
Output-Voltage Range	V_{OUT_RNG}	Low range (Mx_RNG[1:0] = 0x0)	0.3		1.3	V
		Mid range (Mx_RNG[1:0] = 0x1)	0.6		2.6	
		High range (Mx_RNG[1:0] = 0x2)	1.2		5.2	
Line Regulation		1Φ, FPWM mode, V_{INx} = 2.8V to 16V, V_{OUT} = default, I_{OUT} = 0A	-0.1		+0.1	%/V
Load Regulation		1Φ, FPWM mode, I_{OUT} = 0A to 4A (*Note 7*)		0.1		%/A

Electrical Characteristics—Quad-Phase Configurable Buck Converter (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 0.8V (M1_RNG = 0x0), V_{OUT2} = 1.1V (M2_RNG = 0x1), V_{OUT3} = 1.8V (M3_RNG = 0x1), V_{OUT4} = 3.3V (M4_RNG = 0x2), single-phase configuration, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC Output-Voltage Accuracy	V_{OUT_ACC}	1Φ, FPWM mode, V_{INx} = 2.8V to 16V, I_{OUT} = 0A, T_A = T_J = 0°C to +85°C	0.3V ≤ V_{OUT} < 0.5V (Mx_RNG = 0x0)	-3.0		+3.0	%
			0.5V ≤ V_{OUT} < 0.8V (Mx_RNG = 0x0)	-2.0		+2.0	
			0.8V ≤ V_{OUT} ≤ 1.3V (Mx_RNG = 0x0)	-1.0		+1.0	
			0.6V ≤ V_{OUT} < 1.2V (Mx_RNG = 0x1)	-3.0		+3.0	%
			1.2V ≤ V_{OUT} < 1.9V (Mx_RNG = 0x1)	-1.5		+1.5	
			1.9V ≤ V_{OUT} ≤ 2.6V (Mx_RNG = 0x1)	-1.0		+1.0	
			1.2V ≤ V_{OUT} < 2.2V (Mx_RNG = 0x2)	-3.0		+3.0	
			2.2V ≤ V_{OUT} < 3.6V (Mx_RNG = 0x2)	-1.5		+1.5	
			3.6V ≤ V_{OUT} ≤ 5.2V (Mx_RNG = 0x2)	-1.0		+1.0	
		1Φ, FPWM mode, V_{INx} = 2.8V to 16V, I_{OUT} = 0A	V_{OUT} = factory default, T_J = +25°C	-0.5		+0.5	
POWER STAGE							
High-Side MOSFET Peak Current Limit	I_{PLIM}	Mx_ILIM[1:0] = 0x0		3.1	3.5	3.9	A
		Mx_ILIM[1:0] = 0x1		4.0	4.5	5.0	
		Mx_ILIM[1:0] = 0x2		4.9	5.5	6.1	
		Mx_ILIM[1:0] = 0x3		5.4	6.0	6.6	
Low-Side MOSFET Valley Current Limit	I_{VLIM}	Tracks I_{PLIM}			I_{PLIM} - 1		A
Low-Side MOSFET Negative Current Limit	I_{NLIM}	FPWM mode		-3.6	-3.0	-2.4	A
Low-Side MOSFET Zero-Crossing Current Threshold	I_{ZX}	Skip or LP-skip mode			150		mA
High-Side MOSFET On-Resistance	R_{ON_HS}	1Φ, I_{LXx} = 190mA			35	70	mΩ

Electrical Characteristics—Quad-Phase Configurable Buck Converter (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 0.8V (M1_RNG = 0x0), V_{OUT2} = 1.1V (M2_RNG = 0x1), V_{OUT3} = 1.8V (M3_RNG = 0x1), V_{OUT4} = 3.3V (M4_RNG = 0x2), single-phase configuration, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Side MOSFET On-Resistance	R_{ON_LS}	1Φ, I_{LXx} = -190mA			18	40	mΩ
Nominal Switching Frequency	F_{SW}	FPWM mode, no load, no external clock, T_J = +25°C (Note 4)	Mx_FREQ[1:0] = 0x0		0.5		MHz
			Mx_FREQ[1:0] = 0x1		1		
			Mx_FREQ[1:0] = 0x2		1.5		
Maximum Duty Cycle	D_{MAX}	Drop-out region (V_{OUT} falls below its regulation target)		97	98		%
LX Active Discharge Resistance	R_{AD1}	1Φ, buck output disabled, active discharge enabled (Mx_ADIS1 = 1), resistance from corresponding LX_X to PGNDx			1		Ω
	R_{AD100}	1Φ, buck output disabled, active discharge enabled (Mx_ADIS100 = 1), resistance from corresponding LX_X to PGNDx			100		
LX Leakage Current	I_{LX_LKG}	1Φ, V_{LXx} = 0V or 16V, Mx_ADIS100 = 0	T_J = +25°C		1	15	µA
			T_J = -40°C to +85°C (Note 5)		1		
SLEW RATE AND TIMING							
Soft-Start Slew Rate (Note 6)	$\Delta V_{OUT}/\Delta t$	Mx_SSTRT_SR[2:0] = 0x0			0.15		mV/µs
		Mx_SSTRT_SR[2:0] = 0x1			0.625		
		Mx_SSTRT_SR[2:0] = 0x2			1.25		
		Mx_SSTRT_SR[2:0] = 0x3			2.5		
		Mx_SSTRT_SR[2:0] = 0x4			5		
		Mx_SSTRT_SR[2:0] = 0x5			10		
		Mx_SSTRT_SR[2:0] = 0x6			20		
		Mx_SSTRT_SR[2:0] = 0x7			40		
Soft-Stop Slew Rate (Note 6)	$\Delta V_{OUT}/\Delta t$	Mx_SSTOP_SR[2:0] = 0x0			-0.15		mV/µs
		Mx_SSTOP_SR[2:0] = 0x1			-0.625		
		Mx_SSTOP_SR[2:0] = 0x2			-1.25		
		Mx_SSTOP_SR[2:0] = 0x3			-2.5		
		Mx_SSTOP_SR[2:0] = 0x4			-5		
		Mx_SSTOP_SR[2:0] = 0x5			-10		
		Mx_SSTOP_SR[2:0] = 0x6			-20		
		Mx_SSTOP_SR[2:0] = 0x7			-40		

Electrical Characteristics—Quad-Phase Configurable Buck Converter (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 0.8V (M1_RNG = 0x0), V_{OUT2} = 1.1V (M2_RNG = 0x1), V_{OUT3} = 1.8V (M3_RNG = 0x1), V_{OUT4} = 3.3V (M4_RNG = 0x2), single-phase configuration, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Ramp-Up Slew Rate (Note 6)	$\Delta V_{OUT}/\Delta t$	Mx_RU_SR[2:0] = 0x0			0.15		mV/µs
		Mx_RU_SR[2:0] = 0x1			0.625		
		Mx_RU_SR[2:0] = 0x2			1.25		
		Mx_RU_SR[2:0] = 0x3			2.5		
		Mx_RU_SR[2:0] = 0x4			5		
		Mx_RU_SR[2:0] = 0x5			10		
		Mx_RU_SR[2:0] = 0x6			20		
		Mx_RU_SR[2:0] = 0x7			40		
Ramp-Down Slew Rate (Note 6)	$\Delta V_{OUT}/\Delta t$	Mx_RD_SR[2:0] = 0x0			-0.15		mV/µs
		Mx_RD_SR[2:0] = 0x1			-0.625		
		Mx_RD_SR[2:0] = 0x2			-1.25		
		Mx_RD_SR[2:0] = 0x3			-2.5		
		Mx_RD_SR[2:0] = 0x4			-5		
		Mx_RD_SR[2:0] = 0x5			-10		
		Mx_RD_SR[2:0] = 0x6			-20		
		Mx_RD_SR[2:0] = 0x7			-40		
Slew-Rate Accuracy		REFDAC slew-rate accuracy		-5		+5	%
Turn-On Delay	t_{DLY}	Delay from rising edge of EN_Mx (MFIOx) signal to V_{OUTx} ramping start-off	V_{Lx} is pre-enabled		90	110	µs
			V_{Lx} is not pre-enabled		110	150	
FREQUENCY TRACKING							
External Frequency Tracking Lockable Range (Note 6)	F_{FTRAK}	Expressed as a percentage of the nominal frequency set by Mx_FREQ[1:0]		95		105	%
SPREAD-SPECTRUM							
Modulation Frequency (Note 6)	F_{SS_MOD}	Mx_SS_FREQ[1:0] = 0x0			1		kHz
		Mx_SS_FREQ[1:0] = 0x1			3		
		Mx_SS_FREQ[1:0] = 0x2			5		
		Mx_SS_FREQ[1:0] = 0x3			7		
Modulation Envelope	ΔF_{SS}	Mx_SS_ENV[1:0] = 0x1			±8		%
		Mx_SS_ENV[1:0] = 0x2			±12		
		Mx_SS_ENV[1:0] = 0x3			±16		
POWER-OK AND SHORT-CIRCUIT PROTECTION							
Power-OK Rising Threshold	V_{POK_R}	Expressed as a percentage of V_{OUT}		77	82	87	%
Power-OK Falling Threshold	V_{POK_F}	Expressed as a percentage of V_{OUT}		73	78	83	%

Electrical Characteristics—Quad-Phase Configurable Buck Converter (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 0.8V (M1_RNG = 0x0), V_{OUT2} = 1.1V (M2_RNG = 0x1), V_{OUT3} = 1.8V (M3_RNG = 0x1), V_{OUT4} = 3.3V (M4_RNG = 0x2), single-phase configuration, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-OK Fault Time-Out (*Note 6*)	t_{POK_TO}	POK_TO[1:0] = 0x1		1		ms
		POK_TO[1:0] = 0x2		5		
		POK_TO[1:0] = 0x3		10		
Short-Circuit Detection Threshold	V_{SCP}	V_{OUT} falling, expressed as a percentage of target V_{OUT}		20		%

Electrical Characteristics—Multifunction I/Os

(V_{SYS} = 12V, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MULTIFUNCTION I/O (MFIO)							
MFIO Input Logic High Threshold	V_{IH}			0.75 x V_{IO}			V
MFIO Input Logic Low Threshold	V_{IL}					0.25 x V_{IO}	V
MFIO Output High Voltage	V_{OH_MFIO}	Push-pull output mode, sourcing 2mA		0.8 x V_{IO}			V
MFIO Output Low Voltage	V_{OL_MFIO}	Sinking 2mA				0.2	V
MFIO Input Debounce Time	t_{DB_MFIO}	MFIOx_DEB[2:0] = 0x0			0		µs
		MFIOx_DEB[2:0] = 0x1			0.5		
		MFIOx_DEB[2:0] = 0x2			1		
		MFIOx_DEB[2:0] = 0x3			2		
		MFIOx_DEB[2:0] = 0x4			4		
		MFIOx_DEB[2:0] = 0x5			8		
		MFIOx_DEB[2:0] = 0x6			16		
		MFIOx_DEB[2:0] = 0x7			32		
MFIO Pull-Down Resistance	R_{PD_MFIO}	Input mode, MFIOx_PDPU = 0x0		400	800	1600	kΩ
		Input mode, MFIOx_PDPU = 0x1		50	100	200	
MFIO Pull-Up Resistance	R_{PU_MFIO}	Input mode, MFIOx_PDPU = 0x2		50	100	200	kΩ
MFIO Leakage Current	I_{LK_MFIO}	V_{MFIOx} = 0V and 2.0V, MFIOx_PDPU = 0x3	T_J = +25°C	-1.5	0.01	1.5	µA
			T_J = +85°C (*Note 5*)		0.1		

Electrical Characteristics—ADC

(V_{SYS} = 12V, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
READBACK ACCURACY (*Note 7*)							
Output-Current Readback Accuracy	I_{OUT_ADC}	1Φ, I_{OUT} = $I_{OUT(MAX)}$	T_J = -40°C to +85°C		5		%
			T_J = +125°C		7.5		
Output-Voltage Readback Accuracy	V_{OUT_ADC}	T_J = -40°C to +85°C			3		%
		T_J = +125°C			5		
SYS Input-Voltage Readback Accuracy	V_{SYS_ADC}	3.0V ≤ V_{SYS} ≤ 16V	T_J = -40°C to +85°C		3		%
			T_J = +125°C		5		
Junction Temperature Readback Accuracy	T_{J_ADC}	T_J = +85°C to +125°C			5		%
MFIO Voltage Readback Accuracy	V_{MFIO_ADC}	T_J = -40°C to +85°C			3		%
		T_J = +125°C			5		
TIMING (*Note 6*)							
Clock Frequency	f_{ADC}				1		MHz
ADC Startup Time	t_{ADC_SU}	One of buck outputs is enabled			22		µs
		All buck outputs are disabled			26		
ADC Sampling Time	t_{SAMPLE}	Per channel	I_{OUTx}, T_J		1		ms
			V_{OUTx}, V_{SYS}, V_{MFIOx}		18		µs
Conversion Time	t_{CONV}	Per channel			18		µs
Sampling Interval for Averaging Mode	t_{INT_AVG}	Sampling interval for the same channel in averaging mode			5		ms
Sampling Interval for Continuous Measurement	t_{INT_CONT}	Sampling interval for the same channel during continuous measurement operation			1		s

Electrical Characteristics—I^2C Serial Interface

(V_{SYS} = 12V, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O STAGE						
V_{IO} Supply Voltage	V_{IO}		1.1	1.8	2.0	V
V_{IO} Dynamic Supply Current	I_{IO}	f_{SCL} = f_{SDA} = 3.4MHz, V_{CE} = 1.8V, all bucks are disabled		5		µA
SYS Dynamic Supply Current	I_{SYS}	f_{SCL} = f_{SDA} = 3.4MHz, V_{CE} = 1.8V, all bucks are disabled		40		µA
V_{IO} Undervoltage Lock-Out (UVLO)	$V_{IO\_UVLO\_R}$	V_{IO} rising	1.06	1.09	1.12	V
	$V_{IO\_UVLO\_F}$	V_{IO} falling	0.96	0.99	1.02	
SCL, SDA Input Logic Low Threshold	V_{IL}				0.25 x V_{IO}	V

Electrical Characteristics—I²C Serial Interface (continued)

(V_{SYS} = 12V, V_{CE} = 1.8V, V_{IO} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL, SDA Input Logic High Threshold	V_{IH}		0.75 x V_{IO}			V
SCL, SDA Input Hysteresis	V_{HYS}			0.3		V
SDA Output Logic Low Threshold	V_{OL_SDA}	Sinking 20mA			0.2	V
SCL, SDA Input Leakage Current	I_{LKG}	V_{SCL} = V_{SDA} = 0V or 2.0V	-10		+10	µA
SCL, SDA Pin Capacitance		(Note 7)		10		pF
STANDARD, FAST, AND FAST MODE PLUS TIMING						
Clock Frequency	f_{SCL}				1	MHz
Hold Time (Repeated) Start Condition	$t_{HD;STA}$		260			ns
SCL Low Period	t_{LOW}		500			ns
SCL High Period	t_{HIGH}		260			ns
Setup Time Repeated Start Condition	$t_{SU;STA}$		260			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Data Setup Time	$t_{SU;DAT}$		50			ns
Setup Time for Stop Condition	$t_{SU;STO}$		260			ns
Bus Free Time Between Stop and Start Condition	t_{BUF}		0.5			µs
Input Filter Suppressed Spike Pulse Width	t_{SP}	(Note 7)		50		ns
HIGH-SPEED MODE TIMING						
Clock Frequency	f_{SCL}	High-speed mode			3.4	MHz
Setup Time Repeated Start Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) Start Condition	$t_{HD;STA}$		160			ns
SCL Low Period	t_{LOW}		160			ns
SCL High Period	t_{HIGH}		60			ns
Data Setup Time	$t_{SU;DAT}$		10			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Setup Time for Stop Condition	$t_{SU;STO}$		160			ns
Input Filter Suppressed Spike Pulse Width	t_{SP}	(Note 7)		10		ns

Note 2: The MAX77542 is tested under pulsed load conditions such that $T_J \approx T_A$. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) are guaranteed by design and characterization using statistical process control methods. Note that the maximum ambient temperature consistent with this specification is determined by specific operating conditions, board layout, rated package thermal impedance, and other environmental factors.

Note 3: Supply Current = I_{SYS} + I_{IN1} + I_{IN2} + I_{IN3} + I_{IN4}.

Note 4: Switching frequency is not set by a clock oscillator. F_{SW} varies depending on input voltage, output voltage, load, and spread-spectrum settings.

Note 5: Guaranteed by ATE characterization. Not directly tested in production.

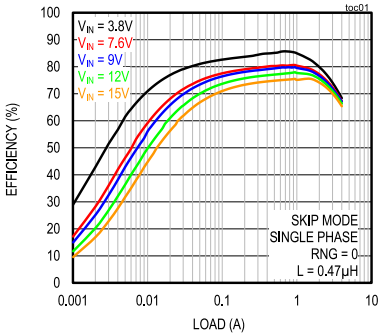
Note 6: Guaranteed by design. Production tested through scan.

Note 7: Not production tested. Design guidance only.

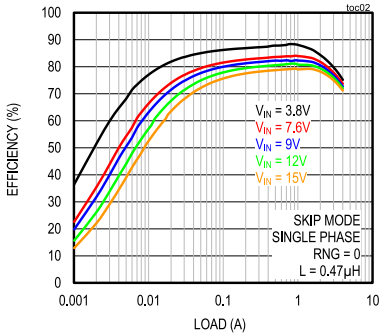
Typical Operating Characteristics

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 1.0V, single-phase configuration, V_{VIO} = 1.8V, skip mode, T_A = +25°C, unless otherwise noted.)

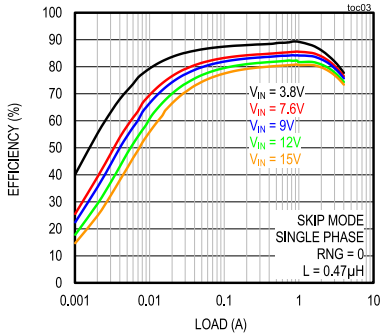
EFFICIENCY vs. LOAD
0.5V OUTPUT



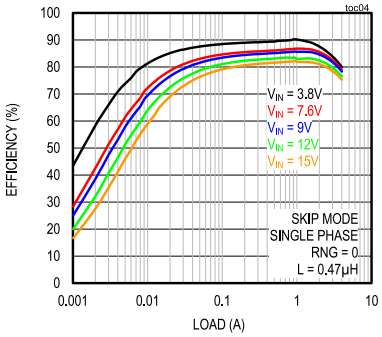
EFFICIENCY vs. LOAD
0.72V OUTPUT



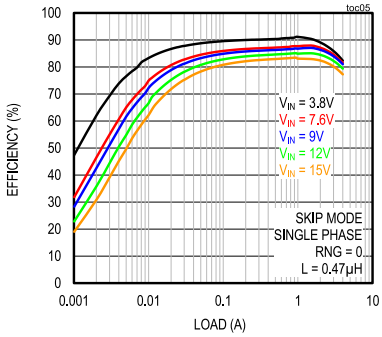
EFFICIENCY vs. LOAD
0.85V OUTPUT



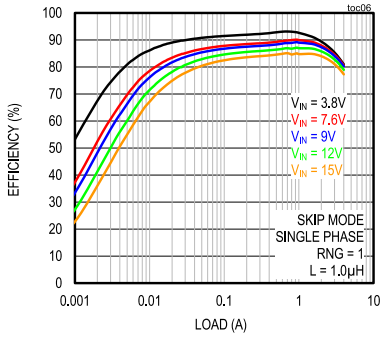
EFFICIENCY vs. LOAD
1.0V OUTPUT



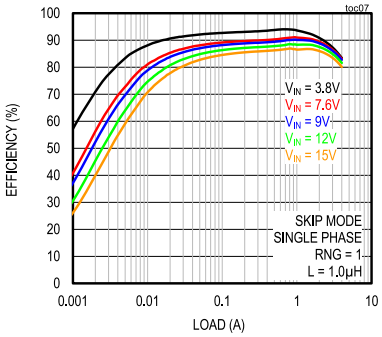
EFFICIENCY vs. LOAD
1.2V OUTPUT



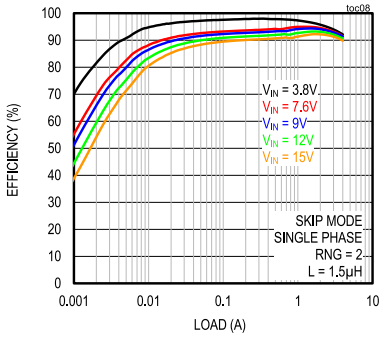
EFFICIENCY vs. LOAD
1.5V OUTPUT



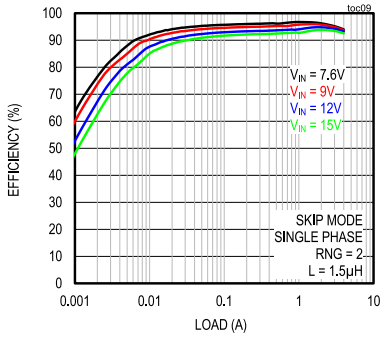
EFFICIENCY vs. LOAD
1.8V OUTPUT



EFFICIENCY vs. LOAD
3.3V OUTPUT



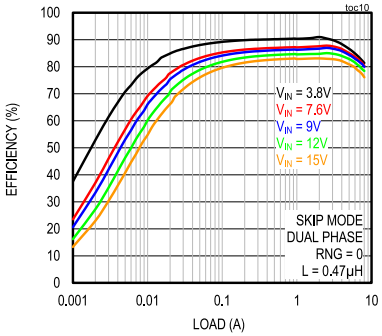
EFFICIENCY vs. LOAD
5.0V OUTPUT



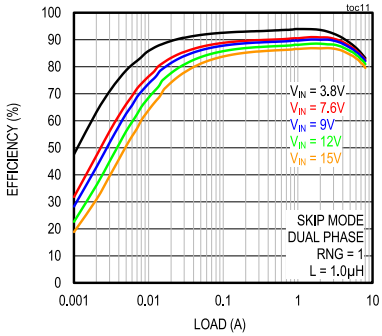
Typical Operating Characteristics (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 1.0V, single-phase configuration, V_{VIO} = 1.8V, skip mode, T_A = +25°C, unless otherwise noted.)

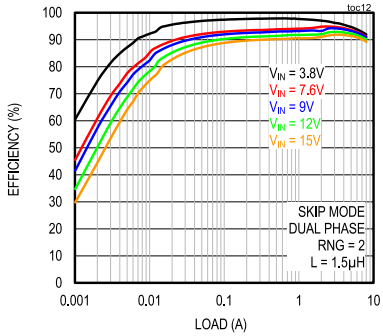
EFFICIENCY vs. LOAD
1.2V OUTPUT



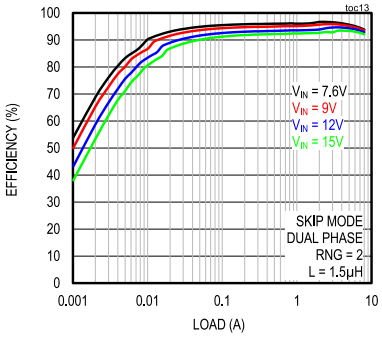
EFFICIENCY vs. LOAD
1.8V OUTPUT



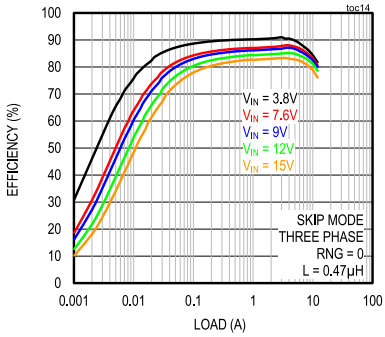
EFFICIENCY vs. LOAD
3.3V OUTPUT



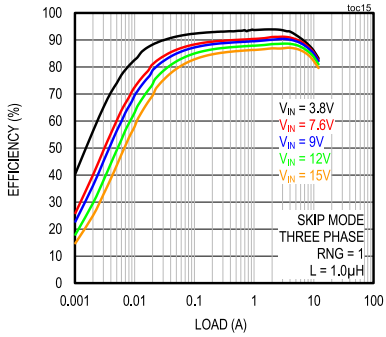
EFFICIENCY vs. LOAD
5.0V OUTPUT



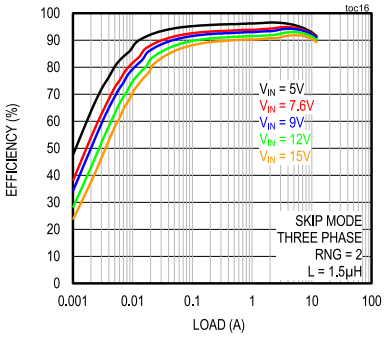
EFFICIENCY vs. LOAD
1.2V OUTPUT



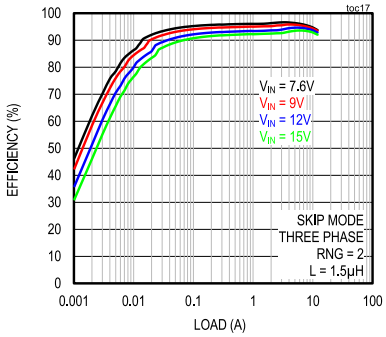
EFFICIENCY vs. LOAD
1.8V OUTPUT



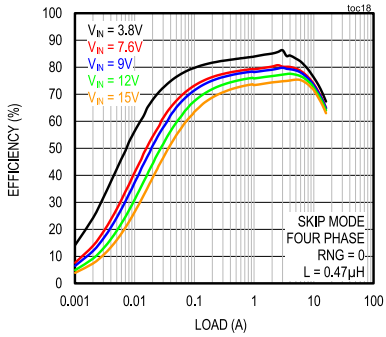
EFFICIENCY vs. LOAD
3.3V OUTPUT



EFFICIENCY vs. LOAD
5.0V OUTPUT



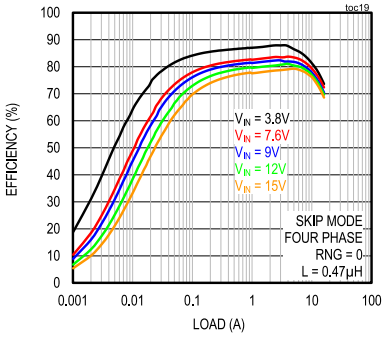
EFFICIENCY vs. LOAD
0.5V OUTPUT



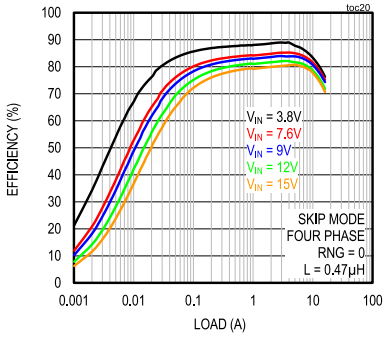
Typical Operating Characteristics (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 1.0V, single-phase configuration, V_{VIO} = 1.8V, skip mode, T_A = +25°C, unless otherwise noted.)

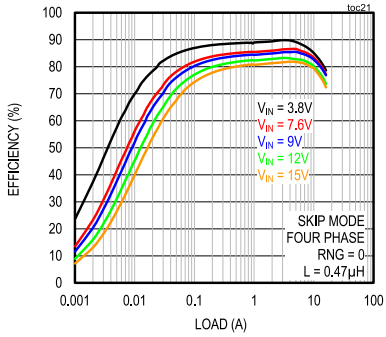
EFFICIENCY vs. LOAD
0.72V OUTPUT



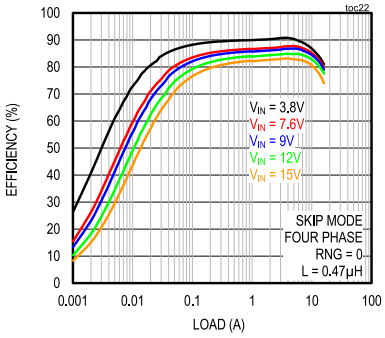
EFFICIENCY vs. LOAD
0.85V OUTPUT



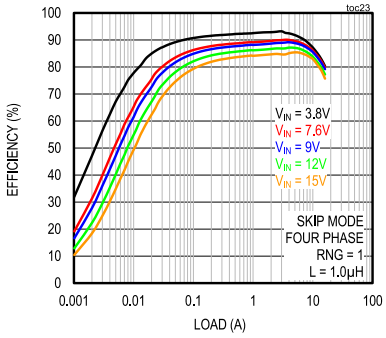
EFFICIENCY vs. LOAD
1.0V OUTPUT



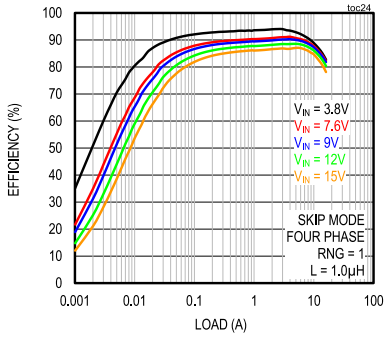
EFFICIENCY vs. LOAD
1.2V OUTPUT



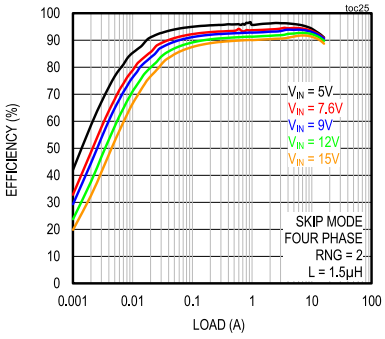
EFFICIENCY vs. LOAD
1.5V OUTPUT



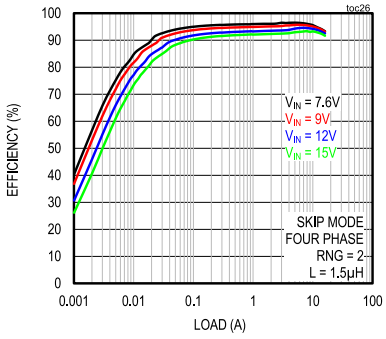
EFFICIENCY vs. LOAD
1.8V OUTPUT



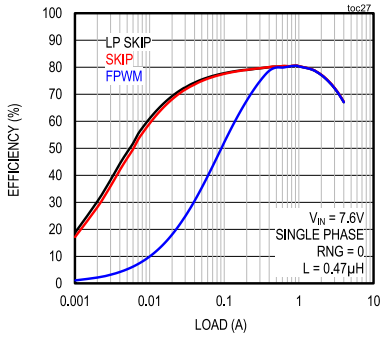
EFFICIENCY vs. LOAD
3.3V OUTPUT



EFFICIENCY vs. LOAD
5.0V OUTPUT



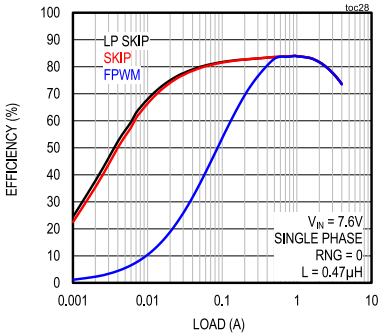
EFFICIENCY vs. LOAD
0.5V OUTPUT



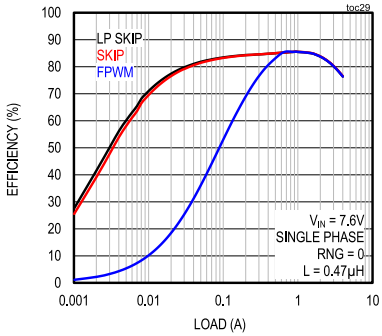
Typical Operating Characteristics (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 1.0V, single-phase configuration, V_{VIO} = 1.8V, skip mode, T_A = +25°C, unless otherwise noted.)

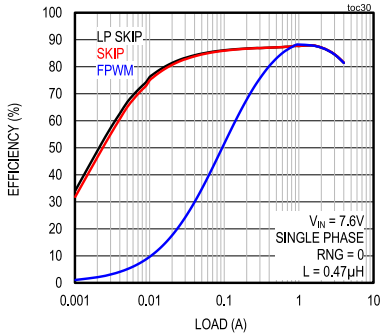
EFFICIENCY vs. LOAD
0.72V OUTPUT



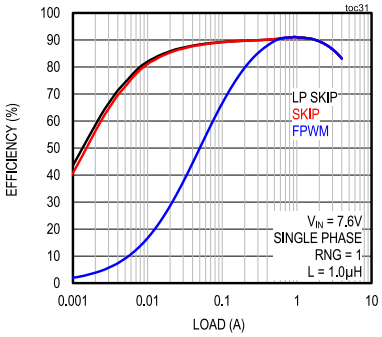
EFFICIENCY vs. LOAD
0.85V OUTPUT



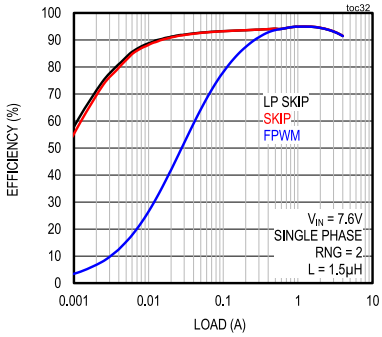
EFFICIENCY vs. LOAD
1.2V OUTPUT



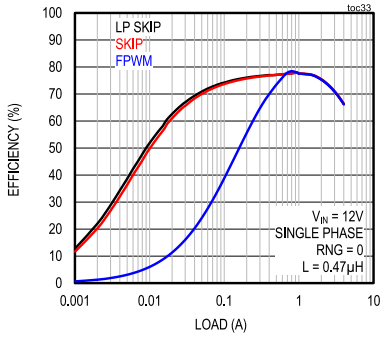
EFFICIENCY vs. LOAD
1.8V OUTPUT



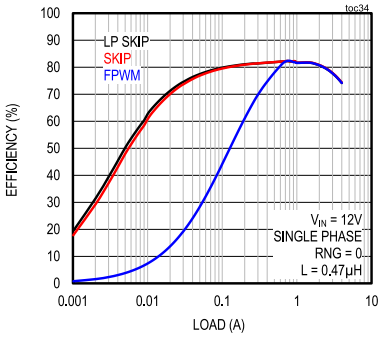
EFFICIENCY vs. LOAD
3.3V OUTPUT



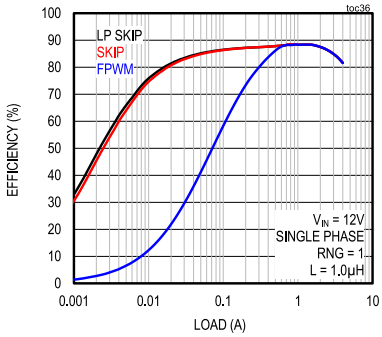
EFFICIENCY vs. LOAD
0.5V OUTPUT



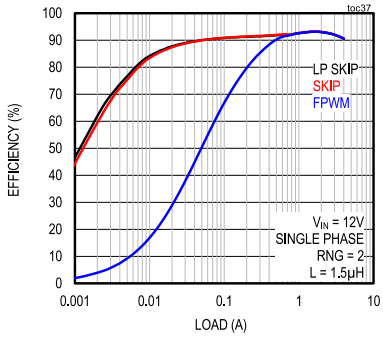
EFFICIENCY vs. LOAD
0.85V OUTPUT



EFFICIENCY vs. LOAD
1.8V OUTPUT



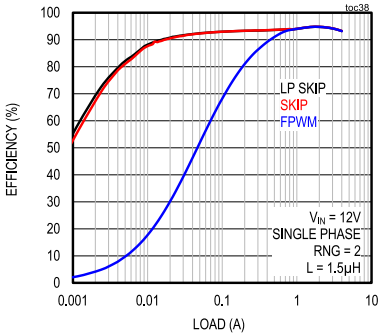
EFFICIENCY vs. LOAD
3.3V OUTPUT



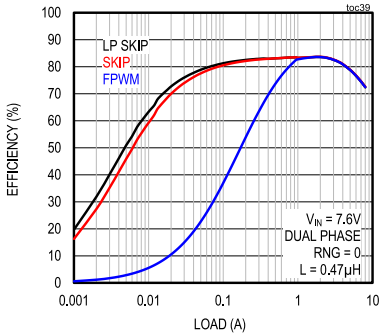
Typical Operating Characteristics (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 1.0V, single-phase configuration, V_{VIO} = 1.8V, skip mode, T_A = +25°C, unless otherwise noted.)

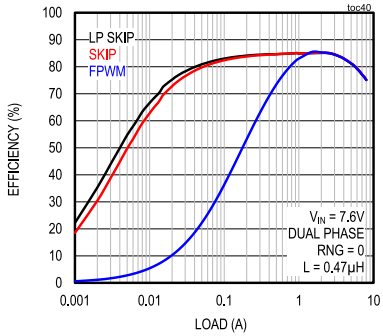
EFFICIENCY vs. LOAD
5.0V OUTPUT



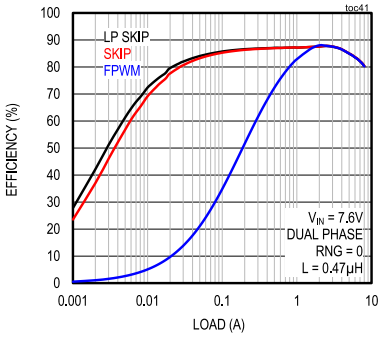
EFFICIENCY vs. LOAD
0.72V OUTPUT



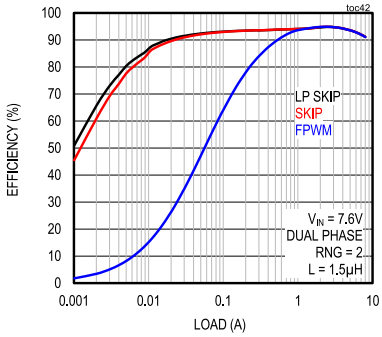
EFFICIENCY vs. LOAD
0.85V OUTPUT



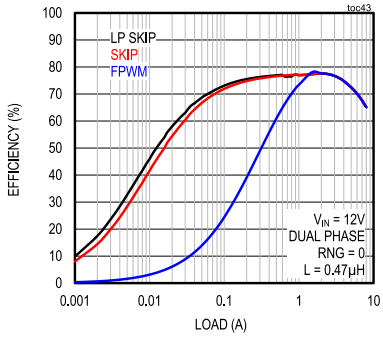
EFFICIENCY vs. LOAD
1.2V OUTPUT



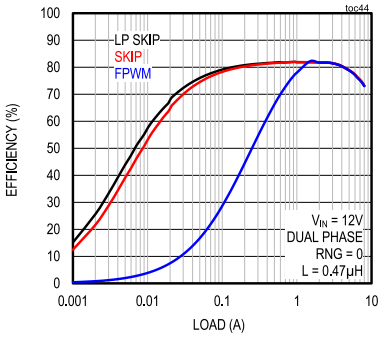
EFFICIENCY vs. LOAD
3.3V OUTPUT



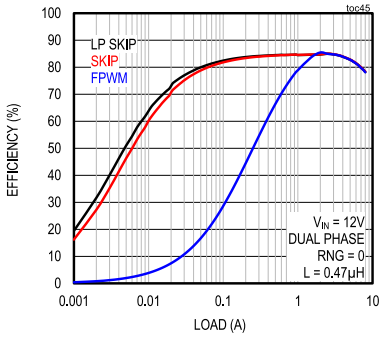
EFFICIENCY vs. LOAD
0.5V OUTPUT



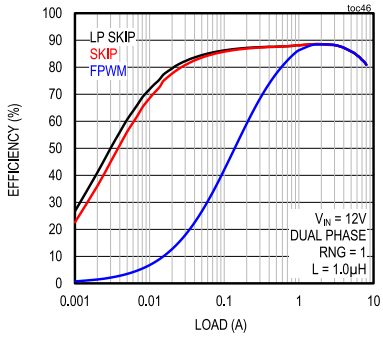
EFFICIENCY vs. LOAD
0.85V OUTPUT



EFFICIENCY vs. LOAD
1.2V OUTPUT



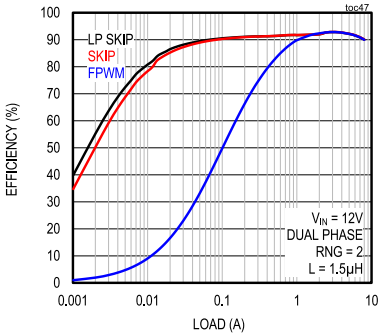
EFFICIENCY vs. LOAD
1.8V OUTPUT



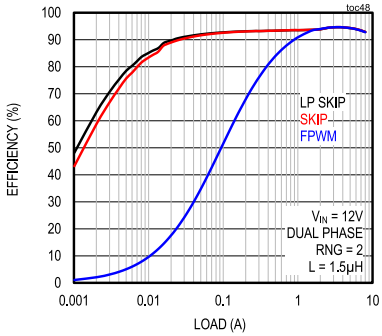
Typical Operating Characteristics (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 1.0V, single-phase configuration, V_{VIO} = 1.8V, skip mode, T_A = +25°C, unless otherwise noted.)

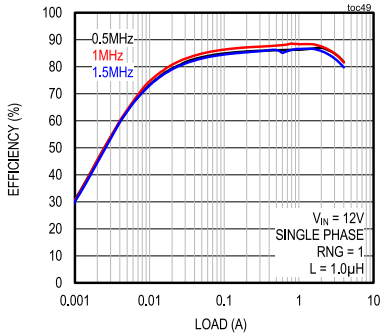
EFFICIENCY vs. LOAD
3.3V OUTPUT



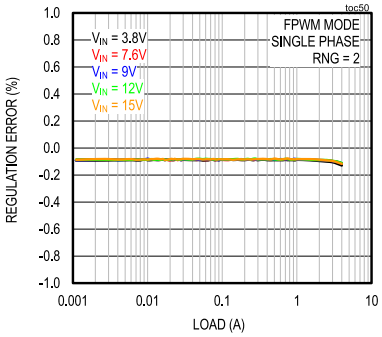
EFFICIENCY vs. LOAD
5.0V OUTPUT



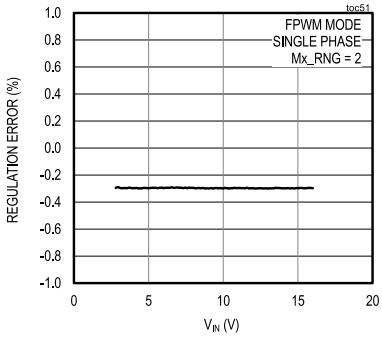
EFFICIENCY vs. LOAD
1.8V OUTPUT



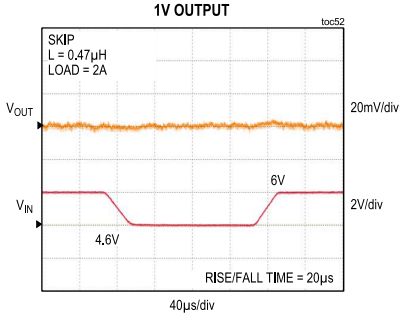
LOAD REGULATION
3.3V OUTPUT



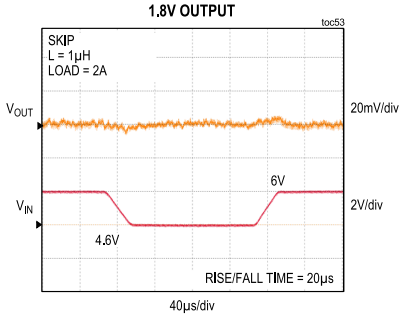
LINE REGULATION
1.8V OUTPUT



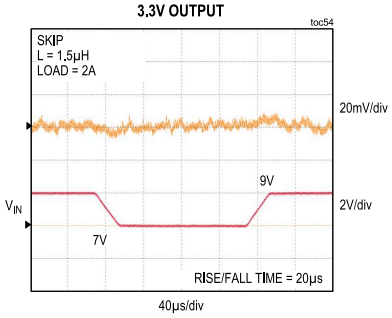
LINE TRANSIENT RESPONSE
1V OUTPUT



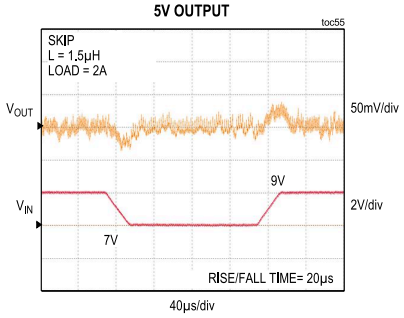
LINE TRANSIENT RESPONSE
1.8V OUTPUT



LINE TRANSIENT RESPONSE
3.3V OUTPUT



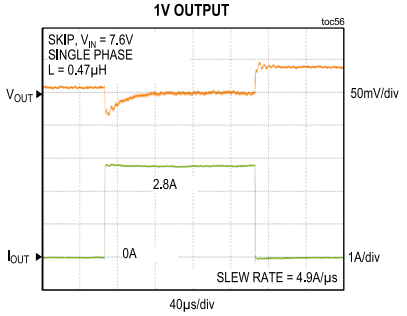
LINE TRANSIENT RESPONSE
5V OUTPUT



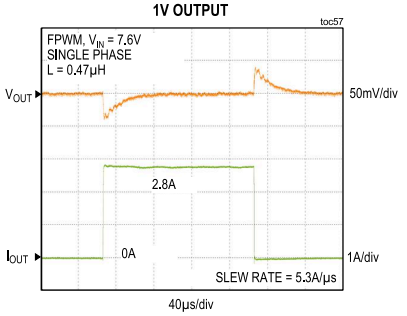
Typical Operating Characteristics (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 1.0V, single-phase configuration, V_{VIO} = 1.8V, skip mode, T_A = +25°C, unless otherwise noted.)

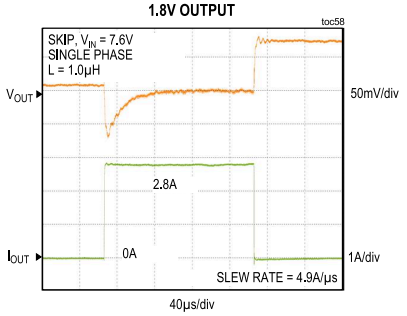
LOAD TRANSIENT RESPONSE
1V OUTPUT



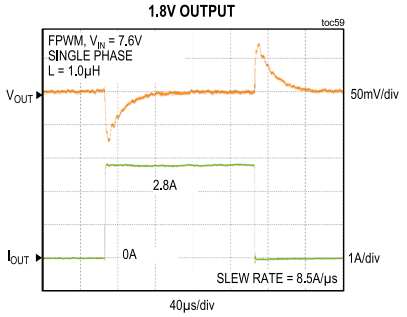
LOAD TRANSIENT RESPONSE
1V OUTPUT



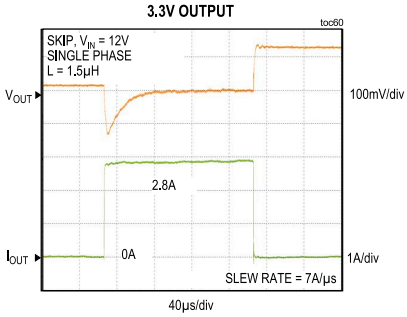
LOAD TRANSIENT RESPONSE
1.8V OUTPUT



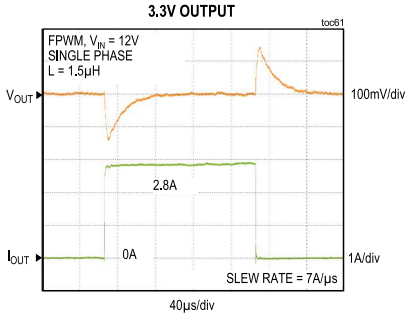
LOAD TRANSIENT RESPONSE
1.8V OUTPUT



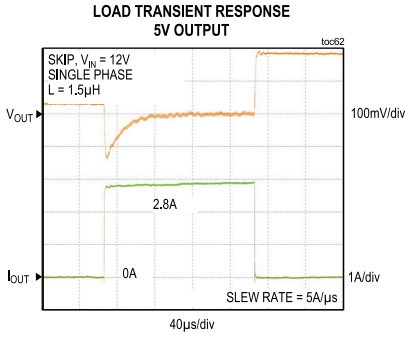
LOAD TRANSIENT RESPONSE
3.3V OUTPUT



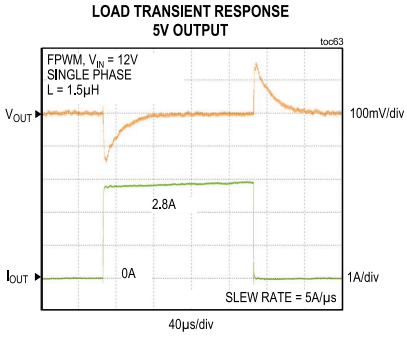
LOAD TRANSIENT RESPONSE
3.3V OUTPUT



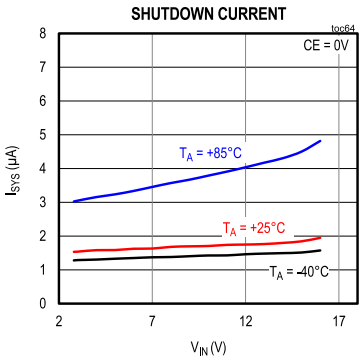
LOAD TRANSIENT RESPONSE
5V OUTPUT



LOAD TRANSIENT RESPONSE
5V OUTPUT



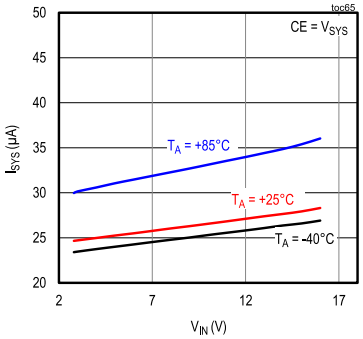
SHUTDOWN CURRENT



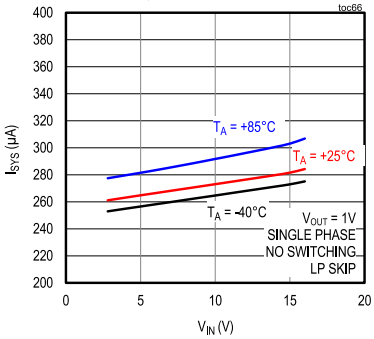
Typical Operating Characteristics (continued)

(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 1.0V, single-phase configuration, V_{VIO} = 1.8V, skip mode, T_A = +25°C, unless otherwise noted.)

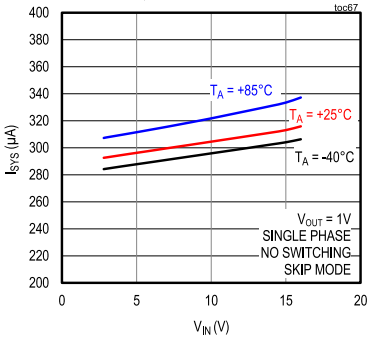
STANDBY CURRENT



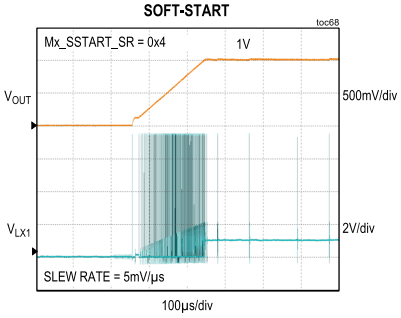
QUIESCENT CURRENT



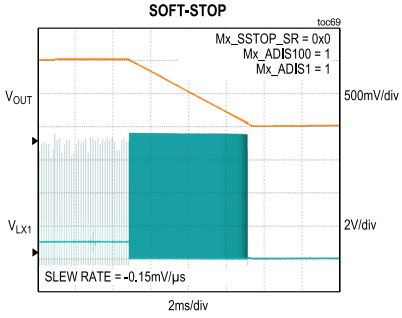
QUIESCENT CURRENT



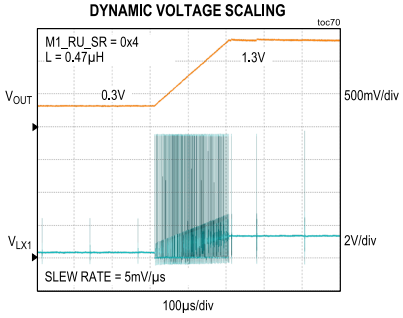
SOFT-START



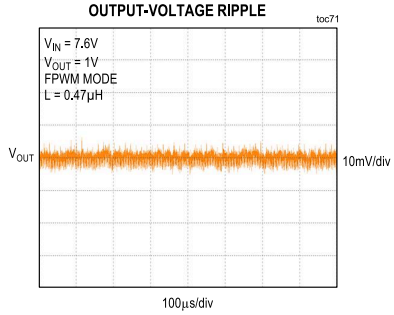
SOFT-STOP



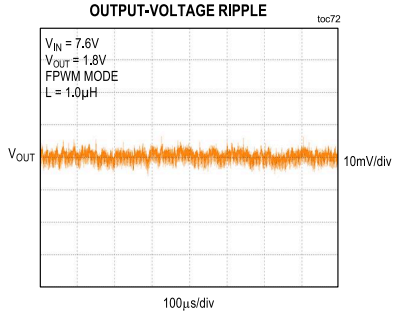
DYNAMIC VOLTAGE SCALING



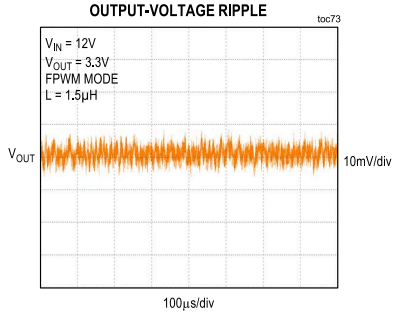
OUTPUT-VOLTAGE RIPPLE



OUTPUT-VOLTAGE RIPPLE

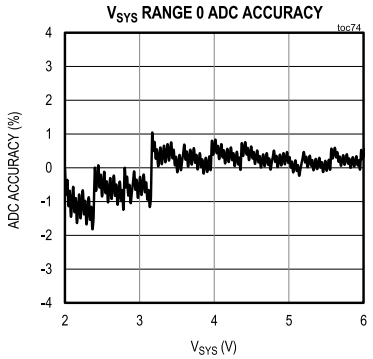


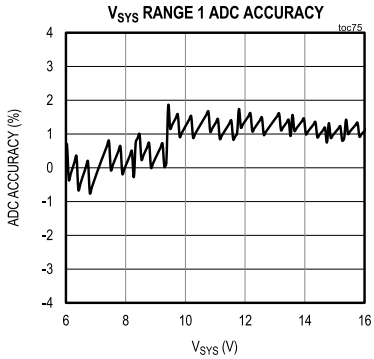
OUTPUT-VOLTAGE RIPPLE

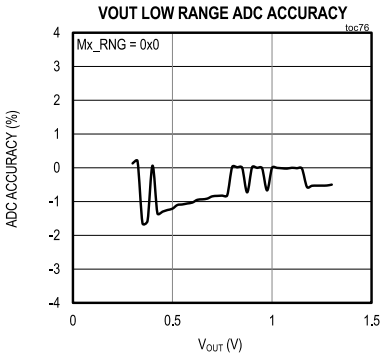


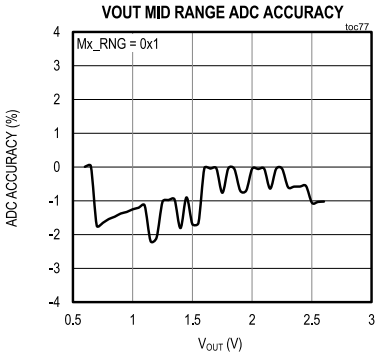
Typical Operating Characteristics (continued)

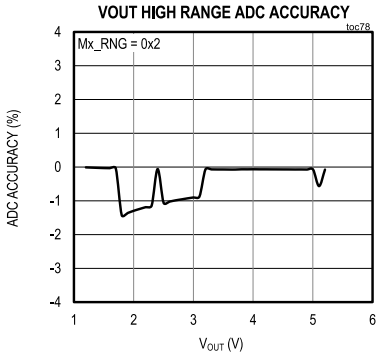
(V_{SYS} = V_{INx} = 12V, V_{OUT1} = 1.0V, single-phase configuration, V_{VIO} = 1.8V, skip mode, T_A = +25°C, unless otherwise noted.)

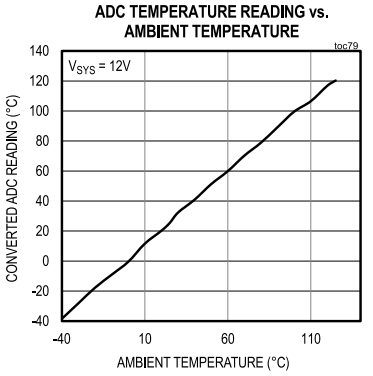






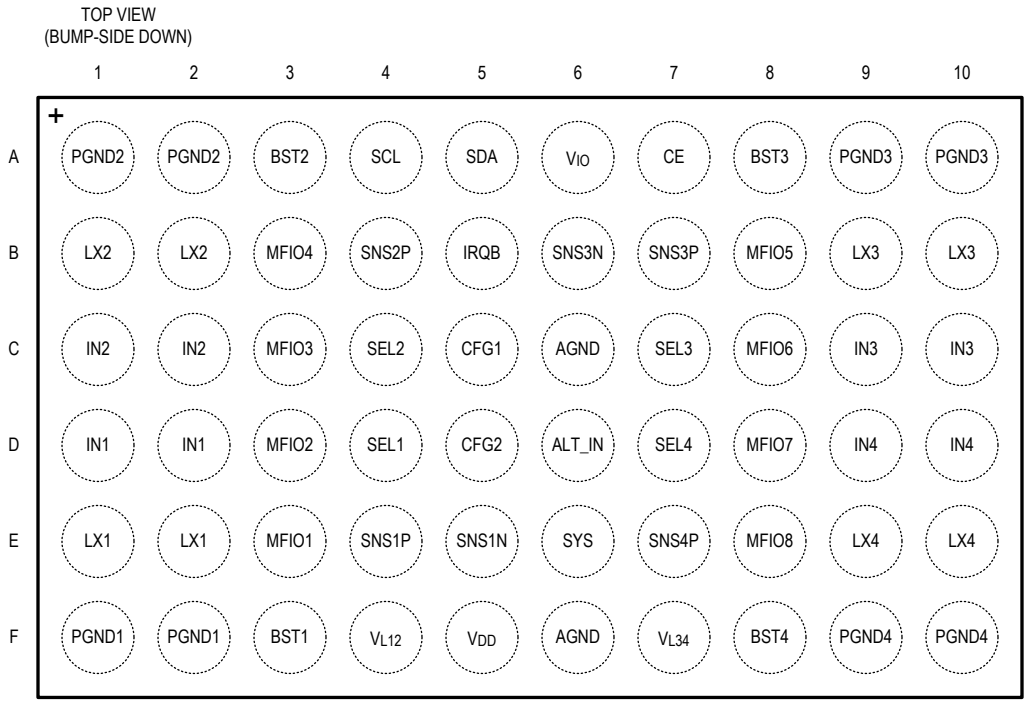






Pin Configuration

MAX77542



60 WLP (4.357mm x 2.557mm x 0.65mm, 0.4mm PITCH)

Pin Description

PIN	NAME	FUNCTION	TYPE
BUCK SWITCHING PHASE			
F3	BST1	Phase1 High-Side MOSFET Driver Supply. Connect a 0.1µF ceramic capacitor between BST1 and LX1.	Power Input
A3	BST2	Phase2 High-Side MOSFET Driver Supply. Connect a 0.1µF ceramic capacitor between BST2 and LX2.	Power Input
A8	BST3	Phase3 High-Side MOSFET Driver Supply. Connect a 0.1µF ceramic capacitor between BST3 and LX3.	Power Input
F8	BST4	Phase4 High-Side MOSFET Driver Supply. Connect a 0.1µF ceramic capacitor between BST4 and LX4.	Power Input
D1, D2	IN1	Phase1 Input. Bypass to PGND1 with a 10µF ceramic capacitor.	Power Input
C1, C2	IN2	Phase2 Input. Bypass to PGND2 with a 10µF ceramic capacitor.	Power Input
C9, C10	IN3	Phase3 Input. Bypass to PGND3 with a 10µF ceramic capacitor.	Power Input
D9, D10	IN4	Phase4 Input. Bypass to PGND4 with a 10µF ceramic capacitor.	Power Input
E1, E2	LX1	Phase1 Switching Node	Power Output
B1, B2	LX2	Phase2 Switching Node	Power Output
B9, B10	LX3	Phase3 Switching Node	Power Output
E9, E10	LX4	Phase4 Switching Node	Power Output

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
F1, F2	PGND1	Phase1 Power Ground	Power Ground
A1, A2	PGND2	Phase2 Power Ground	Power Ground
A9, A10	PGND3	Phase3 Power Ground	Power Ground
F9, F10	PGND4	Phase4 Power Ground	Power Ground
E5	SNS1N	Phase1 Negative Differential Output-Voltage Sensing Input	Analog Input
E4	SNS1P	Phase1 Positive Differential Output-Voltage Sensing Input	Analog Input
B4	SNS2P	Phase2 Positive Differential Output-Voltage Sensing Input. Connect to AGND or leave unconnected (floating) when Phase2 becomes a slave phase of a multiphase converter.	Analog Input
B6	SNS3N	Phase3 Negative Differential Output-Voltage Sensing Input. Connect to AGND or leave unconnected (floating) when Phase3 becomes a slave phase of a multiphase converter.	Analog Input
B7	SNS3P	Phase3 Positive Differential Output-Voltage Sensing Input. Connect to AGND or leave unconnected (floating) when Phase3 becomes a slave phase of a multiphase converter.	Analog Input
E7	SNS4P	Phase4 Positive Differential Output-Voltage Sensing Input. Connect to AGND or leave unconnected (floating) when Phase4 becomes a slave phase of a multiphase converter.	Analog Input
INTERNAL BIAS SUPPLY			
C6, F6	AGND	Analog (Quiet) Ground	Ground
D6	ALT_IN	Alternative Power Input for V_{DD}, V_{L12}, and V_{L34}. Bypass to AGND with a 2.2µF ceramic capacitor when used. See the *Alternative Low-Voltage Input (ALT_IN)* section for more information.	Power Input
E6	SYS	System Power Input (Supply to Internal V_{DD}, V_{L12}, and V_{L34} Linear Regulators). Bypass to AGND with a 2.2µF ceramic capacitor.	Power Input
F5	V_{DD}	Internal Bias Supply Output. Powered from SYS. Bypass to AGND with a 1µF ceramic capacitor. Do not load this pin externally.	Power Output
F4	V_{L12}	Internal Gate Driver Supply Output for Phase1 and Phase2. Powered from SYS. Bypass V_{L12} to PGND with a 2.2µF ceramic capacitor. Do not load this pin externally.	Power Output
F7	V_{L34}	Internal Gate Driver Supply Output for Phase3 and Phase4. Powered from SYS. Bypass V_{L34} to PGND with a 2.2µF ceramic capacitor. Do not load this pin externally.	Power Output
A6	V_{IO}	I/O Supply Input. Bypass to AGND with a 1µF ceramic capacitor.	Power Input
CONTROL AND SERIAL INTERFACE			
A7	CE	Chip Enable Input (Active-High). Enables V_{DD}, V_{L12}, and V_{L34} regulators and I^2C serial interface. See the *Chip Enable (CE) and Internal Bias Supplies* section for more information.	Digital Input
C5	CFG1	Device Configuration1 Selection Input. Connect a selection resistor (R_{CFG1}) between CFG1 and AGND to configure the I^2C slave address and the default MFIO functions. Default settings can be overwritten through I^2C. See the *Device Configuration (CFGx)* section for more information.	Analog Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
D5	CFG2	Device Configuration2 Selection Input. Connect a selection resistor (R_{CFG2}) between CFG2 and AGND to configure the current limits and the switching frequency. Default settings can be overwritten through I^2C. See the *Device Configuration (CFGx)* section for more information.	Analog Input
B5	IRQB	Interrupt Output (Active-Low, Open-Drain). A 100kΩ external pull-up resistor to V_{IO} is required. High impedance when CE = low.	Digital Output
A4	SCL	I^2C Serial Interface Clock Input. (High impedance in shutdown mode.) A pull-up resistor of 1.5kΩ–2.2kΩ to V_{IO} is required. Connect to ground if not used.	Digital Input
A5	SDA	I^2C Serial Interface Data I/O (High impedance in shutdown mode.) A pull-up resistor of 1.5kΩ –2.2kΩ to V_{IO} is required. Connect to ground if not used.	Digital I/O
D4	SEL1	Buck1 Default V_{OUT} Selection Input. Connect a selection resistor (R_{SEL1}) between SEL1 and AGND to configure the default V_{OUT1} and V_{OUT1} range. Default settings can be overwritten through I^2C. See the *Default Output Voltage Selection (SELx)* section for more information.	Analog Input
C4	SEL2	Buck2 Default V_{OUT} Selection Input. Connect a selection resistor (R_{SEL2}) between SEL2 and AGND to configure the default target V_{OUT2} and V_{OUT2} range. Default settings can be overwritten through I^2C. When $R_{SEL2} \le 95.3\Omega$, Buck2 becomes a slave phase of a multiphase converter. See the *Default Output Voltage Selection (SELx)* section for more information.	Analog Input
C7	SEL3	Buck3 Default V_{OUT} Selection Input. Connect a selection resistor (R_{SEL3}) between SEL3 and AGND to configure the default target V_{OUT3} and V_{OUT3} range. Default settings can be overwritten through I^2C. When $R_{SEL3} \le 95.3\Omega$, Buck3 becomes a slave phase of a multiphase converter. See the *Default Output Voltage Selection (SELx)* section for more information.	Analog Input
D7	SEL4	Buck4 Default V_{OUT} Selection Input. Connect a selection resistor (R_{SEL4}) between SEL4 and AGND to configure the default target V_{OUT4} and V_{OUT4} range. Default settings can be overwritten through I^2C. When $R_{SEL4} \le 95.3\Omega$, Buck4 becomes a slave phase of a multiphase converter. See the *Default Output Voltage Selection (SELx)* section for more information.	Analog Input
MULTIFUNCTION I/O			
E3	MFIO1	Multifunction Input/Output. If this pin is not used, leave it floating. See the *MFIO Functions* section for more information.	Digital I/O
D3	MFIO2	Multifunction Input/Output. If this pin is not used, leave it floating. See the *MFIO Functions* section for more information.	Digital I/O
C3	MFIO3	Multifunction Input/Output. If this pin is not used, leave it floating. See the *MFIO Functions* section for more information.	Digital I/O
B3	MFIO4	Multifunction Input/Output. If this pin is not used, leave it floating. See the *MFIO Functions* section for more information.	Digital I/O
B8	MFIO5	Multifunction Input/Output. If this pin is not used, leave it floating. See the *MFIO Functions* section for more information.	Digital I/O
C8	MFIO6	Multifunction Input/Output. If this pin is not used, leave it floating. See the *MFIO Functions* section for more information.	Digital I/O
D8	MFIO7	Multifunction Input/Output. If this pin is not used, leave it floating. See the *MFIO Functions* section for more information.	Digital I/O
E8	MFIO8	Multifunction Input/Output. If this pin is not used, leave it floating. See the *MFIO Functions* section for more information.	Digital I/O

Detailed Description—Top-Level

Chip Enable (CE) and Internal Bias Supplies

The MAX77542 has dedicated internal supplies which are the V_{DD}, the V_{L12}, and the V_{L34}. The V_{DD} provides power for internal logic and control while the V_{L12} and the V_{L34} provide power to gate drivers for switching MOSFETs. These three regulators are powered from the SYS (or the ALT_IN if applicable) input.

When the V_{SYS} supply is valid, a logic high on the CE pin turns on the internal bias circuitry including the V_{DD} regulator. As soon as the V_{DD} supply becomes stable, the MAX77542 reads the R_{CFGx} and the R_{SELx} values for configuring the device and enters standby mode. It takes typically 430µs from pulling the CE pin high. In standby mode, the I^2C serial interface is activated so that a host processor can overwrite all user-accessible registers including default output voltage, startup delay setting, and output enable control for each regulator.

The V_{L12} supply is turned on when either Buck1 or Buck2 is enabled. When Buck3 or Buck4 is enabled, the V_{L34} supply automatically is turned on. To reduce the turn-on delay time, the V_{L12} and the V_{L34} supplies can be turned on by setting the VL_EN bit to 1 through I^2C even when the corresponding buck outputs are disabled. In case both the CE and a MFIO (when EN_Mx function is selected) pins are pulled high at the same time, the buck outputs require even longer time to startup because the internal bias circuitry needs to be turned on first before propagating the buck enable signals.

When the CE pin is pulled low, the MAX77542 goes into shutdown mode and turns off all the regulators regardless of the Mx_EN bits and the EN_Mx (MFIOx) pins. This event also resets all registers to their POR default values.

Table 1. V_{DD} and I^2C Enable Truth Table

CE PIN	V_{DD} AND I^2C SERIAL INTERFACE
Low	Disabled
High	Enabled

Alternative Low-Voltage Input (ALT_IN)

When an alternative power source (V_{ALT_IN}) is available between the V_{SWO} and the V_{SYS}, it may optionally be used to power the dedicated internal linear regulator (V_{DD}, V_{L12}, and V_{L34}) to improve the efficiency. As shown in Figure 1, the switchover circuit dynamically selects the input of the V_{DD} and the V_{L12} & V_{L34} supplies between the SYS and the ALT_IN pins as needed to maintain steady operation. When the device exits shutdown mode (CE = 1), the linear regulator is initially powered from the SYS pin and it can be switched over to the ALT_IN pin if a valid power source is connected to the ALT_IN. The ALT_IN_I interrupt and the ALT_SWO status bits indicate the status of the switchover circuit.

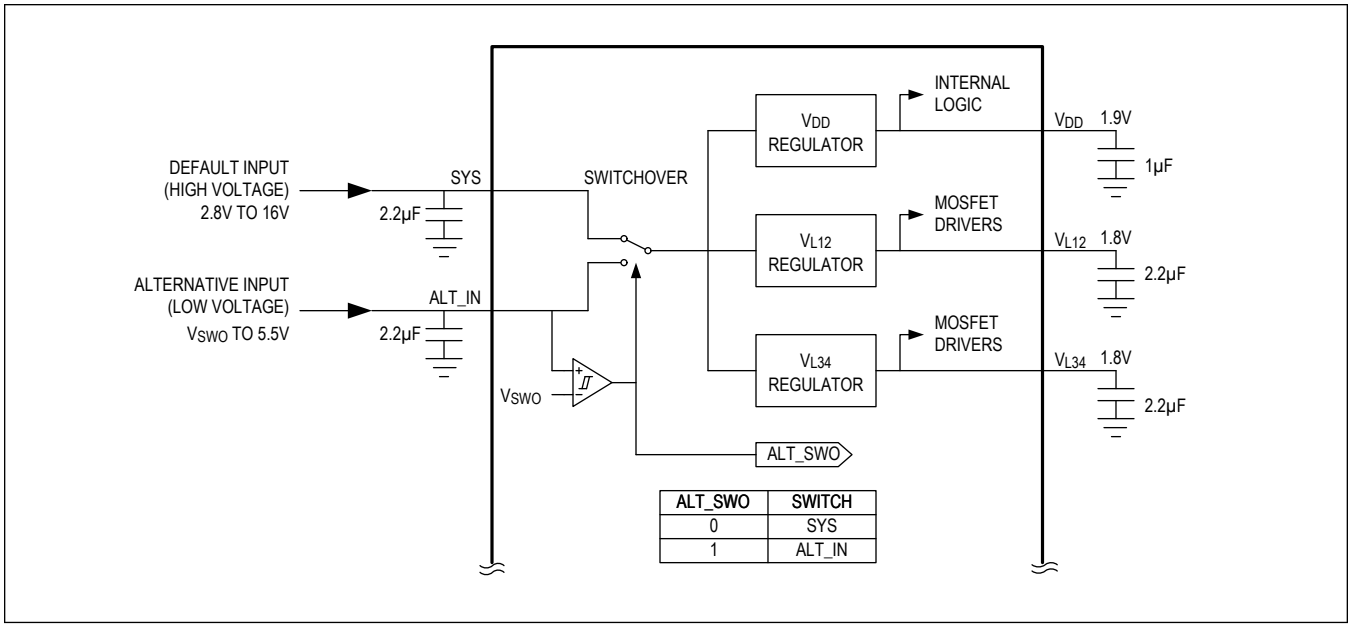


Figure 1. Alternative Input Switchover Circuit

There are three ways of using the ALT_IN input:

- Option 1: Connect the ALT_IN pin to the AGND (not used). In this case, the internal linear regulator permanently receives power from the SYS pin.
- Option 2: Connect the ALT_IN pin to one of the buck outputs which is greater than the V_{SWO}. Using a buck output for powering up the linear regulator improves the total efficiency of the device. (The buck output can be turned on and off dynamically.)
- Option 3: Connect the ALT_IN pin to an external high-efficiency DC source greater than the V_{SWO} when neither buck output is greater than the V_{SWO}. (Using a high-efficiency power source also improves the total system efficiency.)

Device Configuration (CFGx)

The MAX77542 supports user-selectable device configurations with a 1% tolerance (or better) resistor. The MAX77542 evaluates the resistances between the CFGx and the AGND whenever the V_{DD} regulator first turns on (exits shutdown mode). The decoded values of the R_{CFGx} are latched until the next time the device exits shutdown mode. The CFGx_LATCH[4:0] status bits reflect the latched decoded value of the R_{CFGx}. See the *Register Map* section for more details.

Table 2 decodes the default selection options for the I²C slave address and the default MFIO functions. Once latched, the MFIOx_FUNC[3:0] bits reflect the selected the MFIO options. The decoded values for R_{CFG1} ≥ 75kΩ are programmable at the factory. Note that all MFIOs are pulled down to AGND with an internal 800kΩ resistor until the R_{CFGx} decoding is complete.

Table 2. Device Configuration by R_{CFG1}

R_{CFG1} (Ω)	I²C SLAVE ADDRESS (7-BIT ADDRESS)	MFIO1	MFIO2	MFIO3	MFIO4	MFIO5	MFIO6	MFIO7	MFIO8
≤ 95.3	7'h60 (110 0000)	EN_M1	POK_M1	EN_M2	POK_M2	EN_M3	POK_M3	EN_M4	POK_M4
200	7'h61 (110 0001)	EN_M1	POK_M1	EN_M2	POK_M2	EN_M3	POK_M3	EN_M4	POK_M4

Table 2. Device Configuration by R_{CFG1} (continued)

R_{CFG1} (Ω)	I^2C SLAVE ADDRESS (7-BIT ADDRESS)	MFIO1	MFIO2	MFIO3	MFIO4	MFIO5	MFIO6	MFIO7	MFIO8
309	7'h62 (110 0010)	EN_M1	POK_M1	EN_M2	POK_M2	EN_M3	POK_M3	EN_M4	POK_M4
422	7'h63 (110 0011)	EN_M1	POK_M1	EN_M2	POK_M2	EN_M3	POK_M3	EN_M4	POK_M4
536	7'h60 (110 0000)	EN_M1	POK_M1	FPWM_M1	EN_M2	EN_M3	POK_M3	EN_M4	FPWM_M3
649	7'h61 (110 0001)	EN_M1	POK_M1	FPWM_M1	EN_M2	EN_M3	POK_M3	EN_M4	FPWM_M3
768	7'h62 (110 0010)	EN_M1	POK_M1	FPWM_M1	EN_M2	EN_M3	POK_M3	EN_M4	FPWM_M3
909	7'h63 (110 0011)	EN_M1	POK_M1	FPWM_M1	EN_M2	EN_M3	POK_M3	EN_M4	FPWM_M3
1.05k	7'h60 (110 0000)	EN_M1	POK_M1	FPWM_M1	CLKDET_GLB	EN_M3	POK_M3	EN_M4	POK_M4
1.21k	7'h61 (110 0001)	EN_M1	POK_M1	FPWM_M1	CLKDET_GLB	EN_M3	POK_M3	EN_M4	POK_M4
1.40k	7'h62 (110 0010)	EN_M1	POK_M1	FPWM_M1	CLKDET_GLB	EN_M3	POK_M3	EN_M4	POK_M4
1.62k	7'h63 (110 0011)	EN_M1	POK_M1	FPWM_M1	CLKDET_GLB	EN_M3	POK_M3	EN_M4	POK_M4
1.87k	7'h60 (110 0000)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	EN_M3	POK_M3	FPWM_M3	CLKDET_M3
2.15k	7'h61 (110 0001)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	EN_M3	POK_M3	FPWM_M3	CLKDET_M3
2.49k	7'h62 (110 0010)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	EN_M3	POK_M3	FPWM_M3	CLKDET_M3
2.87k	7'h63 (110 0011)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	EN_M3	POK_M3	FPWM_M3	CLKDET_M3
3.74k	7'h60 (110 0000)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	CLKDET_M4	POK_M4	FPWM_M4	EN_M4
8.06k	7'h61 (110 0001)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	CLKDET_M4	POK_M4	FPWM_M4	EN_M4
12.4k	7'h62 (110 0010)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	CLKDET_M4	POK_M4	FPWM_M4	EN_M4
16.9k	7'h63 (110 0011)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	CLKDET_M4	POK_M4	FPWM_M4	EN_M4
21.5k	7'h60 (110 0000)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	CLKDET_M4	VSEL_M1	FPWM_M4	EN_M4
26.1k	7'h61 (110 0001)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	CLKDET_M4	VSEL_M1	FPWM_M4	EN_M4
30.9k	7'h62 (110 0010)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	CLKDET_M4	VSEL_M1	FPWM_M4	EN_M4
36.5k	7'h63 (110 0011)	EN_M1	POK_M1	FPWM_M1	CLKDET_M1	CLKDET_M4	VSEL_M1	FPWM_M4	EN_M4
42.2k	7'h60 (110 0000)	FPSI	POK_M1	FPWM_M1	CLKDET_M1	VB_GLB	RSTINB	TWARNB	RSTOB

Table 2. Device Configuration by R_{CFG1} (continued)

R_{CFG1} (Ω)	I^2C SLAVE ADDRESS (7-BIT ADDRESS)	MFIO1	MFIO2	MFIO3	MFIO4	MFIO5	MFIO6	MFIO7	MFIO8
48.7k	7'h61 (110 0001)	FPSI	POK_M1	FPWM_M1	CLKDET_M1	VB_GLB	RSTINB	TWARNB	RSTOB
56.2k	7'h62 (110 0010)	FPSI	POK_M1	FPWM_M1	CLKDET_M1	VB_GLB	RSTINB	TWARNB	RSTOB
64.9k	7'h63 (110 0011)	FPSI	POK_M1	FPWM_M1	CLKDET_M1	VB_GLB	RSTINB	TWARNB	RSTOB
75.0k	7'h60 (110 0000)	Factory Option							
86.6k	7'h61 (110 0001)								
100k	7'h62 (110 0010)								
≥ 115k	7'h63 (110 0011)								

Table 3 decodes the default selection options for the peak current limit of master phases and the switching frequency setting. Once latched, the Mx_ILIM[1:0] and the Mx_FREQ[1:0] bits reflect the selected options. The decoded values for R_{CFG2} ≥ 115kΩ are programmable at the factory.

Table 3. Device Configuration by R_{CFG2}

R_{CFG2} (Ω)	M1_ILIM (A)	M2_ILIM (A)	M3_ILIM (A)	M4_ILIM (A)	Mx_FREQ (MHz)
≤ 95.3	5.5	5.5	5.5	5.5	1.0
200	5.5	5.5	5.5	5.5	1.5
309	5.5	5.5	5.5	3.5	1.0
422	5.5	5.5	5.5	3.5	1.5
536	5.5	5.5	3.5	5.5	1.0
649	5.5	5.5	3.5	5.5	1.5
768	5.5	5.5	3.5	3.5	1.0
909	5.5	5.5	3.5	3.5	1.5
1.05k	5.5	3.5	5.5	5.5	1.0
1.21k	5.5	3.5	5.5	5.5	1.5
1.40k	5.5	3.5	5.5	3.5	1.0
1.62k	5.5	3.5	5.5	3.5	1.5
1.87k	5.5	3.5	3.5	5.5	1.0
2.15k	5.5	3.5	3.5	5.5	1.5
2.49k	5.5	3.5	3.5	3.5	1.0
2.87k	5.5	3.5	3.5	3.5	1.5
3.74k	3.5	5.5	5.5	5.5	1.0
8.06k	3.5	5.5	5.5	5.5	1.5
12.4k	3.5	5.5	5.5	3.5	1.0
16.9k	3.5	5.5	5.5	3.5	1.5
21.5k	3.5	5.5	3.5	5.5	1.0
26.1k	3.5	5.5	3.5	5.5	1.5

Table 3. Device Configuration by R_{CFG2} (continued)

R_{CFG2} (Ω)	M1_ILIM (A)	M2_ILIM (A)	M3_ILIM (A)	M4_ILIM (A)	Mx_FREQ (MHz)
30.9k	3.5	5.5	3.5	3.5	1.0
36.5k	3.5	5.5	3.5	3.5	1.5
42.2k	3.5	3.5	5.5	5.5	1.0
48.7k	3.5	3.5	5.5	5.5	1.5
56.2k	3.5	3.5	5.5	3.5	1.0
64.9k	3.5	3.5	5.5	3.5	1.5
75.0k	3.5	3.5	3.5	5.5	1.0
86.6k	3.5	3.5	3.5	5.5	1.5
100k	3.5	3.5	3.5	3.5	1.0
≥ 115k	Factory Option				

Output Enable Control

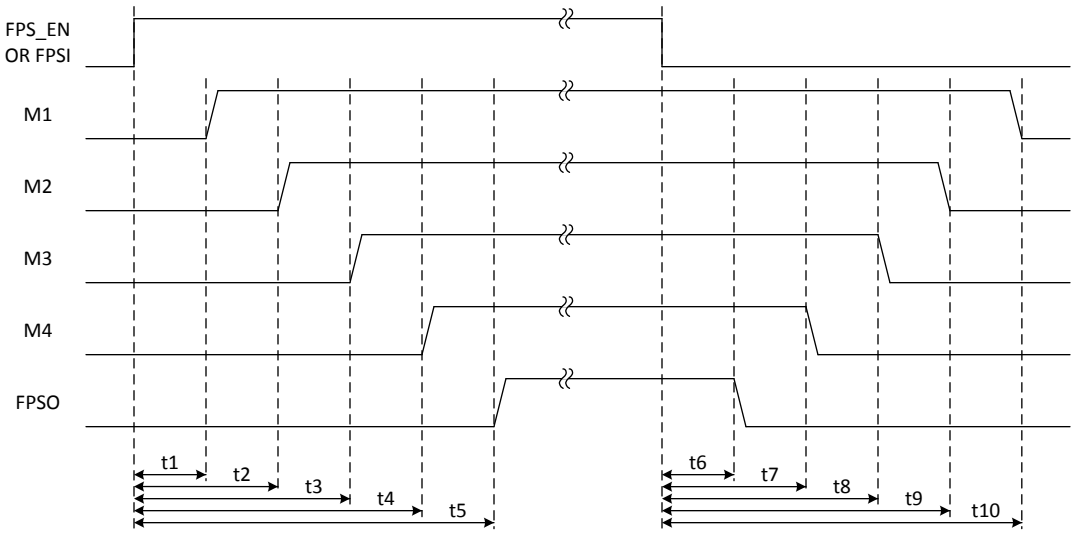
The MAX77542 has eight multifunction I/Os that can be selected for output enable inputs. When the MFIOx is pulled above the V_{IH} (EN_Mx function is selected), the corresponding buck output is enabled. The buck outputs can also be turned on by setting the Mx_EN bits to 1 through I^2C. The logical interaction between the EN_Mx (MFIOx) pins and their corresponding I^2C enable bits (Mx_EN) is OR. For example, the Master1 is enabled when the M1_EN bit or the EN_M1 (MFIOx) signal is set to 1. When all active signals are 0, the corresponding master phase is turned off. The serial interface is active whenever the V_{DD} regulator is enabled (see Table 1).

Flexible Power Sequencer (FPS)

The MAX77542 supports a flexible power sequencer that controls programmable startup and shutdown delay times of each master phase. A startup or a shutdown sequence is initiated by either the FPS_EN bit or global output enable function (FPSI) of the MFIOx. The startup and shutdown delay times between are individually programmable from 0ms to 56ms (15 slots with 0.5ms/1ms/2ms/4ms of step size) with a no-startup option. The startup delay times are programmable by the Mx_STUP_DLY[3:0] and the FPSO_STUP_DLY[3:0] bits and their default values are set by OTPs, while the shutdown delay times are programmable by the Mx_SHDN_DLY[3:0] and the FPSO_SHDN_DLY[3:0] bits only. The delay time steps and the delay times for all master phases are programmable. When the no-startup option is selected, the corresponding buck is excluded from the FPS resources.

Once a startup or a shutdown sequence is initiated, the FPS_EN bit or the FPSI input is ignored (deactivated) until the sequence is completed. During startup and shutdown sequences, any changes in the Mx_STUP_DLY[3:0], the Mx_SHDN_DLY[3:0], and the DLY_STEP[1:0] bits are also not effective until the sequence ends.

If any master phases are turned on by the Mx_EN bits or the enable function (EN_Mx) of the MFIOx before initiating a startup or a shutdown sequence, the startup or the shutdown sequence does not affect the master phase(s) already turned on individually. A typical startup and shutdown sequence are shown in Figure 2.



t1–t5: SET BY Mx_STUP_DLY[3:0] AND FPSO_STUP_DLY[3:0] REGISTERS (FACTORY PROGRAMMABLE).
t6–t10: SET BY Mx_SHDN_DLY[3:0] AND FPSO_SHDN_DLY[3:0] REGISTERS.

Figure 2. Typical Startup and Shutdown Sequence

Undervoltage Lock-Out (UVLO)

When the V_{SYS} voltage falls below V_{UVLO_F} (typ 2.7V), the MAX77542 disables all individual buck outputs immediately and resets all buck output-voltage setting registers (Type F). See the *Fault Protection* section for more information.

A UVLO event forces the device to a dormant state until the V_{SYS} voltage rises above the UVLO rising threshold (typ 2.9V). The UVLO falling threshold is programmable through I^2C. If the V_{SYS} voltage drops down to the POR threshold (typ 1.7V), the V_{DD} supply turns off (all the registers are reset) and the MAX77542 enters shutdown state.

V_{IO} Fault

When the I/O supply falls below $V_{IO\_UVLO\_F}$, the I^2C buffer is cleared and all MFIO input and output functions are deactivated. The I^2C buffer and the MFIOs remain inactive until the V_{IO} supply goes above $V_{IO\_UVLO\_R}$. When unmasked, the V_{IO} fault event triggers the VIOFLT_I interrupt. See the *Register Map* section for more details. The V_{IO} fault condition can initiate a shutdown of all buck outputs immediately when the VIOFLT_SHDN bit is set to 1.

Thermal Warning and Thermal Shutdown (TSHDN)

The MAX77542 has a thermal warning to monitor whether the junction temperature rises above a programmable threshold temperature. As shown in Figure 3, the device enters thermal shutdown (TSHDN) if the junction temperature exceeds the T_{SHDN} (approximately +165°C typ). A TSHDN event disables all individual buck outputs immediately and resets all buck output-voltage setting registers (Type F). See the *Fault Protection* section for more information. Thermal monitoring is active whenever any of the following conditions are true:

- One of the buck outputs is enabled.
- The force thermal protection enable bit is set (FTMON_EN = 1).
- Thermal protection is enabled (for any reason) and detects $T_J \geq$ TWARN_TH[2:0]. (In this case, thermal monitoring remains active until $T_J \leq$ TWARN_TH[2:0] - 15°C.)

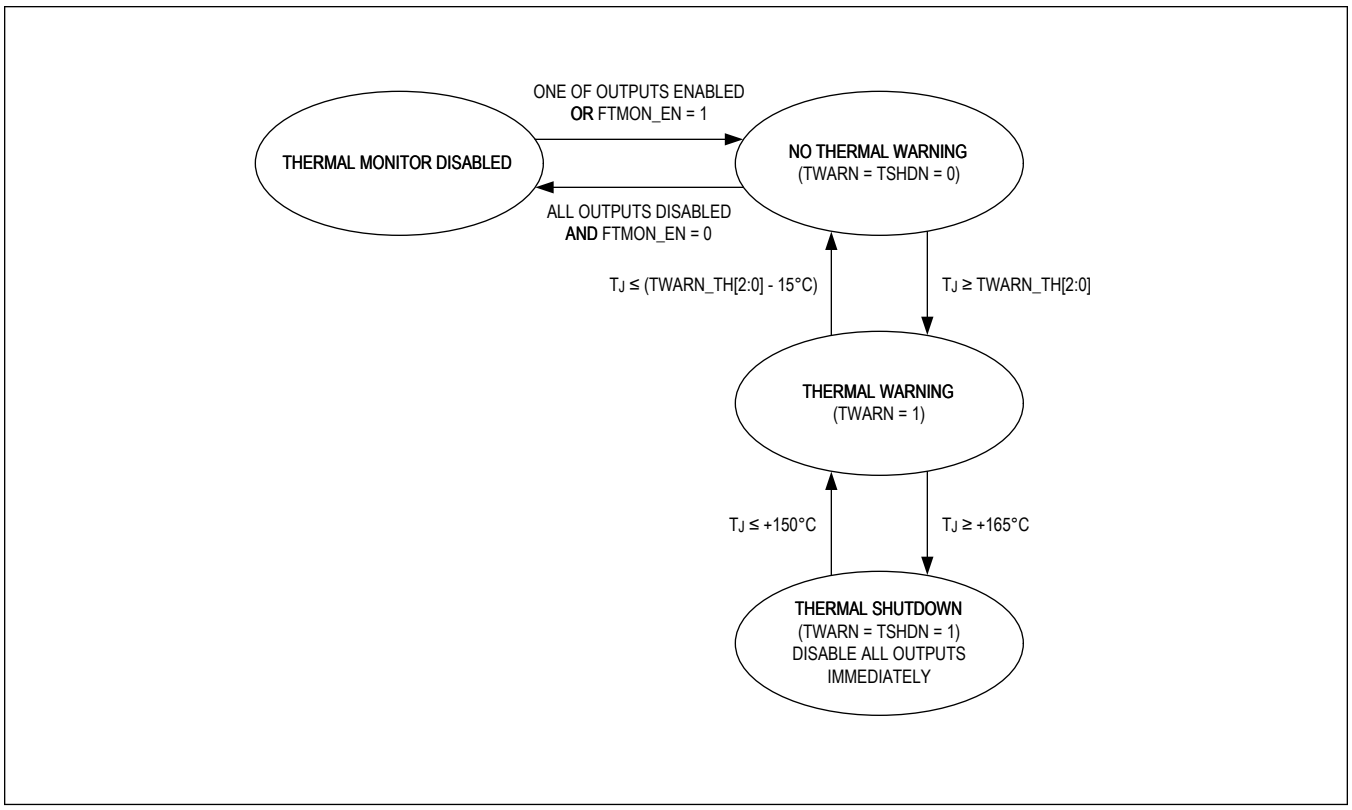


Figure 3. Thermal Warning and Thermal Shutdown

Reset Input and Output

All functional registers (both Type O and Type F) of the MAX77542 can be reset to their POR default values when a valid reset signal is detected at one of the MFIOx pins. To activate this feature, one of the MFIOx pins must be configured as system reset input (active-low) function (MFIOx_FUNC[3:0] = 0xA) and the RSTINB_SHDN needs to be set to 1. To avoid a false trigger by glitches, it is recommended to have a proper debounce timer on this input by setting the corresponding MFIOx_DEB[2:0] bit. See the *System Reset Input (RSTINB)* for more details.

The MAX77542 also features "System Reset Output" by configuring one of the MFIOx pins (MFIOx_FUNC[3:0] = 0xB). "System Reset Output" is an active-low open drain and it asserts when one of fault events (which are linked to the reset output) occurs. To link "System Reset Output" to specific fault considerations, the Mx_RSTOB_EN, the TSHDN_RSTOB_EN, and/or the UVLO_RSTOB_EN bits need to be set to 1. As soon as the fault condition that caused the reset output to assert is cleared, the reset output signal will be de-asserted. See the *System Reset Output (RSTOB)* section for more details.

Interrupt (IRQB), Mask and Status

The IRQB is an active-low, open-drain output that indicates to a host processor that the status on the MAX77542 has changed. The IRQB is the logical "NOR" of all unmasked interrupt bits. See the *Register Map* section for a full list of available status and interrupt bits.

The IRQB output asserts (goes low) anytime an unmasked interrupt bit is triggered. The host processor reads the interrupt source register (0x00) and the interrupt registers that are indicated by the interrupt source register to check the cause of the interrupt event. Note that the interrupt source register is cleared when the corresponding interrupt register group is read by the host processor. All the interrupt events are edge-triggered. Therefore, the same interrupt is not generated repeatedly even though the interrupt condition persists.

Each interrupt register can be read at a time and all interrupt bits are clear-on-read bits. The IRQB output de-asserts

(goes high) when all interrupt bits have been cleared. If an interrupt is captured during the read sequence, the IRQB output is held low. When the IRQB output is pulled low by an unmasked interrupt event, the IRQB output stays low until the interrupt bit is cleared by the reading operation of the host processor or the corresponding interrupt mask bit is set to 1 (masked). All interrupts (except UVLO_I) are masked by default. Masked interrupt bits do not cause the IRQB pin to assert.

The MAX77542 has two interrupt mask modes. With MASK_MODE = 0 (default), an interrupt bit sets for an interrupt event regardless of the corresponding mask bit, however the interrupt event does not propagate to the interrupt source register when masked. When the MASK_MODE is set to 1, it prevents the interrupt register bit from asserting for the corresponding interrupt event (gated at the interrupt bit).

In addition to interrupt bits, the MAX77542 has read-only status bits. These bits always represent the current status of the device. It is highly recommended that the host processor read status bits whenever the MAX77542 is initialized by the host processor. These status bits do not directly affect the state of interrupt bits.

Register Reset Conditions

All registers (both Type O and Type F) are reset to the POR default values specified in the *Register Map* section when the CE pin is pulled low or the V_{SYS} supply drops below its POR threshold (typ 1.7V). Whenever the CE pin is pulled high, the MAX77542 updates the default register values based on R_{CFGx} and R_{SELx} detection, and the updated default values are latched until the CE pin is pulled low or a POR event occurs. A UVLO or a TSHDN event resets all buck output-voltage setting registers (Type F) to their default values, while a SCP event only resets buck output-voltage setting registers (Type F) for the corresponding output.

Factory Options

The MAX77542 is factory-configurable with a variety of one-time programmable (OTP) options. See Table 4 for a selector guide. Contact Analog Devices to request a variant of the device with specialized OTP options.

Table 4. MAX77542 Factory-Programmed Defaults (OTP Options)

	MAX77542A
SELx OPTIONS	
VOUT1 (V)	0.8
VOUT2 (V)	1.1
VOUT3 (V)	1.8
VOUT4 (V)	3.3
CFG1 OPTIONS	
MFIO1	FPSI
MFIO2	POK_M1
MFIO3	FPWM_M1
MFIO4	CLKDET_M1
MFIO5	VB_GLB
MFIO6	RSTINB
MFIO7	TWARNB
MFIO8	RSTOB
CFG2 OPTIONS	
M1_ILIM (A)	5.5
M2_ILIM (A)	5.5
M3_ILIM (A)	5.5
M4_ILIM (A)	5.5
Mx_FREQ (MHz)	1.0

Detailed Description—Quad-Phase Configurable Buck Converter

The MAX77542 is a high-efficiency, phase-configurable buck converter with four 4A phases (Φ). A differential pair of output-voltage sensing input (SNSxP and SNSxN) ensures best-in-class output-voltage regulation at the point of load. Each buck converter operates on an input supply between 2.8V and 16V. The output voltages are preset using the SELx inputs and further configurable with an I^2C serial interface between 0.3V and 5.2V in 5mV, 10mV, or 20mV steps depending on the Mx_RNG[1:0] bits. See the *Output-Voltage Setting* section.

Each switching phase supports 4A and a four-phase (4Φ) configuration supports up to 16A. The phase configuration is user-programmable by tying the SEL2, the SEL3 and/or the SEL4 pins to the AGND on the PCB. See the *Phase and Output Configuration* section.

Buck Converter Control Scheme

The MAX77542 uses an adaptive constant on-time (COT) current-mode control scheme. The adaptive COT control provides fast response to load transients, inherent compensation to input-voltage variation, and stable performance at low-duty cycles. As shown in Figure 4, Buck1 is referenced in the following explanation.

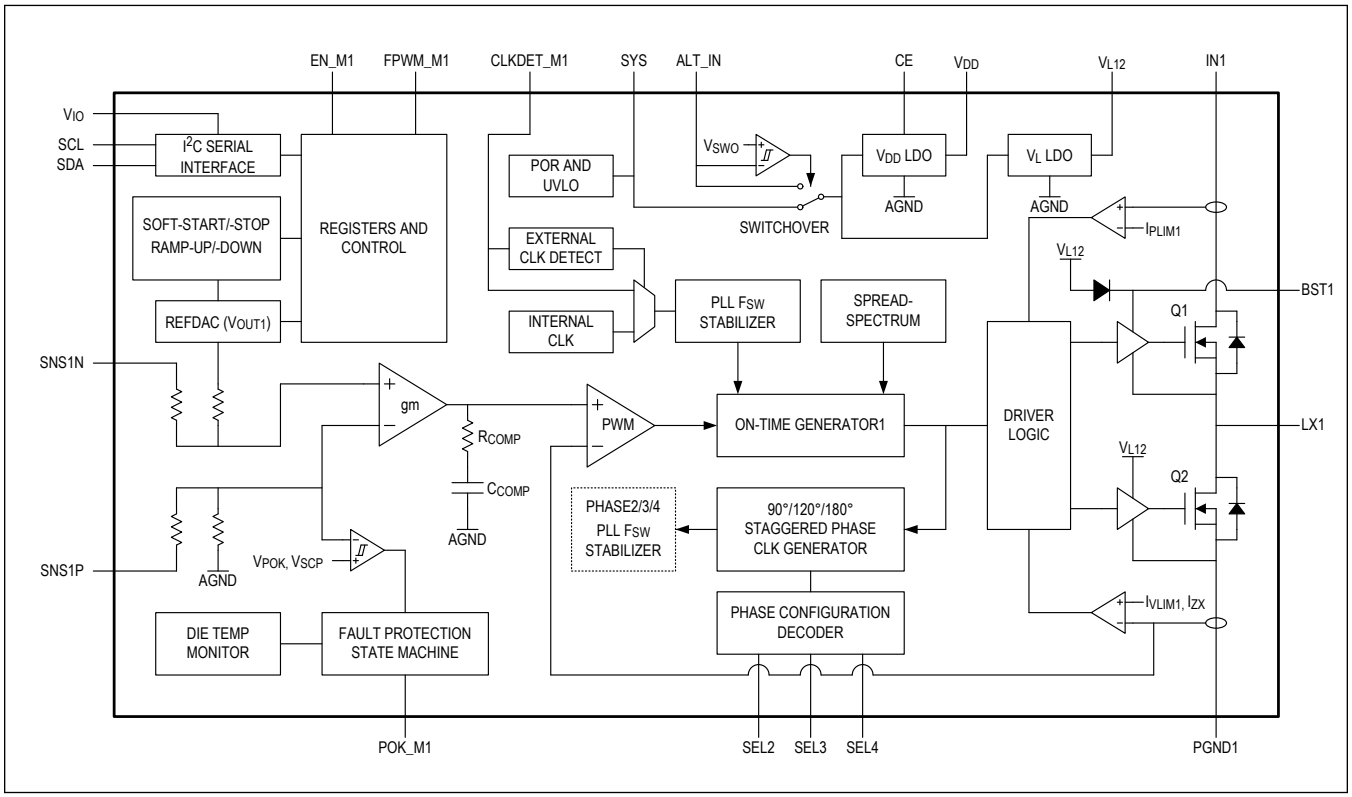


Figure 4. Functional Block Diagram

An on-time (MOSFET Q1 is on) is controlled by an on-time generator circuit which calculates an on-time based on the input voltage (V_{IN1}), the output voltage (V_{OUT1}), and the target switching frequency (F_{SW1}). An off-time (MOSFET Q2 is on) begins when the on-time ends. During the dead-time, the inductor current conducts through the intrinsic body diode. A PWM comparator regulates the V_{OUT1} by modulating off-time. The positive input of the PWM comparator is a voltage proportional to the actual output voltage error. The negative input is a voltage proportional to the inductor current sensed through the MOSFET Q2. The PWM comparator begins an on-time when the error voltage becomes higher than the current-sense signal. The off-time automatically begins again when the calculated on-time expires. A phase-locked loop (PLL) stabilizes the switching frequency and controls phase spacing. The PLL stabilizes slave phases 90°, 120°, or 180° apart from the master phase when the output is configured for multiphase operations. In multiphase configurations, all

master and slave phases are activated and always switch in sequence during steady-state operation. The phases do not add or shed.

Buck Operating Modes

The buck converters have three operating modes shown in Figure 5. Transitions between the modes are determined by operating conditions and mode control settings. The operating mode setting can be changed any time while the I^2C communication is available. Toggling between skip and FPWM modes is also controlled by the MFIOx pins (when the FPWM_Mx function is selected). Pull the FPWM_Mx (MFIOx) pin high to operate the corresponding buck in forced-PWM mode. When the FPWM_Mx (MFIOx) pin is held low, the operating mode is controlled by the Mx_LPM and the Mx_FPWM bits.

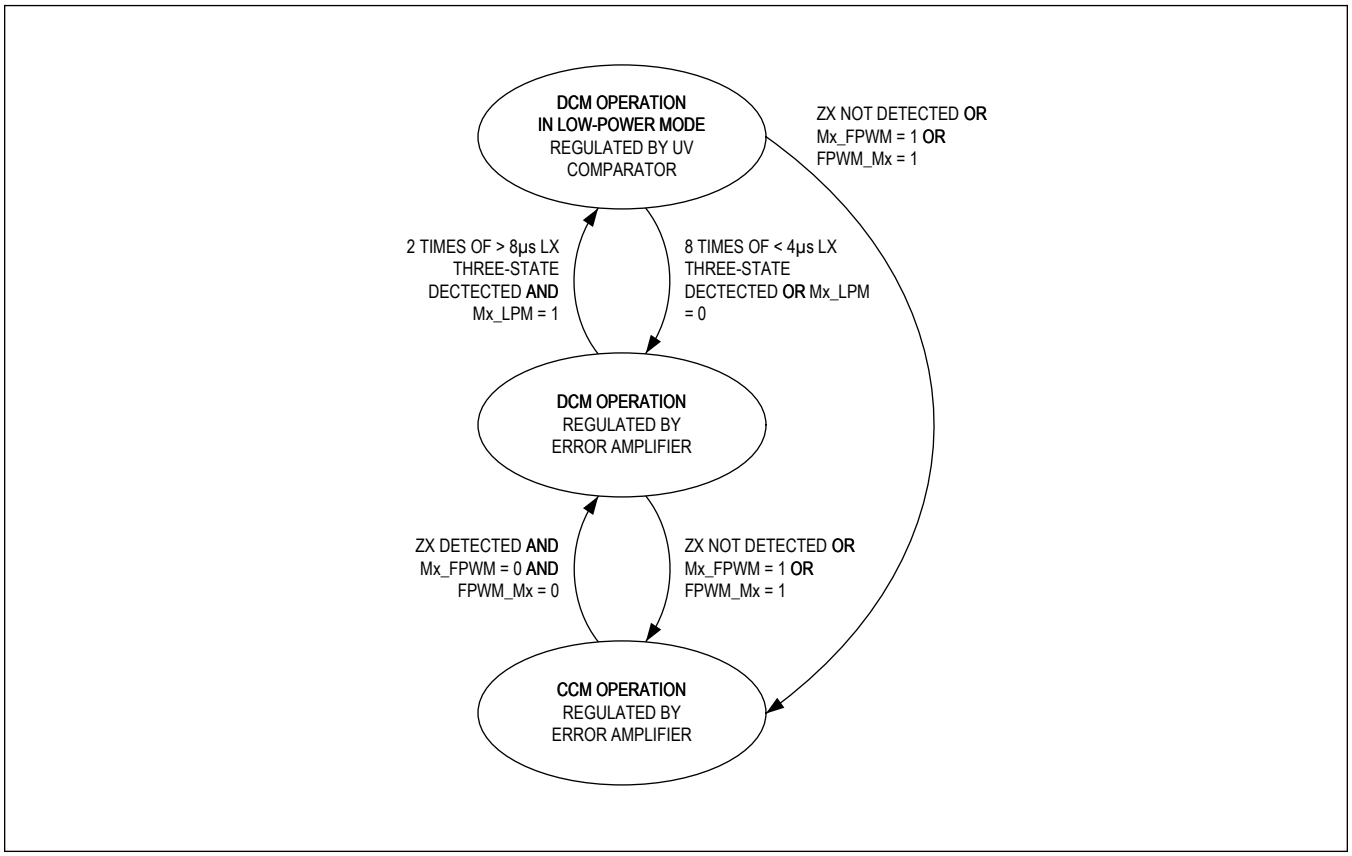


Figure 5. Buck Operating Modes

Detail mode control settings are described below:

Skip Mode

In skip mode (Mx_LPM = LPM_Mx = Mx_FPWM = FPWM_Mx = 0), the buck converter operates either in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) depending on loading. If the averaged output current is lower than a half of inductor peak-to-peak ripple current under light load condition, the low-side MOSFET turns off as soon as the inductor current drops to near zero ampere (zero-crossing). Then, the switching node (LX) remains in three-state (high impedance) until the next on-time is triggered. In this way, the buck prevents a negative inductor current which results in improving light-load efficiency by reducing the total number of switching cycles needed to regulate the output voltage.

When no zero crossing (ZX) is detected (under heavier load), the buck controller goes into CCM where the averaged

output current is greater than a half of inductor ripple current. In both DCM and CCM, the output voltage is regulated by an error amplifier. In case the on-time determined by a given operating condition in high output-voltage range (Mx_RNG[1:0] = 0x2) is not long enough, the on-time automatically extends until the inductor current reaches 500mA to ensure enough off-time to detect the ZX reliably.

Low-Power Skip (LP-Skip) Mode

Low-power skip mode {(Mx_LPM = 1 **OR** LPM_Mx = 1) **AND** Mx_FPWM = FPWM_Mx = 0} is similar to skip mode because a negative inductor current is also not allowed in LP-skip mode. When the averaged output current is decreased further down (> 8µs of LX three-state is detected two times consecutively) in skip mode, the buck converter enters LP-skip mode when low-power mode is enabled. In LP-skip mode, the error amplifier and other internal blocks are deactivated to reduce I_Q consumption. Instead of the error amplifier, a low-power comparator monitors the output voltage in LP-skip mode.

The buck enters DCM operation in skip mode when the duration of LX three-state is shorter than 4µs for eight times in a row or LP-skip mode is disabled (Mx_LPM = LPM_Mx = 0). If no zero-crossing is detected (e.g., sudden load transient) or FPWM mode is enabled (Mx_FPWM = 1 **OR** FPWM_Mx = 1), the buck enters CCM operation directly from LP-skip mode.

LP-skip mode is not recommended for 4Φ configuration.

Forced-PWM (FPWM) Mode

Forced-PWM mode (Mx_FPWM = 1 **OR** FPWM_Mx = 1) ensures a continuous inductor current under all load conditions. In FPWM mode, a negative inductor current through the low-side MOSFET is allowed but the maximum current is limited to the I_{NLIM} (typ -3A). In case a valid external frequency is detected on the MFIOx input (when the CLKDET_Mx function is selected), the corresponding buck enters FPWM mode regardless of its operating mode settings. See the *Frequency Tracking (FTRAK)* section for more information.

Drop-Out Mode

The MAX77542 architecture allows the buck converter to operate even when the input voltage approaches the target output voltage. When the headroom between the input and the output voltages reduces during operation, the buck controller tries to maintain the output-voltage regulation by increasing the duty cycle. In case the buck is not able to regulate the target output voltage with the maximum duty cycle (typ 98%), it automatically extends the on-time by skipping the off-times (drop-out mode). In drop-out mode, the low-side MOSFET turns on occasionally to refresh the bootstrap circuit for driving the high-side MOSFET. See the *Bootstrap Refresh* section for more information.

Switching Frequency

The MAX77542 has three nominal switching frequency options (0.5MHz, 1.0MHz, and 1.5MHz) to optimize the efficiency, the transient response, the noise performance, and the solution size. The default switching frequency of the bucks are set by the CFG2 input (see Table 3) and the switching frequencies of individual bucks are also selectable with the Mx_FREQ[1:0] bits.

At any given time, the switching frequency (F_{SW}) of the adaptive on-time buck converter is not fixed and is heavily influenced by the instantaneous load current. More on-time pulses in a given time (higher F_{SW}) are observed as the output current increases, while fewer on-times in a given time (lower F_{SW}) are observed when the output current decreases. A valid external frequency at the MFIOx input (when the CLKDET_Mx function is selected) or enabling the internal frequency tracking feature (Mx_FTRAK = 1) stabilizes the switching frequency of the corresponding buck in steady-state operation. See the *Frequency Tracking (FTRAK)* section for more information.

In case the on-time calculated by the given operating condition is less than the minimum on-time (typ 90ns), the buck controller regulates the output voltage by increasing the off-time. As a result, the actual switching frequency becomes slower than its nominal frequency setting. For example, the calculated duty cycle for 16V_{IN} and 0.8V_{OUT} is about 5%, which gives less than 90ns of on-time at 1MHz of nominal switching frequency. It means that the actual switching frequency under this condition is slower than 1MHz. Therefore, a 0.5MHz of nominal switching frequency setting is recommended.

Phase and Output Configuration

The MAX77542 has four 4A switching phases configurable to five phase configurations. As shown in Table 5, the buck converters are configured from a single output (4Φ) to four individual outputs (1Φ + 1Φ + 1Φ + 1Φ) based on resistor values on the SELx inputs.

Table 5. Phase-Configuration Selection

R_{SEL1} (Ω)	R_{SEL2} (Ω)	R_{SEL3} (Ω)	R_{SEL4} (Ω)	PHASE (Φ) CONFIGURATION	NUMBER OF OUTPUTS
Any	≥ 200	≥ 200	≥ 200	1Φ + 1Φ + 1Φ + 1Φ	4
Any	≤ 95.3	≥ 200	≥ 200	2Φ + 1Φ + 1Φ	3
Any	≤ 95.3	≥ 200	≤ 95.3	2Φ + 2Φ	2
Any	≤ 95.3	≤ 95.3	≥ 200	3Φ + 1Φ	2
Any	≤ 95.3	≤ 95.3	≤ 95.3	4Φ	1

Also, the output-voltage sensing of the buck converters is assigned based on the phase-configuration setting. In multiphase configurations, the buck controllers regulate the output voltage using the differential output-voltage sensing inputs (SNSxP/SNSxN) of the master phases. Table 6 shows how the output-voltage sensing inputs are configured for each phase configuration.

Table 6. Buck Output-Voltage Sensing Assignment

PHASE (Φ) CONFIGURATION	PHASE ASSIGNED*	BUCK NAMING CONVENTION	V_{OUT} SENSING INPUT
1Φ + 1Φ + 1Φ + 1Φ (4 Outputs)	Phase1 (M1)	Buck1 (V_{OUT1})	SNS1P/SNS1N
	Phase2 (M2)	Buck2 (V_{OUT2})	SNS2P
	Phase3 (M3)	Buck3 (V_{OUT3})	SNS3P/SNS3N
	Phase4 (M4)	Buck4 (V_{OUT4})	SNS4P
2Φ + 1Φ + 1Φ (3 Outputs)	Phase1 (M1) Phase2 (S1)	Buck1 (V_{OUT1})	SNS1P/SNS1N
	Phase3 (M3)	Buck3 (V_{OUT3})	SNS3P/SNS3N
	Phase4 (M4)	Buck4 (V_{OUT4})	SNS4P
2Φ + 2Φ (2 Output)	Phase1 (M1) Phase2 (S1)	Buck1 (V_{OUT1})	SNS1P/SNS1N
	Phase3 (M3) Phase4 (S3)	Buck3 (V_{OUT3})	SNS3P/SNS3N
3Φ + 1Φ (2 Output)	Phase1 (M1) Phase2 (S1) Phase3 (S1)	Buck1 (V_{OUT1})	SNS1P/SNS1N
	Phase4 (M4)	Buck4 (V_{OUT4})	SNS4P
4Φ (1 Output)	Phase1 (M1) Phase2 (S1) Phase3 (S1) Phase4 (S1)	Buck1 (V_{OUT1})	SNS1P/SNS1N

*Mx = Master phase.

Sx = Slave phase.

In multiphase configurations, the logic I/O pins and the control registers assigned to slave phases are deactivated so that register settings of the corresponding master phases dictate the operation of the slave phase as shown in Figure 6.

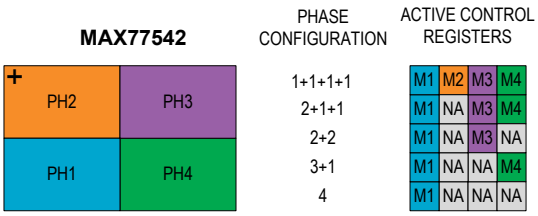


Figure 6. Active Control Registers

Default Output-Voltage Selection (SELx)

The MAX77542 supports user-selectable default voltages of individual buck outputs with 1% tolerance (or better) resistors. The MAX77542 evaluates the resistances between the SELx and the AGND whenever the V_{DD} regulator first turns on (exits shutdown). The decoded values of the R_{SELx} are latched until the next time the device exits shutdown mode. The SELx_LATCH[4:0] status bits reflect the latched decoded values of the R_{SELx}. See the *Register Map* section for more details.

The resistances between the SELx and the AGND (R_{SELx}) configure the default voltages of corresponding buck outputs. The R_{SEL2}, the R_{SEL3}, and the R_{SEL4} are also used in selecting phase configuration. When the SEL2, the SEL3, and/or the SEL4 pins are tied to the AGND on the PCB ($R_{SELx} \leq 95.3\Omega$), the corresponding buck is configured as a slave phase of a multiphase converter. See the *Phase and Output Configuration* section for more information.

In case multiphase configuration is selected, the decoded resistance (R_{SELx}) on the master phase sets the default output voltage. Table 7 and Table 8 decode the default selection options for the V_{OUT1}, the V_{OUT2}, the V_{OUT3}, and the V_{OUT4}, respectively. Once latched, the Mx_VOUT_H[7:0], the Mx_VOUT_L[7:0], the Mx_VOUT_B[7:0], and the Mx_RNG[1:0] bits reflect the selected options. The decoded values for $R_{SELx} \geq 115k\Omega$ are programmable at the factory.

Table 7. Default V_{OUT1} Selection

R_{SEL1} (Ω)	TARGET V_{OUT1} (V)	V_{OUT1} RANGE
≤ 95.3	0.500	Low
200	0.550	Low
309	0.600	Low
422	0.650	Low
536	0.675	Low
649	0.700	Low
768	0.720	Low
909	0.750	Low
1.05k	0.800	Low
1.21k	0.820	Low
1.40k	0.900	Low
1.62k	0.950	Low
1.87k	1.000	Low
2.15k	1.050	Low
2.49k	1.100	Low
2.87k	1.150	Low
3.74k	1.200	Low
8.06k	1.20	Mid
12.4k	1.25	Mid
16.9k	1.35	Mid

Table 7. Default V_{OUT1} Selection (continued)

R_{SEL1} (Ω)	TARGET V_{OUT1} (V)	V_{OUT1} RANGE
21.5k	1.40	Mid
26.1k	1.50	Mid
30.9k	1.80	Mid
36.5k	2.00	Mid
42.2k	2.5	High
48.7k	2.8	High
56.2k	3.0	High
64.9k	3.3	High
75.0k	3.4	High
86.6k	3.8	High
100k	5.0	High
≥ 115k	Factory Option	

Table 8. Default $V_{OUT2/3/4}$ Selection

$R_{SEL2/3/4}$ (Ω)	TARGET $V_{OUT2/3/4}$ (V)	$V_{OUT2/3/4}$ RANGE
≤ 95.3	Multiphase Configuration	
200	0.500	Low
309	0.550	Low
422	0.600	Low
536	0.650	Low
649	0.700	Low
768	0.720	Low
909	0.750	Low
1.05k	0.800	Low
1.21k	0.820	Low
1.40k	0.850	Low
1.62k	0.900	Low
1.87k	0.950	Low
2.15k	1.000	Low
2.49k	1.050	Low
2.87k	1.100	Low
3.74k	1.150	Low
8.06k	1.200	Low
12.4k	1.25	Mid
16.9k	1.35	Mid
21.5k	1.40	Mid
26.1k	1.50	Mid
30.9k	1.80	Mid
36.5k	2.00	Mid
42.2k	2.5	High
48.7k	2.8	High
56.2k	3.0	High

Table 8. Default $V_{OUT2/3/4}$ Selection (continued)

$R_{SEL2/3/4}$ (Ω)	TARGET $V_{OUT2/3/4}$ (V)	$V_{OUT2/3/4}$ RANGE
64.9k	3.3	High
75.0k	3.4	High
86.6k	3.8	High
100k	5.0	High
≥ 115k	Factory Option	

Output-Voltage Setting

The output voltages (V_{OUTx}) are adjustable between 0.3V and 5.2V in 5mV, 10mV, or 20mV steps depending on the Mx_RNG[1:0] bits as shown in Table 9. In each output-voltage range, the lowest code (0x00) of the output-voltage setting registers represents the minimum output voltage and the target output voltage is increased by one LSB step as the code increases. The Mx_VOUT_M[7:0] registers digitally limit the maximum programmable output voltages in each range even if the code increases beyond that point.

Each master phase has three output-voltage control registers. The Mx_VOUT_H[7:0] register is used for normal operation when the VSEL function and VB functions are not used (VSEL_Mx and VB_Mx signals are considered logic high). When the VSEL or VB function of the MFIOx is selected, the Mx_VOUT_L[7:0] or the Mx_VOUT_B[7:0] register controls the output voltage depending on the logic inputs. See the *Output-Voltage Selection (VSEL)* and *Boot (Default) Output-Voltage Selection (VB)* sections for more information.

The default values of the Mx_VOUT_H[7:0], the Mx_VOUT_L[7:0], the Mx_VOUT_B[7:0], and the Mx_RNG[1:0] registers are set by the corresponding R_{SELx} values. See the *Default Output-Voltage Selection (SELx)* section for more information.

For output voltages that have overlapping ranges (e.g., 1V), select the desired range by trading off the load transient response and the required effective output capacitance. Using the 1V output example: use low range for a slightly better load transient response, or mid range for a slightly worse transient response but with less effective output capacitance requirement. See the *Output-Capacitor Selection* for more information on the required effective output capacitance for the different output-voltage ranges.

Table 9. Buck Output-Voltage Range

Mx_RNG[1:0]	V_{OUT} PROGRAMMING RANGE	STEP PER LSB
0x0 (Low range)	0.3V to 1.3V	5mV
0x1 (Mid range)	0.6V to 2.6V	10mV
0x2 (High range)	1.2V to 5.2V	20mV

Note that the Mx_RNG[1:0] bits are latched by R_{SELx} detection and are protected from unauthorized access. In case the output-voltage range needs to be changed during operation, contact sales representatives.

Soft-Start and Soft-Stop

The bucks always soft-start whenever they are enabled (regardless of the EN_Mx (MFIOx) or I^2C command) or when recovering from a fault condition. When the individual buck is disabled by the EN_Mx (MFIOx) or I^2C command, the buck always initiates soft-stop. When a POK fault time-out or a SCP event occurs to a buck output, only the corresponding buck stops switching immediately (LX node becomes high impedance) without affecting the operation of the other buck outputs. In case a UVLO or a TSHDN fault happens, all buck outputs stop switching immediately.

Each buck has internal ramps that control the slew rate of output-voltage changes during soft-start and soft-stop. The soft-start and the soft-stop slew rates are set individually by the Mx_SSTRT_SR[2:0] and the Mx_SSTOP_SR[2:0] bits, respectively. During soft-start and soft-stop, the bucks automatically enter FPWM mode regardless of operating mode settings when the Mx_FSREN bits are set to 1 (default). To support "Pre-biased" startup (startup without discharging pre-existing voltage at the output), the Mx_FSREN and the Mx_ADIS100 bits need to be set to 0 before the buck is enabled.

The Mx_SSTRT_SR[2:0] and the Mx_SSTOP_SR[2:0] bits set the slew rates of a voltage reference to an error amplifier. When the fastest slew-rate option is selected, the actual output-voltage slew rate might be slower than the target

setting due to limited sourcing and the sinking current capabilities of bucks under given circuit parameters and operating conditions. See Table 10 for more information.

Dynamic Output-Voltage Scaling

In a typical processing power application, there are several power domains in which the operating (clock) frequency of the processor is increased or decreased based on the amount of tasks in a given time. When the operating frequency needs to be changed, it is expected that the corresponding buck converter responds to a command for changing its output voltage to a new target value with a specific slew rate.

Whenever a new target value is written in the Mx_VOUT_H[7:0] bits through I^2C while the corresponding buck is enabled, the output voltage starts to change. The output voltage ramps up (or down) at a positive (or negative) slew rate set by the corresponding Mx_RU_SR[2:0] (or Mx_RD_SR[2:0]) bits. When the Mx_FSREN bit is set, the corresponding buck enters FPWM mode automatically (regardless of the Mx_FPWM bit) during the output voltage ramp-down (or soft-stop). In FPWM mode, the buck can sink current from the C_{OUTx} to the PGNDx through the low-side MOSFET which allows the V_{OUTx} to track the negative rate set by the Mx_RD_SR[2:0] bits.

Table 10. Mx_FSREN Effect on Buck Behavior

OPERATING MODE	Mx_FSREN	BUCK BEHAVIOR IN STEADY STATE	BUCK BEHAVIOR DURING DYNAMIC VOLTAGE SCALING
Skip or LP-Skip	0	Source Only	Source Only
	1	Source Only	Source or Sink
FPWM	X	Source or Sink	Source or Sink

Note: Buck outputs (V_{OUTx}) with current sinking capability can follow the negative ramp rates set by the Mx_RD_SR[2:0] or the Mx_SSTOP_SR[2:0].

If the negative inductor current reaches the I_{NLIM} (typ -3A), the low-side MOSFET is turned off immediately and the buck initiates a new on-time (high-side MOSFET turn-on). Thus, the maximum slew rate during output-voltage ramp-down (or soft-stop) is limited if an effective output capacitance is very high for the selected ramp-down (or soft-stop) slew rate. The maximum output-voltage slew rate is calculated by following formula, $dV_C/dt = i_C/C$.

Output-Voltage Active Discharge

Each buck converter integrates a 100Ω active discharge resistor between the LXx and the PGNDx for discharging the output capacitor when the buck output is disabled. For faster output-voltage discharge at the end of soft-stop, a 1Ω active discharge function is added. Those two active discharge resistors are individually enabled by setting the Mx_ADIS100 and the Mx_ADIS1 bits, respectively. If both the Mx_ADIS100 and the Mx_ADIS1 are set to 1, the 1Ω active discharge is first activated for 1ms right after soft-stop is completed, and the 100Ω active discharge is then enabled until the next time the buck is enabled. In shutdown mode (CE = 0), the 100Ω active discharge of each buck phase is deactivated.

Note that the 1Ω active discharge function of the corresponding output must be disabled (Mx_ADIS1 = 0) to avoid excessive power dissipation when the falling slew-rate control feature is disabled (Mx_FSREN = 0).

Bootstrap Refresh

When the buck is in drop-out operation or in skip (or LP-skip) mode under extremely light load condition, the low-side MOSFET does not turn on for a long period of time. In this case, the buck controller occasionally turns on the low-side MOSFET for about 100ns (typ) to charge a bootstrap circuit for driving the high-side MOSFET. The bootstrap-refresh interval is set to 128µs by default. The bootstrap-refresh interval can be reduced to 10µs when the Mx_REFRESH bit is set to 1. The bootstrap-refresh interval selection is shown in Table 11.

Table 11. Bootstrap-Refresh Interval Selection

Mx_REFRESH	REFRESH INTERVAL
0	128µs
1	10µs

The bootstrap refresh is also required when the buck converter starts switching. As a part of the startup procedure, the

buck controller forces refresh pulses 16 times with an interval of 3µs.

Frequency Tracking (FTRAK)

The MAX77542 supports the frequency tracking feature. When a valid external clock is detected on the MFIOx input (when CLKDET_Mx function is selected), the corresponding buck converter enters FPWM mode regardless of its operating mode setting and tracks the external frequency by modulating on-times. This event triggers the MFIOx_I interrupt if unmasked. When the external tracking feature is enabled, Buck1 and Buck3 attempt to track the beginning of on-times to the rising edges of the external clock, while Buck2 and Buck4 attempt to track the beginning of on-times to the falling edges of the external clock.

Table 12. Mx_FTRAK Enable Truth Table

CLKDET_Mx (MFIOx)	Mx_FTRAK	PLL	BUCK OPERATING MODE	NOTE
Not Detected	0	Disabled	Depends on Buck Mode Setting	No Tracking
Not Detected	1	Enabled	Depends on Buck Mode Setting	Internal Frequency Tracking
Detected	0	Enabled	FPWM	External Frequency Tracking
Detected	1	Enabled	FPWM	External Frequency Tracking

As shown in Table 12, the bucks can also track an internal clock. When the FTRAK function is enabled (Mx_FTRAK = 1), the corresponding buck tracks the internal PLL frequency (set by the Mx_FREQ[1:0] bits) if no valid external clock is applied. In case a valid external clock is detected while the corresponding buck is tracking the internal PLL, it switches to the external clock tracking. The frequency window for both external and internal tracking is about ±5% of the nominal switching frequency. The frequency tracking operation is vaild whenever one of the buck converters is enabled. The CLKDET_Mx (MFIOx) must be driven either low or high to prevent chattering or false tracking (see Figure 7).

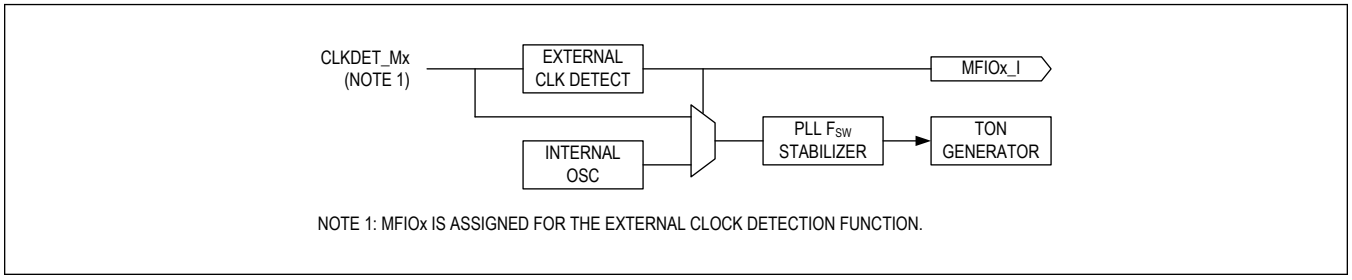


Figure 7. Frequency Tracking

The phase sequences with the internal and the external frequency tracking are shown in Table 13.

Table 13. Phase Sequence

PHASE CONFIGURATION	INTERNAL FTRAK	EXTERNAL FTRAK
1+1+1+1	PH1(M): 0° PH2(M): 180° PH3(M): 90° PH4(M): 270°	PH1(M): Rising Edge PH2(M): Falling Edge PH3(M): Rising Edge PH4(M): Falling Edge
2+1+1	PH1(M): 0° PH2(S): 180° PH3(M): 90° PH4(M): 270°	PH1(M): Rising Edge PH2(S): 180° from M1 PH3(M): Rising Edge PH4(M): Falling Edge
2+2	PH1(M): 0° PH2(S): 180° PH3(M): 90° PH4(S): 270°	PH1(M): Rising Edge PH2(S): 180° from M1 PH3(M): Rising Edge PH4(S): 180° from M3

Table 13. Phase Sequence (continued)

3+1	PH1(M): 0° PH2(S): 240° PH3(S): 120° PH4(M): 270°	PH1(M): Rising Edge PH2(S): 240° from M1 PH3(S): 120° from M1 PH4(M): Falling Edge
4	PH1(M): 0° PH2(S): 180° PH3(S): 90° PH4(S): 270°	PH1(M): Rising Edge PH2(S): 180° from M1 PH3(S): 90° from M1 PH4(S): 270° from M1

Spread-Spectrum Modulation

The bucks are capable of dithering its switching frequency for noise-sensitive applications. The spread-spectrum function of each buck is individually enabled by setting the Mx_SS_ENV[1:0] bits. The spread-spectrum function is activated only in continuous conduction mode (CCM) and it is automatically deactivated when the bucks enter discontinuous conduction mode (DCM). The spread-spectrum modulation pattern is programmable either in pseudo-random or triangular patterns by the Mx_SSM_PAT[1:0] bits. The spread-spectrum modulation is characterized by modulation envelope and modulation frequency:

- The modulation envelope (ΔF_{SS}) determines the maximum difference between the modulated switching frequency and the nominal switching frequency. The modulation envelope is programmable (±8%, ±12%, or ±16%) with the Mx_SS_ENV[1:0] bits and it controls how wide the switching frequency dithers.
- The modulation frequency (F_{SS_MOD}) determines how often the switching frequency changes from one value to another. The modulation frequency is also programmable (1kHz, 3kHz, 5kHz, or 7kHz) with the Mx_SS_FREQ[1:0] bits and it controls how fast the switching frequency dithers.

Pseudo-Random Pattern

The pseudo-random engine uses a 4-bit linear feedback shift register (LFSR) to create a pseudo-random value as shown in Figure 8. The LFSR value is converted to an analog signal and then amplified before being added to the output of the on-time generator circuit. The pseudo-random value shortens or lengthens the on-time. This causes the buck controller to increase or decrease the switching frequency to maintain voltage regulation. Each buck has its own pseudo-random pattern generator.

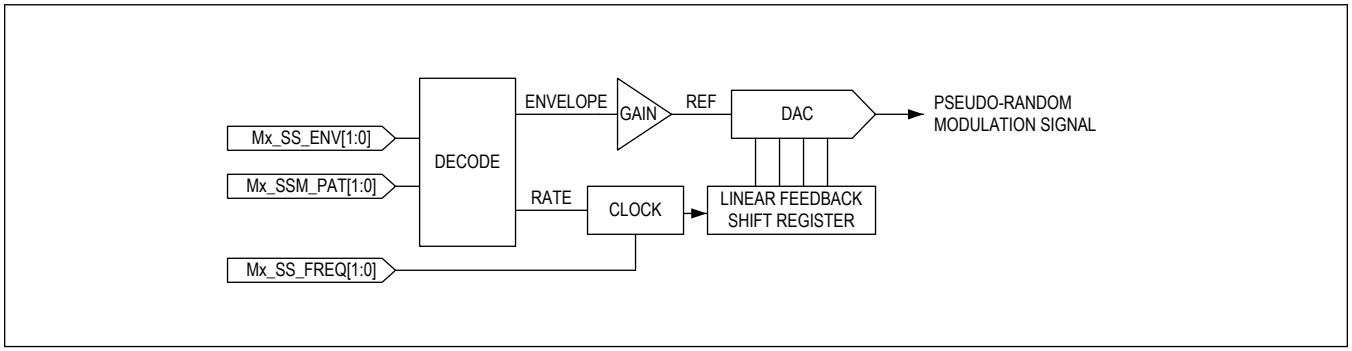


Figure 8. Pseudo-Random Modulator Engine

The modulation envelope and frequency are programmable with the Mx_SS_ENV[1:0] and the Mx_FREQ[1:0] bits. The F_{SS_MOD} sets the frequency at which the LFSR wraps back to the seed value. The clock rate of the LFSR is the F_{LFSR}. This is the frequency at which one pseudo-random value changes to another. An example is shown in Figure 9.

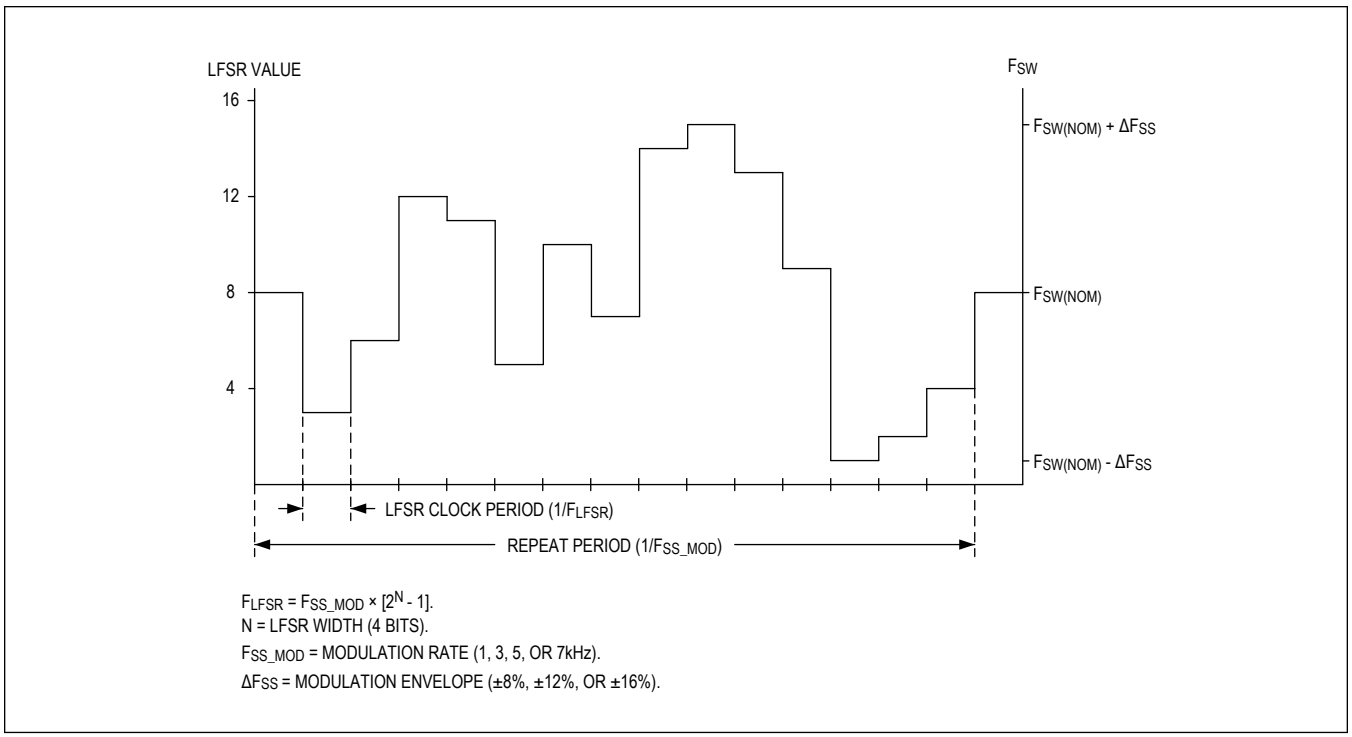


Figure 9. 4-Bit Pseudo-Random Modulation Signal Example

Triangular Pattern

The triangular engine uses a 4-bit up/down synchronous counter to create a stepped triangle pattern as shown in Figure 10. The counter value is converted to an analog signal and then amplified before being added to the output of the on-time generator circuit. The counter value progressively shortens and lengthens the on-time. This causes the buck controller to progressively increase and decrease the switching frequency to maintain voltage regulation. Each buck has its own triangular pattern generator.

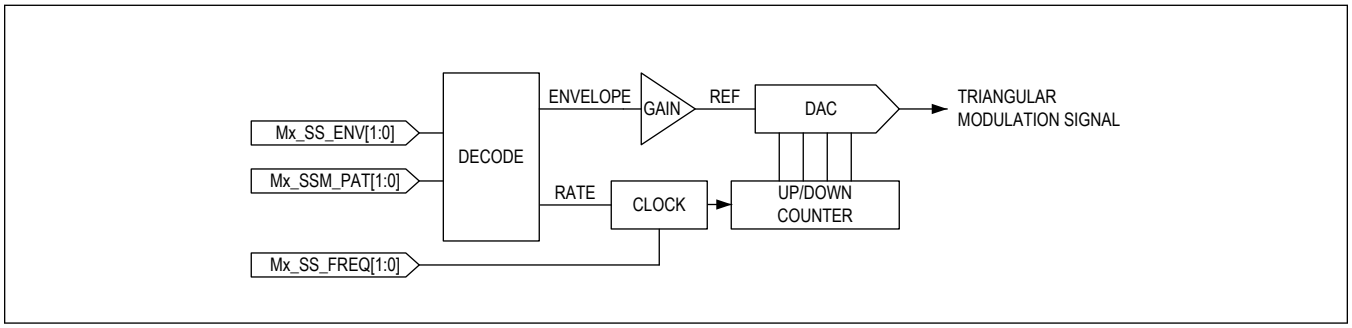


Figure 10. Triangular Modulator Engine

The modulation envelope and frequency are programmable with the Mx_SS_ENV[1:0] and the Mx_FREQ[1:0] bits. The F_{SS_MOD} sets the frequency at which the counter returns to the same value. The clock rate of the counter is the F_{COUNT}. This is the frequency at which the frequency changes from one value to another. An example is shown in Figure 11.

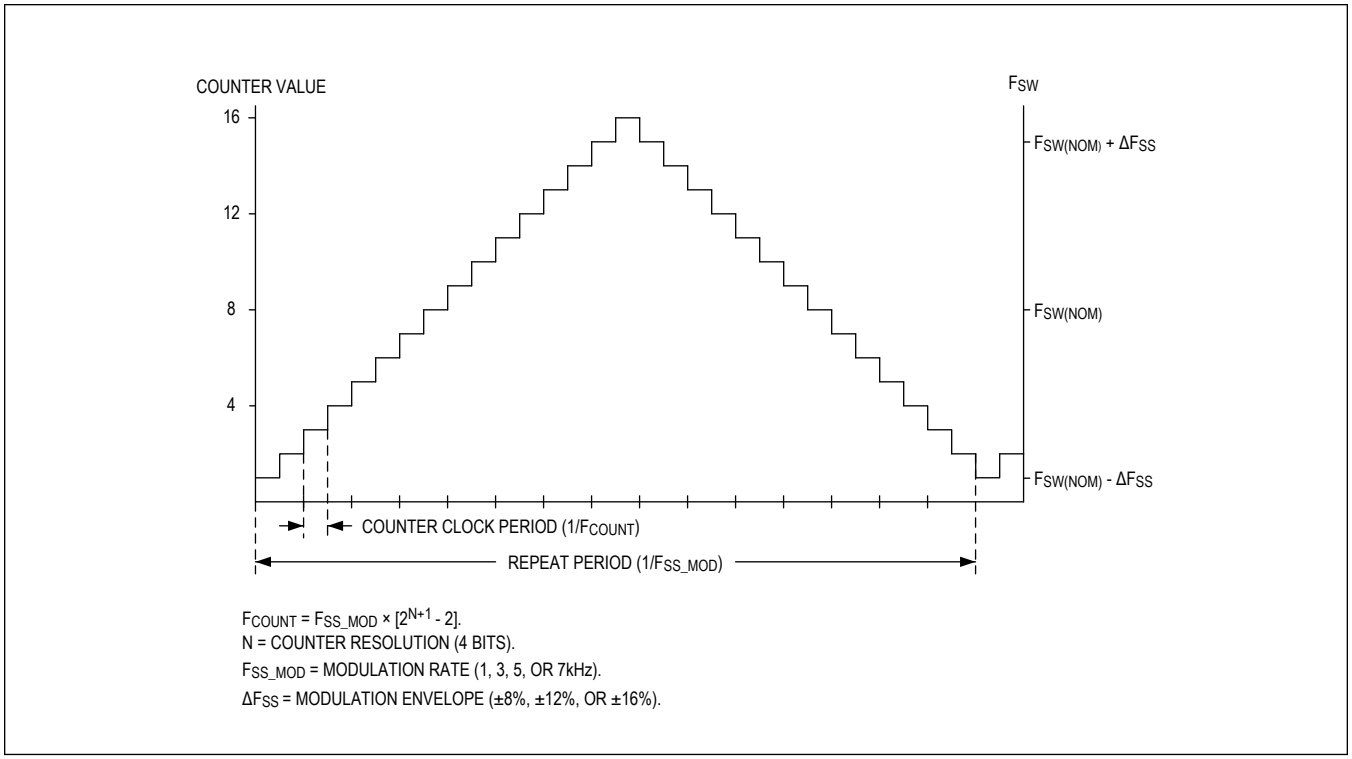


Figure 11. 4-Bit Triangular Modulation Signal Example

Inductor Current Limits

The MAX77542 has a cycle-by-cycle current limit feature that prevents the inductor current (in each phase) from increasing beyond the I_{PLIM}. If an on-time is ended by the peak current limit, the buck prevents a new on-time from starting until the inductor current falls below the valley current limit (I_{VLIM}) which is typically set 1A less than the I_{PLIM}. This prevents the inductor current from increasing uncontrollably due to the overloaded output. In case the on-time determined by the given operating condition is less than 130ns (typ), the next on-time pulse is not triggered until the inductor current hits the I_{VLIM}. Each buck has four PLIM thresholds which are individually set with the Mx_ILIM[1:0] bits. See the *Register Map* section for more details. The programmable PLIM thresholds allow an optimal circuit protection and inductor selections for the given operating conditions and load requirements.

Power-OK (POK)

The MAX77542 features power-OK (POK) comparators to monitor the quality of each buck output. The Mx_POK status bits continuously reflect the status of these monitors. The Mx_POK bit goes high if the corresponding buck output voltage rises above the V_{POK_R} (typ 82% of the V_{OUT} target) when soft-start is completed. When the corresponding buck output falls below the V_{POK_F} (typ 78% of the V_{OUT} target), the Mx_POK bit goes low. When unmasked, the Mx_POKFLT_I interrupt sets whenever the Mx_POK status bit changes from 1 to 0. The Mx_POKFLT_I bits are individually maskable. See the *Register Map* section for more details.

The quality of the buck output can be directly monitored using the POK function of the MFIOx pins. See the *Power-OK (POK) Output* section for more information.

Fault Protection

The MAX77542 has a fault-protection scheme designed to protect itself from abnormal conditions. Each individual buck has its own fault state machine (shown in Figure 12) which is independently triggered by a short-circuit protection (SCP), a thermal shutdown (TSHDN), and/or an undervoltage lock-out (UVLO) event. The operation of the state machine is summarized as follows:

- If the V_{SYS} falls below the V_{UVLO_F} (typ 2.7V), all individual buck outputs are disabled immediately (the UVLO_I interrupt asserts) and the output-voltage setting registers (Type F) of all buck phases are reset to their default values (enters buck x output off state).
- If the V_{IO} falls below the $V_{IO\_UVLO\_F}$ (typ 0.97V), all individual buck outputs are disabled immediately (the VIOFLT_I interrupt asserts) and the output-voltage setting registers (Type F) of all buck phases are reset to their default values (enters buck x output off state).
- If one of the enabled buck outputs falls below the V_{POK_F} (typ 78% of regulation target), the Mx_POKFLT_I asserts.
- If one of the enabled buck outputs stays below the V_{POK_R} (typ 82% of regulation target) for longer than the t_{POK_TO}, only the corresponding output is disabled immediately and the output-voltage setting registers (Type F) of the corresponding buck are reset to their default values.
- If one of the enabled buck outputs falls below the V_{SCP} (typ 20% of regulation target), only the corresponding output is disabled immediately (the Mx_SCFLT_I interrupt asserts) and the output-voltage setting registers (Type F) of the corresponding buck are reset to their default values.
- If the junction temperature exceeds the T_{SHDN} (typ +165°C), all individual buck outputs are disabled immediately (the TSHDN_I interrupt asserts) and the output-voltage setting registers (Type F) of all buck phases are reset to their default values.
- POK and SCP monitoring are not active (masked) during soft-start and soft-stop.

When POK fault time-out, SCP, and/or TSHDN fault occurs, the corresponding buck enters either the latch-off or the wait state from the reset state, depending on the AUTO_RSTRT bit setting.

- If AUTO_RSTRT = 0,
  - The output of the individual buck is forced disabled in latch-off state.
  - When Mx_EN = EN_Mx = 0 **AND** $T_J \le +150°C$, the individual buck exits latch-off state and enters buck x output off state.
- If AUTO_RSTRT = 1,
  - After 500ms of forced-disable in wait state, the individual buck automatically exits wait state and enters buck x output off state, if the junction temperature falls below +150°C (TSHDN = 0).
  - If the enable logic of individual buck is still valid when it enters buck x output off state, the corresponding buck initiates soft-start as it goes into buck x output on state immediately.

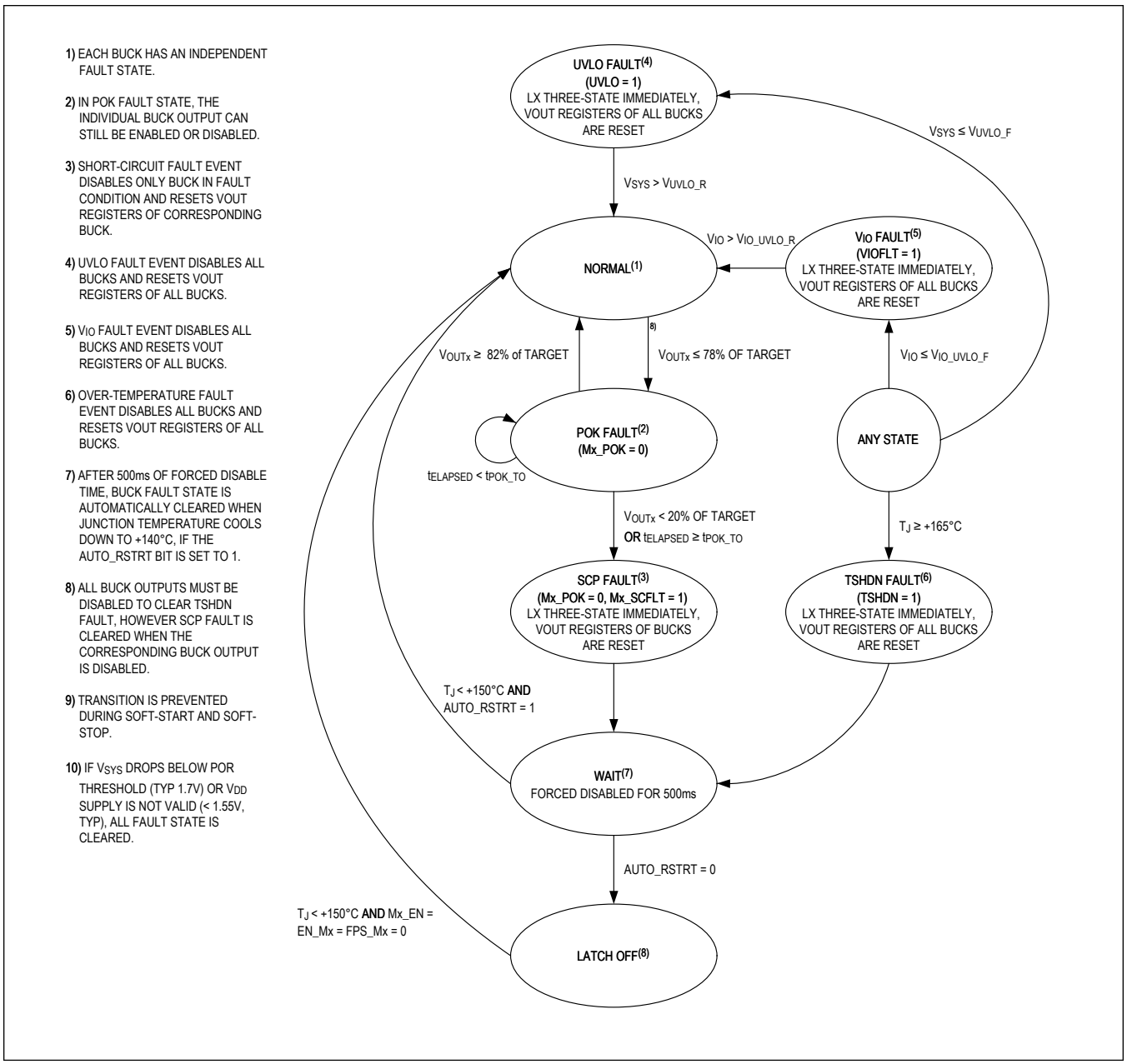


Figure 12. Fault-Protection State Diagram

Detailed Description—Multifunction I/Os

The MAX77542 has eight multifunction I/Os (MFIO1 through MFIO8) which can be configured as output enable, low-power mode, forced-PWM mode, external clock detection, clock output, output-voltage selection, POK output, FPS input, FPS output, system reset input, system reset output, thermal-warning output, GPIO, and ADC mux input. The default functions of the MFIOs are selected by the R_{CFG1} (see the *Device Configuration (CFGx)* section for more information) and they are individually selectable through the I²C interface. The I/O supply voltage (V_{IO}) must be valid for the MFIOx to operate in the GPO function with push-pull mode. Each MFIO has a set of interrupt, interrupt mask, and status bits. When unmasked, the interrupt bit sets whenever activated input state toggles.

MFIO Functions

The user-selectable functions of the MFIOs are shown in Table 14 and the function of each MFIO is selected by the MFIOx_FUNC[3:0] bits.

Table 14. MFIO Functions

MFIOx_FUNC[3:0]	FUNCTION	LOGIC POLARITY	OUTPUT DRIVER	INTERNAL RESISTOR	DEBOUNCE TIMER AND INTERRUPT
0x0	Output Enable (EN)	Active-High	N/A	Programmable Pull-Up/Pull-Down	Enabled
0x1	Low-Power Mode (LPM)	Active-High	N/A	Programmable Pull-Up/Pull-Down	Enabled
0x2	Forced-PWM Mode (FPWM)	Active-High	N/A	Programmable Pull-Up/Pull-Down	Enabled
0x3	External Clock Detection (CLKDET)	Active-High	N/A	Disabled*	Enabled
0x4	Clock Output (CLKOUT)	Active-High	Push-Pull*	N/A	Disabled
0x5	Output-Voltage Selection (VSEL)	Active-High	N/A	Programmable Pull-Up/Pull-Down	Enabled
0x6	Boot (Default) Output-Voltage Selection (VB)	Active-Low	N/A	Programmable Pull-Up/Pull-Down	Enabled
0x7	Power-OK Output (POK)	Active-High	Open Drain or Push-Pull	N/A	Disabled
0x8	FPS Input (FPSI)	Active-High	N/A	Programmable Pull-Up/Pull-Down	Enabled
0x9	FPS Output (FPSO)	Active-High	Open Drain or Push-Pull	N/A	Disabled
0xA	System Reset Input (RSTINB)	Active-Low	N/A	100kΩ Pull-Up to V_{IO}*	Enabled
0xB	System Reset Output (RSTOB)	Active-Low	Open Drain*	N/A	Disabled
0xC	Thermal-Warning Output (TWARNB)	Active-Low	Open Drain*	N/A	Disabled
0xD	General-Purpose Input (GPI)	Active-High	N/A	Programmable Pull-Up/Pull-Down	Enabled
0xE	General-Purpose Output (GPO)	Active-High	Open Drain or Push-Pull	N/A	Disabled
0xF	ADC MUX Input (ADCMUX) for MFIO8	N/A	N/A	N/A	N/A

*Settings by R_{CFG1} override the MFIOx_PDPU[1:0] and the MFIOx_DRV_MODE bits.

The I/O signal of each function is selected by the MFIOx_SEL[2:0] bits as shown in Table 15.

Table 15. MFIO I/O Selection

MFIOx_SEL[2:0]*	EN, LPM, FPWM, CLKDET, VSEL, VB	CLKOUT	POK	GPO
0x0	M1	0 Clock Shifts	M1	High Impedance
0x1	M2	1 Clock Shift	M2	High Impedance
0x2	M3	2 Clock Shifts	M3	High Impedance
0x3	M4	3 Clock Shifts	M4	High Impedance
0x4	GLB (M1, M2, M3, M4)	Low	POK_M1, POK_M2, POK_M3, and POK_M4	High Impedance

Table 15. MFIO I/O Selection (continued)

0x5	N/A	Low	Low	High
0x6	N/A	Low	Low	Low
0x7	N/A	Low	Low	High Impedance

*MFIOx_SEL[2:0] bits are redundant to FPSI, FPSO, RSTINB, RSTOB, TWARNB, GPI, and ADCMUX functions.

Output Enable (EN)

When the MFIOx are configured as output enable pins, the enable logic of a buck converter is an OR logic of the MFIOx and the corresponding enable register bit (Mx_EN). For example, if the MFIO1 is assigned to Buck Master1 enable (MFIO1_FUNC[3:0] = 0x0 and MFIO1_SEL[2:0] = 0x0), Buck Master1 enable is controlled by the MFIO1 pin and the M1_EN bit. In case more than one MFIO is configured as the same enable function (e.g., MFIO2_FUNC[3:0] = MFIO3_FUNC[3:0] = 0x0 and MFIO2_SEL[2:0] = MFIO3_SEL[2:0] = 0x1), those inputs are OR'ed with the M2_EN bit.

Low-Power Mode (LPM)

When the MFIOx are configured as low-power mode pins, the low-power mode logic of a specific buck converter is an OR logic of the MFIOx and the corresponding enable register bit (Mx_LPM). See the *Low-Power Skip (LP-SKIP) Mode* section for more information.

FPWM Mode (FPWM)

When the MFIOx are configured as the FPWM control input, the FPWM control logic of a specific buck converter is an OR logic of the MFIOx and the corresponding enable register bit (Mx_FPWM). See the *Forced-PWM (FPWM) Mode* section for more information.

External Clock Detection (CLKDET)

When the MFIOx are configured as external clock detection inputs, the corresponding buck converter tracks a valid external clock signal at the MFIOx input. When a valid external clock is detected, the MFIOx status bit sets to 1 which initiates a corresponding interrupt bit when unmasked. The external frequency detection is deactivated when all buck outputs are disabled. Note that no more than one MFIO must be assigned as an external clock detection function for a specific buck converter at a time. See the *Frequency Tracking (FTRAK)* section for more information.

Clock Output (CLKOUT)

The MFIOx is configured as a clock output (active-high, push-pull) when MFIOx_FUNC[3:0] = 0x4. The CLKOUT provides the same frequency as the nominal switching frequency of the Buck Master1 which is selected by the M1_FREQ[1:0] bits. For supporting a phase interleaving feature between multiple devices, the CLKOUT signal can be shifted by 0 to 3 clocks from the Buck Master1 frequency with the MFIOx_SEL[2:0] bits. The CLKOUT is disabled when all the buck outputs are turned off. In case the CLKOUT is required in the system even when all the buck outputs are disabled, the CLK_EN bit (0x0C) needs to be set to 1.

Output-Voltage Selection (VSEL)

When the MFIOx are configured as voltage-selection pins, the output voltage of a specific buck converter is set by the Mx_VOUT_H[7:0] and Mx_VOUT_L[7:0] registers based on the VSEL_Mx input. For example, if MFIO1_FUNC[3:0] = 0x5 and MFIO1_SEL[2:0] = 0x0, the output voltage of Buck Master1 is set by the M1_VOUT_H[7:0] and the M1_VOUT_L[7:0] when MFIO1 = high and MFIO1 = low, respectively. In case more than one MFIO isconfigured as the same voltage-selection function, those inputs are OR'ed. During the output-voltage transition, the ramp-up/ramp-down slew rate is controlled by the Mx_RU_SR[2:0] and the Mx_RD_SR[2:0].

Boot (Default) Output-Voltage Selection (VB)

When the MFIOx are configured as boot (default) voltage-selection pins, the output voltage of a specific buck converter is set by the Mx_VOUT_H[7:0] (or the Mx_VOUT_L[7:0]) and Mx_VOUT_B[7:0] registers based on the input logic. For example, if MFIO1_FUNC[3:0] = 0x6 and MFIO1_SEL[2:0] = 0x1, the output voltage of Buck Master2 is set by the M2_VOUT_H[7:0] (or the M2_VOUT_L[7:0]) and the M2_VOUT_B[7:0] when MFIO1 = high and MFIO1 = low, respectively. In case more than one MFIO is configured as the same voltage-selection function, the VB is an AND logic of

those inputs. During the output-voltage transition, the ramp-up/ramp-down slew rate is controlled by the Mx_RU_SR[2:0] and the Mx_RD_SR[2:0].

Power-OK (POK) Output

The MFIOx can be configured as a power-OK (POK) output of a specific buck converter. For example, if the MFIO1 is assigned to Buck Master1 POK output (MFIO1_FUNC[3:0] = 0x7 and MFIO1_SEL[2:0] = 0x0), the MFIO1 pin goes high if Buck Master1 output voltage rises above the V_{POK_R} (typ 82% of the V_{OUT} target) when soft-start is completed. In case Buck Master1 output falls below the V_{POK_F} (typ 78% of the V_{OUT} target), the MFIO1 goes low. When the MFIOx is configured as an open-drain POK output, an external pull-up resistor (typ 10kΩ to 100kΩ) is required.

FPS Input (FPSI)

When a MFIOx is configured as an FPS enable input, the enable logic of the flexible power sequencer is an OR logic of the MFIOx and the FPS_EN bit. When either signal becomes logic high, the MAX77542 initiates a startup sequence which is determined by the GLB_CFG1 through GLB_CFG6 registers. If both signals become logic low, it triggers a shutdown sequence.

FPS Output (FPSO)

When a MFIOx is configured as an FPS output pin, the MFIOx pin can drive the enable signals of other devices. As a part of the startup and shutdown sequence, the MFIOx goes high or low based on the FPSO_STUP_DLY[3:0], the FPSO_SHDN_DLY[3:0], and the DLY_STEP[1:0] bits. When the MFIOx is configured as an open-drain FPS output, an external pull-up resistor (typ 10kΩ to 100kΩ) is required.

System Reset Input (RSTINB)

When a MFIOx is configured as a system reset input pin, a logic-low signal (active-low, pulled up to the V_{IO} pin with an internal 100kΩ resistor) longer than its debounce timer setting is considered as a valid reset input signal. If the RSTINB_SHDN bit is set to 1, a valid reset input signal initiates a reset of all functional registers (both Type O and Type F) to their POR default values for 1µs. When the RSTINB_SHDN bit is set to 0, the MAX77542 ignores the RSTINB input and takes no action. In case more than one MFIO is configured as the system reset input function, the RSTINB is an AND logic of those inputs.

System Reset Output (RSTOB)

When a MFIOx is configured as a system reset output pin, the MAX77542 generates a reset output signal (active-low, open drain) to indicate a fault condition of the device to a host processor or companion devices. The Mx_RSTOB_EN, the TSHDN_RSTOB_EN, and the UVLO_RSTOB_EN bits allow the host processor to configure which fault condition triggers the reset output signal. Note that a short-circuit protection (SCP) event asserts the system reset signal for about 3µs and de-asserts it as the SCP event turns off the corresponding buck output.

Thermal Warning Output (TWARNB)

When a MFIOx is configured as a thermal warning output pin, the MAX77542 generates a logic signal (active-low, open drain) to indicate that the junction temperature of the die reaches the thermal warning threshold. The TWARN_TH[2:0] bits allow a host processor to set the thermal warning threshold between +95ºC and +130ºC with 5ºC steps.

General-Purpose Input (GPI)

The MFIOx pins are configured as general-purpose inputs when MFIOx_FUNC[3:0] = 0xD. In GPI mode, the corresponding status bits (MFIOx) represent the current logic data at the MFIOx inputs. When unmasked, toggling of input logic generates an interrupt. The debounce timer and the internal pull-down resistor settings are configured by the MFIOx_DEB[2:0] and the MFIOx_PDPU[1:0] bits.

General-Purpose Output (GPO)

The MFIOx pins are configured as general-purpose outputs when MFIOx_FUNC[3:0] = 0xE. In GPO mode, the MFIOx_SEL[2:0] determines the output data either logic high, logic low, or high impedance (see Table 15). When the MFIOx is configured as an open-drain GPO, an external pull-up resistor (typ 10kΩ to 100kΩ) is required.

ADC Mux Input (ADCMUX)

When the MFIO8 is configured as an ADC mux input, the MAX77542 can covert the voltage applied to this input. The effective input-voltage range is from 0V to 1.195V and the readback data will be available at the ADC_DATA11[7:0] register bits. See the *External Voltage Measurement* section for more information. Note that the maximum voltage at the ADC mux must not exceed the V_{DD} (1.9V typ).

Debounce Timer

When the MFIOx are configured as logic inputs, a debounce timer is set by the MFIOx_DEB[2:0] bits to avoid logic signal chattering due to input-signal glitches or bouncing. The timer-setting options are shown in Table 16.

When the system clock is disabled (all the buck outputs are in an off state and the ADC is disabled), there is an additional debounce time (< 5µs) in addition to the selected debounce timer value (except for the no-debounce option). The additional debounce time is avoided when the CLK_EN bit is set to 1 through the I^2C interface, allowing the system clock to be enabled even in standby state at a cost of 35µA (typ) additional quiescent current.

Table 16. Debounce Timer Setting

MFIOx_DEB[2:0]	TIMER SETTING
0x0	No Debounce
0x1	0.55µs
0x2	1µs
0x3	2µs
0x4	4µs
0x5	8µs
0x6	16µs
0x7	32µs

Internal Pull-Down and Pull-Up Resistor

When the MFIOx are configured as logic inputs, an internal pull-down or pull-up resistance is selected by the MFIOx_PDPU[1:0] bits as shown in Table 17. For the system reset input function (MFIOx_FUNC[3:0] = 0xA), the corresponding MFIOx pin is pulled up to the V_{IO} pin with an internal 100kΩ resistor regardless of the MFIOx_PDPU[1:0] bits.

Table 17. Internal Resistor Setting

MFIOx_PDPU[1:0]	RESISTOR SETTING
0x0	800kΩ Pull-Down to AGND
0x1	100kΩ Pull-Down to AGND
0x2	100kΩ Pull-Up to V_{IO}
0x3	Disable (No Pull-Down or Pull-Up)

Output Driver Mode

When the MFIOx are configured as POK, FPSO, or GPO function, either an open-drain or a push-pull output mode can be selected by MFIOx_DRV_MODE bits. In push-pull mode, the maximum driving current is limited to 2mA.

Detailed Description—ADC

The MAX77542 has an 8-bit successive approximation register (SAR) ADC with eleven multiplexers for supporting the telemetry feature (see Figure 13). The eleven multiplexers are assigned for the output current and the output voltage of each buck converter, the V_{SYS} voltage, the junction temperature, and an external input through a MFIO. Each ADC channel is individually controlled through the I^2C interface and has a set of interrupt and interrupt mask bits. When unmasked, the interrupt bit sets whenever the ADC data is ready to be read.

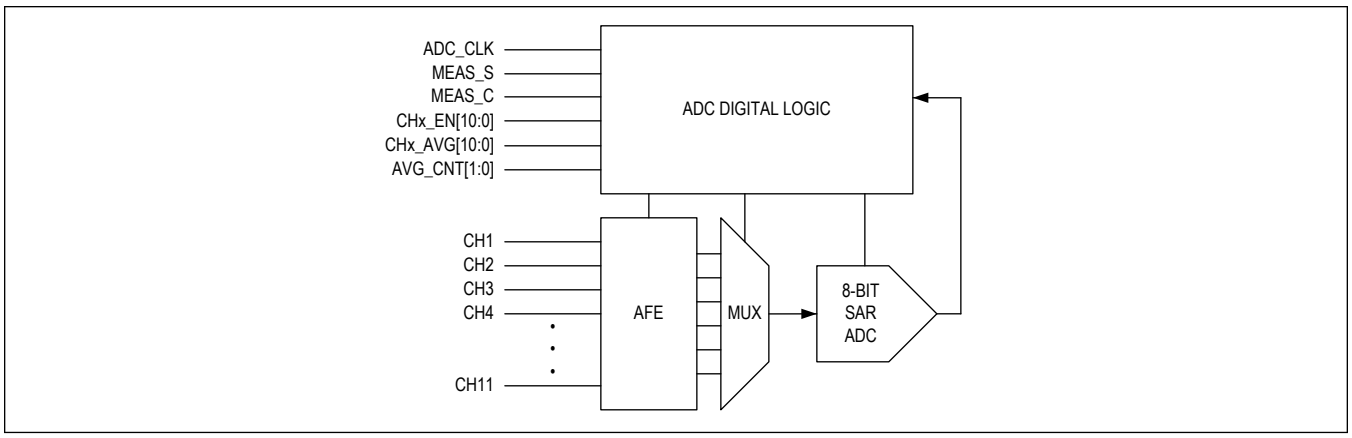


Figure 13. ADC Block Diagram

The measurement range and its LSB size for each ADC channel is listed in Table 18.

Table 18. ADC Functions and Measurement Ranges

CHANNEL NUMBER	DESCRIPTION	MEASUREMENT RANGE	LSB SIZE
1	PH1 Output Current (I_{OUT1})	-6.69A to 9.2475A	62.5mA
2	PH2 Output Current (I_{OUT2})	-6.69A to 9.2475A	62.5mA
3	PH3 Output Current (I_{OUT3})	-6.69A to 9.2475A	62.5mA
4	PH4 Output Current (I_{OUT4})	-6.69A to 9.2475A	62.5mA
5	PH1 Output Voltage (V_{OUT1})	0V to 1.59375V (M1_RNG = 0x0)	6.25mV
		0V to 3.1875V (M1_RNG = 0x1)	12.5mV
		0V to 6.375V (M1_RNG = 0x2)	25mV
6	PH2 Output Voltage (V_{OUT2})	0V to 1.59375V (M2_RNG = 0x0)	6.25mV
		0V to 3.1875V (M2_RNG = 0x1)	12.5mV
		0V to 6.375V (M2_RNG = 0x2)	25mV
7	PH3 Output Voltage (V_{OUT3})	0V to 1.59375V (M3_RNG = 0x0)	6.25mV
		0V to 3.1875V (M3_RNG = 0x1)	12.5mV
		0V to 6.375V (M3_RNG = 0x2)	25mV
8	PH4 Output Voltage (V_{OUT4})	0V to 1.59375V (M4_RNG = 0x0)	6.25mV
		0V to 3.1875V (M4_RNG = 0x1)	12.5mV
		0V to 6.375V (M4_RNG = 0x2)	25mV
9	SYS Input Voltage (V_{SYS})	0V to 6.375V	25mV
		0V to 19.125V	75mV
10	Junction Temperature (T_J)	-273°C to +167°C	1.725°C
11	External Input (V_{MFIOx})	0V to 1.195V	4.6875mV

ADC Enable and Measurement Options

Each individual ADC channel is enabled by setting the CHx_EN bit. The ADC starts sampling the data about 20µs after the MEAS_S bit is set (single measurement). Once the sampling is completed, it takes about 10µs of conversion time to upload the readback data into its corresponding data register (ADC_DATAx). In case more than one channel is enabled, the ADC engine measures all enabled channels one by one and uploads the readback data to the ADC_DATAx registers in turn. The AVG_CNT[1:0] bits set the number of readings (2, 4, 8, or 16 points) before the ADC uploads the averaged data into the ADC_DATAx registers.

The ADC also provides continuous reading options by setting the MEAS_C bit. When MEAS_C = 1, the ADC engine reads all enabled channels and uploads the data onto the ADC_DATAx registers every second. While continuous measurement is enabled (MEAS_C = 1), the MEAS_S bit is ignored.

When unmasked, an interrupt (ADC_CHx_I) is triggered whenever the new data is uploaded into the corresponding data register. This is to indicate to the host processor that the data is ready to be read.

Output-Current Measurement

The MAX77542 is capable of measuring the DC output current in each switching phase. The sampling time for the current measurement is about 1ms per channel. The data codes in the ADC_DATA1 –ADC_DATA4 registers represent the measured output current values of Phase1–Phase4, respectively. In multiphase configurations, a readback data of an ADC channel still represents a measured DC output current of the corresponding phase, so that the output current data of each phase in the same multiphase group needs to be summed for the total output current. See the *Register Map* section for the conversion formula between the readback code and the measured output current.

The on-time of the low-side MOSFET given by the operating condition of the buck converter is less than 230ns (typ), the MAX77542 is not able to measure the output current reliably and clears the corresponding status bits (CH1_IMON_OK–CH4_IMON_OK) to 0 so that a host processor can skip reading the readback data.

Output-Voltage Measurement

The MAX77542 is also capable of measuring the DC output voltage of each switching phase. It takes about 10µs to sample the output voltage. The data codes in the ADC_DATA5 –ADC_DATA8 registers represent the measured output voltages of Phase1 –Phase4, respectively. In multiphase configurations, it is redundant to measure the output voltages of slave phases in the same multiphase group if the output voltage of the master phase is already measured. See the *Register Map* section for the conversion formula between the readback code and the measured output voltage.

SYS-Voltage Measurement

The supply voltage at the SYS node (V_{SYS}) can be monitored using the ADC CH9. There are two measurement ranges (0V to 6.375V and 0V to 19.125V) selected by the SYS_RNG bit. It takes about 10µs to sample the input voltage. See the *Register Map* section for the conversion formula between the readback code and the measured SYS voltage.

Junction-Temperature Measurement

The ADC CH10 is dedicated to measuring the junction temperature of the device. This allows a host processor to optimize its power consumption for reliable operation. It takes about 1ms to sample the junction temperature. See the *Register Map* section for the conversion formula between the readback code and the measured junction temperature.

External-Voltage Measurement

The ADC CH11 is dedicated to measuring external voltages through the ADCMUX function of the MFIOs. This feature allows a host processor to use the ADC for general purpose (0V to 1.195V input range). It takes about 10µs to sample the external voltage. See the *Register Map* section for the conversion formula between the readback code and the measured input voltage. See the *ADC Mux Input (ADCMUX)* section for more information.

Detailed Description—I²C Serial Interface

The MAX77542 features a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a serial clock line (SCL) and a bidirectional serial data line (SDA). The MAX77542 is a slave-only device that relies on an external bus master to generate the SCL clock. The SCL clock rates from 0Hz to 3.4MHz are supported. As I²C is an open-drain bus, the SCL and the SDA require external pull-up resistors.

Slave Address

The I²C communication controller implements 7-bit slave addressing. An I²C bus master initiates communication with the slave by issuing a start condition followed by the slave address. The MAX77542 supports four slave addresses which is selected by R_{CFG1} (see the *Device Configuration (CFGx)* section). All slave addresses not mentioned in Table 2 are not acknowledged. The device uses 8-bit registers with 8-bit register addressing. They support standard communication

protocols:

- Writing to a single register
- Writing to multiple sequential registers with an automatically incrementing data pointer
- Reading from a single register
- Reading from multiple sequential registers with an automatically increased data pointer

For additional information about the I²C protocols, refer to the I²C specification.

HS Extension Mode

The MAX77542 supports a special I²C feature called HS extension mode. The HS extension feature keeps the high-speed operation even after a stop condition. This eliminates the need for a HS master code issued by an I²C master controller when the I²C master controller wants to stay in the HS mode for multiple read/write cycles.

As shown in Figure 14, the HS extension mode can be enabled by setting the HS_EXT_EN bit while the I²C bus operates in the LS (standard, fast, or fast-mode plus) mode only.

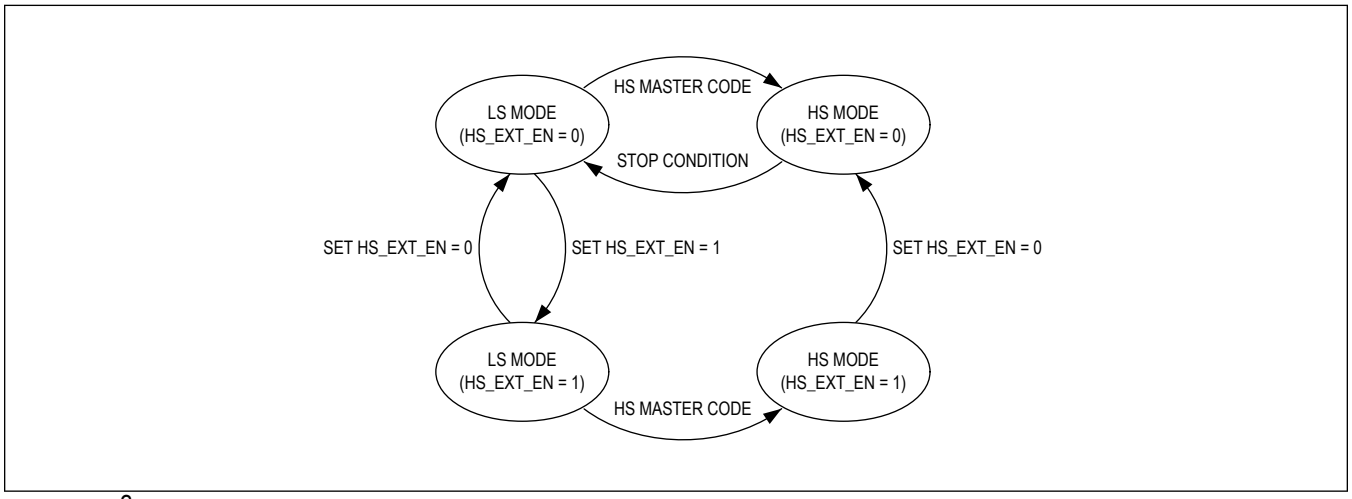


Figure 14. I²C Operating Mode State Diagram

I²C Watchdog Timer

The MAX77542 contains an I²C watchdog timer to ensure reliable operation of the I²C bus. The I²C watchdog timer helps the system recover from I²C bus hang-ups that can occur when devices on the I²C bus operate out of sync from each other due to noise or poor system design. In most cases, the bus master can clear the I²C bus hang-ups by issuing nine consecutive STOP commands. However, to account for unforeseen system issues, the I²C watchdog timer serves as a backup protection method for recovering from the I²C bus hang-ups.

The MAX77542 supports four timer options (31ms, 62ms, 124ms, and 248ms) controlled by the WD_TMR[1:0] bit. The I²C watchdog timer is enabled when WD_EN bit is set to 1. While the I²C watchdog timer is enabled, the MAX77542 monitors the time between a start and a stop condition and resets the I²C state machine if this time ever exceeds the selected timer option.

The I²C watchdog timer is disabled by default. With the I²C watchdog timer disabled, the device meets the 0Hz SCL frequency requirements in the I²C specification. Activating the I²C watchdog timer defeats the 0Hz specification and this 0Hz capability is not needed in many cases.

Register Map

MAX77542

ADDRESS	NAME	MSB							LSB
GLOBAL CONFIGURATION 1									
0x00	INT_SRC[7:0]	RESERVED[3:0]				ADC_I	MFIO_I	BUCK_I	TOPSYS_I
0x01	INT_SRC_MSK[7:0]	RESERVED[3:0]				ADC_M	MFIO_M	BUCK_M	TOPSYS_M
0x02	TOPSYS_INT[7:0]	RESERVED[2:0]			ALT_SWO_I	VIOFLT_I	UVLO_I	TSHDN_I	TWARN_I
0x03	TOPSYS_MSK[7:0]	RESERVED[2:0]			ALT_SWO_M	VIOFLT_M	UVLO_M	TSHDN_M	TWARN_M
0x04	TOPSYS_STAT[7:0]	RESERVED[2:0]			ALT_SWO	VIOFLT	UVLO	TSHDN	TWARN
0x06	DEVICE_CFG1[7:0]	PH_CFG[2:0]			CFG1_LATCH[4:0]				
0x07	DEVICE_CFG2[7:0]	RESERVED[2:0]			CFG2_LATCH[4:0]				
0x08	DEVICE_CFG3[7:0]	RESERVED[2:0]			SEL1_LATCH[4:0]				
0x09	DEVICE_CFG4[7:0]	RESERVED[2:0]			SEL2_LATCH[4:0]				
0x0A	DEVICE_CFG5[7:0]	RESERVED[2:0]			SEL3_LATCH[4:0]				
0x0B	DEVICE_CFG6[7:0]	RESERVED[2:0]			SEL4_LATCH[4:0]				
0x0C	TOPSYS_CFG[7:0]	RESERVED[1:0]		ALT_IN_EN	CE_PD_EN	MASK_MODE	FTMON_EN	CLK_EN	VL_EN
0x0D	PROT_CFG[7:0]	RESERVED	TWARN_TH[2:0]			RESERVED	UVLO_F	POK_TO[1:0]	
0x0E	RESET_CFG1[7:0]	RESERVED[4:0]					RSTINB_SHDN	VIOFLT_SHDN	AUTO_RSTRT
0x0F	RESET_CFG2[7:0]	RESERVED[1:0]		UVLO_RSTOB_EN	TSHDN_RSTOB_EN	M4_RSTOB_EN	M3_RSTOB_EN	M2_RSTOB_EN	M1_RSTOB_EN
GLOBAL CONFIGURATION 2									
0x10	EN_CTRL[7:0]	M4_LPM	M3_LPM	M2_LPM	M1_LPM	M4_EN	M3_EN	M2_EN	M1_EN
0x11	GLB_CFG1[7:0]	M1_SHDN_DLY[3:0]				M1_STUP_DLY[3:0]			
0x12	GLB_CFG2[7:0]	M2_SHDN_DLY[3:0]				M2_STUP_DLY[3:0]			
0x13	GLB_CFG3[7:0]	M3_SHDN_DLY[3:0]				M3_STUP_DLY[3:0]			
0x14	GLB_CFG4[7:0]	M4_SHDN_DLY[3:0]				M4_STUP_DLY[3:0]			
0x15	GLB_CFG5[7:0]	FPSO_SHDN_DLY[3:0]				FPSO_STUP_DLY[3:0]			
0x16	GLB_CFG6[7:0]	RESERVED[5:0]						DLY_STEP[1:0]	
0x17	GLB_CFG7[7:0]	RESERVED[6:0]							FPS_EN
I2C_CONFIGURATION									
0x1A	I2C_CFG1[7:0]	RESERVED[5:0]						WD_TMR[1:0]	
0x1B	I2C_CFG2[7:0]	RESERVED[5:0]						WD_EN	HS_EXT_EN
BUCK1 CONFIGURATION									
0x20	BUCK_INT[7:0]	M4_SCFLT_I	M3_SCFLT_I	M2_SCFLT_I	M1_SCFLT_I	M4_POKFLT_I	M3_POKFLT_I	M2_POKFLT_I	M1_POKFLT_I

ADDRESS	NAME	MSB							LSB
0x21	BUCK_MSK[7:0]	M4_SCFLT_M	M3_SCFLT_M	M2_SCFLT_M	M1_SCFLT_M	M4_POKFLT_M	M3_POKFLT_M	M2_POKFLT_M	M1_POKFLT_M
0x22	BUCK_STAT[7:0]	M4_SCFLT	M3_SCFLT	M2_SCFLT	M1_SCFLT	M4_POK	M3_POK	M2_POK	M1_POK
0x23	M1_VOUT_H[7:0]	M1_VOUT_H[7:0]							
0x24	M1_VOUT_L[7:0]	M1_VOUT_L[7:0]							
0x25	M1_VOUT_B[7:0]	M1_VOUT_B[7:0]							
0x26	M1_VOUT_M[7:0]	M1_VOUT_M[4:0]					RESERVED	M1_RNG[1:0]	
0x27	M1_CFG1[7:0]	RESERVED[1:0]		M1_RD_SR[2:0]			M1_RU_SR[2:0]		
0x28	M1_CFG2[7:0]	RESERVED[1:0]		M1_SSTOP_SR[2:0]			M1_SSTRT_SR[2:0]		
0x29	M1_CFG3[7:0]	M1_BBRK[1:0]		M1_ADIS100	M1_ADIS1	M1_FTRAK	M1_REFRESH	M1_FSREN	M1_FPWM
0x2A	M1_CFG4[7:0]	M1_SS_ENV[1:0]		M1_SS_FREQ[1:0]		M1_SSM_PAT[1:0]		M1_FREQ[1:0]	
0x2B	M1_CFG5[7:0]	RESERVED[2:0]			RESERVED	RESERVED[1:0]		M1_ILIM[1:0]	
BUCK2 CONFIGURATION									
0x33	M2_VOUT_H[7:0]	M2_VOUT_H[7:0]							
0x34	M2_VOUT_L[7:0]	M2_VOUT_L[7:0]							
0x35	M2_VOUT_B[7:0]	M2_VOUT_B[7:0]							
0x36	M2_VOUT_M[7:0]	M2_VOUT_M[4:0]					RESERVED	M2_RNG[1:0]	
0x37	M2_CFG1[7:0]	RESERVED[1:0]		M2_RD_SR[2:0]			M2_RU_SR[2:0]		
0x38	M2_CFG2[7:0]	RESERVED[1:0]		M2_SSTOP_SR[2:0]			M2_SSTRT_SR[2:0]		
0x39	M2_CFG3[7:0]	M2_BBRK[1:0]		M2_ADIS100	M2_ADIS1	M2_FTRAK	M2_REFRESH	M2_FSREN	M2_FPWM
0x3A	M2_CFG4[7:0]	M2_SS_ENV[1:0]		M2_SS_FREQ[1:0]		M2_SSM_PAT[1:0]		M2_FREQ[1:0]	
0x3B	M2_CFG5[7:0]	RESERVED[2:0]			RESERVED	RESERVED[1:0]		M2_ILIM[1:0]	
BUCK3 CONFIGURATION									
0x43	M3_VOUT_H[7:0]	M3_VOUT_H[7:0]							
0x44	M3_VOUT_L[7:0]	M3_VOUT_L[7:0]							
0x45	M3_VOUT_B[7:0]	M3_VOUT_B[7:0]							
0x46	M3_VOUT_M[7:0]	M3_VOUT_M[4:0]					RESERVED	M3_RNG[1:0]	
0x47	M3_CFG1[7:0]	RESERVED[1:0]		M3_RD_SR[2:0]			M3_RU_SR[2:0]		
0x48	M3_CFG2[7:0]	RESERVED[1:0]		M3_SSTOP_SR[2:0]			M3_SSTRT_SR[2:0]		
0x49	M3_CFG3[7:0]	M3_BBRK[1:0]		M3_ADIS100	M3_ADIS1	M3_FTRAK	M3_REFRESH	M3_FSREN	M3_FPWM
0x4A	M3_CFG4[7:0]	M3_SS_ENV[1:0]		M3_SS_FREQ[1:0]		M3_SSM_PAT[1:0]		M3_FREQ[1:0]	
0x4B	M3_CFG5[7:0]	RESERVED[2:0]			RESERVED	RESERVED[1:0]		M3_ILIM[1:0]	
BUCK4 CONFIGURATION									
0x53	M4_VOUT_H[7:0]	M4_VOUT_H[7:0]							
0x54	M4_VOUT_L[7:0]	M4_VOUT_L[7:0]							
0x55	M4_VOUT_B[7:0]	M4_VOUT_B[7:0]							

ADDRESS	NAME	MSB							LSB
0x56	M4_VOUT_M[7:0]	M4_VOUT_M[4:0]					RESERVED	M4_RNG[1:0]	
0x57	M4_CFG1[7:0]	RESERVED[1:0]		M4_RD_SR[2:0]			M4_RU_SR[2:0]		
0x58	M4_CFG2[7:0]	RESERVED[1:0]		M4_SSTOP_SR[2:0]			M4_SSTRT_SR[2:0]		
0x59	M4_CFG3[7:0]	M4_BBRK[1:0]		M4_ADIS100	M4_ADIS1	M4_FTRAK	M4_REFRESH	M4_FSREN	M4_FPWM
0x5A	M4_CFG4[7:0]	M4_SS_ENV[1:0]		M4_SS_FREQ[1:0]		M4_SSM_PAT[1:0]		M4_FREQ[1:0]	
0x5B	M4_CFG5[7:0]	RESERVED[2:0]			RESERVED	RESERVED[1:0]		M4_ILIM[1:0]	
MFIO_CONFIGURATION									
0x60	MFIO_INT[7:0]	MFIO8_I	MFIO7_I	MFIO6_I	MFIO5_I	MFIO4_I	MFIO3_I	MFIO2_I	MFIO1_I
0x61	MFIO_MSK[7:0]	MFIO8_M	MFIO7_M	MFIO6_M	MFIO5_M	MFIO4_M	MFIO3_M	MFIO2_M	MFIO1_M
0x62	MFIO_STAT[7:0]	MFIO8	MFIO7	MFIO6	MFIO5	MFIO4	MFIO3	MFIO2	MFIO1
0x63	MFIO1_CFG1[7:0]	RESERVED	MFIO1_SEL[2:0]			MFIO1_FUNC[3:0]			
0x64	MFIO1_CFG2[7:0]	RESERVED[1:0]		MFIO1_DRV_MODE	MFIO1_PDPU[1:0]		MFIO1_DEB[2:0]		
0x65	MFIO2_CFG1[7:0]	RESERVED	MFIO2_SEL[2:0]			MFIO2_FUNC[3:0]			
0x66	MFIO2_CFG2[7:0]	RESERVED[1:0]		MFIO2_DRV_MODE	MFIO2_PDPU[1:0]		MFIO2_DEB[2:0]		
0x67	MFIO3_CFG1[7:0]	RESERVED	MFIO3_SEL[2:0]			MFIO3_FUNC[3:0]			
0x68	MFIO3_CFG2[7:0]	RESERVED[1:0]		MFIO3_DRV_MODE	MFIO3_PDPU[1:0]		MFIO3_DEB[2:0]		
0x69	MFIO4_CFG1[7:0]	RESERVED	MFIO4_SEL[2:0]			MFIO4_FUNC[3:0]			
0x6A	MFIO4_CFG2[7:0]	RESERVED[1:0]		MFIO4_DRV_MODE	MFIO4_PDPU[1:0]		MFIO4_DEB[2:0]		
0x6B	MFIO5_CFG1[7:0]	RESERVED	MFIO5_SEL[2:0]			MFIO5_FUNC[3:0]			
0x6C	MFIO5_CFG2[7:0]	RESERVED[1:0]		MFIO5_DRV_MODE	MFIO5_PDPU[1:0]		MFIO5_DEB[2:0]		
0x6D	MFIO6_CFG1[7:0]	RESERVED	MFIO6_SEL[2:0]			MFIO6_FUNC[3:0]			
0x6E	MFIO6_CFG2[7:0]	RESERVED[1:0]		MFIO6_DRV_MODE	MFIO6_PDPU[1:0]		MFIO6_DEB[2:0]		
0x6F	MFIO7_CFG1[7:0]	RESERVED	MFIO7_SEL[2:0]			MFIO7_FUNC[3:0]			
0x70	MFIO7_CFG2[7:0]	RESERVED[1:0]		MFIO7_DRV_MODE	MFIO7_PDPU[1:0]		MFIO7_DEB[2:0]		

ADDRESS	NAME	MSB							LSB
0x71	MFIO8_CFG1[7:0]	RESERVED	MFIO8_SEL[2:0]			MFIO8_FUNC[3:0]			
0x72	MFIO8_CFG2[7:0]	RESERVED[1:0]		MFIO8_DRV_MODE	MFIO8_PDPU[1:0]		MFIO8_DEB[2:0]		
ADC CONFIGURATION									
0x80	ADC_INT1[7:0]	ADC_CH8_I	ADC_CH7_I	ADC_CH6_I	ADC_CH5_I	ADC_CH4_I	ADC_CH3_I	ADC_CH2_I	ADC_CH1_I
0x81	ADC_INT2[7:0]	RESERVED[2:0]			RESERVED	RESERVED	ADC_CH11_I	ADC_CH10_I	ADC_CH9_I
0x82	ADC_MSK1[7:0]	ADC_CH8_M	ADC_CH7_M	ADC_CH6_M	ADC_CH5_M	ADC_CH4_M	ADC_CH3_M	ADC_CH2_M	ADC_CH1_M
0x83	ADC_MSK2[7:0]	RESERVED[2:0]			RESERVED	RESERVED	ADC_CH11_M	ADC_CH10_M	ADC_CH9_M
0x84	ADC_STAT[7:0]	RESERVED[3:0]				CH4_IMON_OK	CH3_IMON_OK	CH2_IMON_OK	CH1_IMON_OK
0x85	ADC_DATA_CH1[7:0]	ADC_DATA1[7:0]							
0x86	ADC_DATA_CH2[7:0]	ADC_DATA2[7:0]							
0x87	ADC_DATA_CH3[7:0]	ADC_DATA3[7:0]							
0x88	ADC_DATA_CH4[7:0]	ADC_DATA4[7:0]							
0x89	ADC_DATA_CH5[7:0]	ADC_DATA5[7:0]							
0x8A	ADC_DATA_CH6[7:0]	ADC_DATA6[7:0]							
0x8B	ADC_DATA_CH7[7:0]	ADC_DATA7[7:0]							
0x8C	ADC_DATA_CH8[7:0]	ADC_DATA8[7:0]							
0x8D	ADC_DATA_CH9[7:0]	ADC_DATA9[7:0]							
0x8E	ADC_DATA_CH10[7:0]	ADC_DATA10[7:0]							
0x8F	ADC_DATA_CH11[7:0]	ADC_DATA11[7:0]							
0x92	ADC_CFG1[7:0]	CH8_EN	CH7_EN	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN
0x93	ADC_CFG2[7:0]	RESERVED[2:0]			RESERVED	RESERVED	CH11_EN	CH10_EN	CH9_EN
0x94	ADC_CFG3[7:0]	CH8_AVG	CH7_AVG	CH6_AVG	CH5_AVG	CH4_AVG	CH3_AVG	CH2_AVG	CH1_AVG
0x95	ADC_CFG4[7:0]	RESERVED[2:0]			RESERVED	RESERVED	CH11_AVG	CH10_AVG	CH9_AVG
0x96	ADC_CFG5[7:0]	RESERVED[1:0]		SYS_RNG	RESERVED	AVG_CNT[1:0]		MEAS_C	MEAS_S

Register Details

INT_SRC (0x00)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[3:0]				ADC_I	MFIO_I	BUCK_I	TOPSYS_I
Reset	0x0				0x0	0x0	0x0	0x0
Access Type	Read Clears All				Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:4	O	Reserved. Returns 0.	
ADC_I	3	O	ADC Interrupt Source	0x0 = Interrupt event in ADC has not been detected. 0x1 = Interrupt event in ADC has been detected.
MFIO_I	2	O	MFIO Interrupt Source	0x0 = Interrupt event in MFIO has not been detected. 0x1 = Interrupt event in MFIO has been detected.
BUCK_I	1	O	Buck Interrupt Source	0x0 = Interrupt event in Buck has not been detected. 0x1 = Interrupt event in Buck has been detected.
TOPSYS_I	0	O	Top-Level Interrupt Source	0x0 = Interrupt event in TOPSYS has not been detected. 0x1 = Interrupt event in TOPSYS has been detected.

INT_SRC_MSK (0x01)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[3:0]				ADC_M	MFIO_M	BUCK_M	TOPSYS_M
Reset	0xF				0x1	0x1	0x1	0x0
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:4	O	Reserved. Returns 1.	
ADC_M	3	O	ADC Interrupt Source Mask	0x0 = Enable ADC_I. 0x1 = Mask ADC_I.
MFIO_M	2	O	MFIO Interrupt Source Mask	0x0 = Enable MFIO_I. 0x1 = Mask MFIO_I.
BUCK_M	1	O	Buck Interrupt Source Mask	0x0 = Enable BUCK_I. 0x1 = Mask BUCK_I.
TOPSYS_M	0	O	Top-Level Interrupt Source Mask	0x0 = Enable TOPSYS_I. 0x1 = Mask TOPSYS_I.

TOPSYS_INT (0x02)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			ALT_SWO_I	VIOFLT_I	UVLO_I	TSHDN_I	TWARN_I
Reset	0x0			0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All			Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	O	Reserved. Returns 0.	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ALT_SWO_I	4	O	Alternate Input Switchover Interrupt	0x0 = Input voltage of internal bias circuitry has not switched to ALT_IN input. 0x1 = Input voltage of internal bias circuitry has switched to ALT_IN input.
VIOFLT_I	3	O	V_{IO} Fault Interrupt	0x0 = I/O supply (V_{IO}) has not dropped below its UVLO threshold. 0x1 = I/O supply (V_{IO}) has dropped below its UVLO threshold.
UVLO_I	2	O	SYS Undervoltage Lock-Out Interrupt	0x0 = Input voltage (V_{SYS}) has not dropped below UVLO threshold. 0x1 = Input voltage (V_{SYS}) has dropped below UVLO threshold.
TSHDN_I	1	O	Thermal-Shutdown Interrupt	0x0 = Junction temperature has not risen above thermal-shutdown threshold (+165°C). 0x1 = Junction temperature has risen above thermal-shutdown threshold (+165°C).
TWARN_I	0	O	Thermal-Warning Interrupt	0x0 = Junction temperature has not risen above TWARN_TH[2:0]. 0x1 = Junction temperature has risen above TWARN_TH[2:0].

TOPSYS_MSK (0x03)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			ALT_SWO_M	VIOFLT_M	UVLO_M	TSHDN_M	TWARN_M
Reset	0x7			0x1	0x1	0x0	0x1	0x1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	O	Reserved. Returns 1.	
ALT_SWO_M	4	O	Alternate Input Switchover Interrupt Mask	0x0 = Enable ALT_SWO_I. 0x1 = Mask ALT_SWO_I.
VIOFLT_M	3	O	V_{IO} Fault Interrupt Mask	0x0 = Enable VIOFLT_I. 0x1 = Mask VIOFLT_I.
UVLO_M	2	O	SYS Undervoltage Lock-Out Interrupt Mask	0x0 = Enable UVLO_I. 0x1 = Mask UVLO_I.
TSHDN_M	1	O	Thermal-Shutdown Interrupt Mask	0x0 = Enable TSHDN_I. 0x1 = Mask TSHDN_I.
TWARN_M	0	O	Thermal-Warning Interrupt Mask	0x0 = Enable TWARN_I. 0x1 = Mask TWARN_I.

TOPSYS_STAT (0x04)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			ALT_SWO	VIOFLT	UVLO	TSHDN	TWARN
Reset	0x0			0x0	0x0	0x0	0x0	0x0
Access Type	Read Only			Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	O	Reserved. Returns 0.	
ALT_SWO	4	O	Alternate Input Switchover Status	0x0 = V_{DD}, V_{L12}, and V_{L34} LDOs are powered from SYS. 0x1 = V_{DD}, V_{L12}, and V_{L34} LDOs are powered from ALT_IN.
VIOFLT	3	O	V_{IO} Fault Status	0x0 = $V_{IO} \geq V_{IO\_UVLO\_R}$. 0x1 = $V_{IO} \leq V_{IO\_UVLO\_F}$.
UVLO	2	O	SYS Undervoltage Lock-Out Status	0x0 = $V_{SYS} \geq V_{UVLO\_R}$. 0x1 = $V_{SYS} \leq V_{UVLO\_F}$.
TSHDN	1	O	Thermal-Shutdown Status	0x0 = $T_J \leq +150°C$. 0x1 = $T_J \geq +165°C$.
TWARN	0	O	Thermal-Warning Status	0x0 = $T_J \leq$ TWARN_TH[2:0]. 0x1 = $T_J \geq$ TWARN_TH[2:0].

DEVICE_CFG1 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	PH_CFG[2:0]			CFG1_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
PH_CFG	7:5	O	Phase Configuration	0x0 = 1PH + 1PH + 1PH + 1PH (4 outputs). 0x1 = 2PH + 1PH + 1PH (3 outputs). 0x2 = 2PH + 2PH (2 outputs). 0x3 = 3PH + 1PH (2 outputs). 0x4 = 4PH (1 output). 0x5–0x7 = Reserved.
CFG1_LATCH	4:0	O	CFG1 Latched Code	

DEVICE_CFG2 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			CFG2_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	TYPE	DESCRIPTION
RESERVED	7:5	O	Reserved. Returns 0.

BITFIELD	BITS	TYPE	DESCRIPTION
CFG2_LATCH	4:0	O	CFG2 Latched Code

DEVICE_CFG3 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			SEL1_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	TYPE	DESCRIPTION
RESERVED	7:5	O	Reserved. Returns 0.
SEL1_LATCH	4:0	O	SEL1 Latched Code

DEVICE_CFG4 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			SEL2_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	TYPE	DESCRIPTION
RESERVED	7:5	O	Reserved. Returns 0.
SEL2_LATCH	4:0	O	SEL2 Latched Code

DEVICE_CFG5 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			SEL3_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	TYPE	DESCRIPTION
RESERVED	7:5	O	Reserved. Returns 0.
SEL3_LATCH	4:0	O	SEL3 Latched Code

DEVICE_CFG6 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			SEL4_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	TYPE	DESCRIPTION
RESERVED	7:5	O	Reserved. Returns 0.
SEL4_LATCH	4:0	O	SEL4 Latched Code

TOPSYS_CFG (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		ALT_IN_EN	CE_PD_EN	MASK_MODE	FTMON_EN	CLK_EN	VL_EN
Reset	0x0		0x1	0x1	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
ALT_IN_EN	5	O	Alternative Input Control	0x0 = V_{DD}, V_{L12} and V_{L34} LDOs are powered from SYS. 0x1 = V_{DD}, V_{L12} and V_{L34} LDOs are powered from ALT_IN.
CE_PD_EN	4	O	CE Pull-Down Control	0x0 = Disable an internal pull-down. 0x1 = Enable an internal pull-down.
MASK_MODE	3	O	Interrupt Mask Mode Setting	0x0 = Interrupt signal is gated after the corresponding interrupt bit when masked. 0x1 = Interrupt signal is gated before the corresponding interrupt bit when masked.
FTMON_EN	2	O	Forced Junction Temperature Monitor	0x0 = Monitor junction temperature only when one or more outputs is/are enabled. 0x1 = Monitor junction temperature even when all the outputs are disabled.
CLK_EN	1	O	System Clock Pre-Enable Control	0x0 = Disable. 0x1 = Enable (enable internal OSC even when all buck outputs are disabled).
VL_EN	0	O	V_{L12} and V_{L34} LDOs Pre-Enable Control	0x0 = Disable. 0x1 = Enable (Allow shorter buck turn-on delay).

PROT_CFG (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	TWARN_TH[2:0]			RESERVED	UVLO_F	POK_TO[1:0]	
Reset	0x0	0x5			0x0	0x1	0x0	
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7	O	Reserved. Returns 0.	
TWARN_TH	6:4	O	Thermal-Warning Threshold	0x0 = +95°C. 0x1 = +100°C. 0x2 = +105°C. 0x3 = +110°C. 0x4 = +115°C. 0x5 = +120°C. 0x6 = +125°C. 0x7 = +130°C.
RESERVED	3	O	Reserved. Returns 0.	
UVLO_F	2	O	V_{SYS} UVLO Falling Threshold (Relative to UVLO Rising Threshold)	0x0 = UVLO_R - 150mV. 0x1 = UVLO_R - 200mV.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
POK_TO	1:0	O	Power-OK Fault Time-Out Setting	0x0 = Disable. 0x1 = 1ms. 0x2 = 5ms. 0x3 = 10ms.

RESET_CFG1 (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[4:0]					RSTINB_SHDN	VIOFLT_SHDN	AUTO_RSTRT
Reset	0x0					0x0	0x1	0x0
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:3	O	Reserved. Returns 0.	
RSTINB_SHDN	2	O	Shutdown and Register Reset Control for RSTINB (MFIO) Input	0x0 = Disable. 0x1 = Enable.
VIOFLT_SHDN	1	O	V_{IO} Fault Shutdown Control	0x0 = Disable. 0x1 = Enable (initiates a shutdown of all buck outputs when V_{IO} fault occurs).
AUTO_RSTRT	0	O	Auto Restart from POK Fault Time-Out, SCP, and TSHDN	0x0 = Disable (Mx_EN and/or MFIOx signals need to be toggled to exit latch-off state). 0x1 = Enable (allow auto-restart after 500ms of forced off time).

RESET_CFG2 (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		UVLO_RSTOB_EN	TSHDN_RSTOB_EN	M4_RSTOB_EN	M3_RSTOB_EN	M2_RSTOB_EN	M1_RSTOB_EN
Reset	0x0		0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
UVLO_RSTOB_EN	5	O	RSTOB (MFIO) Output Control for UVLO Fault	0x0 = Disable. 0x1 = Enable (assert RSTOB signal when UVLO fault occurs).
TSHDN_RSTOB_EN	4	O	RSTOB (MFIO) Output Control for Thermal-Shutdown Fault	0x0 = Disable. 0x1 = Enable (assert RSTOB signal when TSHDN fault occurs).
M4_RSTOB_EN	3	O	RSTOB (MFIO) Control for Buck Master4 Fault	0x0 = Disable. 0x1 = Enable (assert RSTOB signal when Buck Master4 SCP fault occurs).
M3_RSTOB_EN	2	O	RSTOB (MFIO) Control for Buck Master3 Fault	0x0 = Disable. 0x1 = Enable (assert RSTOB signal when Buck Master3 SCP fault occurs).

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M2_RSTOB_EN	1	O	RSTOB (MFIO) Control for Buck Master2 Fault	0x0 = Disable. 0x1 = Enable (assert RSTOB signal when Buck Master2 SCP fault occurs).
M1_RSTOB_EN	0	O	RSTOB (MFIO) Control for Buck Master1 Fault	0x0 = Disable. 0x1 = Enable (assert RSTOB signal when Buck Master1 SCP fault occurs).

EN_CTRL (0x10)

BIT	7	6	5	4	3	2	1	0
Field	M4_LPM	M3_LPM	M2_LPM	M1_LPM	M4_EN	M3_EN	M2_EN	M1_EN
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_LPM	7	O	Buck Master4 Low-Power Mode Control	0x0 = Disable. 0x1 = Enable (OR logic with LPM_M4 input).
M3_LPM	6	O	Buck Master3 Low-Power Mode Control	0x0 = Disable. 0x1 = Enable (OR logic with LPM_M3 input).
M2_LPM	5	O	Buck Master2 Low-Power Mode Control	0x0 = Disable. 0x1 = Enable (OR logic with LPM_M2 input).
M1_LPM	4	O	Buck Master1 Low-Power Mode Control	0x0 = Disable. 0x1 = Enable (OR logic with LPM_M1 input).
M4_EN	3	O	Buck Master4 Enable Control	0x0 = Disable. 0x1 = Enable (OR logic with EN_M4 input).
M3_EN	2	O	Buck Master3 Enable Control	0x0 = Disable. 0x1 = Enable (OR logic with EN_M3 input).
M2_EN	1	O	Buck Master2 Enable Control	0x0 = Disable. 0x1 = Enable (OR logic with EN_M2 input).
M1_EN	0	O	Buck Master1 Enable Control	0x0 = Disable. 0x1 = Enable (OR logic with EN_M1 input).

GLB_CFG1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	M1_SHDN_DLY[3:0]				M1_STUP_DLY[3:0]			
Reset	0x8				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M1_SHDN_DLY	7:4	O	Buck Master1 Shutdown Delay Control	0x0–0xE = (DLY_STEP x M1_SHDN_DLY)ms. 0xF = Reserved.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M1_STUP_DLY	3:0	O	Buck Master1 Startup Delay Control	0x0–0xE = (DLY_STEP x M1_STUP_DLY)ms. 0xF = No startup (excluded from FPS).

GLB_CFG2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	M2_SHDN_DLY[3:0]				M2_STUP_DLY[3:0]			
Reset	0x6				0x2			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M2_SHDN_DLY	7:4	O	Buck Master2 Shutdown Delay Control	0x0–0xE = (DLY_STEP x M2_SHDN_DLY)ms. 0xF = Reserved.
M2_STUP_DLY	3:0	O	Buck Master2 Startup Delay Control	0x0–0xE = (DLY_STEP x M2_STUP_DLY)ms. 0xF = No startup (excluded from FPS).

GLB_CFG3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	M3_SHDN_DLY[3:0]				M3_STUP_DLY[3:0]			
Reset	0x4				0x4			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M3_SHDN_DLY	7:4	O	Buck Master3 Shutdown Delay Control	0x0–0xE = (DLY_STEP x M3_SHDN_DLY)ms. 0xF = Reserved.
M3_STUP_DLY	3:0	O	Buck Master3 Startup Delay Control	0x0–0xE = (DLY_STEP x M3_STUP_DLY)ms. 0xF = No startup (excluded from FPS).

GLB_CFG4 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	M4_SHDN_DLY[3:0]				M4_STUP_DLY[3:0]			
Reset	0x2				0x6			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_SHDN_DLY	7:4	O	Buck Master4 Shutdown Delay Control	0x0–0xE = (DLY_STEP x M4_SHDN_DLY)ms. 0xF = Reserved.
M4_STUP_DLY	3:0	O	Buck Master4 Startup Delay Control	0x0–0xE = (DLY_STEP x M4_STUP_DLY)ms. 0xF = No startup (excluded from FPS).

GLB_CFG5 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	FPSO_SHDN_DLY[3:0]				FPSO_STUP_DLY[3:0]			
Reset	0x0				0x8			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
FPSO_SHDN_DLY	7:4	O	FPSO Shutdown Delay Control	0x0–0xE = (DLY_STEP x FPSO_SHDN_DLY)ms. 0xF = Reserved.
FPSO_STUP_DLY	3:0	O	FPSO Startup Delay Control	0x0–0xE = (DLY_STEP x FPSO_STUP_DLY)ms. 0xF = No startup (excluded from FPS).

GLB_CFG6 (0x16)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[5:0]						DLY_STEP[1:0]	
Reset	0x0						0x1	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:2	O	Reserved. Returns 0.	
DLY_STEP	1:0	O	Delay Step Size	0x0 = 0.5ms. 0x1 = 1ms. 0x2 = 2ms. 0x3 = 4ms.

GLB_CFG7 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[6:0]							FPS_EN
Reset	0x0							0x0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:1	O	Reserved. Returns 0.	
FPS_EN	0	O	Flexible Power Sequencer Enable for Startup and Shutdown	0-to-1 Transition: Initialize startup sequence (OR logic with FPSI input). 1-to-0 Transition: Initialize shutdown sequence (OR logic with FPSI input).

I2C_CFG1 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[5:0]						WD_TMR[1:0]	
Reset	0x0						0x0	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:2	O	Reserved. Returns 0.	
WD_TMR	1:0	O	I^2C Watchdog Timer Setting	0x0 = 31ms. 0x1 = 62ms. 0x2 = 124ms. 0x3 = 248ms.

I2C_CFG2 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[5:0]						WD_EN	HS_EXT_EN
Reset	0x0						0x0	0x0
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:2	O	Reserved. Returns 0.	
WD_EN	1	O	I^2C Watchdog Control	0x0 = Disable. 0x1 = Enable.
HS_EXT_EN	0	O	High-speed Mode Extension Control	0x0 = Disable HS-mode extension. 0x1 = Enable HS-mode extension (HS-mode is extended during/after stop condition).

BUCK_INT (0x20)

BIT	7	6	5	4	3	2	1	0
Field	M4_SCFLT_I	M3_SCFLT_I	M2_SCFLT_I	M1_SCFLT_I	M4_POKFLT_I	M3_POKFLT_I	M2_POKFLT_I	M1_POKFLT_I
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_SCFLT_I	7	O	Buck Master4 Short-Circuit Fault Interrupt	0x0 = Buck Master4 short-circuit fault has not been detected. 0x1 = Buck Master4 short-circuit fault has been detected.
M3_SCFLT_I	6	O	Buck Master3 Short-Circuit Fault Interrupt	0x0 = Buck Master3 short-circuit fault has not been detected. 0x1 = Buck Master3 short-circuit fault has been detected.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M2_SCFLT_I	5	O	Buck Master2 Short-Circuit Fault Interrupt	0x0 = Buck Master2 short-circuit fault has not been detected. 0x1 = Buck Master2 short-circuit fault has been detected.
M1_SCFLT_I	4	O	Buck Master1 Short-Circuit Fault Interrupt	0x0 = Buck Master1 short-circuit fault has not been detected. 0x1 = Buck Master1 short-circuit fault has been detected.
M4_POKFLT_I	3	O	Buck Master4 Power-OK Fault Interrupt	0x0 = Buck Master4 power-OK fault has not been detected. 0x1 = Buck Master4 power-OK fault has been detected.
M3_POKFLT_I	2	O	Buck Master3 Power-OK Fault Interrupt	0x0 = Buck Master3 power-OK fault has not been detected. 0x1 = Buck Master3 power-OK fault has been detected.
M2_POKFLT_I	1	O	Buck Master2 Power-OK Fault Interrupt	0x0 = Buck Master2 power-OK fault has not been detected. 0x1 = Buck Master2 power-OK fault has been detected.
M1_POKFLT_I	0	O	Buck Master1 Power-OK Fault Interrupt	0x0 = Buck Master1 power-OK fault has not been detected. 0x1 = Buck Master1 power-OK fault has been detected.

BUCK_MSK (0x21)

BIT	7	6	5	4	3	2	1	0
Field	M4_SCFLT_M	M3_SCFLT_M	M2_SCFLT_M	M1_SCFLT_M	M4_POKFLT_M	M3_POKFLT_M	M2_POKFLT_M	M1_POKFLT_M
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_SCFLT_M	7	O	Buck Master4 Short-Circuit Fault Interrupt Mask	0x0 = Enable M4_SCFLT_I. 0x1 = Mask M4_SCFLT_I.
M3_SCFLT_M	6	O	Buck Master3 Short-Circuit Fault Interrupt Mask	0x0 = Enable M3_SCFLT_I. 0x1 = Mask M3_SCFLT_I.
M2_SCFLT_M	5	O	Buck Master2 Short-Circuit Fault Interrupt Mask	0x0 = Enable M2_SCFLT_I. 0x1 = Mask M2_SCFLT_I.
M1_SCFLT_M	4	O	Buck Master1 Short-Circuit Fault Interrupt Mask	0x0 = Enable M1_SCFLT_I. 0x1 = Mask M1_SCFLT_I.
M4_POKFLT_M	3	O	Buck Master4 Power-OK Fault Interrupt Mask	0x0 = Enable M4_POKFLT_I. 0x1 = Mask M4_POKFLT_I.
M3_POKFLT_M	2	O	Buck Master3 Power-OK Fault Interrupt Mask	0x0 = Enable M3_POKFLT_I. 0x1 = Mask M3_POKFLT_I.
M2_POKFLT_M	1	O	Buck Master2 Power-OK Fault Interrupt Mask	0x0 = Enable M2_POKFLT_I. 0x1 = Mask M2_POKFLT_I.
M1_POKFLT_M	0	O	Buck Master1 Power-OK Fault Interrupt Mask	0x0 = Enable M1_POKFLT_I. 0x1 = Mask M1_POKFLT_I.

BUCK_STAT (0x22)

BIT	7	6	5	4	3	2	1	0
Field	M4_SCFLT	M3_SCFLT	M2_SCFLT	M1_SCFLT	M4_POK	M3_POK	M2_POK	M1_POK
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_SCFLT	7	O	Buck Master4 Short-Circuit Fault Status	0x0 = Buck Master4 output voltage is higher than its SCP threshold, or Buck Master1 is disabled. 0x1 = Buck Master4 output voltage is lower than its SCP threshold.
M3_SCFLT	6	O	Buck Master3 Short-Circuit Fault Status	0x0 = Buck Master3 output voltage is higher than its SCP threshold, or Buck Master1 is disabled. 0x1 = Buck Master3 output voltage is lower than its SCP threshold.
M2_SCFLT	5	O	Buck Master2 Short-Circuit Fault Status	0x0 = Buck Master2 output voltage is higher than its SCP threshold, or Buck Master1 is disabled. 0x1 = Buck Master2 output voltage is lower than its SCP threshold.
M1_SCFLT	4	O	Buck Master1 Short-Circuit Fault Status	0x0 = Buck Master1 output voltage is higher than its SCP threshold, or Buck Master1 is disabled. 0x1 = Buck Master1 output voltage is lower than its SCP threshold.
M4_POK	3	O	Buck Master4 Power-OK Status	0x0 = Buck Master4 output voltage is lower than its POK threshold, or Buck Master1 is disabled. 0x1 = Buck Master4 output voltage is higher than its POK threshold.
M3_POK	2	O	Buck Master3 Power-OK Status	0x0 = Buck Master3 output voltage is lower than its POK threshold, or Buck Master1 is disabled. 0x1 = Buck Master3 output voltage is higher than its POK threshold.
M2_POK	1	O	Buck Master2 Power_OK Status	0x0 = Buck Master2 output voltage is lower than its POK threshold, or Buck Master1 is disabled. 0x1 = Buck Master2 output voltage is higher than its POK threshold.
M1_POK	0	O	Buck Master1 Power-OK Status	0x0 = Buck Master1 output voltage is lower than its POK threshold, or Buck Master1 is disabled. 0x1 = Buck Master1 output voltage is higher than its POK threshold.

M1_VOUT_H (0x23)

BIT	7	6	5	4	3	2	1	0
Field	M1_VOUT_H[7:0]							
Reset	0x8C							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M1_VOUT_H	7:0	F	Buck Master1 Normal Output-Voltage Control Register (V_{OUT} Selected When VSEL_M1 = High and VB_M1 = High, or VSEL and VB Functions are not Used)	When M1_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M1_VOUT_H)V, 0xC8–0xFF = 1.3V. When M1_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M1_VOUT_H)V, 0xC8–0xFF = 2.6V. When M1_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M1_VOUT_H)V, 0xC8–0xFF = 5.2V.

M1_VOUT_L (0x24)

BIT	7	6	5	4	3	2	1	0
Field	M1_VOUT_L[7:0]							
Reset	0x8C							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M1_VOUT_L	7:0	F	Buck Master1 Normal Output-Voltage Control Register (V_{OUT} Selected When VSEL_M1 = Low and VB_M1 = High)	When M1_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M1_VOUT_L)V, 0xC8–0xFF = 1.3V. When M1_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M1_VOUT_L)V, 0xC8–0xFF = 2.6V. When M1_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M1_VOUT_L)V, 0xC8–0xFF = 5.2V.

M1_VOUT_B (0x25)

BIT	7	6	5	4	3	2	1	0
Field	M1_VOUT_B[7:0]							
Reset	0x8C							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M1_VOUT_B	7:0	F	Buck Master1 Boot (Default) Output-Voltage Control Register (V_{OUT} Selected When VB_M1 = Low)	When M1_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M1_VOUT_B)V, 0xC8–0xFF = 1.3V. When M1_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M1_VOUT_B)V, 0xC8–0xFF = 2.6V. When M1_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M1_VOUT_B)V, 0xC8–0xFF = 5.2V.

M1_VOUT_M (0x26)

BIT	7	6	5	4	3	2	1	0
Field	M1_VOUT_M[4:0]					RESERVED	M1_RNG[1:0]	
Reset	0x19					0x0	0x0	
Access Type	Write, Read					Write, Read	Read Only	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M1_VOUT_M	7:3	F	Buck Master1 Maximum Output-Voltage Control Register	When M1_RNG = 0x0, 0x0–0x18 = (0.3 + 0.04 x M1_VOUT_M)V, 0x19–0x1F = 1.3V. When M1_RNG = 0x1, 0x0–0x18 = (0.6 + 0.08 x M1_VOUT_M)V, 0x19–0x1F = 2.6V. When M1_RNG = 0x2, 0x0–0x18 = (1.2 + 0.16 x M1_VOUT_M)V, 0x19–0x1F = 5.2V.
RESERVED	2	F	Reserved. Returns 0.	
M1_RNG	1:0	F	Buck Master1 Output-Voltage Range Setting	0x0 = Low range (0.3V to 1.3V, 5mV step). 0x1 = Mid range (0.6V to 2.6V, 10mV step). 0x2 = High range (1.2V to 5.2V, 20mV step). 0x3 = Reserved.

M1_CFG1 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M1_RD_SR[2:0]			M1_RU_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M1_RD_SR	5:3	O	Buck Master1 Ramp-Down Slew-Rate Setting	0x0 = -0.15mV/µs. 0x1 = -0.625mV/µs. 0x2 = -1.25mV/µs. 0x3 = -2.5mV/µs. 0x4 = -5.0mV/µs. 0x5 = -10mV/µs. 0x6 = -20mV/µs. 0x7 = -40mV/µs.
M1_RU_SR	2:0	O	Buck Master1 Ramp-Up Slew-Rate Setting	0x0 = 0.15mV/µs. 0x1 = 0.625mV/µs. 0x2 = 1.25mV/µs. 0x3 = 2.5mV/µs. 0x4 = 5.0mV/µs. 0x5 = 10mV/µs. 0x6 = 20mV/µs. 0x7 = 40mV/µs.

M1_CFG2 (0x28)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M1_SSTOP_SR[2:0]			M1_SSTRT_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
M1_SSTOP_SR	5:3	O	Buck Master1 Soft-Stop Slew-Rate Setting	0x0 = -0.15mV/µs. 0x1 = -0.625mV/µs. 0x2 = -1.25mV/µs. 0x3 = -2.5mV/µs. 0x4 = -5.0mV/µs. 0x5 = -10mV/µs. 0x6 = -20mV/µs. 0x7 = -40mV/µs.
M1_SSTRT_SR	2:0	O	Buck Master1 Soft-Start Slew-Rate Setting	0x0 = 0.15mV/µs. 0x1 = 0.625mV/µs. 0x2 = 1.25mV/µs. 0x3 = 2.5mV/µs. 0x4 = 5.0mV/µs. 0x5 = 10mV/µs. 0x6 = 20mV/µs. 0x7 = 40mV/µs.

M1_CFG3 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	M1_BBRK[1:0]		M1_ADIS100	M1_ADIS1	M1_FTRAK	M1_REFRESH	M1_FSREN	M1_FPWM
Reset	0x0		0x1	0x0	0x0	0x0	0x1	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M1_BBRK	7:6	O	Buck Master1 Body-Braking Control Setting	0x0 = Disable. 0x1 = Body braking for 8µs. 0x2 = Body braking for 8µs. followed by FPWM for 8µs. 0x3 = Reserved.
M1_ADIS100	5	O	Buck Master1 100Ω Active Discharge	0x0 = Disable. 0x1 = Enable.
M1_ADIS1	4	O	Buck Master1 1Ω Active Discharge: Note that 1Ω active discharge must be disabled when falling slew-rate function of corresponding output is disabled (M1_FSREN = 0).	0x0 = Disable. 0x1 = Enable (active for 1ms after soft-stop is completed).
M1_FTRAK	3	O	Buck Master1 Internal Frequency Tracking Control	0x0 = Disable. 0x1 = Enable.
M1_REFRESH	2	O	Buck Master1 Bootstrap Refresh Interval Control	0x0 = 128µs. 0x1 = 10µs.
M1_FSREN	1	O	Buck Master1 Falling Slew-Rate Control	0x0 = Disable (buck does not sink current from C_{OUT} in skip or LP-skipmode). 0x1 = Enable (buck operates in FPWM mode to sink current from C_{OUT} when its $V_{OUT(TARGET)}$ is lower than the actual V_{OUT}).
M1_FPWM	0	O	Buck Master1 Forced-PWM Control	0x0 = Disable (automatic skip mode operation under light load condition). 0x1 = Enable (OR logic with FPWM_M1 input).

M1_CFG4 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	M1_SS_ENV[1:0]		M1_SS_FREQ[1:0]		M1_SSM_PAT[1:0]		M1_FREQ[1:0]	
Reset	0x0		0x0		0x0		0x1	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M1_SS_ENV	7:6	O	Buck Master1 Spread Spectrum Envelope Setting	0x0 = Disable. 0x1 = ±8%. 0x2 = ±12%. 0x3 = ±16%.
M1_SS_FREQ	5:4	O	Buck Master1 Spread Spectrum Frequency Setting	0x0 = 1kHz. 0x1 = 3kHz. 0x2 = 5kHz. 0x3 = 7kHz.
M1_SSM_PAT	3:2	O	Buck Master1 Spread Spectrum Pattern Setting	0x0 = Triangular pattern (0001b to 1111b). 0x1 = Pseudo-random polynomial ($x^4 + x + 1$). 0x2 = Pseudo-random polynomial ($x^4 + x^3 + 1$). 0x3 = Pseudo-random polynomial (alternating $x^4 + x + 1$ and $x^4 + x^3 + 1$ every cycle).

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M1_FREQ	1:0	O	Buck Master1 Switching Frequency Setting	0x0 = 0.5MHz. 0x1 = 1.0MHz. 0x2 = 1.5MHz. 0x3 = Reserved.

M1_CFG5 (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			RESERVED	RESERVED[1:0]		M1_ILIM[1:0]	
Reset	0x0			0x0	0x2		0x2	
Access Type	Write, Read			Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	O	Reserved. Returns 0.	
RESERVED	4	O	Reserved. Returns 0.	
RESERVED	3:2	O	Reserved. Returns 0b10.	
M1_ILIM	1:0	O	Buck Master1 Peak Current Limit Setting	0x0 = 3.5A. 0x1 = 4.5A. 0x2 = 5.5A. 0x3 = Reserved.

M2_VOUT_H (0x33)

BIT	7	6	5	4	3	2	1	0
Field	M2_VOUT_H[7:0]							
Reset	0x78							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M2_VOUT_H	7:0	F	Buck Master2 Normal Output-Voltage Control Register (V_{OUT} Selected When VSEL_M2 = High and VB_M2 = High, or VSEL and VB Functions are not Used)	When M2_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M2_VOUT_H)V, 0xC8–0xFF = 1.3V. When M2_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M2_VOUT_H)V, 0xC8–0xFF = 2.6V. When M2_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M2_VOUT_H)V, 0xC8–0xFF = 5.2V.

M2_VOUT_L (0x34)

BIT	7	6	5	4	3	2	1	0
Field	M2_VOUT_L[7:0]							
Reset	0x78							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M2_VOUT_L	7:0	F	Buck Master2 Normal Output-Voltage Control Register (V_{OUT} Selected When VSEL_M2 = Low and VB_M2 = High)	When M2_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M2_VOUT_L)V, 0xC8–0xFF = 1.3V. When M2_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M2_VOUT_L)V, 0xC8–0xFF = 2.6V. When M2_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M2_VOUT_L)V, 0xC8–0xFF = 5.2V.

M2_VOUT_B (0x35)

BIT	7	6	5	4	3	2	1	0
Field	M2_VOUT_B[7:0]							
Reset	0x78							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M2_VOUT_B	7:0	F	Buck Master2 Boot (Default) Output-Voltage Control Register (V_{OUT} Selected When VB_M2 = Low)	When M2_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M2_VOUT_B)V, 0xC8–0xFF = 1.3V. When M2_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M2_VOUT_B)V, 0xC8–0xFF = 2.6V. When M2_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M2_VOUT_B)V, 0xC8–0xFF = 5.2V.

M2_VOUT_M (0x36)

BIT	7	6	5	4	3	2	1	0
Field	M2_VOUT_M[4:0]					RESERVED	M2_RNG[1:0]	
Reset	0x19					0x0	0x1	
Access Type	Write, Read					Write, Read	Read Only	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M2_VOUT_M	7:3	F	Buck Master2 Maximum Output-Voltage Control Register	When M2_RNG = 0x0, 0x0–0x18 = (0.3 + 0.04 x M2_VOUT_M)V, 0x19–0x1F = 1.3V. When M2_RNG = 0x1, 0x0–0x18 = (0.6 + 0.08 x M2_VOUT_M)V, 0x19–0x1F = 2.6V. When M2_RNG = 0x2, 0x0–0x18 = (1.2 + 0.16 x M2_VOUT_M)V, 0x19–0x1F = 5.2V.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	2	F	Reserved. Returns 0.	
M2_RNG	1:0	F	Buck Master2 Output-Voltage Range Setting	0x0 = Low range (0.3V to 1.3V, 5mV step), 0x1 = Mid range (0.6V to 2.6V, 10mV step), 0x2 = High range (1.2V to 5.2V, 20mV step), 0x3 = Reserved.

M2_CFG1 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M2_RD_SR[2:0]			M2_RU_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
M2_RD_SR	5:3	O	Buck Master2 Ramp-Down Slew-Rate Setting	0x0 = -0.15mV/µs. 0x1 = -0.625mV/µs. 0x2 = -1.25mV/µs. 0x3 = -2.5mV/µs. 0x4 = -5.0mV/µs. 0x5 = -10mV/µs. 0x6 = -20mV/µs. 0x7 = -40mV/µs.
M2_RU_SR	2:0	O	Buck Master2 Ramp-Up Slew-Rate Setting	0x0 = 0.15mV/µs. 0x1 = 0.625mV/µs. 0x2 = 1.25mV/µs. 0x3 = 2.5mV/µs. 0x4 = 5.0mV/µs. 0x5 = 10mV/µs. 0x6 = 20mV/µs. 0x7 = 40mV/µs.

M2_CFG2 (0x38)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M2_SSTOP_SR[2:0]			M2_SSTRT_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
M2_SSTOP_SR	5:3	O	Buck Master2 Soft-Stop Slew-Rate Setting	0x0 = -0.15mV/µs. 0x1 = -0.625mV/µs. 0x2 = -1.25mV/µs. 0x3 = -2.5mV/µs. 0x4 = -5.0mV/µs. 0x5 = -10mV/µs. 0x6 = -20mV/µs. 0x7 = -40mV/µs.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M2_SSTRT_SR	2:0	O	Buck Master2 Soft-Start Slew-Rate Setting	0x0 = 0.15mV/µs. 0x1 = 0.625mV/µs. 0x2 = 1.25mV/µs. 0x3 = 2.5mV/µs. 0x4 = 5.0mV/µs. 0x5 = 10mV/µs. 0x6 = 20mV/µs. 0x7 = 40mV/µs.

M2_CFG3 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	M2_BBRK[1:0]		M2_ADIS100	M2_ADIS1	M2_FTRAK	M2_REFRESH	M2_FSREN	M2_FPWM
Reset	0x0		0x1	0x0	0x0	0x0	0x1	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M2_BBRK	7:6	O	Buck Master2 Body-Braking Control Setting	0x0 = Disable. 0x1 = Body braking for 8µs. 0x2 = Body braking for 8µs followed by FPWM for 8µs. 0x3 = Reserved.
M2_ADIS100	5	O	Buck Master2 100Ω Active Discharge	0x0 = Disable. 0x1 = Enable.
M2_ADIS1	4	O	Buck Master2 1Ω Active Discharge: Note that 1Ω active discharge must be disabled when falling slew-rate function of corresponding output is disabled (M2_FSREN = 0).	0x0 = Disable. 0x1 = Enable (Active for 1ms after soft-stop is completed).
M2_FTRAK	3	O	Buck Master2 Internal Frequency Tracking Control	0x0 = Disable. 0x1 = Enable.
M2_REFRESH	2	O	Buck Master2 Bootstrap Refresh Interval Control	0x0 = 128µs. 0x1 = 10µs.
M2_FSREN	1	O	Buck Master2 Falling Slew-Rate Control	0x0 = Disable (buck does not sink current from C_{OUT} in skip or LP-skip mode). 0x1 = Enable (buck operates in FPWM mode to sink current from C_{OUT} when its $V_{OUT(TARGET)}$ is lower than the actual V_{OUT}).
M2_FPWM	0	O	Buck Master2 Forced-PWM Control	0x0 = Disable (automatic skip mode operation under light load condition). 0x1 = Enable (OR logic with FPWM_M2 input).

M2_CFG4 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	M2_SS_ENV[1:0]		M2_SS_FREQ[1:0]		M2_SSM_PAT[1:0]		M2_FREQ[1:0]	
Reset	0x0		0x0		0x0		0x1	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M2_SS_ENV	7:6	–	Buck Master2 Spread Spectrum Envelope Setting	0x0 = Disable. 0x1 = ±8%. 0x2 = ±12%. 0x3 = ±16%.
M2_SS_FREQ	5:4	O	Buck Master2 Spread Spectrum Frequency Setting	0x0 = 1kHz. 0x1 = 3kHz. 0x2 = 5kHz. 0x3 = 7kHz.
M2_SSM_PAT	3:2	O	Buck Master2 Spread Spectrum Pattern Setting	0x0 = Triangular pattern (0001b to 1111b). 0x1 = Pseudo-random polynomial ($x^4 + x + 1$). 0x2 = Pseudo-random polynomial ($x^4 + x^3 + 1$). 0x3 = Pseudo-random polynomial (alternating $x^4 + x + 1$ and $x^4 + x^3 + 1$ every cycle).
M2_FREQ	1:0	O	Buck Master2 Switching Frequency Setting	0x0 = 0.5MHz. 0x1 = 1.0MHz. 0x2 = 1.5MHz. 0x3 = Reserved.

M2_CFG5 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			RESERVED	RESERVED[1:0]		M2_ILIM[1:0]	
Reset	0x0			0x0	0x2		0x2	
Access Type	Write, Read			Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	O	Reserved. Returns 0.	
RESERVED	4	O	Reserved. Returns 0.	
RESERVED	3:2	O	Reserved. Returns 0b10.	
M2_ILIM	1:0	O	Buck Master2 Peak Current Limit Setting	0x0 = 3.5A. 0x1 = 4.5A. 0x2 = 5.5A. 0x3 = Reserved.

M3_VOUT_H (0x43)

BIT	7	6	5	4	3	2	1	0
Field	M3_VOUT_H[7:0]							
Reset	0x69							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M3_VOUT_H	7:0	F	Buck Master3 Normal Output-Voltage Control Register (V_{OUT} Selected When VSEL_M3 = High and VB_M3 = High, or VSEL and VB Functions are not Used)	When M3_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M3_VOUT_H)V, 0xC8–0xFF = 1.3V. When M3_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M3_VOUT_H)V, 0xC8–0xFF = 2.6V. When M3_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M3_VOUT_H)V, 0xC8–0xFF = 5.2V.

M3_VOUT_L (0x44)

BIT	7	6	5	4	3	2	1	0
Field	M3_VOUT_L[7:0]							
Reset	0x69							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M3_VOUT_L	7:0	F	Buck Master3 Normal Output-Voltage Control Register (V_{OUT} Selected When VSEL_M3 = Low and VB_M3 = High)	When M3_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M3_VOUT_L)V, 0xC8–0xFF = 1.3V. When M3_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M3_VOUT_L)V, 0xC8–0xFF = 2.6V. When M3_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M3_VOUT_L)V, 0xC8–0xFF = 5.2V.

M3_VOUT_B (0x45)

BIT	7	6	5	4	3	2	1	0
Field	M3_VOUT_B[7:0]							
Reset	0x69							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M3_VOUT_B	7:0	F	Buck Master3 Boot (Default) Output-Voltage Control Register (V_{OUT} Selected When VB_M3 = Low)	When M3_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M3_VOUT_B)V, 0xC8–0xFF = 1.3V. When M3_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M3_VOUT_B)V, 0xC8–0xFF = 2.6V. When M3_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M3_VOUT_B)V, 0xC8–0xFF = 5.2V.

M3_VOUT_M (0x46)

BIT	7	6	5	4	3	2	1	0
Field	M3_VOUT_M[4:0]					RESERVED	M3_RNG[1:0]	
Reset	0x19					0x0	0x2	
Access Type	Write, Read					Write, Read	Read Only	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M3_VOUT_M	7:3	F	Buck Master3 Maximum Output-Voltage Control Register	When M3_RNG = 0x0, 0x0–0x18 = (0.3 + 0.04 x M3_VOUT_M)V, 0x19–0x1F = 1.3V. When M3_RNG = 0x1, 0x0–0x18 = (0.6 + 0.08 x M3_VOUT_M)V, 0x19–0x1F = 2.6V. When M3_RNG = 0x2, 0x0–0x18 = (1.2 + 0.16 x M3_VOUT_M)V, 0x19–0x1F = 5.2V.
RESERVED	2	F	Reserved. Returns 0.	
M3_RNG	1:0	F	Buck Master3 Output-Voltage Range Setting	0x0 = Low range (0.3V to 1.3V, 5mV step). 0x1 = Mid range (0.6V to 2.6V, 10mV step). 0x2 = High range (1.2V to 5.2V, 20mV step). 0x3 = Reserved.

M3_CFG1 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M3_RD_SR[2:0]			M3_RU_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M3_RD_SR	5:3	O	Buck Master3 Ramp-Down Slew-Rate Setting	0x0 = -0.15mV/µs. 0x1 = -0.625mV/µs. 0x2 = -1.25mV/µs. 0x3 = -2.5mV/µs. 0x4 = -5.0mV/µs. 0x5 = -10mV/µs. 0x6 = -20mV/µs. 0x7 = -40mV/µs.
M3_RU_SR	2:0	O	Buck Master3 Ramp-Up Slew-Rate Setting	0x0 = 0.15mV/µs. 0x1 = 0.625mV/µs. 0x2 = 1.25mV/µs. 0x3 = 2.5mV/µs. 0x4 = 5.0mV/µs. 0x5 = 10mV/µs. 0x6 = 20mV/µs. 0x7 = 40mV/µs.

M3_CFG2 (0x48)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M3_SSTOP_SR[2:0]			M3_SSTRT_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
M3_SSTOP_SR	5:3	O	Buck Master3 Soft-Stop Slew-Rate Setting	0x0 = -0.15mV/µs. 0x1 = -0.625mV/µs. 0x2 = -1.25mV/µs. 0x3 = -2.5mV/µs. 0x4 = -5.0mV/µs. 0x5 = -10mV/µs. 0x6 = -20mV/µs. 0x7 = -40mV/µs.
M3_SSTRT_SR	2:0	O	Buck Master3 Soft-Start Slew-Rate Setting	0x0 = 0.15mV/µs. 0x1 = 0.625mV/µs. 0x2 = 1.25mV/µs. 0x3 = 2.5mV/µs. 0x4 = 5.0mV/µs. 0x5 = 10mV/µs. 0x6 = 20mV/µs. 0x7 = 40mV/µs.

M3_CFG3 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	M3_BBRK[1:0]		M3_ADIS100	M3_ADIS1	M3_FTRAK	M3_REFRESH	M3_FSREN	M3_FPWM
Reset	0x0		0x1	0x0	0x0	0x0	0x1	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M3_BBRK	7:6	O	Buck Master3 Body-Braking Control Setting	0x0 = Disable. 0x1 = Body braking for 8µs. 0x2 = Body braking for 8µs followed by FPWM for 8µs. 0x3 = Reserved.
M3_ADIS100	5	O	Buck Master3 100Ω Active Discharge	0x0 = Disable. 0x1 = Enable.
M3_ADIS1	4	O	Buck Master3 1Ω Active Discharge: Note that 1Ω active discharge must be disabled when falling slew-rate function of corresponding output is disabled (M3_FSREN = 0)	0x0 = Disable. 0x1 = Enable (active for 1ms after soft-stop is completed).
M3_FTRAK	3	O	Buck Master3 Internal Frequency Tracking Control	0x0 = Disable. 0x1 = Enable.
M3_REFRESH	2	O	Buck Master3 Bootstrap Refresh Interval Control	0x0 = 128µs. 0x1 = 10µs.
M3_FSREN	1	O	Buck Master3 Falling Slew-Rate Control	0x0 = Disable (buck does not sink current from C_{OUT} in skip or LP-skip mode). 0x1 = Enable (buck operates in FPWM mode to sink current from C_{OUT} when its $V_{OUT(TARGET)}$ is lower than the actual V_{OUT}).
M3_FPWM	0	O	Buck Master3 Forced-PWM Control	0x0 = Disable (automatic skip mode operation under light load condition). 0x1 = Enable (OR logic with FPWM_M3 input).

M3_CFG4 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	M3_SS_ENV[1:0]		M3_SS_FREQ[1:0]		M3_SSM_PAT[1:0]		M3_FREQ[1:0]	
Reset	0x0		0x0		0x0		0x1	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M3_SS_ENV	7:6	O	Buck Master3 Spread Spectrum Envelope Setting	0x0 = Disable. 0x1 = ±8%. 0x2 = ±12%. 0x3 = ±16%.
M3_SS_FREQ	5:4	O	Buck Master3 Spread Spectrum Frequency Setting	0x0 = 1kHz. 0x1 = 3kHz. 0x2 = 5kHz. 0x3 = 7kHz.
M3_SSM_PAT	3:2	O	Buck Master3 Spread Spectrum Pattern Setting	0x0 = Triangular pattern (0001b to 1111b). 0x1 = Pseudo-random polynomial ($x^4 + x + 1$). 0x2 = Pseudo-random polynomial ($x^4 + x^3 + 1$). 0x3 = Pseudo-random polynomial (alternating $x^4 + x + 1$ and $x^4 + x^3 + 1$ every cycle).

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M3_FREQ	1:0	O	Buck Master3 Switching Frequency Setting	0x0 = 0.5MHz. 0x1 = 1.0MHz. 0x2 = 1.5MHz. 0x3 = Reserved.

M3_CFG5 (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			RESERVED	RESERVED[1:0]		M3_ILIM[1:0]	
Reset	0x0			0x0	0x2		0x2	
Access Type	Write, Read			Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	O	Reserved. Returns 0.	
RESERVED	4	O	Reserved. Returns 0.	
RESERVED	3:2	O	Reserved. Returns 0b10.	
M3_ILIM	1:0	O	Buck Master3 Peak Current Limit Setting	0x0 = 3.5A. 0x1 = 4.5A. 0x2 = 5.5A. 0x3 = Reserved.

M4_VOUT_H (0x53)

BIT	7	6	5	4	3	2	1	0
Field	M4_VOUT_H[7:0]							
Reset	0xBE							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_VOUT_H	7:0	F	Buck Master4 Normal Output-Voltage Control Register (V_{OUT} Selected When VSEL_M4 = High and VB_M4 = High, or VSEL and VB Functions are not Used)	When M4_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M4_VOUT_H)V, 0xC8–0xFF = 1.3V. When M4_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M4_VOUT_H)V, 0xC8–0xFF = 2.6V. When M4_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M4_VOUT_H)V, 0xC8–0xFF = 5.2V.

M4_VOUT_L (0x54)

BIT	7	6	5	4	3	2	1	0
Field	M4_VOUT_L[7:0]							
Reset	0xBE							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_VOUT_L	7:0	F	Buck Master4 Normal Output-Voltage Control Register (V_{OUT} Selected When VSEL_M4 = Low and VB_M4 = High)	When M4_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M4_VOUT_L)V, 0xC8–0xFF = 1.3V. When M4_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M4_VOUT_L)V, 0xC8–0xFF = 2.6V. When M4_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M4_VOUT_L)V, 0xC8–0xFF = 5.2V.

M4_VOUT_B (0x55)

BIT	7	6	5	4	3	2	1	0
Field	M4_VOUT_B[7:0]							
Reset	0xBE							
Access Type	Write, Read							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_VOUT_B	7:0	F	Buck Master4 Boot (Default) Output-Voltage Control Register (V_{OUT} Selected When VB_M4 = Low)	When M4_RNG = 0x0, 0x0–0xC7 = (0.3 + 0.005 x M4_VOUT_B)V, 0xC8–0xFF = 1.3V. When M4_RNG = 0x1, 0x0–0xC7 = (0.6 + 0.01 x M4_VOUT_B)V, 0xC8–0xFF = 2.6V. When M4_RNG = 0x2, 0x0–0xC7 = (1.2 + 0.02 x M4_VOUT_B)V, 0xC8–0xFF = 5.2V.

M4_VOUT_M (0x56)

BIT	7	6	5	4	3	2	1	0
Field	M4_VOUT_M[4:0]					RESERVED	M4_RNG[1:0]	
Reset	0x19					0x0	0x2	
Access Type	Write, Read					Write, Read	Read Only	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_VOUT_M	7:3	F	Buck Master4 Maximum Output-Voltage Control Register	When M4_RNG = 0x0, 0x0–0x18 = (0.3 + 0.04 x M4_VOUT_M)V, 0x19–0x1F = 1.3V. When M4_RNG = 0x1, 0x0–0x18 = (0.6 + 0.08 x M4_VOUT_M)V, 0x19–0x1F = 2.6V. When M4_RNG = 0x2, 0x0–0x18 = (1.2 + 0.16 x M4_VOUT_M)V, 0x19–0x1F = 5.2V.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	2	F	Reserved. Returns 0.	
M4_RNG	1:0	F	Buck Master4 Output-Voltage Range Setting	0x0 = Low range (0.3V to 1.3V, 5mV step). 0x1 = Mid range (0.6V to 2.6V, 10mV step). 0x2 = High range (1.2V to 5.2V, 20mV step). 0x3 = Reserved.

M4_CFG1 (0x57)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M4_RD_SR[2:0]			M4_RU_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
M4_RD_SR	5:3	O	Buck Master4 Ramp-Down Slew-Rate Setting	0x0 = -0.15mV/µs. 0x1 = -0.625mV/µs. 0x2 = -1.25mV/µs. 0x3 = -2.5mV/µs. 0x4 = -5.0mV/µs. 0x5 = -10mV/µs. 0x6 = -20mV/µs. 0x7 = -40mV/µs.
M4_RU_SR	2:0	O	Buck Master4 Ramp-Up Slew-Rate Setting	0x0 = 0.15mV/µs. 0x1 = 0.625mV/µs. 0x2 = 1.25mV/µs. 0x3 = 2.5mV/µs. 0x4 = 5.0mV/µs. 0x5 = 10mV/µs. 0x6 = 20mV/µs. 0x7 = 40mV/µs.

M4_CFG2 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M4_SSTOP_SR[2:0]			M4_SSTRT_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
M4_SSTOP_SR	5:3	O	Buck Master4 Soft-Stop Slew-Rate Setting	0x0 = -0.15mV/µs. 0x1 = -0.625mV/µs. 0x2 = -1.25mV/µs. 0x3 = -2.5mV/µs. 0x4 = -5.0mV/µs. 0x5 = -10mV/µs. 0x6 = -20mV/µs. 0x7 = -40mV/µs.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_SSTRT_SR	2:0	O	Buck Master4 Soft-Start Slew-Rate Setting	0x0 = 0.15mV/µs. 0x1 = 0.625mV/µs. 0x2 = 1.25mV/µs. 0x3 = 2.5mV/µs. 0x4 = 5.0mV/µs. 0x5 = 10mV/µs. 0x6 = 20mV/µs. 0x7 = 40mV/µs.

M4_CFG3 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	M4_BBRK[1:0]		M4_ADIS100	M4_ADIS1	M4_FTRAK	M4_REFRESH	M4_FSREN	M4_FPWM
Reset	0x0		0x1	0x0	0x0	0x0	0x1	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_BBRK	7:6	O	Buck Master4 Body-Braking Control Setting	0x0 = Disable. 0x1 = Body braking for 8µs. 0x2 = Body braking for 8µs followed by FPWM for 8µs. 0x3 = Reserved.
M4_ADIS100	5	O	Buck Master4 100Ω Active Discharge	0x0 = Disable. 0x1 = Enable.
M4_ADIS1	4	O	Buck Master4 1Ω Active Discharge: Note that 1Ω active discharge must be disabled when falling slew-rate function of corresponding output is disabled (M4_FSREN = 0)	0x0 = Disable. 0x1 = Enable (active for 1ms after soft-stop is completed).
M4_FTRAK	3	O	Buck Master4 Internal Frequency Tracking Control	0x0 = Disable. 0x1 = Enable.
M4_REFRESH	2	O	Buck Master4 Bootstrap Refresh Interval Control	0x0 = 128µs. 0x1 = 10µs.
M4_FSREN	1	O	Buck Master4 Falling Slew-Rate Control	0x0 = Disable (buck does not sink current from C_{OUT} in skip or LP-skip mode). 0x1 = Enable (buck operates in FPWM mode to sink current from C_{OUT} when its $V_{OUT(TARGET)}$ is lower than the actual V_{OUT}).
M4_FPWM	0	O	Buck Master4 Forced-PWM Control	0x0 = Disable (automatic skip mode operation under light load condition). 0x1 = Enable (OR logic with FPWM_M4 input).

M4_CFG4 (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	M4_SS_ENV[1:0]		M4_SS_FREQ[1:0]		M4_SSM_PAT[1:0]		M4_FREQ[1:0]	
Reset	0x0		0x0		0x0		0x1	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
M4_SS_ENV	7:6	O	Buck Master4 Spread Spectrum Envelope Setting	0x0 = Disable. 0x1 = ±8%. 0x2 = ±12%. 0x3 = ±16%.
M4_SS_FREQ	5:4	O	Buck Master4 Spread Spectrum Frequency Setting	0x0 = 1kHz. 0x1 = 3kHz. 0x2 = 5kHz. 0x3 = 7kHz.
M4_SSM_PAT	3:2	O	Buck Master4 Spread Spectrum Pattern Setting	0x0 = Triangular pattern (0001b to 1111b). 0x1 = Pseudorandom polynomial ($x^4 + x + 1$). 0x2 = Pseudorandom polynomial ($x^4 + x^3 + 1$). 0x3 = Pseudorandom polynomial (alternating $x^4 + x + 1$ and $x^4 + x^3 + 1$ every cycle).
M4_FREQ	1:0	O	Buck Master4 Switching Frequency Setting	0x0 = 0.5MHz. 0x1 = 1.0MHz. 0x2 = 1.5MHz. 0x3 = Reserved.

M4_CFG5 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			RESERVED	RESERVED[1:0]		M4_ILIM[1:0]	
Reset	0x0			0x0	0x2		0x2	
Access Type	Write, Read			Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	Od	Reserved. Returns 0.	
RESERVED	4	O	Reserved. Returns 0.	
RESERVED	3:2	O	Reserved. Returns 0b10.	
M4_ILIM	1:0	O	Buck Master4 Peak Current Limit Setting	0x0 = 3.5A. 0x1 = 4.5A. 0x2 = 5.5A. 0x3 = Reserved.

MFIO_INT (0x60)

BIT	7	6	5	4	3	2	1	0
Field	MFIO8_I	MFIO7_I	MFIO6_I	MFIO5_I	MFIO4_I	MFIO3_I	MFIO2_I	MFIO1_I
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
MFIO8_I	7	O	Multifunction I/O 8 Interrupt	0x0 = MFIO8 input has not toggled. 0x1 = MFIO8 input has toggled.
MFIO7_I	6	O	Multifunction I/O 7 Interrupt	0x0 = MFIO7 input has not toggled. 0x1 = MFIO7 input has toggled.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
MFIO6_I	5	O	Multifunction I/O 6 Interrupt	0x0 = MFIO6 input has not toggled. 0x1 = MFIO6 input has toggled.
MFIO5_I	4	O	Multifunction I/O 5 Interrupt	0x0 = MFIO5 input has not toggled. 0x1 = MFIO5 input has toggled.
MFIO4_I	3	O	Multifunction I/O 4 Interrupt	0x0 = MFIO4 input has not toggled. 0x1 = MFIO4 input has toggled.
MFIO3_I	2	O	Multifunction I/O 3 Interrupt	0x0 = MFIO3 input has not toggled. 0x1 = MFIO3 input has toggled.
MFIO2_I	1	O	Multifunction I/O 2 Interrupt	0x0 = MFIO2 input has not toggled. 0x1 = MFIO2 input has toggled.
MFIO1_I	0	O	Multifunction I/O 1 Interrupt	0x0 = MFIO1 input has not toggled. 0x1 = MFIO1 input has toggled.

MFIO_MSK (0x61)

BIT	7	6	5	4	3	2	1	0
Field	MFIO8_M	MFIO7_M	MFIO6_M	MFIO5_M	MFIO4_M	MFIO3_M	MFIO2_M	MFIO1_M
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
MFIO8_M	7	O	Multifunction I/O 8 Interrupt Mask	0x0 = Enable MFIO8_I. 0x1 = Mask MFIO8_I.
MFIO7_M	6	O	Multifunction I/O 7 Interrupt Mask	0x0 = Enable MFIO7_I. 0x1 = Mask MFIO7_I.
MFIO6_M	5	O	Multifunction I/O 6 Interrupt Mask	0x0 = Enable MFIO6_I. 0x1 = Mask MFIO6_I.
MFIO5_M	4	O	Multifunction I/O 5 Interrupt Mask	0x0 = Enable MFIO5_I. 0x1 = Mask MFIO5_I.
MFIO4_M	3	O	Multifunction I/O 4 Interrupt Mask	0x0 = Enable MFIO4_I. 0x1 = Mask MFIO4_I.
MFIO3_M	2	O	Multifunction I/O 3 Interrupt Mask	0x0 = Enable MFIO3_I. 0x1 = Mask MFIO3_I.
MFIO2_M	1	O	Multifunction I/O 2 Interrupt Mask	0x0 = Enable MFIO2_I. 0x1 = Mask MFIO2_I.
MFIO1_M	0	O	Multifunction I/O 1 Interrupt Mask	0x0 = Enable MFIO1_I. 0x1 = Mask MFIO1_I.

MFIO_STAT (0x62)

BIT	7	6	5	4	3	2	1	0
Field	MFIO8	MFIO7	MFIO6	MFIO5	MFIO4	MFIO3	MFIO2	MFIO1
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
MFIO8	7	O	Multifunction I/O 8 Status	0x0 = MFIO8 input is not asserted. 0x1 = MFIO8 input is asserted.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
MFIO7	6	O	Multifunction I/O 7 Status	0x0 = MFIO7 input is not asserted. 0x1 = MFIO7 input is asserted.
MFIO6	5	O	Multifunction I/O 6 Status	0x0 = MFIO6 input is not asserted. 0x1 = MFIO6 input is asserted.
MFIO5	4	O	Multifunction I/O 5 Status	0x0 = MFIO5 input is not asserted. 0x1 = MFIO5 input is asserted.
MFIO4	3	O	Multifunction I/O 4 Status	0x0 = MFIO4 input is not asserted. 0x1 = MFIO4 input is asserted.
MFIO3	2	O	Multifunction I/O 3 Status	0x0 = MFIO3 input is not asserted. 0x1 = MFIO3 input is asserted.
MFIO2	1	O	Multifunction I/O 2 Status	0x0 = MFIO2 input is not asserted. 0x1 = MFIO2 input is asserted.
MFIO1	0	O	Multifunction I/O 1 Status	0x0 = MFIO1 input is not asserted. 0x1 = MFIO1 input is asserted.

MFIO1_CFG1 (0x63)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	MFIO1_SEL[2:0]			MFIO1_FUNC[3:0]			
Reset	0x0	0x0			0x8			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7	O	Reserved. Returns 0.	
MFIO1_SEL	6:4	O	MFIO1 Selection Setting	0x0 = M1 (Master1). 0x1 = M2 (Master2). 0x2 = M3 (Master3). 0x3 = M4 (Master4). 0x4 = GLB (M1, M2, M3, M4). 0x5 = Logic high (GPO mode only). 0x6 = Logic low (GPO mode only). 0x7 = High impedance (GPO mode only).
MFIO1_FUNC	3:0	O	MFIO1 Function Setting	0x0 = Output enable (EN). 0x1 = Low-power mode (LPM). 0x2 = Forced-PWM mode (FPWM). 0x3 = External clock detection (CLKDET). 0x4 = Clock output (CLKOUT). 0x5 = Output-voltage selection (VSEL). 0x6 = Boot (default) output-voltage selection (VB). 0x7 = Power-OK output (POK). 0x8 = FPS input (FPSI). 0x9 = FPS output (FPSO). 0xA = System reset input (RSTINB). 0xB = System reset output (RSTOB). 0xC = Thermal-warning output (TWARNB). 0xD = General-purpose input (GPI). 0xE = General-purpose output (GPO). 0xF = Reserved.

MFIO1_CFG2 (0x64)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		MFIO1_DRV_MODE	MFIO1_PDPU[1:0]		MFIO1_DEB[2:0]		
Reset	0x0		0x0	0x0		0x2		
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
MFIO1_DRV_MODE	5	O	MFIO1 Output Driver Mode Setting	0x0 = Open drain. 0x1 = Push-pull.
MFIO1_PDPU	4:3	O	MFIO1 Pull-Down and Pull-Up Control	0x0 = 800kΩ pull-down to AGND. 0x1 = 100kΩ pull-down to AGND. 0x2 = 100kΩ pull-up to V_{IO}. 0x3 = Disable (no pull-down or pull-up).
MFIO1_DEB	2:0	O	MFIO1 Debounce Timer Setting	0x0 = No debounce. 0x1 = 0.55µs. 0x2 = 1µs. 0x3 = 2µs. 0x4 = 4µs. 0x5 = 8µs. 0x6 = 16µs. 0x7 = 32µs.

MFIO2_CFG1 (0x65)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	MFIO2_SEL[2:0]			MFIO2_FUNC[3:0]			
Reset	0x0	0x0			0x7			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7	O	Reserved. Returns 0.	
MFIO2_SEL	6:4	O	MFIO2 Selection Setting	0x0 = M1 (Master1). 0x1 = M2 (Master2). 0x2 = M3 (Master3). 0x3 = M4 (Master4). 0x4 = GLB (M1, M2, M3, M4). 0x5 = Logic high (GPO mode only). 0x6 = Logic low (GPO mode only). 0x7 = High impedance (GPO mode only).

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
MFIO2_FUNC	3:0	O	MFIO2 Function Setting	0x0 = Output enable (EN). 0x1 = Low-power mode (LPM). 0x2 = Forced-PWM mode (FPWM). 0x3 = External clock detection (CLKDET). 0x4 = Clock output (CLKOUT). 0x5 = Output-voltage selection (VSEL). 0x6 = Boot (default) output-voltage selection (VB). 0x7 = Power-OK output (POK). 0x8 = FPS input (FPSI). 0x9 = FPS output (FPSO). 0xA = System reset input (RSTINB). 0xB = System reset output (RSTOB). 0xC = Thermal-warning output (TWARNB). 0xD = General-purpose input (GPI). 0xE = General-purpose output (GPO). 0xF = Reserved.

MFIO2_CFG2 (0x66)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		MFIO2_DRV_MODE	MFIO2_PDPU[1:0]		MFIO2_DEB[2:0]		
Reset	0x0		0x0	0x0		0x2		
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
MFIO2_DRV_MODE	5	O	MFIO2 Output Driver Mode Setting	0x0 = Open drain. 0x1 = Push-pull.
MFIO2_PDPU	4:3	O	MFIO2 Pull-Down and Pull-Up Control	0x0 = 800kΩ pull-down to AGND. 0x1 = 100kΩ pull-down to AGND. 0x2 = 100kΩ pull-up to V_{IO}. 0x3 = Disable (no pull-down or pull-up).
MFIO2_DEB	2:0	O	MFIO2 Debounce Timer Setting	0x0 = No debounce. 0x1 = 0.55µs. 0x2 = 1µs. 0x3 = 2µs. 0x4 = 4µs. 0x5 = 8µs. 0x6 = 16µs. 0x7 = 32µs.

MFIO3_CFG1 (0x67)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	MFIO3_SEL[2:0]			MFIO3_FUNC[3:0]			
Reset	0x0	0x0			0x2			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7	O	Reserved. Returns 0.	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
MFIO3_SEL	6:4	O	MFIO3 Selection Setting	0x0 = M1 (Master1). 0x1 = M2 (Master2). 0x2 = M3 (Master3). 0x3 = M4 (Master4). 0x4 = GLB (M1, M2, M3, M4). 0x5 = Logic high (GPO mode only). 0x6 = Logic low (GPO mode only). 0x7 = High impedance (GPO mode only).
MFIO3_FUNC	3:0	O	MFIO3 Function Setting	0x0 = Output enable (EN). 0x1 = Low-power mode (LPM). 0x2 = Forced-PWM mode (FPWM). 0x3 = External clock detection (CLKDET). 0x4 = Clock output (CLKOUT). 0x5 = Output-voltage selection (VSEL). 0x6 = Boot (default) output-voltage selection (VB). 0x7 = Power-OK output (POK). 0x8 = FPS input (FPSI). 0x9 = FPS output (FPSO). 0xA = System reset input (RSTINB). 0xB = System reset output (RSTOB). 0xC = Thermal-warning output (TWARNB). 0xD = General-purpose input (GPI). 0xE = General-purpose output (GPO). 0xF = Reserved.

MFIO3_CFG2 (0x68)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		MFIO3_DRV_MODE	MFIO3_PDPU[1:0]		MFIO3_DEB[2:0]		
Reset	0x0		0x0	0x0		0x2		
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
MFIO3_DRV_MODE	5	O	MFIO3 Output Driver Mode Setting	0x0 = Open drain. 0x1 = Push-pull.
MFIO3_PDPU	4:3	O	MFIO3 Pull-Down and Pull-Up Control	0x0 = 800kΩ pull-down to AGND. 0x1 = 100kΩ pull-down to AGND. 0x2 = 100kΩ pull-up to V_{IO}. 0x3 = Disable (no pull-down or pull-up).
MFIO3_DEB	2:0	O	MFIO3 Debounce Timer Setting	0x0 = No debounce, 0x1 = 0.55µs. 0x2 = 1µs. 0x3 = 2µs. 0x4 = 4µs. 0x5 = 8µs. 0x6 = 16µs. 0x7 = 32µs.

MFIO4_CFG1 (0x69)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	MFIO4_SEL[2:0]			MFIO4_FUNC[3:0]			
Reset	0x0	0x0			0x3			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7	O	Reserved. Returns 0.	
MFIO4_SEL	6:4	O	MFIO4 Selection Setting	0x0 = M1 (Master1). 0x1 = M2 (Master2). 0x2 = M3 (Master3). 0x3 = M4 (Master4). 0x4 = GLB (M1, M2, M3, M4). 0x5 = Logic high (GPO mode only). 0x6 = Logic low (GPO mode only). 0x7 = High impedance (GPO mode only).
MFIO4_FUNC	3:0	O	MFIO4 Function Setting	0x0 = Output enable (EN). 0x1 = Low-power mode (LPM). 0x2 = Forced-PWM mode (FPWM). 0x3 = External clock detection (CLKDET). 0x4 = Clock output (CLKOUT). 0x5 = Output-voltage selection (VSEL). 0x6 = Boot (default) output-voltage selection (VB). 0x7 = Power-OK output (POK). 0x8 = FPS input (FPSI). 0x9 = FPS output (FPSO). 0xA = System reset input (RSTINB). 0xB = System reset output (RSTOB). 0xC = Thermal-warning output (TWARNB). 0xD = General-purpose input (GPI). 0xE = General-purpose output (GPO). 0xF = Reserved.

MFIO4_CFG2 (0x6A)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		MFIO4_DRV_MODE	MFIO4_PDPU[1:0]		MFIO4_DEB[2:0]		
Reset	0x0		0x0	0x0		0x2		
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
MFIO4_DRV_MODE	5	O	MFIO4 Output Driver Mode Setting	0x0 = Open drain. 0x1 = Push-pull.
MFIO4_PDPU	4:3	O	MFIO4 Pull-Down and Pull-Up Control	0x0 = 800kΩ pull-down to AGND. 0x1 = 100kΩ pull-down to AGND. 0x2 = 100kΩ pull-up to V_{IO}. 0x3 = Disable (no pull-down or pull-up).

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
MFIO4_DEB	2:0	O	MFIO4 Debounce Timer Setting	0x0 = No debounce. 0x1 = 0.55µs. 0x2 = 1µs. 0x3 = 2µs. 0x4 = 4µs. 0x5 = 8µs. 0x6 = 16µs. 0x7 = 32µs.

MFIO5_CFG1 (0x6B)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	MFIO5_SEL[2:0]			MFIO5_FUNC[3:0]			
Reset	0x0	0x4			0x6			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7	O	Reserved. Returns 0.	
MFIO5_SEL	6:4	O	MFIO5 Selection Setting	0x0 = M1 (Master1). 0x1 = M2 (Master2). 0x2 = M3 (Master3). 0x3 = M4 (Master4). 0x4 = GLB (M1, M2, M3, M4). 0x5 = Logic high (GPO mode only). 0x6 = Logic low (GPO mode only). 0x7 = High impedance (GPO mode only).
MFIO5_FUNC	3:0	O	MFIO5 Function Setting	0x0 = Output enable (EN). 0x1 = Low-power mode (LPM). 0x2 = Forced-PWM mode (FPWM). 0x3 = External clock detection (CLKDET). 0x4 = Clock output (CLKOUT). 0x5 = Output-voltage selection (VSEL). 0x6 = Boot (default) output-voltage selection (VB). 0x7 = Power-OK output (POK). 0x8 = FPS input (FPSI). 0x9 = FPS output (FPSO). 0xA = System reset input (RSTINB). 0xB = System reset output (RSTOB). 0xC = Thermal-warning output (TWARNB). 0xD = General-purpose input (GPI). 0xE = General-purpose output (GPO). 0xF = Reserved.

MFIO5_CFG2 (0x6C)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		MFIO5_DRV_MODE	MFIO5_PDPU[1:0]		MFIO5_DEB[2:0]		
Reset	0x0		0x0	0x0		0x2		
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
MFIO5_DRV_MODE	5	O	MFIO5 Output Driver Mode Setting	0x0 = Open drain. 0x1 = Push-pull.
MFIO5_PDPU	4:3	O	MFIO5 Pull-Down and Pull-Up Control	0x0 = 800kΩ pull-down to AGND. 0x1 = 100kΩ pull-down to AGND. 0x2 = 100kΩ pull-up to V_{IO}. 0x3 = Disable (no pull-down or pull-up).
MFIO5_DEB	2:0	O	MFIO5 Debounce Timer Setting	0x0 = No debounce. 0x1 = 0.55µs. 0x2 = 1µs. 0x3 = 2µs. 0x4 = 4µs. 0x5 = 8µs. 0x6 = 16µs. 0x7 = 32µs.

MFIO6_CFG1 (0x6D)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	MFIO6_SEL[2:0]			MFIO6_FUNC[3:0]			
Reset	0x0	0x0			0xA			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7	O	Reserved. Returns 0.	
MFIO6_SEL	6:4	O	MFIO6 Selection Setting	0x0 = M1 (Master1). 0x1 = M2 (Master2). 0x2 = M3 (Master3). 0x3 = M4 (Master4). 0x4 = GLB (M1, M2, M3, M4). 0x5 = Logic high (GPO mode only). 0x6 = Logic low (GPO mode only). 0x7 = High impedance (GPO mode only).
MFIO6_FUNC	3:0	O	MFIO6 Function Setting	0x0 = Output enable (EN). 0x1 = Low-power mode (LPM). 0x2 = Forced-PWM mode (FPWM). 0x3 = External clock detection (CLKDET). 0x4 = Clock output (CLKOUT). 0x5 = Output-voltage selection (VSEL). 0x6 = Boot (default) output-voltage selection (VB). 0x7 = Power-OK output (POK). 0x8 = FPS input (FPSI). 0x9 = FPS output (FPSO). 0xA = System reset input (RSTINB). 0xB = System reset output (RSTOB). 0xC = Thermal-warning output (TWARNB). 0xD = General-purpose input (GPI). 0xE = General-purpose output (GPO). 0xF = Reserved.

MFIO6_CFG2 (0x6E)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		MFIO6_DRV_MODE	MFIO6_PDPU[1:0]		MFIO6_DEB[2:0]		
Reset	0x0		0x0	0x0		0x2		
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
MFIO6_DRV_MODE	5	O	MFIO6 Output Driver Mode Setting	0x0 = Open drain. 0x1 = Push-pull.
MFIO6_PDPU	4:3	O	MFIO6 Pull-Down and Pull-Up Control	0x0 = 800kΩ pull-down to AGND. 0x1 = 100kΩ pull-down to AGND. 0x2 = 100kΩ pull-up to V_{IO}. 0x3 = Disable (no pull-down or pull-up).
MFIO6_DEB	2:0	O	MFIO6 Debounce Timer Setting	0x0 = No debounce. 0x1 = 0.55µs. 0x2 = 1µs. 0x3 = 2µs. 0x4 = 4µs. 0x5 = 8µs. 0x6 = 16µs. 0x7 = 32µs.

MFIO7_CFG1 (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	MFIO7_SEL[2:0]			MFIO7_FUNC[3:0]			
Reset	0x0	0x0			0xC			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7	O	Reserved. Returns 0.	
MFIO7_SEL	6:4	O	MFIO7 Selection Setting	0x0 = M1 (Master1). 0x1 = M2 (Master2). 0x2 = M3 (Master3). 0x3 = M4 (Master4). 0x4 = GLB (M1, M2, M3, M4). 0x5 = Logic high (GPO mode only). 0x6 = Logic low (GPO mode only). 0x7 = High impedance (GPO mode only).

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
MFIO7_FUNC	3:0	O	MFIO7 Function Setting	0x0 = Output enable (EN). 0x1 = Low-power mode (LPM). 0x2 = Forced-PWM Mode (FPWM). 0x3 = External clock detection (CLKDET). 0x4 = Clock output (CLKOUT). 0x5 = Output-voltage selection (VSEL). 0x6 = Boot (default) output-voltage selection (VB). 0x7 = Power-OK output (POK). 0x8 = FPS input (FPSI). 0x9 = FPS output (FPSO). 0xA = System reset input (RSTINB). 0xB = System reset output (RSTOB). 0xC = Thermal-warning output (TWARNB). 0xD = General-purpose input (GPI). 0xE = General-purpose output (GPO). 0xF = Reserved.

MFIO7_CFG2 (0x70)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		MFIO7_DRV_MODE	MFIO7_PDPU[1:0]		MFIO7_DEB[2:0]		
Reset	0x0		0x0	0x0		0x2		
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
MFIO7_DRV_MODE	5	O	MFIO7 Output Driver Mode Setting	0x0 = Open drain. 0x1 = Push-pull.
MFIO7_PDPU	4:3	O	MFIO7 Pull-Down and Pull-Up Control	0x0 = 800kΩ pull-down to AGND. 0x1 = 100kΩ pull-down to AGND. 0x2 = 100kΩ pull-up to V_{IO}. 0x3 = Disable (no pull-down or pull-up).
MFIO7_DEB	2:0	O	MFIO7 Debounce Timer Setting	0x0 = No debounce. 0x1 = 0.55µs. 0x2 = 1µs. 0x3 = 2µs. 0x4 = 4µs. 0x5 = 8µs. 0x6 = 16µs. 0x7 = 32µs.

MFIO8_CFG1 (0x71)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	MFIO8_SEL[2:0]			MFIO8_FUNC[3:0]			
Reset	0x0	0x0			0xB			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7	O	Reserved. Returns 0.	

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
MFIO8_SEL	6:4	O	MFIO8 Selection Setting	0x0 = M1 (Master1). 0x1 = M2 (Master2). 0x2 = M3 (Master3). 0x3 = M4 (Master4). 0x4 = GLB (M1, M2, M3, M4). 0x5 = Logic high (GPO mode only). 0x6 = Logic low (GPO mode only). 0x7 = High impedance (GPO mode only).
MFIO8_FUNC	3:0	O	MFIO8 Function Setting	0x0 = Output enable (EN). 0x1 = Low-power mode (LPM). 0x2 = Forced-PWM mode (FPWM). 0x3 = External clock detection (CLKDET). 0x4 = Clock output (CLKOUT). 0x5 = Output-voltage selection (VSEL). 0x6 = Boot (default) output-voltage selection (VB). 0x7 = Power-OK output (POK), 0x8 = FPS input (FPSI). 0x9 = FPS output (FPSO). 0xA = System reset input (RSTINB). 0xB = System reset output (RSTOB). 0xC = Thermal-warning output (TWARNB). 0xD = General-purpose Input (GPI). 0xE = General-purpose output (GPO). 0xF = ADC mux input (ADCMUX).

MFIO8_CFG2 (0x72)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		MFIO8_DRV_MODE	MFIO8_PDPU[1:0]		MFIO8_DEB[2:0]		
Reset	0x0		0x0	0x0		0x2		
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
MFIO8_DRV_MODE	5	O	MFIO8 Output Driver Mode Setting	0x0 = Open drain. 0x1 = Push-pull.
MFIO8_PDPU	4:3	O	MFIO8 Pull-Down and Pull-Up Control	0x0 = 800kΩ pull-down to AGND. 0x1 = 100kΩ pull-down to AGND. 0x2 = 100kΩ pull-up to V_{IO}. 0x3 = Disable (no pull-down or pull-up).
MFIO8_DEB	2:0	O	MFIO8 Debounce Timer Setting	0x0 = No debounce. 0x1 = 0.55µs. 0x2 = 1µs. 0x3 = 2µs. 0x4 = 4µs. 0x5 = 8µs. 0x6 = 16µs. 0x7 = 32µs.

ADC_INT1 (0x80)

BIT	7	6	5	4	3	2	1	0
Field	ADC_CH8_I	ADC_CH7_I	ADC_CH6_I	ADC_CH5_I	ADC_CH4_I	ADC_CH3_I	ADC_CH2_I	ADC_CH1_I
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_CH8_I	7	O	ADC Channel8 Interrupt	0x0 = ADC Channel8 data has not updated. 0x1 = ADC Channel8 data has updated.
ADC_CH7_I	6	O	ADC Channel7 Interrupt	0x0 = ADC Channel7 data has not updated. 0x1 = ADC Channel7 data has updated.
ADC_CH6_I	5	O	ADC Channel6 Interrupt	0x0 = ADC Channel6 data has not updated. 0x1 = ADC Channel6 data has updated.
ADC_CH5_I	4	O	ADC Channel5 Interrupt	0x0 = ADC Channel5 data has not updated. 0x1 = ADC Channel5 data has updated.
ADC_CH4_I	3	O	ADC Channel4 Interrupt	0x0 = ADC Channel4 data has not updated. 0x1 = ADC Channel4 data has updated.
ADC_CH3_I	2	O	ADC Channel3 Interrupt	0x0 = ADC Channel3 data has not updated. 0x1 = ADC Channel3 data has updated.
ADC_CH2_I	1	O	ADC Channel2 Interrupt	0x0 = ADC Channel2 data has not updated. 0x1 = ADC Channel2 data has updated.
ADC_CH1_I	0	O	ADC Channel1 Interrupt	0x0 = ADC Channel1 data has not updated. 0x1 = ADC Channel1 data has updated.

ADC_INT2 (0x81)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			RESERVED	RESERVED	ADC_CH11_I	ADC_CH10_I	ADC_CH9_I
Reset	0x0			0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All			Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	O	Reserved. Returns 0.	
RESERVED	4	O	Reserved. Returns 0.	
RESERVED	3	O	Reserved. Returns 0.	
ADC_CH11_I	2	O	ADC Channel11 Interrupt	0x0 = ADC Channel11 data has not updated. 0x1 = ADC Channel11 data has updated.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_CH10_I	1	O	ADC Channel10 Interrupt	0x0 = ADC Channel10 data has not updated. 0x1 = ADC Channel10 data has updated.
ADC_CH9_I	0	O	ADC Channel9 Interrupt	0x0 = ADC Channel9 data has not updated. 0x1 = ADC Channel9 data has updated.

ADC_MSK1 (0x82)

BIT	7	6	5	4	3	2	1	0
Field	ADC_CH8_M	ADC_CH7_M	ADC_CH6_M	ADC_CH5_M	ADC_CH4_M	ADC_CH3_M	ADC_CH2_M	ADC_CH1_M
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_CH8_M	7	O	ADC Channel8 Interrupt Mask	0x0 = Enable ADC_CH8_I. 0x1 = Mask ADC_CH8_I.
ADC_CH7_M	6	O	ADC Channel7 Interrupt Mask	0x0 = Enable ADC_CH7_I. 0x1 = Mask ADC_CH7_I.
ADC_CH6_M	5	O	ADC Channel6 Interrupt Mask	0x0 = Enable ADC_CH6_I. 0x1 = Mask ADC_CH6_I.
ADC_CH5_M	4	O	ADC Channel5 Interrupt Mask	0x0 = Enable ADC_CH5_I. 0x1 = Mask ADC_CH5_I.
ADC_CH4_M	3	O	ADC Channel4 Interrupt Mask	0x0 = Enable ADC_CH4_I. 0x1 = Mask ADC_CH4_I.
ADC_CH3_M	2	O	ADC Channel3 Interrupt Mask	0x0 = Enable ADC_CH3_I. 0x1 = Mask ADC_CH3_I.
ADC_CH2_M	1	O	ADC Channel2 Interrupt Mask	0x0 = Enable ADC_CH2_I. 0x1 = Mask ADC_CH2_I.
ADC_CH1_M	0	O	ADC Channel1 Interrupt Mask	0x0 = Enable ADC_CH1_I. 0x1 = Mask ADC_CH1_I.

ADC_MSK2 (0x83)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			RESERVED	RESERVED	ADC_CH11_M	ADC_CH10_M	ADC_CH9_M
Reset	0x7			0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	O	Reserved. Returns 1.	
RESERVED	4	O	Reserved. Returns 1.	
RESERVED	3	O	Reserved. Returns 1.	
ADC_CH11_M	2	O	ADC Channel11 Interrupt Mask	0x0 = Enable ADC_CH11_I. 0x1 = Mask ADC_CH11_I.

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_CH10_M	1	O	ADC Channel10 Interrupt Mask	0x0 = Enable ADC_CH10_I. 0x1 = Mask ADC_CH10_I.
ADC_CH9_M	0	O	ADC Channel9 Interrupt Mask	0x0 = Enable ADC_CH9_I. 0x1 = Mask ADC_CH9_I.

ADC_STAT (0x84)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[3:0]				CH4_IMON_OK	CH3_IMON_OK	CH2_IMON_OK	CH1_IMON_OK
Reset	0x0				0x0	0x0	0x0	0x0
Access Type	Read Only				Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:4	O	Reserved. Returns 0.	
CH4_IMON_OK	3	O	ADC Channel4 Current Monitor Status	0x0 = ADC Channel4 current monitor data is not valid. 0x1 = ADC Channel4 current monitior data is valid.
CH3_IMON_OK	2	O	ADC Channel3 Current Monitor Status	0x0 = ADC Channel3 current monitor data is not valid. 0x1 = ADC Channel3 current monitior data is valid.
CH2_IMON_OK	1	O	ADC Channel2 Current Monitor Status	0x0 = ADC Channel2 current monitor data is not valid. 0x1 = ADC Channel2 current monitior data is valid.
CH1_IMON_OK	0	O	ADC Channel1 Current Monitor Status	0x0 = ADC Channel1 current monitor data is not valid. 0x1 = ADC Channel1 current monitior data is valid.

ADC_DATA_CH1 (0x85)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA1	7:0	O	ADC Channel1 (I_{OUT1}) Data Readback	0x0–0xFF = (-6.69 + 0.0625 x ADC_DATA1)A.

ADC_DATA_CH2 (0x86)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA2[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA 2	7:0	O	ADC Channel2 (I_{OUT2}) Data Readback	0x0–0xFF = (-6.69 + 0.0625 x ADC_DATA2)A.

ADC_DATA_CH3 (0x87)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA3[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA 3	7:0	O	ADC Channel3 (I_{OUT3}) Data Readback	0x0–0xFF = (-6.69 + 0.0625 x ADC_DATA3)A.

ADC_DATA_CH4 (0x88)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA4[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA 4	7:0	O	ADC Channel4 (I_{OUT4}) Data Readback	0x0–0xFF = (-6.69 + 0.0625 x ADC_DATA4)A.

ADC_DATA_CH5 (0x89)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA5[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA5	7:0	O	ADC Channel5 (V_{OUT1}) Data Readback	When M1_RNG = 0x0, 0x0–0xFF = (0.00625 x ADC_DATA5)V. When M1_RNG = 0x1, 0x0–0xFF = (0.0125 x ADC_DATA5)V. When M1_RNG = 0x2, 0x0–0xFF = (0.025 x ADC_DATA5)V.

ADC_DATA_CH6 (0x8A)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA6[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA6	7:0	O	ADC Channel6 (V_{OUT2}) Data Readback	When M2_RNG = 0x0, 0x0–0xFF = (0.00625 x ADC_DATA6)V. When M2_RNG = 0x1, 0x0–0xFF = (0.0125 x ADC_DATA6)V. When M2_RNG = 0x2, 0x0–0xFF = (0.025 x ADC_DATA6)V.

ADC_DATA_CH7 (0x8B)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA7[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA7	7:0	O	ADC Channel7 (V_{OUT3}) Data Readback	When M3_RNG = 0x0, 0x0–0xFF = (0.00625 x ADC_DATA7)V. When M3_RNG = 0x1, 0x0–0xFF = (0.0125 x ADC_DATA7)V. When M3_RNG = 0x2, 0x0–0xFF = (0.025 x ADC_DATA7)V.

ADC_DATA_CH8 (0x8C)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA8[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA8	7:0	O	ADC Channel8 (V_{OUT4}) Data Readback	When M4_RNG = 0x0, 0x0–0xFF = (0.00625 x ADC_DATA8)V. When M4_RNG = 0x1, 0x0–0xFF = (0.0125 x ADC_DATA8)V. When M4_RNG = 0x2, 0x0–0xFF = (0.025 x ADC_DATA8)V.

ADC_DATA_CH9 (0x8D)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA9[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA9	7:0	O	ADC Channel9 (V_{SYS}) Data Readback	When SYS_RNG = 0x0, 0x0–0xFF = (0.025 x ADC_DATA9)V. When SYS_RNG = 0x1, 0x0–0xFF = (0.075 x ADC_DATA9)V.

ADC_DATA_CH10 (0x8E)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA10[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA10	7:0	O	ADC Channel10 (Junction Temperature) Data Readback	0x0–0xFF = (-273 + 1.725 x ADC_DATA10)°C.

ADC_DATA_CH11 (0x8F)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA11[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
ADC_DATA11	7:0	O	ADC Channel11 (V_{MFIO}) Data Readback	0x0–0xFF = (0.0046875 x ADC_DATA11)V.

ADC_CFG1 (0x92)

BIT	7	6	5	4	3	2	1	0
Field	CH8_EN	CH7_EN	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
CH8_EN	7	O	ADC Channel8 Data Readback Control	0x0 = Disable. 0x1 = Enable.
CH7_EN	6	O	ADC Channel7 Data Readback Control	0x0 = Disable. 0x1 = Enable.
CH6_EN	5	O	ADC Channel6 Data Readback Control	0x0 = Disable. 0x1 = Enable.
CH5_EN	4	O	ADC Channel5 Data Readback Control	0x0 = Disable. 0x1 = Enable.
CH4_EN	3	O	ADC Channel4 Data Readback Control	0x0 = Disable. 0x1 = Enable.
CH3_EN	2	O	ADC Channel3 Data Readback Control	0x0 = Disable. 0x1 = Enable.
CH2_EN	1	O	ADC Channel2 Data Readback Control	0x0 = Disable. 0x1 = Enable.
CH1_EN	0	O	ADC Channel1 Data Readback Control	0x0 = Disable. 0x1 = Enable.

ADC_CFG2 (0x93)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			RESERVED	RESERVED	CH11_EN	CH10_EN	CH9_EN
Reset	0x0			0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	O	Reserved. Returns 0.	
RESERVED	4	O	Reserved. Returns 0.	
RESERVED	3	O	Reserved. Returns 0.	
CH11_EN	2	O	ADC Channel11 Data Readback Control	0x0 = Disable. 0x1 = Enable.
CH10_EN	1	O	ADC Channel10 Data Readback Control	0x0 = Disable. 0x1 = Enable.
CH9_EN	0	O	ADC Channel9 Data Readback Control	0x0 = Disable. 0x1 = Enable.

ADC_CFG3 (0x94)

BIT	7	6	5	4	3	2	1	0
Field	CH8_AVG	CH7_AVG	CH6_AVG	CH5_AVG	CH4_AVG	CH3_AVG	CH2_AVG	CH1_AVG
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
CH8_AVG	7	O	ADC Channel8 Data Averaging Control	0x0 = Disable. 0x1 = Enable.
CH7_AVG	6	O	ADC Channel7 Data Averaging Control	0x0 = Disable. 0x1 = Enable.
CH6_AVG	5	O	ADC Channel6 Data Averaging Control	0x0 = Disable. 0x1 = Enable.
CH5_AVG	4	O	ADC Channel5 Data Averaging Control	0x0 = Disable. 0x1 = Enable.
CH4_AVG	3	O	ADC Channel4 Data Averaging Control	0x0 = Disable. 0x1 = Enable.
CH3_AVG	2	O	ADC Channel3 Data Averaging Control	0x0 = Disable. 0x1 = Enable.
CH2_AVG	1	O	ADC Channel2 Data Averaging Control	0x0 = Disable. 0x1 = Enable.
CH1_AVG	0	O	ADC Channel1 Data Averaging Control	0x0 = Disable. 0x1 = Enable.

ADC_CFG4 (0x95)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			RESERVED	RESERVED	CH11_AVG	CH10_AVG	CH9_AVG
Reset	0x0			0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:5	O	Reserved. Returns 0.	
RESERVED	4	O	Reserved. Returns 0.	
RESERVED	3	O	Reserved. Returns 0.	
CH11_AVG	2	O	ADC Channel11 Data Averaging Control	0x0 = Disable. 0x1 = Enable.
CH10_AVG	1	O	ADC Channel10 Data Averaging Control	0x0 = Disable. 0x1 = Enable.
CH9_AVG	0	O	ADC Channel9 Data Averaging Control	0x0 = Disable. 0x1 = Enable.

ADC_CFG5 (0x96)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		SYS_RNG	RESERVED	AVG_CNT[1:0]		MEAS_C	MEAS_S
Reset	0x0		0x0	0x0	0x0		0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	TYPE	DESCRIPTION	DECODE
RESERVED	7:6	O	Reserved. Returns 0.	
SYS_RNG	5	O	ADC Channel9 SYS Voltage Measurement Range Setting	0x0 = 2.0V to 6.08V with 16mV LSB. 0x1 = 2.0V to 18.32V with 64mV LSB.
RESERVED	4	O	Reserved. Returns 0.	
AVG_CNT	3:2	O	ADC Averaging Count Setting	0x0 = 2 points. 0x1 = 4 points. 0x2 = 8 points. 0x3 = 16 points.
MEAS_C	1	O	ADC Continuous Measurement Control	0x0 = Disable. 0x1 = Enable (update ADC readback every second).
MEAS_S	0	O	ADC Single Measurement Control	0x0 = Disable. 0x1 = Enable (this bit is ignored when MEAS_C = 1).

Applications Information—Quad-Phase Configurable Buck Converter

Inductor Selection

An inductor with a saturation current that is greater than or equal to the peak current limit setting (I_{PLIM}) is recommended. The load current requirement (per phase) of the system is also a consideration when choosing the RMS current rating of the inductor. Inductors with lower saturation current and higher DCR ratings tend to be physically small. However, higher values of DCR reduce the efficiency. To choose a suitable inductor for the given application, consider the trade-off between the size of the inductor versus the DCR value. It is recommended to choose an inductance so that the ratio of the inductor's ripple current to the average current is between 30% and 60%.

Consider the output-voltage range and switching frequency when choosing the inductance. In general, 0.47µH is suitable for low-range outputs with 1.0MHz or 1.5MHz switching frequency. For mid-range and high-range outputs, 1.0µH–1.5µH is recommended. Note that higher inductances slow down the maximum slew rate of the inductor current, and high-duty cycles (V_{IN} close to V_{OUT}) coupled with large inductance can slow down the load transient response.

Table 19. Recommended Inductors

MANUFACTURER PART NUMBER	INDUCTANCE (µH)	TYPICAL DCR (mΩ)	TYPICAL I_{SAT} (A)	TYPICAL I_{TEMP} (A)	DIMENSION (L x W x H) (mm)
DFE252012F-R47M	0.47 ±20%	23	6.7	4.9	2.5 x 2.0 x 1.2
DFE252012F-1R0M	1.0 ±20%	40	4.7	3.3	2.5 x 2.0 x 1.2
XEL4020-152ME	1.5 ±20%	21.45	7.4	5.2	4.0 x 4.0 x 3.25

For multiphase configurations, each phase on the same output needs its own inductor with the same inductance value (do not short the LX nodes of different phases together on the PCB). See the *Phase and Output Configuration* section for more information regarding different phase configurations.

Input-Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the battery or the input power source and reduces switching noise in the device. The impedance of the C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

Output-Capacitor Selection

The output-capacitor (C_{OUT}) is required to keep the output-voltage ripple small and to ensure regulation loop stability. The C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. The recommended minimum effective output capacitance per phase is shown in Table 20.

Table 20. Recommended Minimum Effective Output Capacitance

V_{OUT} RANGE	SWITCHING FREQUENCY	MINIMUM EFFECTIVE C_{OUT}*
Low (0.3V to 1.3V)	1MHz	42µF
Mid (0.6V to 2.6V)	1MHz	24µF
High (1.2V to 5.2V)	1MHz	16µF

*Required minimum $C_{OUT(EFF)}$ is inversely proportional to the switching frequency setting. For example, a buck output using Mx_RNG = 0x0 and 1MHz switching frequency requires 42µF of minimum effective output capacitance. Changing the switching frequency to 1.5MHz decreases the effective output capacitance requirement to 28µF (= 42µF/1.5).

The effective C_{OUT} is the actual capacitance value seen by the buck output during operation. The nominal capacitance (C_{OUT}) needs to be selected carefully by considering the capacitor's initial tolerance, variation with temperature, and derating with DC bias. Refer to *Tutorial 5527* for more information. Larger values of the C_{OUT} (above the required minimum effective) improve load transient performance, but increase the input inrush currents during startup. The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance

must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple in continuous conduction mode. Therefore, the size of the output capacitor depends on the maximum ESR required to meet the output-voltage ripple specifications.

General PCB Layout Guidelines

- The power components should be placed first followed by the small analog control signals (see Figure 15).
- It is important to always have a ground layer next to the power stage layer because a solid ground layer provides an uninterrupted ground return path between the input and the output capacitors during switch on-time (a solid plane minimizes inductance to the absolute minimum and is also a very good thermal conductor that can act as a heat sink).
- Thick copper is recommended for the external high current power layers to minimize the PCB conduction loss and thermal impedance.
- The power stage loop that is made by the input capacitor (C_{IN}), the LX trace, the inductor (L), and the output capacitor (C_{OUT}) coming back to the PGNDx pins should be minimized in consideration of EMC.
- The input capacitors (C_{IN}) should be located close to the input pins of each phase.
- Bypass capacitors for the V_{DD}, the V_{L12}, the V_{L34}, and the BSTx pins should be placed as close as possible.
- Analog ground (AGND) and power ground (PGND) pins should be directly connected to the ground plane separately to avoid common impedance ground.
- It is recommended to avoid a direct connection of the SYS and its AGND traces to the nearest IN and the PGND traces
- The output-voltage sensing trace should not intersect the power stage (the loop made by the LX trace, inductor, output capacitor and the PGND).
- It is important to have impedance matching between phases for stable operation in multiphase configuration (the output PCB trace of each phase should be as symmetric as possible).
- For multiphase configurations, the output-voltage sensing pins for the master phase should be connected to the middle point of the output phases.

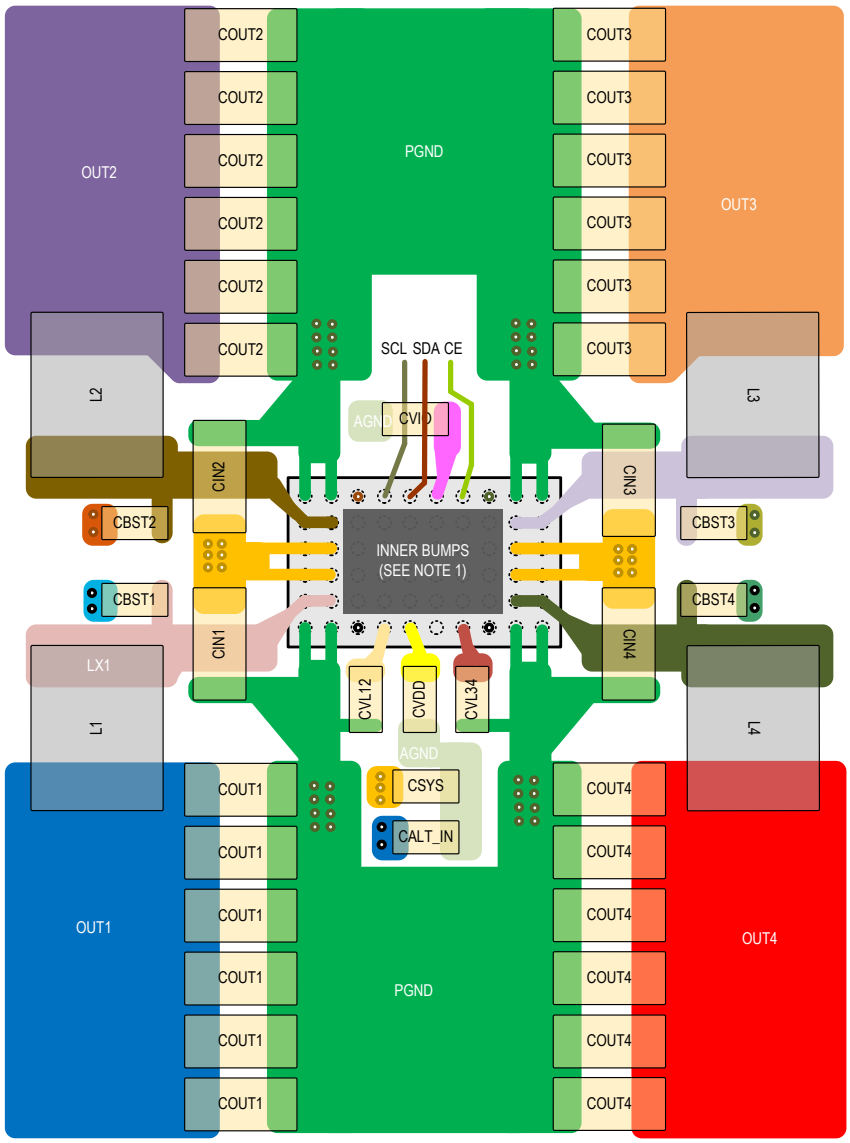


Figure 15. PCB Layout Example

Unused Outputs

When an application has unused buck outputs, follow the guidelines below:

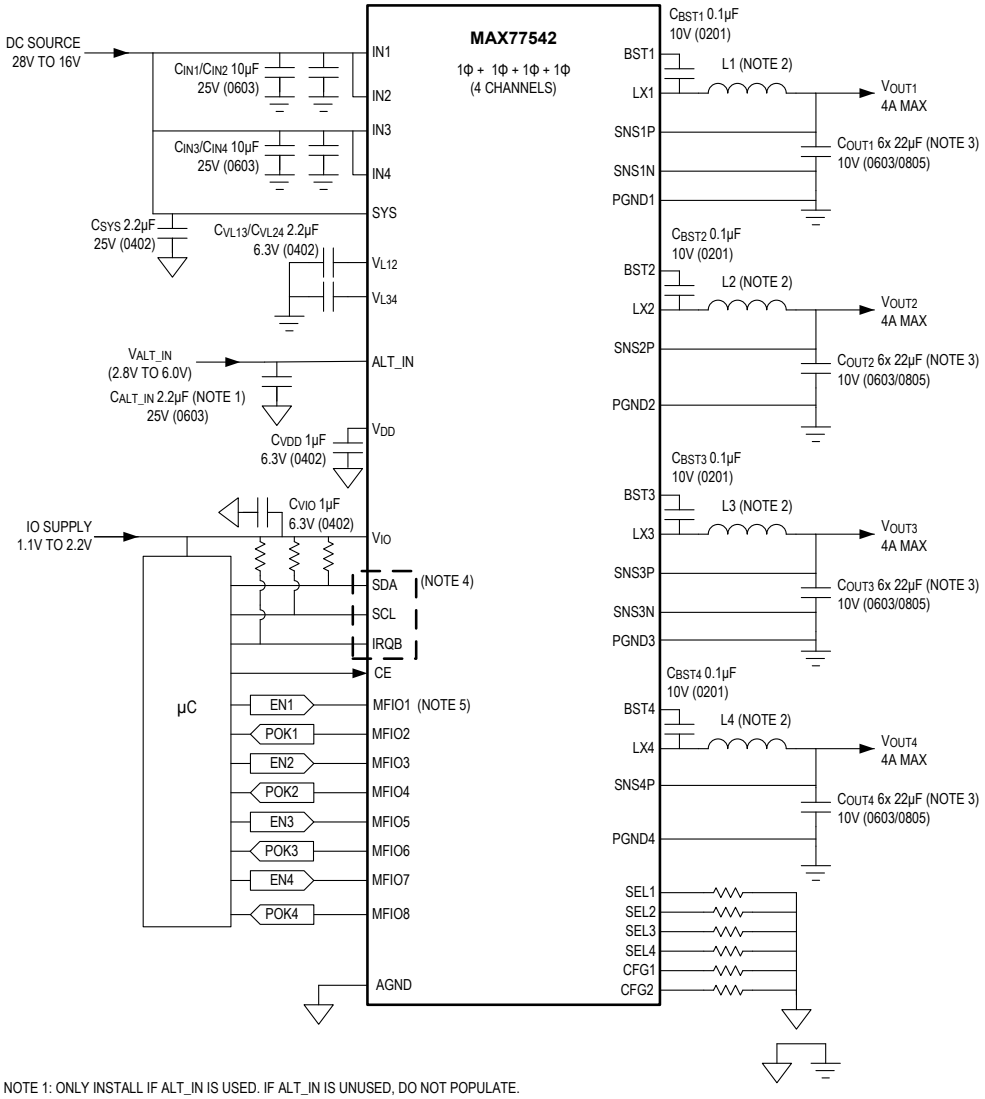
- Connect the unused inputs (INx) to the SYS.
- Leave the unused LXx and the BSTx pins unconnected (open).
- Connect the unused SNSxP and SNSxN inputs to ground (AGND).
- Connect the PGNDx pins to ground.
- Do not enable the unused buck outputs.

The slave phases configured under master controllers must be connected according to Table 6. If an unused buck output

(following the guidelines above) is enabled, a fault state latches (Mx_SCFLT = 1). Disabling the corresponding buck clears the fault state (see Figure 12).

Typical Application Circuits

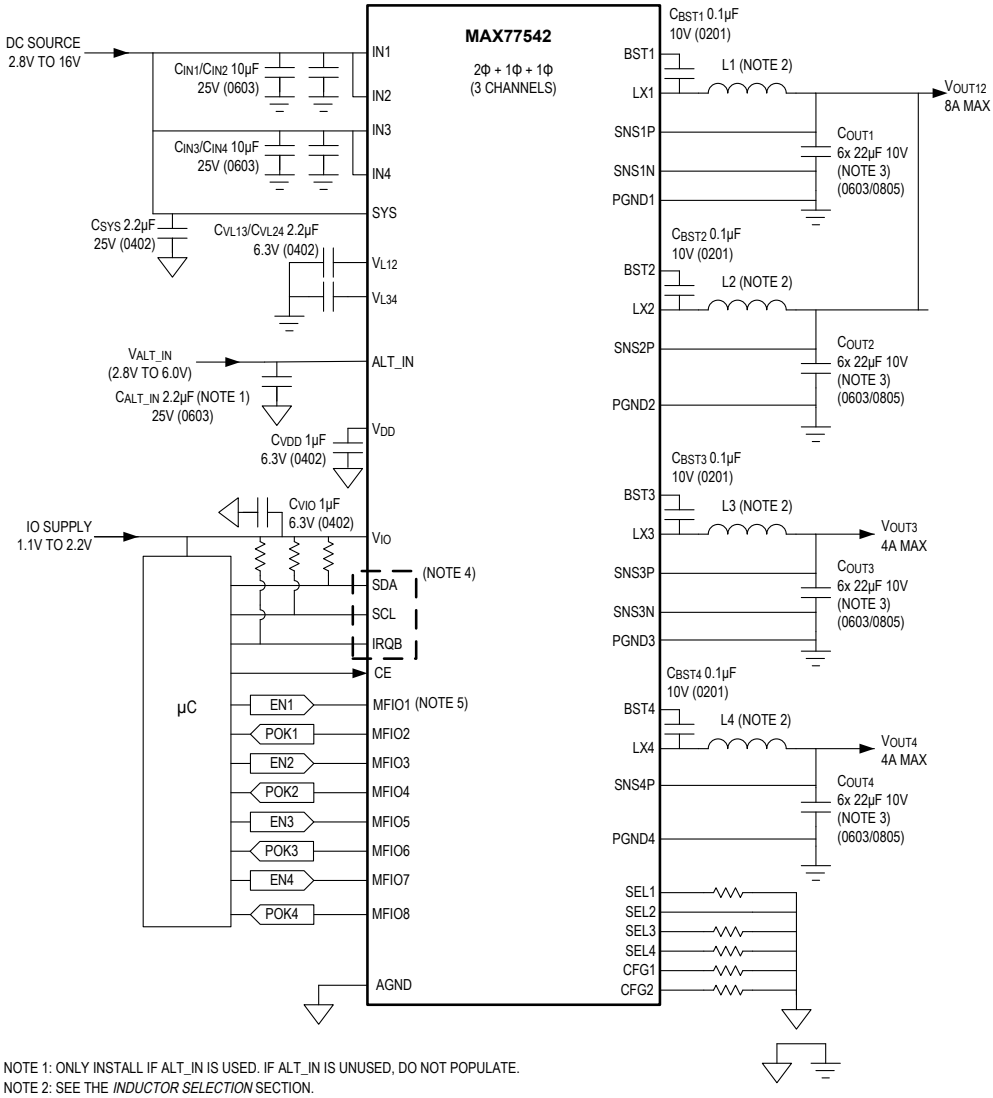
1+1+1+1 Phase Configuration



NOTE 1: ONLY INSTALL IF ALT_IN IS USED. IF ALT_IN IS UNUSED, DO NOT POPULATE.
NOTE 2: SEE THE *INDUCTOR SELECTION* SECTION.
NOTE 3: SEE THE *OUTPUT CAPACITOR SELECTION* SECTION.
NOTE 4: CONNECT IRQB, SDA, AND SCL TO AGND WHEN UNUSED.
NOTE 5: EXAMPLE MFIO FUNCTION MAP. RECONFIGURABLE USING I^2C OR CFG1. SEE THE *MFIO FUNCTIONS* SECTION.

Typical Application Circuits (continued)

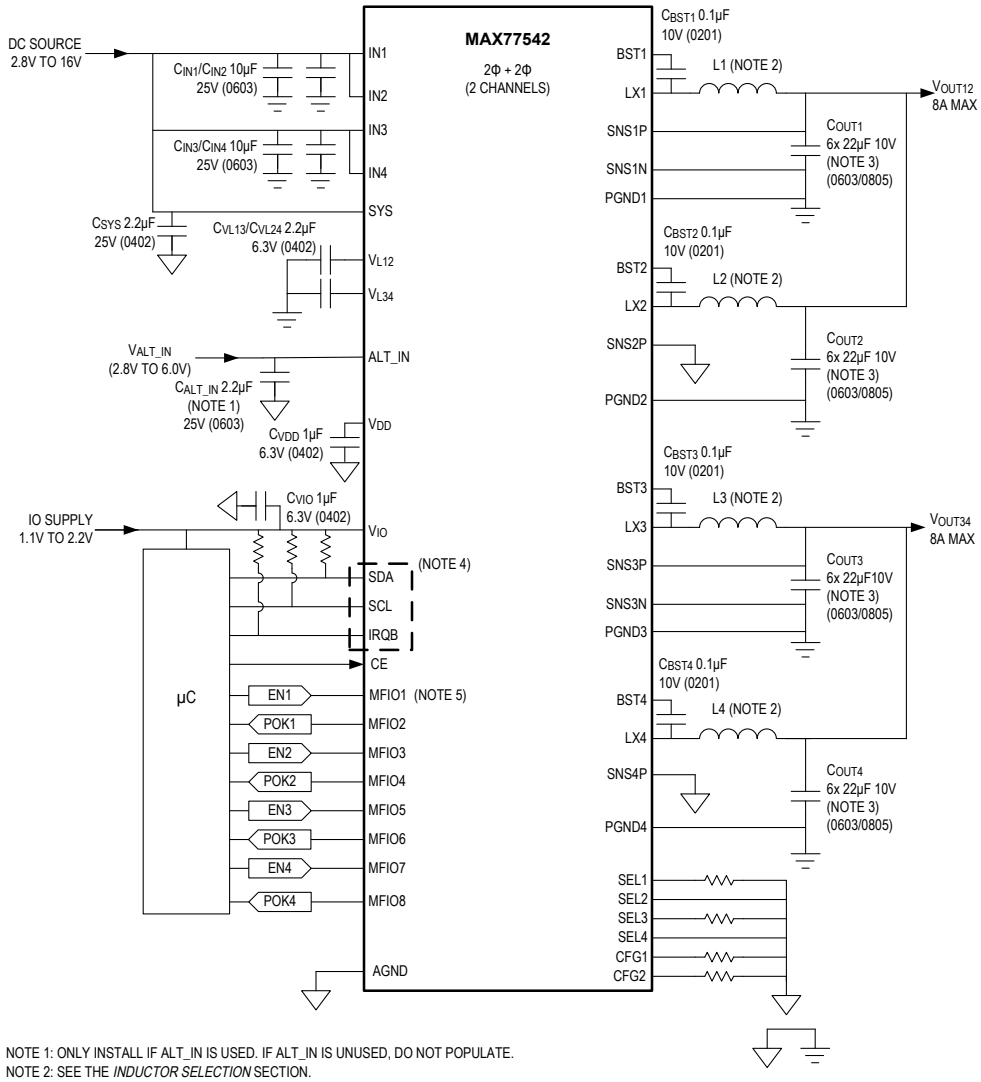
2+1+1 Phase Configuration



NOTE 1: ONLY INSTALL IF ALT_IN IS USED. IF ALT_IN IS UNUSED, DO NOT POPULATE.
NOTE 2: SEE THE *INDUCTOR SELECTION* SECTION.
NOTE 3: SEE THE *OUTPUT CAPACITOR SELECTION* SECTION.
NOTE 4: CONNECT IRQB, SDA, AND SCL TO AGND WHEN UNUSED.
NOTE 5: EXAMPLE MFIO FUNCTION MAP. RECONFIGURABLE USING I^2C OR CFG1. SEE THE *MFIO FUNCTIONS* SECTION.

Typical Application Circuits (continued)

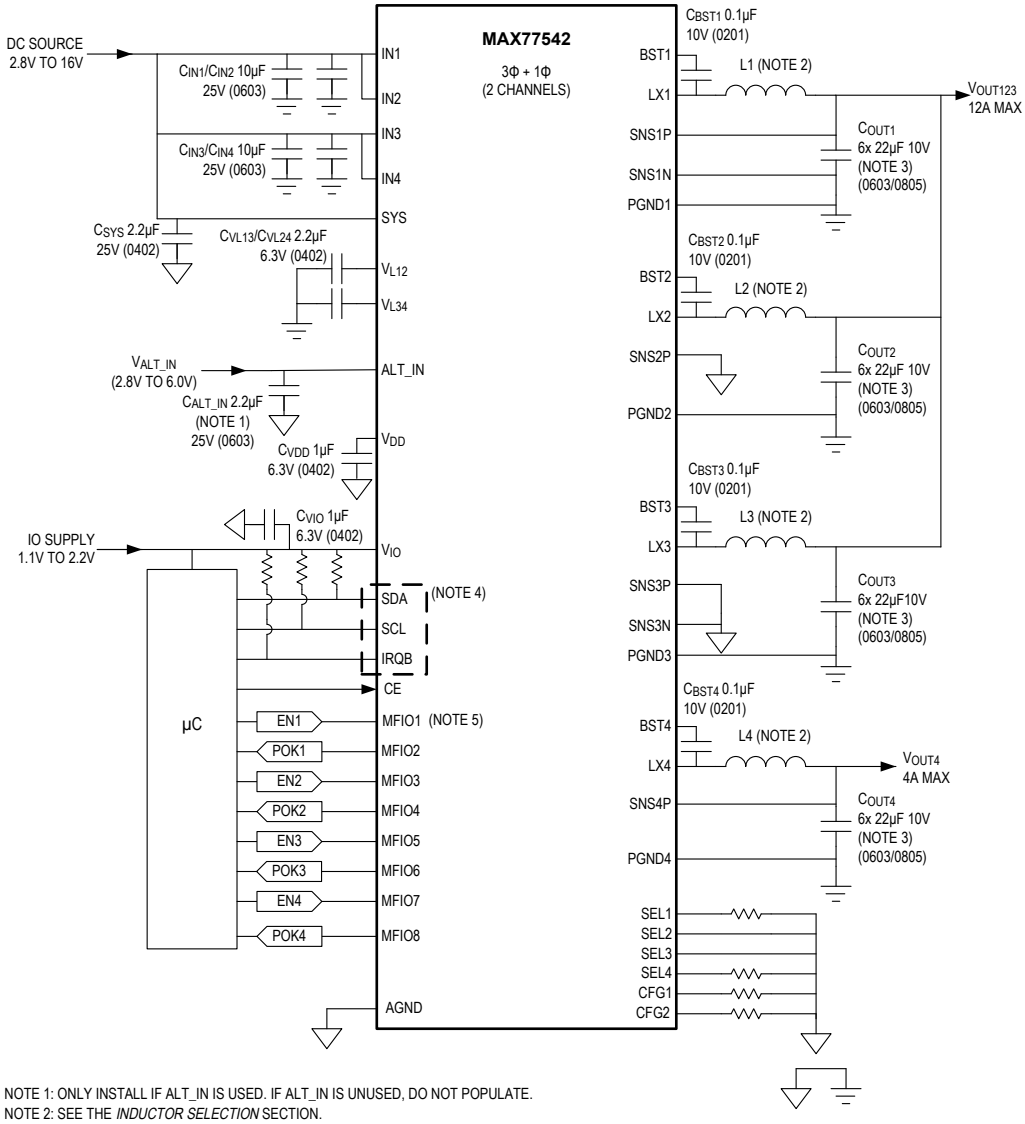
2+2 Phase Configuration



NOTE 1: ONLY INSTALL IF ALT_IN IS USED. IF ALT_IN IS UNUSED, DO NOT POPULATE.
NOTE 2: SEE THE *INDUCTOR SELECTION* SECTION.
NOTE 3: SEE THE *OUTPUT CAPACITOR SELECTION* SECTION.
NOTE 4: CONNECT IRQB, SDA, AND SCL TO AGND WHEN UNUSED.
NOTE 5: EXAMPLE MFIO FUNCTION MAP. RECONFIGURABLE USING I^2C OR CFG1. SEE THE *MFIO FUNCTIONS* SECTION.

Typical Application Circuits (continued)

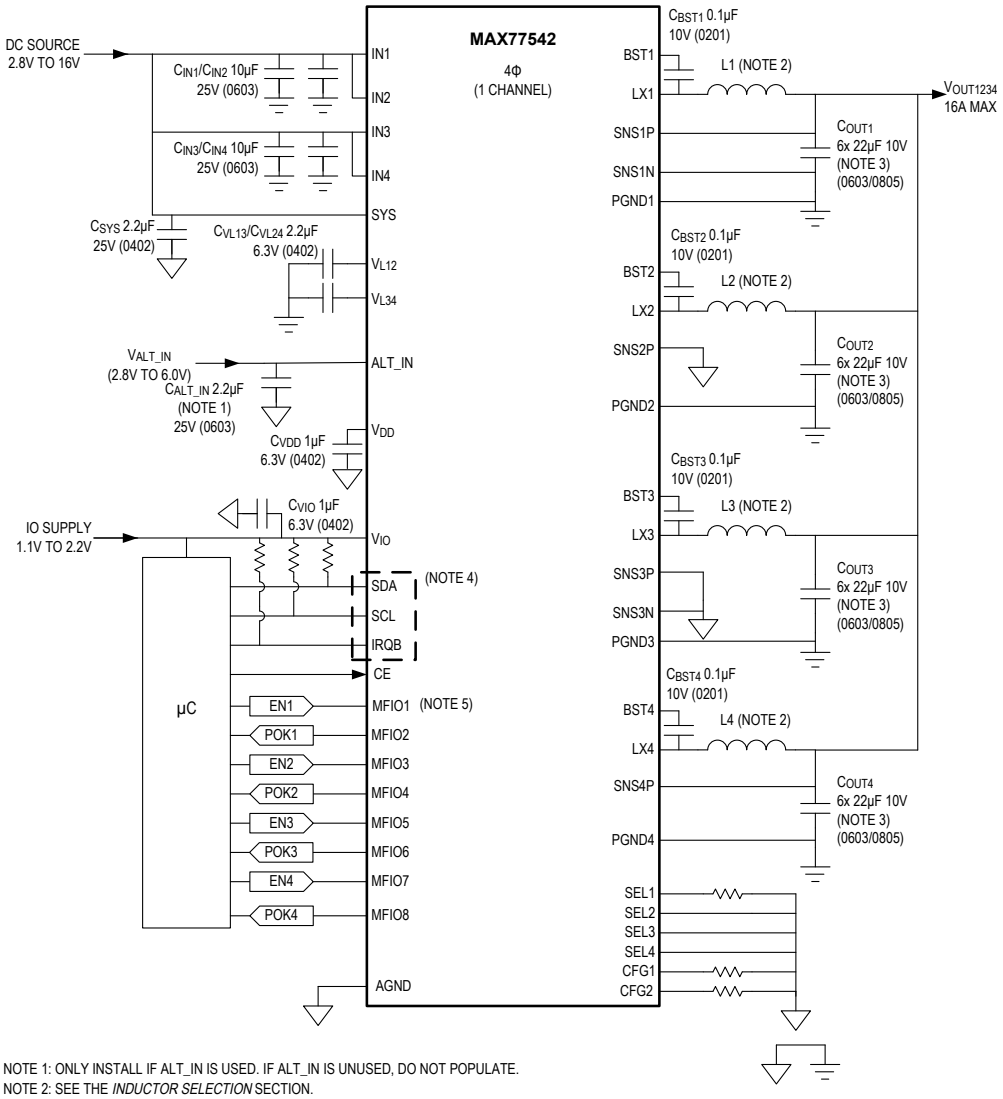
3+1 Phase Configuration



NOTE 1: ONLY INSTALL IF ALT_IN IS USED. IF ALT_IN IS UNUSED, DO NOT POPULATE.
NOTE 2: SEE THE *INDUCTOR SELECTION* SECTION.
NOTE 3: SEE *OUTPUT CAPACITOR SELECTION* SECTION.
NOTE 4: CONNECT IRQB, SDA, AND SCL TO AGND WHEN UNUSED.
NOTE 5: EXAMPLE MFIO FUNCTION MAP. RECONFIGURABLE USING I^2C OR CFG1. SEE THE *MFIO FUNCTIONS* SECTION.

Typical Application Circuits (continued)

4 Phase Configuration



NOTE 1: ONLY INSTALL IF ALT_IN IS USED. IF ALT_IN IS UNUSED, DO NOT POPULATE.
NOTE 2: SEE THE *INDUCTOR SELECTION* SECTION.
NOTE 3: SEE THE *OUTPUT CAPACITOR SELECTION* SECTION.
NOTE 4: CONNECT IRQB, SDA, AND SCL TO AGND WHEN UNUSED.
NOTE 5: EXAMPLE MFIO FUNCTION MAP. RECONFIGURABLE USING I^2C OR CFG1. SEE THE *MFIO FUNCTIONS SECTION.*

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX77542AAWU+T	-40°C to +125°C	60 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/23	Initial release	—
1	5/23	Updated Typical Operating Characteristics section. Updated ADC CONFIGURATION, M1_VOUT_M (0x26), M1_CFG5 (0x2B), M2_VOUT_M (0x36), M2_CFG5 (0x3B), M3_VOUT_M (0x46), M3_CFG5 (0x4B), M4_VOUT_M (0x56), M4_CFG5 (0x5B), ADC_INT2 (0x81), ADC_MSK2 (0x83), ADC_CFG2 (0x93), and ADC_CFG4 (0x95) tables in the Register Map section and Output-Capacitor Selection section.	27, 63, 77, 80, 81, 84, 86, 89, 90, 93, 105, 106, 111, 112, 114