MAX9295D DEV_REV=8 (D-0C) ERRATA SHEET

Corresponds to data sheet 19-100518; Rev6; 11/23

DEV_REV=8 (per reading register 0xE)

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the topside of the package with a four-digit code in the form yyww, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. The revision of these components can be found by reading DEV_REV=8 from register 0xE.

1) UART - The most significant 8 bits of the 16-bit register address cannot change during an auto incremented access

Description:
Any UART transaction that attempts to read or write in an auto incremented access cannot result in the most significant 8 bits of the address register being changed. If the 8 most significant bits are incremented during the access the access will fail. For example, if a read starts at 250 and ends at 260. Since it crossed 255, it fails.

Workaround:
None

Resolution:
No silicon fix currently planned.

2) Spread Spectrum amplitude must be programmed only when video input is active. GMSL1 mode.

Description:
The GMSL1 Link PLL has spread spectrum capability. This feature is enabled using the SSEN register bitfield and by default the spread spectrum percentage is 0.5%. When the user desires to program the spread spectrum value to any other value, the register bit field with name config_spread_bit_ratio at address x1B03 is programmed. Desired behavior would have been to program this bitfield after power up and not require any additional steps afterwards. However, actual behavior requires that the bitfield is programmed after the video input starts and each time the video input stops and restarts. The issue arises from automatic reset of PLL registers when video input is off and due to a handshake mechanism inside the PLL which requires the register to be rewritten even if the register value is correct every time the PLL enable is toggled.

Workaround:
This bitfield must be programmed after the video input starts and each time the video input stops and restarts.

Resolution:
No silicon fix currently planned.

3) GPIO pin glitch

Description:
If VDDIO is brought up before VDD18 there is a potential for a signal glitch on any GPIO pin.

When VDD18 turns on and reaches its final value at the same time or before VDDIO does, the initial state of the outputs is successfully reset by the power manager and the GPIO pins go into a Hi-Z state. This is normal operation. If VDDIO is brought up first, however, the power manager is off, and the IO may not reset and could be in an unknown state, such as an active pullup state, and a pin could output a logic 1 for several ms.

In addition to this, a glitch can also occur in GPIO pins when reset_oneshot is applied during normal operation. If reset_oneshot is applied when transmit operation is enabled on a GPIO and output is driven high, then a glitch (low) happens on GPIO output.

Workaround: (For the glitch issue due to VDDIO before VDD18):
Insure that VDD18 turns on and reaches its final value at the same time or before VDDIO does.

Workaround: (For the glitch issue due to reset_oneshot):
Disable GPIO Tx paths by writing GPIO_TX_EN = 0 before applying RESET_ONESHOT

Resolution:
Planned to be fixed in the next revision**.**

4) Watermark error not latched

Description:
Watermark error register is cleared when read. However, if the error persists when the register is read, the error is not latched again.

Workaround:
Read the WM_ERR register after reading the interrupt to check if the error persists.

Resolution:
No silicon fix currently planned.

5) I2C timeout status bits are not latched

Description:
The “I2C_TIMED_OUT” status bit, at register address 0x47, is intended to indicate when an I2C transaction has hung and has exceeded the timeout threshold. However, the status indicator is not latched and will automatically clear immediately following assertion. The immediate clearing of the status makes this status indicator essentially unusable.

Workaround:
With a robust I2C interface, a timeout event should generally not occur. As an alternate method of validating proper I2C transactions, the master I2C device should always observe and respond appropriately to the presence or absence of I2C acknowledge (ACK) indicators.

Resolution:
No silicon fix currently planned.

6) Termination resistor for unused GMSL2 output in coax mode should be 49.9Ω 1%.

Description:
In the “Typical GMSL1/2 Link Application Circuit for Coax Cable” figure, the termination resistor for the SION pin is indicated as 51Ohm. While the value of this resistor is not critical, all characterization was done with a 49.9Ohm resistor. Maxim recommends that a 49.9Ohm, 1% resistor be used.

Workaround:
In future builds use 49.9Ohm, 1% resistors in termination resistor locations for coax applications.

Resolution:
Data sheet ECN is planned.

7) Functional problems with GPIO TX cascade mode

Description:
By default, multiple GPIO toggles (transitions) can be sent in a series in cascading GPIO toggles within the same GMSL packet. Disabling this behavior, forcing each toggle to be sent in a separate GMSL packet, can cause unreliable GPIO transmission across the GMSL link. Due to this issue, the GPIO TX cascade mode should be left enabled.

Workaround:
Leave the bit-field in it’s default state: GPIO_TX_CASC=1.

Resolution:
Planned to be fixed in a future revision.

8) Lock time typical spec is incorrect.

Description:
Data sheet indicates typical GMSL2 Lock Time as 20ms. It should be 25ms.

Workaround:
None required.

Resolution:
Data sheet ECN is planned.

9) GPIO values received are not retained in sleep mode

Description:
When GPIO values are received from the other side of the link, they are not retained when going to sleep mode. This is because the GPIO logic is incorrectly put in reset before the received values can be retained in the retention memory.

Workaround:
There are several options. The first is to not use sleep mode. The second is to ensure the GPIO is set to a static value before entering sleep mode. This can be done by disabling GPIO receiving (GPIO_RX_EN = 0) and set the GPIO output value in the GPIO_OUT bit.

Resolution:
No silicon fix currently planned.

10) UART permanent bypass mode can disable access to main control channel if link lock is lost

Description:
When UART permanent bypass mode is programmed, access to the main control channel for programming of peripherals may be lost if link lock is lost, even after lock is restored. The device must be power cycled to enable access to the main control channel.

Workaround:
Do not use permanent bypass mode in register BYPASS_TO.

Resolution:
Data sheet ECN is planned.

11) After executing Sleep/Wake sequence, RESET_ALL puts part into Sleep state.

Description:
After a Sleep/Wake sequence has been executed, writing RESET_ALL=1 will put the part into Sleep state and this will cause the part not being fully reset to its POR values. The part can be woken up using the standard local or remote Wake commands. However, after the Wake sequence, the part will be in the state stored in the retention memory during the previous Sleep command instead of being reset to its POR settings. Registers not stored in retention memory will not be affected by this and will be reset to the POR values.

Workaround:
PWDNB pin can be used to fully reset the part and restore all registers to their POR settings.

Resolution:
No silicon fix is planned.

12) GMSL Lock can be lost due to high jitter in a temperature window

Description:
An internal voltage regulator requires a register write to increase its output voltage to avoid excessive jitter on the GMSL link. This jitter can lead to loss of GMSL lock.

Workaround:
Perform the register write below.

Register: 0x302
Write Data: 0x10
Bit(s): PFDDIV_RSHORT[2:0]
Purpose: Increase regulator voltage to the clock system to ensure robust operation

Resolution
No silicon fix is planned.

13) 4.5Gbps GMSL1 data rate not supported

Description:
GMSL1 devices support data rates of up to 3.12Gbps. GMSL2 devices with GMSL1 back-compatibility are capable of 4.5Gbps in GMSL1 mode. However, this capability has not been validated with all combinations of GMSL2 parts which support the feature. No customers are using this capability, so the GMSL1 speed will be limited to 3.12Gbps in the data sheet.

Workaround:
Use the GMSL1 back-compatible feature only up to 3.12Gbps.

Resolution:
Data sheet ECN is planned.

14) When SER device is in GMSL1+UART mode and DES device is in GMSL2 mode, glitches occur on CC pins of the SER device.

Description:
When SER device is in GMSL1+UART mode and DES device is in GMSL2 mode, glitches occur on CC pins of the SER device which can prevent local ECU to access SER using UART. This issue does not exist in I2C mode.
The problem is due to wake patterns sent in reverse channel by the GMSL2 DES, as a part of lock procedure.

Workaround:
For GMSL2 to GMSL2 target configuration:

- Disable REVCCEN (in 0x0404) on SER immediately after power up to disable GMSL1 reverse control channel.
- Alternatively, delay power-up of DES device until SER device is programmed.

For GMSL1 to GMSL1 target configuration:

- Disable REVCCEN (in 0x0404) on SER immediately after power up to disable reverse control channel and re-enable after programming of DES is completed.
- Alternatively, power-up DES in GMSL1 mode or power-up SER in GMSL2 mode and delay switching of SER device to GMSL1 mode until DES device is switched to GMSL1 mode.

Resolution:
No design change planned.

15) ADC has systematic gain error when used with input divider in /2, /3 or /4 Mode and when monitoring internal supplies

Description:
The input dividers in front of the on-board ADC have small systematic deviations from the ideal values /2, /3 and /4 that are used to monitor voltages higher than the reference voltage for the ADC. The deviations from the ideal divide ratios 2, 3 and 4 depend on selected divide ratio and selected ADC input.

Workaround:
When monitoring external voltages, use the following divide ratios in calculating ADC output code

	Divide Ratio		
ADC Input	**/2 Mode**	**/3 Mode**	**/4 Mode**
ADC0	2.011	3.010	4.011
ADC1	2.046	3.079	4.118
ADC2	2.046	3.079	4.118

When monitoring internal supply voltage rails, use the following divide ratios in calculating ADC output code

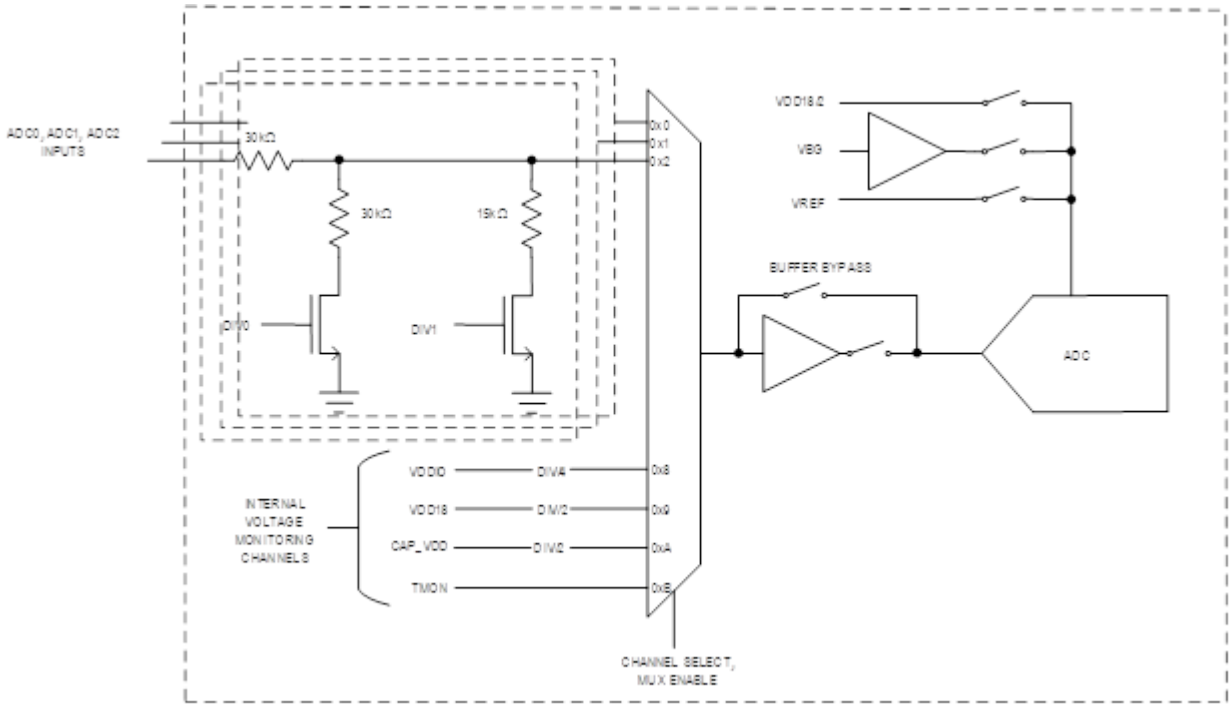
Monitored Voltage Rail	**Divide Ratio**
VDDIO/4	4.013
VDD18/2	2.016
CAP_VDD/2	2.009

Resolution:
Data sheet ECN is planned.

16) ADC input Multiplexer is incorrectly documented in data sheet

Description:
Input 0xA of the ADC input multiplexer (register 0x501, bits [7..4]) should be described as CAP_VDD, not VDD in data sheet figure 32. The ADC input multiplexer is incorrectly documented in data sheet

Workaround:
Use register definition is update in table below.



Resolution:
Data sheet ECN is planned.

17) ADC registers incorrectly documented in data sheet

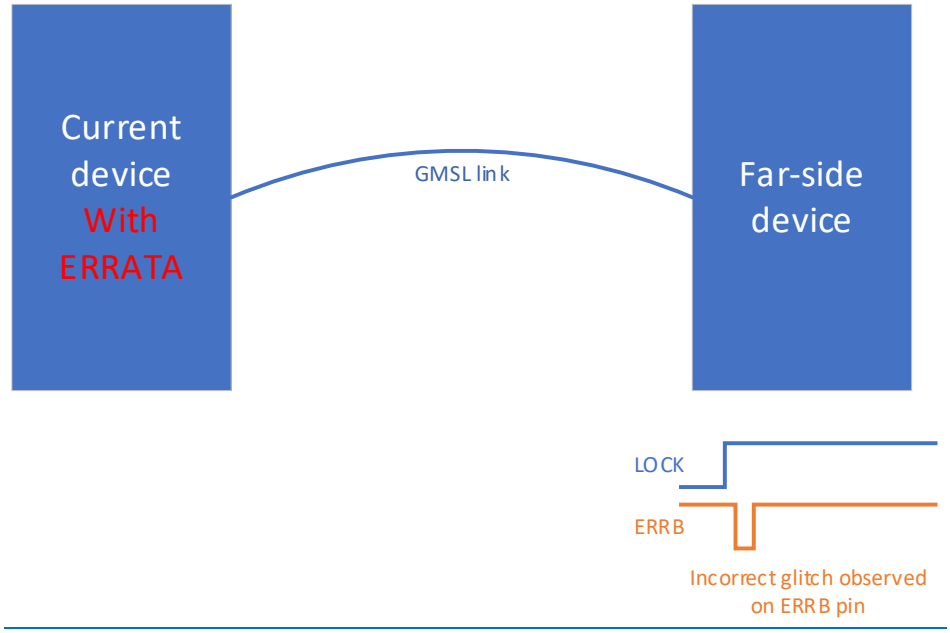
Description:
If REM_ERR_OEN is enabled on far-side device before link lock, there will be a ~1us glitch on far-side ERRB upon link lock if there are no errors on both sides of the link.

Workaround:
Enable REM_ERR_OEN on far-side device only after link lock. If REM_ERR_OEN on far-side device is 1 before link lock:

If SOC is on far-side device:
1. Disable ERR_RX_EN local before link lock
2. Wait for link lock
3. Disable ERR_TX_EN remote
4. Enable ERR_RX_EN local
5. Enable ERR_TX_EN remote

If SOC is on current device:
Disable ERR_TX_EN local before link is down
Wait for link lock
1. Disable ERR_RX_EN remote
2. Enable ERR_TX_EN local
3. Enable ERR_RX_EN remote
4. Disable ERR_TX_EN local
5. Enable ERR_TX_EN local

MAX9295D
ERRATA SHEET



Resolution:
No silicon fix is planned.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/21	Initial release	—
1	4/24	Updated front page, added errata item 15, 16, 17	1, 6, 7, 8

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