

SCOPE: CMOS HIGH SPEED 8-BIT A/D CONVERTER WITH MULTIPLEXER AND REFERENCE

<u>Device Type</u>	<u>Generic Number</u>
01	MAX154AM(x)/883B
02	MAX154BM(x)/883B
03	MAX158AM(x)/883B
04	MAX158BM(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
RG	GDIP1-T24 or CDIP2-T24	24 LEAD Cerdip	J24
JI	GDIP1-T28 or CDIP2-T28	28 LEAD Cerdip	J28

Absolute Maximum Ratings:

V _{DD} to GND	0V, +10V
Digital Input Voltage to GND _____ (RD, CS, A0, A1, A2)	-0.3V, V _{DD}
Digital Output Voltage to GND _____ (D0-D7, RDY, INT).....	-0.3V, V _{DD}
Output Current (REF _{OUT})	30mA
Analog Input (any channel)	-0.3V, V _{DD}
Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature	-65°C to +150°C
Continuous Power Dissipation	T _A =+70°C
24 pin Cerdip(derate 12.5mW/°C above +70°C)	1000mW
28 pin Cerdip(derate 16.7mW/°C above +70°C)	1333mW
Junction Temperature T _J	+150°C
Thermal Resistance, Junction to Case, θ_{JC}	
24 pin Cerdip.....	40°C/W
28 pin Cerdip.....	25°C/W
Thermal Resistance, Junction to Ambient, θ_{JA} :	
24 pin Cerdip.....	80°C/W
28 pin Cerdip.....	60°C/W

Recommended Operating Conditions

Ambient Operating Range (T _A)	-55°C to +125°C
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Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤ T _A ≤ +125°C V _{DD} =+5V, V _{REF+} =+5 V _{REF-} =GND, MODE 0. <u>1</u> / Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
ACCURACY							
Resolution	RES	Guaranteed minimum resolution for which no codes are missing	1,2,3	All	8.0		Bits
Total unadjusted error <u>3</u> /	TUE		1,2,3	01,03 02,04		±0.5 ±1.0	LSB
Channel-to-Channel Mismatch			1,2,3	All		±0.25	LSB
REFERENCE INPUT							
Reference resistance <u>4</u> /	R _{IN}		1,2,3	All	1.0	4.0	kΩ
V _{REF+} Input Voltage Range			1,2,3	All	V _{REF-}	V _{DD}	V
V _{REF-} Input Voltage Range			1,2,3	All	GND	V _{REF+}	V
REFERENCE OUTPUT							
Output Voltage	REF _{OUT}	NOTE 2	1	All	2.47	2.53	V
Load Regulation		I _L =0mA to 10mA	1	All		-10	mV
Power-Supply Sensitivity	PS	V _{DD} =±5%	1	All		±3	mV
Temperature Drift			1,2,3	All		100	ppm/°C
Capacitive Load			4	All		0.01	μF
ANALOG INPUT							
Analog Input Voltage Range	A _{INR}		1,2,3	All	V _{REF-}	V _{REF+}	V
Analog input leakage current	I _{AIN}	Any channel, AIN=0V to 5V	1,2,3	All		±3.0	μA
Analog input capacitance <u>4</u> /	C _{AIN}	0V to 5.0V	4	All		45	pF
Slew rate, tracking <u>4</u> /	SR		4	All		0.157	V/μs
LOGIC INPUTS							
Digital Input Voltage High	V _{IH}	(RD, CS, A0, A1, A2)	1,2,3	All	2.4		V
Digital Input Voltage Low	V _{IL}		1,2,3	All		0.8	V
Digital Input Current High	I _{IH}		1,2,3	All		1.0	μA
Digital Input Current Low	I _{IL}		1,2,3	All		-1.0	μA
Digital Input Capacitance	C _{IN2}	<u>4</u> /	4	All		8.0	pF
LOGIC OUTPUTS							
Digital Output High Voltage	V _{OH}	I _{SOURCE} =360μA	1,2,3	All	4.0		V
Digital Output Low Voltage	V _{OL}	DB0-DB7, RDY, INT I _{SINK} =1.6mA I _{SINK} =2.6mA <u>5</u> /	1,2,3	All		0.4	dB
Floating State Leakage Current	I _{OUT}	DB0-DB7, RDY V _{OUT} =0V to V _{DD}	1,2,3	All		3.0	μA

TEST	Symbol	CONDITIONS -55 °C ≤ T _A ≤ +125°C V _{DD} =+5V, V _{REF+} =+5 V _{REF-} =GND, MODE 0. <u>1/</u> Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Digital Output Capacitance <u>4/</u>	C _{OUT}		4	All		8.0	pF
POWER-SUPPLY							
Supply Voltage	V _{DD}	5V ±5% for specified performance	1,2,3	All	4.75	5.25	V
Supply Current from V _{DD}	I _{DD}	CS=RD=2.4V	1,2,3	All		15	mA
Power Supply Sensitivity	PSS	V _{DD} =+5.0V ±5.0%	1,2,3	All		±0.25	LSB
TIMING							
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ setup time	t _{CSS}	Figure 5 and 6.	9,10,11	All	0		ns
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ hold time	t _{CSH}	Figure 5 and 6.	9,10,11	All	0		ns
$\overline{\text{CS}}$ to RDY delay	t _{RDY}	CL=50pF, pull-up resistor=5.0kΩ Figure 5 and 6.	9 10,11	All		40 60	ns
Conversion Time, Mode 0	t _{CRD}	Figure 5 and 6.	9 10,11	All		2.0 2.8	μs
Data access time after RD	t _{ACC1}	Figure 5 and 6. <u>6/</u>	9 10,11	All		85 120	ns
$\overline{\text{RD}}$ to $\overline{\text{INT}}$ delay	t _{INTH}	Figure 5 and 6. CL=50pF	9 10,11	All		75 100	ns
Data Hold Time	t _{DH}	Figure 5 and 6. <u>4/</u> , <u>7/</u>	9 10,11	All		60 70	ns
Delay Time between conversions	t _p	Figure 5 and 6.	9 10,11	All	500 600		ns
Read pulse width, mode 1	t _{RD}	Figure 5 and 6.	9 10,11	All	60 80	600 400	ns
Data access time after INT mode 0	t _{ACC2}	Figure 5 and 6. <u>6/</u>	9 10,11	All		50 70	ns
Multiplexer address setup time	t _{AS}	Figure 5 and 6.	9,10,11	All	0		ns
Multiplexer address hold time	t _{AH}	Figure 5 and 6.	9 10,11	All	30 40		ns

NOTE 1: V_{DD}=+5.0V, V_{REF+}=+5.0V, and V_{REF-}=GND=0V unless otherwise specified. Specifications apply for mode 0. All input control signals are specified with t_R=t_F=20ns (10% to 90% of +5V) and timed from a 1.6V voltage level.

NOTE 2: Specified with no external load unless otherwise noted.

NOTE 3: Total unadjusted error includes offset, full scale and linearity errors.

NOTE 4: The (C_{IN1}, C_{IN2}, R_{IN}, C_{OUT} and SR measurements) are measured initially and after any process or design change which may affect these tests.

NOTE 5: RDY is an open drain output.

NOTE 6: Measured with load circuits of figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

NOTE 7: Defined as the time required for the data lines to change 0.5V when loaded with the circuits of figure 5 and is measured only for the initial test and after process or design changes which may affect t_{DH}.

FIGURES 1, 5 AND 6: See commercial datasheet.

TRUTH TABLE FOR INPUT CHANNEL SELECTION:

MAX154			MAX158		SELECTED CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	A _{IN1}
0	1	0	0	1	A _{IN2}
1	0	0	1	0	A _{IN3}
1	1	0	1	1	A _{IN4}
		1	0	0	A _{IN5}
		1	0	1	A _{IN6}
		1	1	0	A _{IN7}
		1	1	1	A _{IN8}

	Package	Pkg. Code	ORDERING INFORMATION:
01	24 pin CERDIP	RG	MAX154AMRG/883B
02	24 pin CERDIP	RG	MAX154BMRG/883B
03	28 pin CERDIP	JI	MAX158AMJI/883B
04	28 pin CERDIP	JI	MAX158BMJI/883B

TERMINAL CONNECTIONS:

	MAX154	MAX158		MAX158
Pin			Pin	
1	A _{IN4}	A _{IN6}	25	A0
2	A _{IN3}	A _{IN5}	26	V _{DD}
3	A _{IN2}	A _{IN4}	27	A _{IN8}
4	A _{IN1}	A _{IN3}	28	A _{IN7}
5	REF OUT	A _{IN2}		
6	DB0	A _{IN1}		
7	DB1	REF OUT		
8	DB2	DB0		
9	DB3	DB1		
10	$\overline{\text{RD}}$	DB2		
11	$\overline{\text{INT}}$	DB3		
12	GND	$\overline{\text{RD}}$		
13	V _{REF} ⁻	$\overline{\text{INT}}$		
14	V _{REF} ⁺	GND		
15	RDY	V _{REF} ⁻		
16	$\overline{\text{CS}}$	V _{REF} ⁺		
17	DB4	RDY		
18	DB5	$\overline{\text{CS}}$		
19	DB6	DB4		
20	DB7	DB5		
21	A1	DB6		
22	A0	DB7		
23	NC	A2		
24	V _{DD}	A1		

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 7, 8, 9, 10**, 11**
Group A Test Requirements Method 5005	1, 2, 3, 7, 8, 9, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroups 10 and 11, if not tested shall be guaranteed to the limits specified in Table 1.