REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets																						
REV																						
SHEET	23	24	25	26	27	28	29	30	31	32	33	34	35									
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

Original date of drawing
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TITLE
MICROCIRCUIT, DIGITAL-LINEAR, 14 BIT, 500 MSPS, QUAD ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE
A	16236

DWG NO.
V62/23611

REV

PAGE 1 OF 35

AMSC N/A

5962-V074-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 14 bit, 500 million samples per second (MSPS), quad analog to digital converter microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/23611	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD9694-EP	14 bit, 500 MSPS, quad analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	72	See figure 1	Lead frame chip scale package (LFCSP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage:
- Analog power supply (0.975 V nominal) (AVDD1) to Analog ground (AGND) ..... 1.05 V
- Analog power supply for SYSREF± (AVDD1_SR) to AGND ..... 1.05 V
- Analog power supply (1.8 V nominal) (AVDD2) to AGND ..... 2.00 V
- Analog power supply (2.5 V nominal) (AVDD3) to AGND ..... 2.70 V
- Digital power supply (0.975 V nominal) (DVDD) to Digital ground (DGND) ..... 1.05 V
- Digital power supply (1.8 V nominal) (DRVDD1) to Ground refence (DRGND) ..... 1.05 V
- Digital power supply (2.5 V nominal) (DRVDD2) to DRGND ..... 2.00 V
- Digital power supply for SPI (1.8 V nominal) (SPIVDD) to AGND ..... 2.00 V
- ADC analog input (VIN±x) to AGND ..... -0.3 V to AVDD3 + 0.3 V
- Clock input (CLK±) to AGND ..... -0.3 V to AVDD3 + 0.3 V
- SPI serial clock (SCLK), SPI serial data input/output (SDIO), SPI chip select (active low) (CSB) to DGND ..... -0.3 V to SPIVDD + 0.3 V
- Power down input/Standby (PDWN/STBY) to DGND ..... -0.3 V to SPIVDD + 0.3 V
- System refence (SYSREF±) to AGND_SR ..... 0 V to 2.5 V
- SYNC input (SYNCINB±AB/SYNCINB±CD) to DRGND ..... 0 V to 2.5 V

Maximum junction temperature (T_J) ..... 125°C

Storage temperature range (T_{STG}) ambient ..... -65°C to +150°C

Operating temperature range (T_A) ..... -55°C to +105°C

Thermal resistance, junction-to-ambient (θ_{JA}) ..... 20.69°C/W 2/

Thermal resistance, junction-to-case (bottom) (θ_{JC_BOT}) ..... 0.41°C/W

Characterization parameter, junction-to-top (ψ_{JT}) ..... 0.07°C/W

Characterization parameter, junction-to-board (ψ_{JB}) ..... 6.75°C/W

1.4 Recommended operating conditions. 3/

Supply voltage:
- AVDD1 ..... 0.975 V
- AVDD1_SR ..... 0.975 V
- AVDD2 ..... 1.8 V
- AVDD3 ..... 2.5 V
- DVDD ..... 0.975 V
- DRVDD1 ..... 0.975 V
- DRVDD2 ..... 1.8 V
- SPIVDD ..... 1.8 V

Operating temperature range (T_A) ..... -55°C to +105°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Per JEDEC 51-7, plus JEDEC 51-2 with 2s2p test board.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

EIA/JEDEC 51-2	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air).
EIA/JEDEC 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices.
JESD 204 B	–	Serial Interface for Data Converters (Subclass 1).

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figures 4, 5, and 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC specification							
RESOLUTION			-55°C to +105°C	01	14		Bits
ACCURACY							
No missing code			-55°C to +105°C	01	Guaranteed		
Offset error			+25°C	01	0 typical		% FSR
Offset matching			+25°C	01	0 typical		% FSR
Gain error			-55°C to +105°C	01	-5.0	+5.0	% FSR
Gain matching			-55°C to +105°C	01		3.7	% FSR
			+25°C		1.0 typical		
Differential nonlinearity	DNL		-55°C to +105°C	01	-0.7	+0.7	LSB
			+25°C		±0.4 typical		
Integral nonlinearity	INL		-55°C to +105°C	01	-5.1	+5.1	LSB
			+25°C		±1.0 typical		
TEMPERATURE DRIFT							
Offset error			+25°C	01	8 typical		ppm/°C
Gain error			+25°C	01	214 typical		ppm/°C
INTERNAL VOLTAGE REFERENCE			+25°C	01	0.5 typical		V
INPUT REFERRED NOISE			+25°C	01	2.6 typical		LSB RMS
ANALOG INPUTS							
Differential input voltage			+25°C	01	1.80 typical		V_{P-P}
range (programmable)			-55°C to +105°C		1.44	2.16	
Common mode voltage	V_{CM}		+25°C	01	1.34 typical		V
Differential input capacitance 3/			+25°C	01	1.75 typical		pF
Differential input resistance			+25°C	01	200 typical		Ω
Analog input full power bandwidth			+25°C	01	1.4 typical		GHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
POWER SUPPLY							
Analog power supply (0.975 V nominal)	AVDD1		-55°C to +105°C	01	0.95	1.00	V
			+25°C		0.975 typical		
Analog power supply for SYSREF± (0.975 V nominal)	AVDD1_SR		-55°C to +105°C	01	0.95	1.00	V
			+25°C		0.975 typical		
Analog power supply (1.8 V nominal)	AVDD2		-55°C to +105°C	01	1.71	1.89	V
			+25°C		1.8 typical		
Analog power supply (2.5 V nominal)	AVDD3		-55°C to +105°C	01	2.44	2.56	V
			+25°C		2.5 typical		
Digital power supply (0.975 V nominal)	DVDD		-55°C to +105°C	01	0.95	1.00	V
			+25°C		0.975 typical		
Digital power supply for SERDOUTABx± / SERDOUTCDx± pins (0.975 V nominal)	DRVDD1		-55°C to +105°C	01	0.95	1.00	V
			+25°C		0.975 typical		
Digital power supply for JESD204B PLL (1.8 V nominal)	DRVDD2		-55°C to +105°C	01	1.71	1.89	V
			+25°C		1.8 typical		
Digital power supply for SPI (1.8 V nominal)	SPIVDD		-55°C to +105°C	01	1.71	1.89	V
			+25°C		1.8 typical		
AVDD1 current	I_{AVDD1}		-55°C to +105°C	01		482	mA
			+25°C		3.19 typical		
AVDD1_SR current	I_{AVDD1_SR}		-55°C to +105°C	01		53	mA
			+25°C		21 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
POWER SUPPLY - continued.							
AVDD2 current	I_{AVDD2}		-55°C to +105°C	01		473	mA
			+25°C		438 typical		
AVDD3 current	I_{AVDD3}		-55°C to +105°C	01		103	mA
			+25°C		87 typical		
DVDD current 4/	I_{DVDD}		-55°C to +105°C	01		180	mA
			+25°C		121 typical		
DVDD1 current 3/	IDVDD1		-55°C to +105°C	01		207	mA
			+25°C		162 typical		
DVDD2 current 3/	I_{DVDD2}		-55°C to +105°C	01		29	mA
			+25°C		23 typical		
SPIVDD current	I_{SPIVDD}		-55°C to +105°C	01		1.6	mA
			+25°C		1 typical		
POWER CONSUMPTIO N							
Total power dissipation		(including output drivers) 4/	-55°C to +105°C	01		2.07	W
			+25°C		1.66 typical		
Power down dissipation			+25°C	01	325 typical		mW
Standby 5/			+25°C	01	1.20 typical		W
AC SPECIFICATION		500 MSPS 6/ 7/					
Analog input full scale		AIN full scale = 1.44 V_{PP}	+25°C	01	1.44 typical		V_{PP}
		AIN full scale = 1.80 V_{PP}			1.80 typical		
		AIN full scale = 2.16 V_{PP}			2.16 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION - continued.		500 MSPS 7/					
Noise density 8/		AIN full scale = 1.44 V_{PP}	+25°C	01	-149.7 typical		dBFS / Hz
		AIN full scale = 1.80 V_{PP}			-151.5 typical		
		AIN full scale = 2.16 V_{PP}			-153.0 typical		
Signal to noise ratio	(SNR)	9/					
Input frequency (f_{IN}) = 10 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	65.4 typical		dBFS
		AIN full scale = 1.80 V_{PP}			67.1 typical		
		AIN full scale = 2.16 V_{PP}			68.4 typical		
Input frequency (f_{IN}) = 155 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	65.3 typical		dBFS
		AIN full scale = 1.80 V_{PP}	-55°C to +105°C		64.8		
			+25°C		67.0 typical		
		AIN full scale = 2.16 V_{PP}	+25°C		68.3 typical		
Input frequency (f_{IN}) = 305 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	65.2 typical		dBFS
		AIN full scale = 1.80 V_{PP}			66.8 typical		
		AIN full scale = 2.16 V_{PP}			68.0 typical		
Input frequency (f_{IN}) = 450 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	65.0 typical		dBFS
		AIN full scale = 1.80 V_{PP}			66.6 typical		
		AIN full scale = 2.16 V_{PP}			67.8 typical		
Input frequency (f_{IN}) = 765 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	64.8 typical		dBFS
		AIN full scale = 1.80 V_{PP}			66.5 typical		
		AIN full scale = 2.16 V_{PP}			67.5 typical		
Input frequency (f_{IN}) = 985 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	64.5 typical		dBFS
		AIN full scale = 1.80 V_{PP}			66.0 typical		
		AIN full scale = 2.16 V_{PP}			66.9 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION - continued.		500 MSPS 7/					
Signal to noise and distortion ratio		(SINAD)					
Input frequency (f_{IN}) = 10 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	65.3 typical		dBFS
		AIN full scale = 1.80 V_{PP}			67.0 typical		
		AIN full scale = 2.16 V_{PP}			68.2 typical		
Input frequency (f_{IN}) = 155 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	65.2 typical		dBFS
		AIN full scale = 1.80 V_{PP}	-55°C to +105°C		64.5		
			+25°C		66.8 typical		
		AIN full scale = 2.16 V_{PP}	+25°C		67.9 typical		
Input frequency (f_{IN}) = 305 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	65.1 typical		dBFS
		AIN full scale = 1.80 V_{PP}			66.6 typical		
		AIN full scale = 2.16 V_{PP}			67.6 typical		
Input frequency (f_{IN}) = 450 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	65.0 typical		dBFS
		AIN full scale = 1.80 V_{PP}			66.4 typical		
		AIN full scale = 2.16 V_{PP}			67.3 typical		
Input frequency (f_{IN}) = 765 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	64.7 typical		dBFS
		AIN full scale = 1.80 V_{PP}			66.1 typical		
		AIN full scale = 2.16 V_{PP}			66.9 typical		
Input frequency (f_{IN}) = 985 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	64.2 typical		dBFS
		AIN full scale = 1.80 V_{PP}			65.5 typical		
		AIN full scale = 2.16 V_{PP}			66.2 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION - continued. 500 MSPS 7/							
Effective number of bits (ENOB)							
Input frequency (f_{IN}) = 10 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	10.5 typical		Bits
		AIN full scale = 1.80 V_{PP}			10.8 typical		
		AIN full scale = 2.16 V_{PP}			11.0 typical		
Input frequency (f_{IN}) = 155 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	10.5 typical		Bits
		AIN full scale = 1.80 V_{PP}	-55°C to +105°C		10.4		
			+25°C		10.8 typical		
		AIN full scale = 2.16 V_{PP}	+25°C		10.9 typical		
Input frequency (f_{IN}) = 305 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	10.5 typical		Bits
		AIN full scale = 1.80 V_{PP}			10.7 typical		
		AIN full scale = 2.16 V_{PP}			10.9 typical		
Input frequency (f_{IN}) = 450 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	10.5 typical		Bits
		AIN full scale = 1.80 V_{PP}			10.7 typical		
		AIN full scale = 2.16 V_{PP}			10.8 typical		
Input frequency (f_{IN}) = 765 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	10.4 typical		Bits
		AIN full scale = 1.80 V_{PP}			10.6 typical		
		AIN full scale = 2.16 V_{PP}			10.8 typical		
Input frequency (f_{IN}) = 985 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	10.3 typical		Bits
		AIN full scale = 1.80 V_{PP}			10.6 typical		
		AIN full scale = 2.16 V_{PP}			10.7 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION - continued.		500 MSPS 7/					
Spurious free dynamic range		(SFDR)					
Input frequency (f_{IN}) = 10 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	89 typical		dBFS
		AIN full scale = 1.80 V_{PP}			90 typical		
		AIN full scale = 2.16 V_{PP}			80 typical		
Input frequency (f_{IN}) = 155 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	89 typical		dBFS
		AIN full scale = 1.80 V_{PP}	-55°C to +105°C		75		
			+25°C		85 typical		
		AIN full scale = 2.16 V_{PP}	+25°C		77 typical		
Input frequency (f_{IN}) = 305 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	82 typical		dBFS
		AIN full scale = 1.80 V_{PP}			82 typical		
		AIN full scale = 2.16 V_{PP}			78 typical		
Input frequency (f_{IN}) = 450 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	82 typical		dBFS
		AIN full scale = 1.80 V_{PP}			83 typical		
		AIN full scale = 2.16 V_{PP}			77 typical		
Input frequency (f_{IN}) = 765 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	77 typical		dBFS
		AIN full scale = 1.80 V_{PP}			75 typical		
		AIN full scale = 2.16 V_{PP}			72 typical		
Input frequency (f_{IN}) = 985 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	82 typical		dBFS
		AIN full scale = 1.80 V_{PP}			79 typical		
		AIN full scale = 2.16 V_{PP}			76 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION - continued.		500 MSPS 7/					
Spurious free dynamic range		(SFDR) at-3 dBFS					
Input frequency (f_{IN}) = 10 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	94 typical		dBFS
		AIN full scale = 1.80 V_{PP}			94 typical		
		AIN full scale = 2.16 V_{PP}			86 typical		
Input frequency (f_{IN}) = 155 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	94 typical		dBFS
		AIN full scale = 1.80 V_{PP}			90 typical		
		AIN full scale = 2.16 V_{PP}			82 typical		
Input frequency (f_{IN}) = 305 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	89 typical		dBFS
		AIN full scale = 1.80 V_{PP}			90 typical		
		AIN full scale = 2.16 V_{PP}			83 typical		
Input frequency (f_{IN}) = 450 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	87 typical		dBFS
		AIN full scale = 1.80 V_{PP}			86 typical		
		AIN full scale = 2.16 V_{PP}			84 typical		
Input frequency (f_{IN}) = 765 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	82 typical		dBFS
		AIN full scale = 1.80 V_{PP}			80 typical		
		AIN full scale = 2.16 V_{PP}			77 typical		
Input frequency (f_{IN}) = 985 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	85 typical		dBFS
		AIN full scale = 1.80 V_{PP}			82 typical		
		AIN full scale = 2.16 V_{PP}			79 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION - continued. 500 MSPS 7/							
Worst harmonic, second or third							
Input frequency (f_{IN}) = 10 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-89 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-90 typical		
		AIN full scale = 2.16 V_{PP}			-80 typical		
Input frequency (f_{IN}) = 155 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-89 typical		dBFS
		AIN full scale = 1.80 V_{PP}	-55°C to +105°C			-75	
			+25°C		-85 typical		
		AIN full scale = 2.16 V_{PP}	+25°C		-77 typical		
Input frequency (f_{IN}) = 305 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	- 82 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-82 typical		
		AIN full scale = 2.16 V_{PP}			-78 typical		
Input frequency (f_{IN}) = 450 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-82 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-83 typical		
		AIN full scale = 2.16 V_{PP}			-77 typical		
Input frequency (f_{IN}) = 765 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-77 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-75 typical		
		AIN full scale = 2.16 V_{PP}			-72 typical		
Input frequency (f_{IN}) = 985 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-82 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-79 typical		
		AIN full scale = 2.16 V_{PP}			-76 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION - continued. 500 MSPS 7/							
Worst harmonic, second or third at -3 dBFS							
Input frequency (f_{IN}) = 10 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-94 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-94 typical		
		AIN full scale = 2.16 V_{PP}			-86 typical		
Input frequency (f_{IN}) = 155 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-94 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-90 typical		
		AIN full scale = 2.16 V_{PP}			-82 typical		
Input frequency (f_{IN}) = 305 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	- 89 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-90 typical		
		AIN full scale = 2.16 V_{PP}			-83 typical		
Input frequency (f_{IN}) = 450 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-87 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-86 typical		
		AIN full scale = 2.16 V_{PP}			-84 typical		
Input frequency (f_{IN}) = 765 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-82 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-80 typical		
		AIN full scale = 2.16 V_{PP}			-77 typical		
Input frequency (f_{IN}) = 985 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-85 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-82 typical		
		AIN full scale = 2.16 V_{PP}			-79 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION - continued. 500 MSPS 7/							
Worst other, excluding second or third harmonic							
Input frequency (f_{IN}) = 10 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-96 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-98 typical		
		AIN full scale = 2.16 V_{PP}			-99 typical		
Input frequency (f_{IN}) = 155 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-97 typical		dBFS
		AIN full scale = 1.80 V_{PP}	-55°C to +105°C			-86	
			+25°C		-97 typical		
		AIN full scale = 2.16 V_{PP}	+25°C		-97 typical		
Input frequency (f_{IN}) = 305 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	- 97 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-98 typical		
		AIN full scale = 2.16 V_{PP}			-97 typical		
Input frequency (f_{IN}) = 450 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-95 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-96 typical		
		AIN full scale = 2.16 V_{PP}			-96 typical		
Input frequency (f_{IN}) = 765 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-92 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-91 typical		
		AIN full scale = 2.16 V_{PP}			-88 typical		
Input frequency (f_{IN}) = 985 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-90 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-89 typical		
		AIN full scale = 2.16 V_{PP}			-86 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION - continued.		500 MSPS 7/					
Two tone intermodulation distortion		(IMD) with A_{IN1} and A_{IN2} = -7 dBFS					
Input frequency (f_{IN1}) = 154 MHz and (f_{IN2}) = 157 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-93 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-90 typical		
		AIN full scale = 2.16 V_{PP}			-84 typical		
Input frequency (f_{IN1}) = 302 MHz and (f_{IN2}) = 305 MHz		AIN full scale = 1.44 V_{PP}	+25°C	01	-90 typical		dBFS
		AIN full scale = 1.80 V_{PP}			-90 typical		
		AIN full scale = 2.16 V_{PP}			-84 typical		
Crosstalk 10/		AIN full scale = 1.44 V_{PP}	+25°C	01	82 typical		dB
		AIN full scale = 1.80 V_{PP}			82 typical		
		AIN full scale = 2.16 V_{PP}			82 typical		
Full power 9/ bandwidth		AIN full scale = 1.44 V_{PP}	+25°C	01	1.4 typical		GHz
		AIN full scale = 1.80 V_{PP}			1.4 typical		
		AIN full scale = 2.16 V_{PP}			1.4 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION		600 MSPS 7/					
A_{IN} full scale			+25°C	01	1.80 typical		V_{PP}
Signal to noise ratio	(SNR)						
Input frequency (f_{IN}) = 10 MHz		A_{IN} = 1.80 V_{PP}	+25°C	01	66.6 typical		dBFS
(f_{IN}) = 155 MHz					67 typical		
(f_{IN}) = 305 MHz					66.8 typical		
(f_{IN}) = 450 MHz					66.4 typical		
(f_{IN}) = 765 MHz					66 typical		
(f_{IN}) = 985 MHz					65.5 typical		
Signal to noise and distor tion ratio		(SINAD)					
Input frequency (f_{IN}) = 10 MHz		A_{IN} = 1.80 V_{PP}	+25°C	01	66.5 typical		dBFS
(f_{IN}) = 155 MHz					66.8 typical		
(f_{IN}) = 305 MHz					66.5 typical		
(f_{IN}) = 450 MHz					66.3 typical		
(f_{IN}) = 765 MHz					65.4 typical		
(f_{IN}) = 985 MHz					64.8 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 6/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC SPECIFICATION - continued.		600 MSPS 7/					
Spurious free dynamic range		(SFDR)					
Input frequency (f_{IN}) = 10 MHz		A_{IN} = 1.80 V_{PP}	+25°C	01	86 typical		dBFS
(f_{IN}) = 155 MHz					81 typical		
(f_{IN}) = 305 MHz					81 typical		
(f_{IN}) = 450 MHz					84 typical		
(f_{IN}) = 765 MHz					76 typical		
(f_{IN}) = 985 MHz					75 typical		
Worst harmonic, second or third							
Input frequency (f_{IN}) = 10 MHz		A_{IN} = 1.80 V_{PP}	+25°C	01	-86 typical		dBFS
(f_{IN}) = 155 MHz					-81 typical		
(f_{IN}) = 305 MHz					-81 typical		
(f_{IN}) = 450 MHz					-84 typical		
(f_{IN}) = 765 MHz					-76 typical		
(f_{IN}) = 985 MHz					-75 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
POWER CONSUMPTION		600 = MSPS					
Analog power supply (0.975 V nominal)	AVDD1		-55°C to +105°C	01	0.95	1.00	V
			+25°C		0.975 typical		
Analog power supply for SYSREF± (0.975 V nominal)	AVDD1_SR		-55°C to +105°C	01	0.95	1.00	V
			+25°C		0.975 typical		
Analog power supply (1.8 V nominal)	AVDD2		-55°C to +105°C	01	1.71	1.89	V
			+25°C		1.8 typical		
Analog power supply (2.5 V nominal)	AVVD3		-55°C to +105°C	01	2.44	2.56	V
			+25°C		2.5 typical		
Digital power supply (0.975 V nominal)	DVDD		-55°C to +105°C	01	0.95	1.00	V
			+25°C		0.975 typical		
Digital power supply for SERDOUTABx± / SERDOUTCDx± pins (0.975 V nominal)	DRVDD1		-55°C to +105°C	01	0.95	1.00	V
			+25°C		0.975 typical		
Digital power supply for JESD204B PLL (1.8 V nominal)	DRVDD2		-55°C to +105°C	01	1.71	1.89	V
			+25°C		1.8 typical		
Digital power supply for SPI (1.8 V nominal)	SPIVDD		-55°C to +105°C	01	1.71	1.89	V
			+25°C		1.8 typical		
AVDD1 current	IAVDD1		-55°C to +105°C	01		513	mA
			+25°C		352 typical		
AVDD1_SR current	IAVDD1_SR		-55°C to +105°C	01		55	mA
			+25°C		23 typical		
AVDD2 current	IAVDD2		-55°C to +105°C	01		478	mA
			+25°C		443 typical		
AVDD3 current	IAVDD3		-55°C to +105°C	01		104	mA
			+25°C		87 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
POWER CONSUMPTION - continue d. 600 = MSPS							
DVDD current	IDVDD	Full mode mode	-55°C to +105°C	01		200	mA
			+25°C		146	typical	
DVDD1 current	IDRVDD1	11/	-55°C to +105°C	01		235	mA
			+25°C		183	typical	
DVDD2 current	IDRVDD2		-55°C to +105°C	01		28	mA
			+25°C		23	typical	
SPIVDD current	ISPIVDD		-55°C to +105°C	01		1.6	mA
					1	typical	
Power consumption							
Total power dissipation		Including output drivers	-55°C to +105°C	01		2.16	W
					1.75	typical	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DIGITAL SPECIFICATION							
Clock inputs (CLK+ and CLK-)							
Logic compliance 12/			+25°C	01	LVDS/ typical	LVPECL	
Differential input voltage			-55°C to +105°C	01	600	1600	mV_{PP}
			+25°C		800	typical	
Input common mode voltage			+25°C	01	0.69	typical	V
Input resistance (differential)			+25°C	01	32	typical	kΩ
Input capacitance			-55°C to +105°C	01		0.9	pF
System reference inputs (SYSREF ±) 13/							
Logic compliance 12/			+25°C	01	LVDS/ typical	LVPECL	
Differential input voltage			-55°C to +105°C	01	400	1800	mV_{PP}
			+25°C		800	typical	
Input common mode voltage			-55°C to +105°C	01	0.6	2.2	V
			+25°C		0.69	typical	
Input resistance (differential)			-55°C to +105°C	01	18		kΩ
			+25°C		22	typical	
Input capacitance		Single ended per pin	-55°C to +105°C	01	0.7	typical	pF
Logic inputs (PDWN/STBY)							
Logic compliance 14/			+25°C	01	CMOS	typical	
Logic 1 voltage			-55°C to +105°C	01	0.65 x SPIVDD		V
Logic 0 voltage			-55°C to +105°C	01	0	0.35 x SPIVDD	V
Input resistance			+25°C	01	10	typical	MΩ

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DIGITAL SPECIFICATION - continued.							
Logic inputs (SDIO, SCLK, and CSB							
Logic compliance 14/			+25°C	01	CMOS typical		
Logic 1 voltage			-55°C to +105°C	01	0.65 x SPIVDD		V
Logic 0 voltage			-55°C to +105°C	01	0	0.35 x SPIVDD	V
Input resistance			+25°C	01	56 typical		MΩ
Logic output (SDIO)							
Logic compliance 14/			+25°C	01	CMOS typical		
Logic 1 voltage		I_{OH} = 800 μA	-55°C to +105°C	01	SPIVDD – 0.45		V
Logic 0 voltage		I_{OL} = 50 μA	-55°C to +105°C	01	0	0.45	V
SYNCIN INPUT		(SYNCINB±AB and SYNCINB±CD)					
Logic compliance 12/ 14/			+25°C	01	LVDS/ CMOS	LVPECL/ typical	
Differential input voltage			-55°C to +105°C	01	400	1800	mV_{PP}
			+25°C		800 typical		
Input common mode voltage			-55°C to +105°C	01	0.6	2.2	V
			+25°C		0.69 typical		
Input resistance (differential)			-55°C to +105°C	01	18		kΩ
			+25°C		22 typical		
Input capacitance		Single ended per pin	-55°C to +105°C	01	0.7 typical		pF
Logic outputs		(FD_A, FD_B, FD_C, and FD_D)					
Logic compliance 14/			+25°C	01	CMOS typical		
Logic 1 voltage			-55°C to +105°C	01	0.8 x SPIVDD		V
Logic 0 voltage			-55°C to +105°C	01	0	0.5	V
Input resistance			+25°C	01	56 typical		kΩ

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DIGITAL SPECIFICATION - continued.							
Digital outputs		(SEROUTABx± and SEROUTCDx±, X = 0 OR1					
Logic compliance 15/			+25°C	01	CML typical		
Differential output voltage			+25°C	01	455.8 typical		mV_{PP}
Short circuit current	$I_{D\ SHORT}$		+25°C	01	15 typical		mA
Differential termination impedance			+25°C	01	100 typical		Ω
SWITCHING SPECIFICATION 2/							
Clock							
Clock rate at CLK+ and CLK- pins			-55°C to +105°C	01	0.3	2.4	GHz
Maximum sample rate		16/	-55°C to +105°C	01	600		MSPS
Minimum sample rate		17/	-55°C to +105°C	01	240		MSPS
Clock pulse width high			-55°C to +105°C	01	125		ps
Clock pulse width low			-55°C to +105°C	01	125		ps
Output							
Unit interval 18/	UI		-55°C to +105°C	01	66.67	593	ps
			+25°C		100 typical		
Rise time	t_R	20% to 80% into 100 Ω load	+25°C	01	31.25 typical		ps
Fall time	t_F	80% to 20% into 100 Ω load	+25°C	01	31.37 typical		ps
Phase locked loop (PLL) lock time			+25°C	01	5 typical		ms
Data rate per channel		Nonreturn to zero (NRZ) 19/	-55°C to +105°C	01	1.6875	15	Gbps
			+25°C		10 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
SWITCHING SPECIFICATION continued. 2/							
Latency 20/							
Pipeline latency			+25°C	01	54 typical		Sample clock cycles
Fast detect latency			-55°C to +105°C	01		30	Sample clock cycles
Wake up time							
From standby			+25°C	01	3 typical		ms
From power down			+25°C	01	10 typical		ms
Aperture		See figure 4					
Aperture delay	t_A		+25°C	01	160 typical		ps
Aperture uncertainty	Jitter, t_j		+25°C	01	44 typical		fs rms
Out of range recover time			+25°C	01	1 typical		Sample clock cycles
TIMING SPECIFICATION S							
CLK+ to SYSREF+ timing requirements. See figure 5.							
Device clock to SYSREF+ setup time	t_{SU_SR}		+25°C	01	-44.8 typical		ps
Device clock to SYSREF+ hold time	t_{H_SR}		+25°C	01	64.4 typical		ps
SPI timing requirements		See figure 6.					
Setup time between the data and the rising edge of SCLK	t_{DS}		+25°C	01	4		ns
Hold time between the data and the rising edge of SCLK	t_{DH}		+25°C	01	2		ns
Period of the SCLK	t_{CLK}		+25°C	01	40		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
SPI timing requirements - continued. See figure 6.							
Setup time between CSB and SCLK	t_S		+25°C	01	2		ns
Hold time between CSB and SCLK	t_H		+25°C	01	2		ns
Minimum period that SCLK must be in a logic high state	t_{HIGH}		+25°C	01	10		ns
Minimum period that SCLK must be in a logic low state	t_{LOW}		+25°C	01	10		ns
Maximum time delay between falling edge of SCLK and output data valid for a read operation	t_{ACCESS}		-55°C to +105°C	01		10	ns
			+25°C		6	typical	
Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge	t_{DIS_SDIO}	This test is guaranteed by design and not tested and therefore not specified in figure 6.	-55°C to +105°C	01	10		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 Vpp full-scale differential input, 0.5 V internal reference, and analog input (A_{IN}) = −1.0 dBFS.

3/ All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.

4/ Full bandwidth mode

5/ Standby mode is controlled by the SPI.

6/ Unless otherwise specified, AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, and A_{IN} = −1.0 dBFS, default SPI settings.

7/ See the manufacturer's datasheet for definitions and for details on how these tests were completed.

8/ Noise density is measured at a low AIN frequency (30 MHz).

9/ See the manufacturer's data sheet for more details.

10/ Crosstalk is measured at 155 MHz with a −1.0 dBFS A_{IN} on one channel and no input on the adjacent channel.

11/ All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.

12/ LVDS is low voltage differential signaling, and LVPECL is low voltage positive emitter-coupled logic.

13/ DC-coupled input only.

14/ CMOS is a complementary metal–oxide semiconductor.

15/ CML is current mode logic.

16/ The maximum sample rate is the clock rate after the divider.

17/ The minimum sample rate operates at 240 MSPS with number of lanes (L) = 2 or L = 1.
See SPI Register 0x011A in the manufacturer's data sheet to reduce the threshold of the clock detection circuit.

18/ Baud rate = 1/UI. A subset of this range can be supported.

19/ Default L = 2 for each link. This number can be changed based on the sample rate and decimation ratio.

20/ No digital down converters (DDCs) used. L = 2, number of converters (M) = 2, and number of octets/frames (F) = 2 for each link.

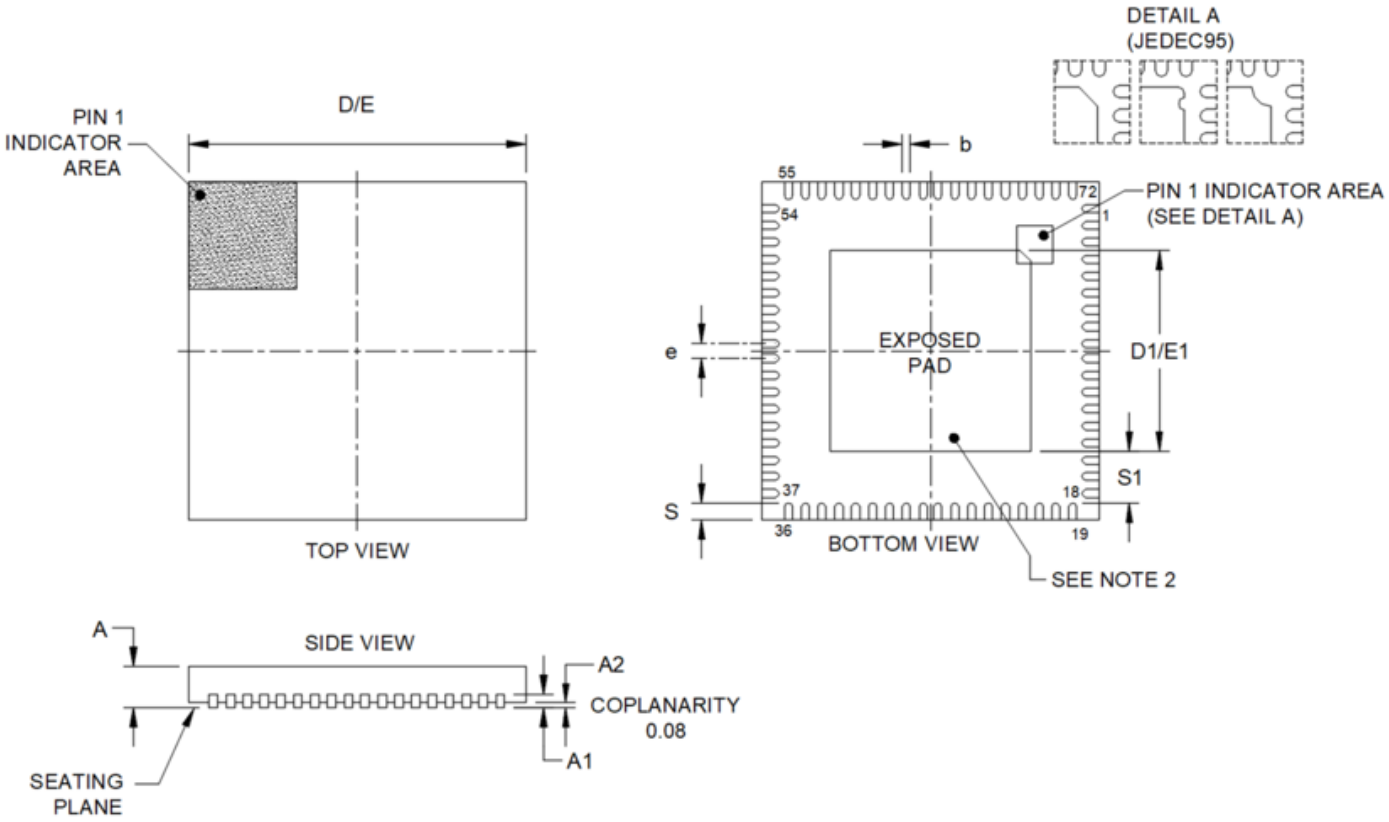

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/23611
		REV	PAGE 27

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.027	.029	.031	0.70	0.75	0.80
A1	.008 REF			0.20 REF		
A2	---	.001	.002	---	0.02	0.05
b	.007	.009	.011	0.18	0.23	0.28
D/E	.390	.394	.398	9.90	10.00	10.10
D1/E1	.232	.236	.240	5.90	6.00	6.10
e	.020 BSC			0.50 BSC		
S	.016	.020	.024	0.40	0.50	0.60
S1	.059 REF			1.50 REF		

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function description section of the manufacturer's datasheet.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AVDD3	19	SYNCINB-AB
2	VIN-A	20	SYNCINB+AB
3	VIN+A	21	DRGND
4	AVDD2	22	DRVDD1
5	AVDD2	23	SERDOUTAB0-
6	AVDD3	24	SERDOUTAB0+
7	VIN+B	25	SERDOUTAB1-
8	VIN-B	26	SERDOUTAB1+
9	AVDD2	27	SERDOUTCD1+
10	AVDD1	28	SERDOUTCD1-
11	AVDD1	29	SERDOUTCD0+
12	VCM_AB	30	SERDOUTCD0-
13	DVDD	31	DRVDD1
14	DGND	32	DRGND
15	DRVDD2	33	SYNCINB+CD
16	PDWN/STBY	34	SYNCINB-CD
17	FD_A	35	FD_D
18	FD_B	36	FD_C

FIGURE 2. Terminal connections.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
37	SDIO	55	AVDD2
38	SCLK	56	AVDD1
39	CSB	57	AVDD1
40	SPIVDD	58	AVDD1
41	DGND	59	AVDD1
42	DVDD	60	CLK+
43	VCM_CD/VREF	61	CLK-
44	AVDD1	62	AVDD1
45	AVDD1	63	AGND_SR
46	AVDD2	64	AVDD1_SR
47	VIN-D	65	SYSREF+
48	VIN+D	66	SYSREF-
49	AVDD3	67	AGND_SR
50	AVDD2	68	AVDD1
51	AVDD2	69	AVDD1
52	VIN+C	70	AVDD1
53	VIN-C	71	AVDD1
54	AVDD3	72	AVDD2

FIGURE 2. Terminal connections - continued.

Device type	01	
Case outline	X	
Terminal symbol	Type	Description
AGND/EPAD	Ground	Exposed Pad. Analog Ground. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx, SPIVDD, DVDD, DRVDD1 and DRVDD2. This exposed pad must be connected to ground for proper operation.
AVDD3	Supply	Analog Power Supply (2.5 V nominal).
VIN-A, VIN+A	Input	ADC A Analog Input Complement/True.
AVDD2	Supply	Analog Power Supply (1.8 V nominal).
VIN+B, VIN-B	Input	ADC B Analog Input True/Complement.
AVDD1	Supply	Analog Power Supply (0.975 V nominal).
VCM_AB	Output	Common-Mode Level Bias Output for Analog Input Channel A and Channel B.
DVDD	Supply	Digital Power Supply (0.975 V nominal).
DGND	Ground	Ground Reference for DVDD and SPIVDD.
DRVDD2	Supply	Digital Power Supply for JESD204B PLL (1.8 V nominal).
PDWN/STBY	Input	Power-Down Input/Standby (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby. This pin requires an external 10 kΩ pull-down resistor.
FD_A, FD_B, FD_C, FD_D	Output	Fast Detect Outputs for Channel A, Channel B, Channel C, and Channel D.
SYNCINB-AB	Input	Active Low JESD204B LVDS Sync Input Complement for Channel A and Channel B.
SYNCINB+AB	Input	Active Low JESD204B LVDS/CMOS Sync Input True for Channel A and Channel B.
DRGND	Ground	Ground Reference for DRVDD1 and DRVDD2.
DRVDD1	Supply	Digital Power Supply for SERDOUTABx±/SERDOUTCDx± pins (0.975 V nominal).
SERDOUTAB0−, SERDOUTAB0+	Output	Lane 0 Output Data Complement/True for Channel A and Channel B.
SERDOUTAB1−, SERDOUTAB1+	Output	Lane 1 Output Data Complement/True for Channel A and Channel B.
SERDOUTCD1+, SERDOUTCD1−	Output	Lane 1 Output Data True/Complement for Channel C and Channel D.

FIGURE 2. Terminal connections - continued.

Device type	01	
Case outline	X	
Terminal symbol	Type	Description
SERDOUTCD0+, SERDOUTCD0−	Output	Lane 0 Output Data True/Complement for Channel C and Channel D.
SYNCINB+CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input True for Channel C and Channel D.
SYNCINB−CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input Complement for Channel C and Channel D.
SDIO	Input/output	SPI Serial Data Input/Output.
SCLK	Input	SPI Serial Clock.
CSB	Input	SPI Chip Select (Active Low).
SPIVDD	Supply	Digital Power Supply for SPI (1.8 V nominal).
VCM_CD/VREF	Output/input	Common-Mode Level Bias Output for Analog Input Channel C and Channel D / 0.5 V Reference Voltage Input. This pin is configurable through the SPI as an output or an input. Use this pin as the common-mode level bias output if using the internal reference. This pin requires a 0.5 V reference voltage input if using an external voltage reference source.
VIN−D, VIN+D	Input	ADC D Analog Input Complement/True.
VIN+C, VIN−C	Input	ADC C Analog Input True/Complement.
CLK+, CLK−	Input	Clock Input True/Complement.
AGND_SR	Ground	Ground Reference for SYSREF±.
AVDD1_SR	Supply	Analog Power Supply for SYSREF± (0.975 V nominal).
SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference Input True/Complement. DC- coupled input only.

FIGURE 2. Terminal connections - continued.

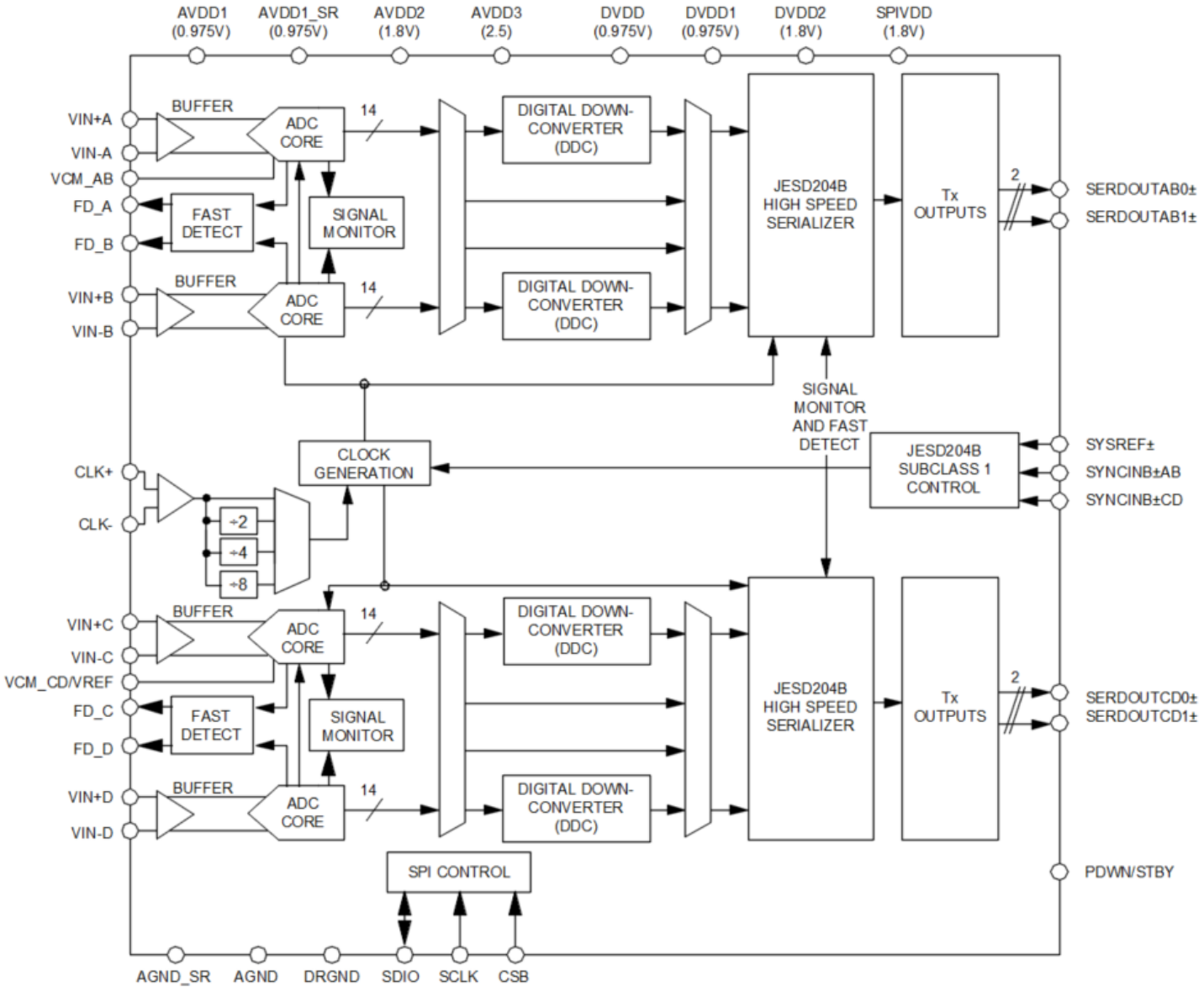

FIGURE 3. Functional block diagram.

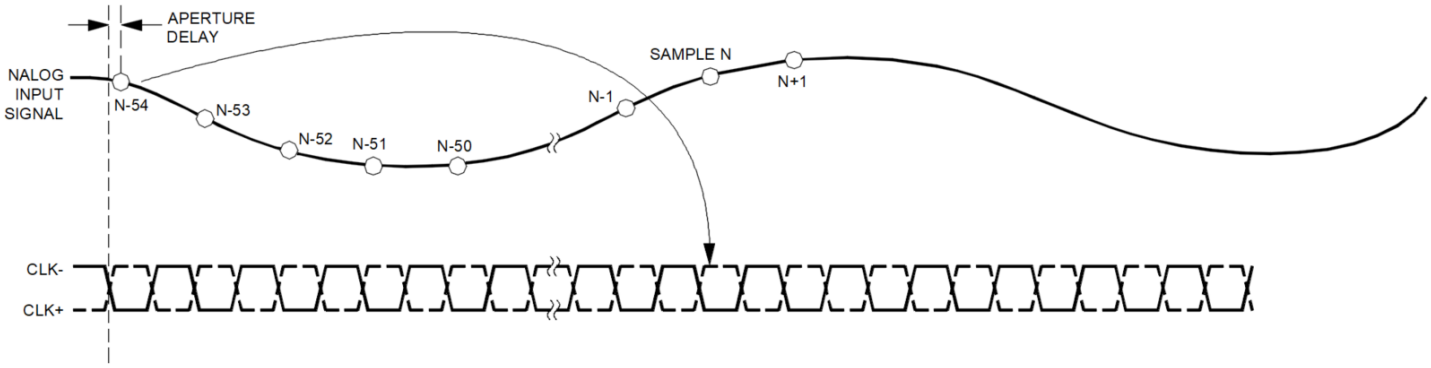

FIGURE 4. Data output timing. (Full bandwidth mode, L = 4, M = 2, F = 1.)

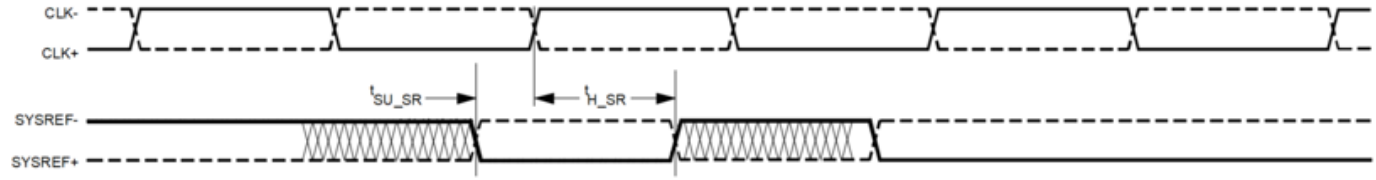

FIGURE 5. SYSREF± setup and hold timing.

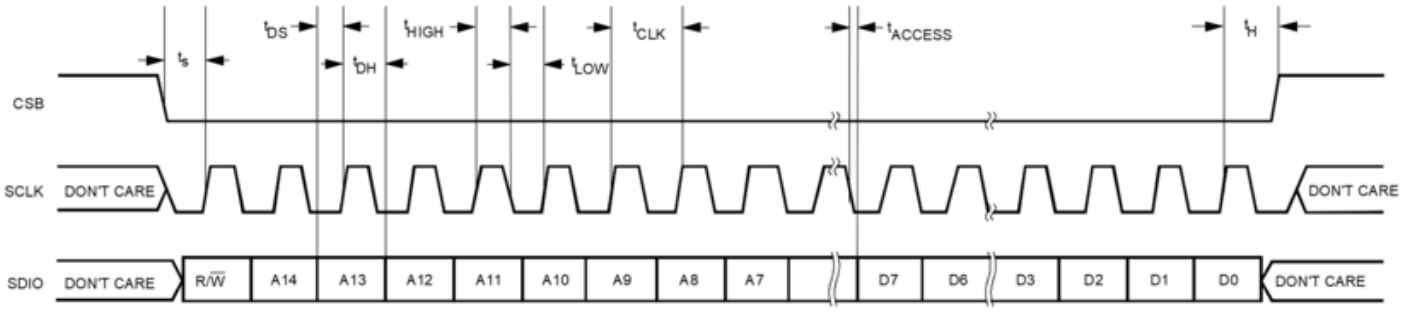

FIGURE 6. Serial port interface timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/23611-01XE	24355	TCPZ-500-EP	AD9694TCPZ-500-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123