Keywords: MC68MH360, 68360, Motorola, processor bus, interface, parallel, serial, communications, single chip transceivers, STCs, TDM, PCM, serial bus, data processor bus

APPLICATION NOTE 319

DS2152, DS2154, DS21x5Y, and DS2155 Interfacing to the MC68360 (QUICC32)

Aug 13, 2002

Abstract: Application note 319 contains information necessary to interface the Motorola MC68360 processor to many of the Dallas Semiconductor single chip transceivers (SCTs). The application note covers interfacing both the address and data processor bus and the communications serial bus. Interfacing the processor bus of the MC68360 to the SCT is straightforward and mapping of address and data lines are shown in detail. Depending on the application, it may be necessary to add external logic to latch the address and data pins isolate other peripheral on the processor bus. The MC68360 contains two serial interfaces, either of which can be used to communicate directly with the SCT. The communication serial bus pin, clock names and descriptions for the MC68360 are located in diagrams in the application note. An example circuit diagram is provided for the processor interface as well as the communication serial interface. The goal of the application note is to give the designer enough information to begin a design based on the MC68360 processor.

Overview

Interconnections between the DS2152, DS2154, DS21x5Y, or DS2155 and the Motorola MC68MH360 (QUICC32) are shown in **Figure 1**. The MC68MH360 can be configured as an HDLC controller implementing protocols such as LAPD for T1 FDL, DS0 channel SS7, or the E1 Sa bits.

However, the DS2152, DS21x52 and DS2155 have a built-in HDLC controller for the T1 FDL. Any combination of the QUICC32's SCCs and SMCs can be processed through an internal timeslot assignor onto one or two time-division multiplex channels, TDMA and TDMB. In the configuration shown, TDM channel A is used for timeslots 0 to 23 (T1) or 0 to 31 (E1), and TDM channel B is used optionally for the Sa bit (E1). Refer to the MC68360 Quad Integrated Communications Controller User's Manual for complete details.

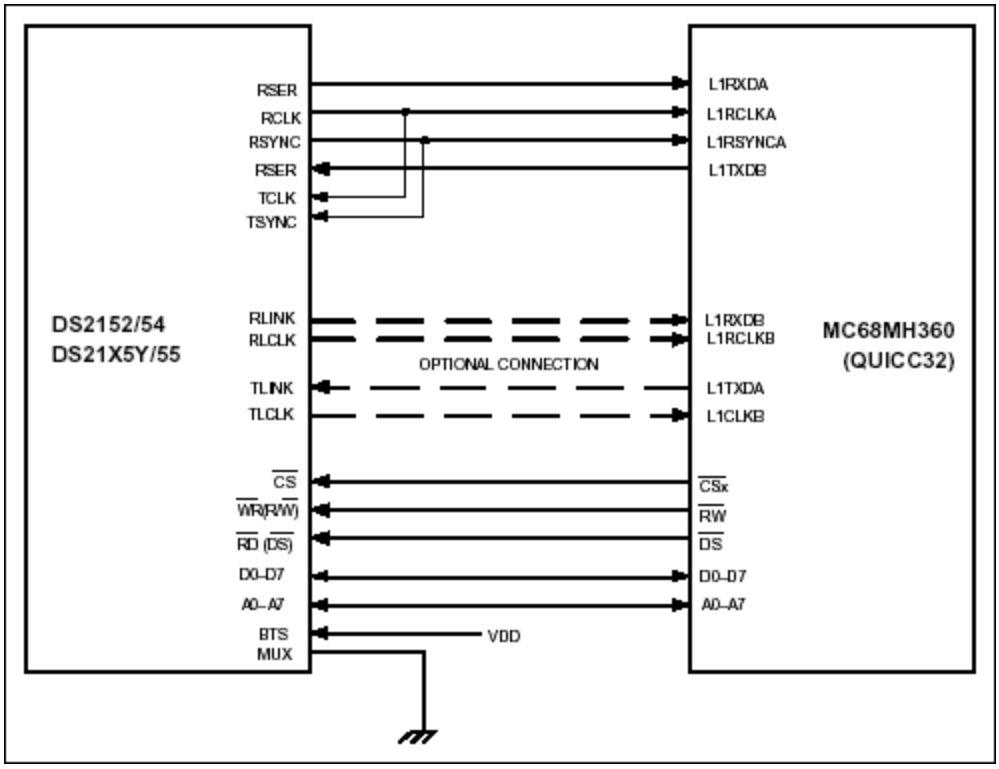

Figure 1. DS2152, DS2154, DS21x5Y, or DS2155–QUICC32 Interconnections.

DS2152, DS2154, DS21x5Y, and DS2155 Notes:

1. Other signals affecting operation of device are not shown.
2. Example circuit has RSYNC in output mode.

MC68360 Notes:

1. Other signals affecting operation of device are not shown.
2. Use SI mode register to:
   A. Set up transmit and receive frame-sync delays (0 to 3 clocks) to mask the F-bit in T1 applications.
   B. Set clock edges for transmit on rising edge and receive on falling edge. CEA = CEB = 0.
   C. In the above example, TDM channel A has a common transmit/receive clock and sync. CTRA = 1. Use the TIMESLOT ASSIGNER to ignore Timeslot 0 for E1 mode.

Related Parts		
DS21352	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21354	3.3V/5V E1 Single Chip Transceivers (SCT)	
DS2152	Enhanced T1 Single Chip Transceiver	
DS2154	Enhanced E1 Single Chip Transceiver	
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples

DS21552	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21554	3.3V/5V E1 Single Chip Transceivers (SCT)	Free Samples
DS21Q55	Quad T1/E1/J1 Transceiver	

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APPLICATION NOTE 319, AN319, AN 319, APP319, Appnote319, Appnote 319