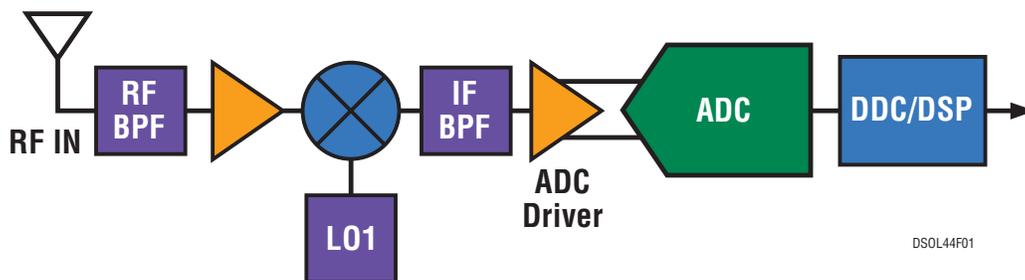


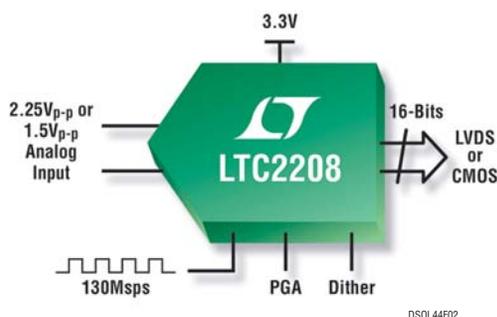
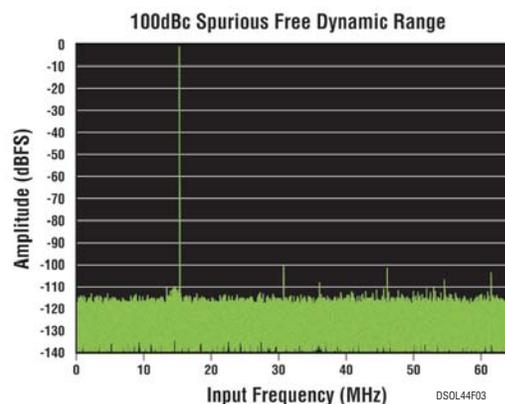
High Sensitivity Receiver Applications Benefit from Unique Features in 16-Bit 130MSPS ADC

by Alison Smith


Figure 1. Direct IF to Digital Single Conversion Receiver

Wireless receiver design requires extreme care in dealing with noise sources that affect the Analog-to-Digital Converter (ADC). High sensitivity receivers such as in satellite or basestation applications demand the highest dynamic range and therefore need to focus on minimizing the noise contribution from every possible source (Figure 1). These include nonlinearities in the ADC and digital feedback from the data output bus. This application note will discuss the LTC[®]2208 (Figure 2), a 16-bit 130MSPS high performance pipelined ADC that is

tailored for the most demanding wideband, low noise, receivers (Figure 3). The LTC2208 ADC addresses the key requirements for maximizing performance of high sensitivity receivers. Here we describe the application of its unique features to simplify receiver design and improve overall system performance. The first is an internal dither circuit to address ADC nonlinearity errors and the second is a digital output randomizer that minimizes digital feedback from the data output bus.


Figure 2. LTC2208 16-Bit 130MSPS ADC

Figure 3. LTC2208 64k FFT
 $F_{IN} = 15.2\text{MHz}$, $A_{IN} = -1\text{dB}$, 2.25V_{p-p}

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Internal Transparent Dither Circuit

Multi-stage converters can potentially contain sources of error that can significantly affect the ADC's spurious free dynamic range (SFDR). The effect of integral non-linearity errors (INL) can be seen as dips in the SFDR curve at more than 10 or 20dB below full-scale (Figure 4). LTC2208 has a linear transfer function with very low INL error; however at these low level inputs, only a small range of the transfer curve is utilized such that even slight linearity imperfections will generate unwanted harmonics.

To maximize SFDR for low level signals, the LTC2208 provides an on-chip dither feature to decorrelate (randomize) the effects of linearity errors at certain locations along the transfer curve. By dithering the input using a pseudo-random number generator driving an internal dither DAC

as shown in Figure 5, the ADC is forced to operate over a wider range of the transfer curve. The pseudo-random number is then subtracted from the ADC result with only a small amount of dither leak-through. The correlated spurious tones are thus converted to random noise that can be reduced by processing gain.

The LTC2208 eliminates the complexity required by external dither circuits that consume valuable ADC bandwidth and head room. As can be seen in Figure 6, the internal transparent dither circuit dramatically improves the ADC's SFDR response well below 100dBc for low level input signals, allowing the ADC to maintain its high dynamic range specification with only a small degradation to the noise floor.

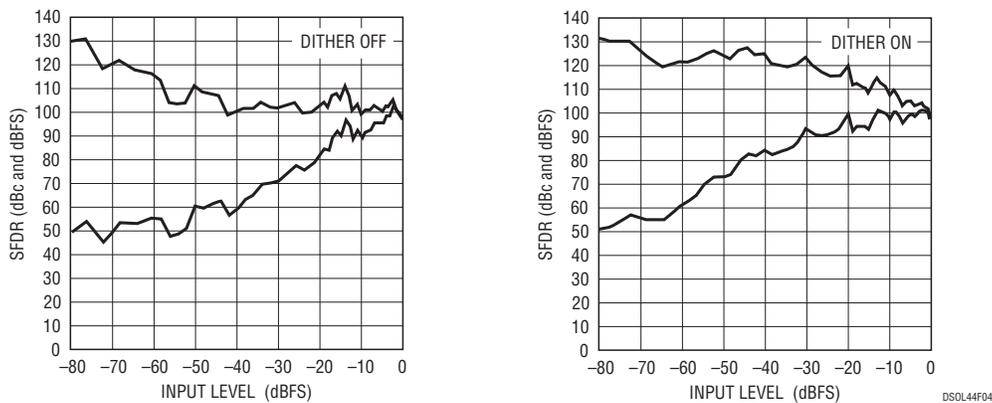


Figure 4. SFDR vs Input Level, $F_{IN} = 15\text{MHz}$

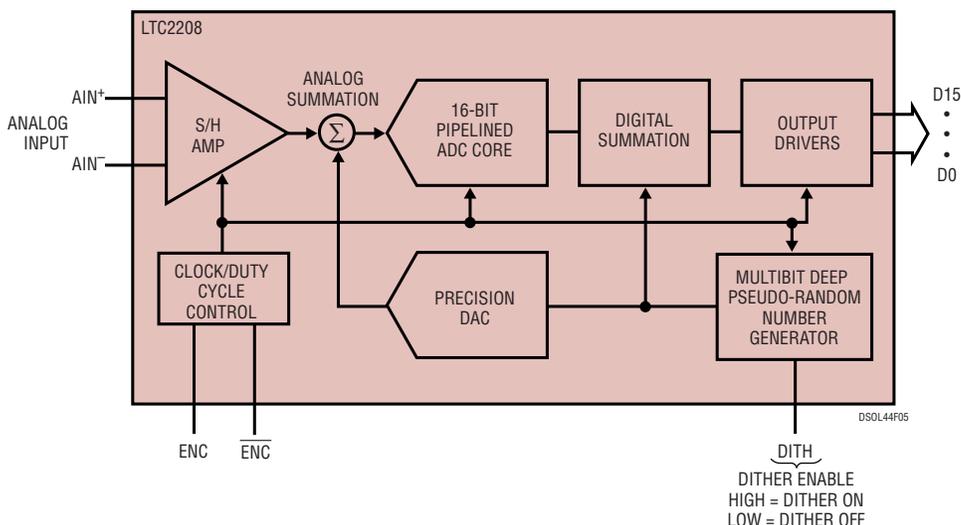


Figure 5. Functional Block Diagram of Internal Dither Circuit

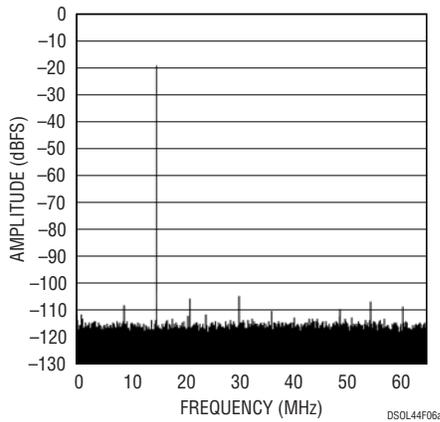


Figure 6a. A 70MHz Low Level Signal with Internal Dither Off. Low Level Tones Are Caused by Small INL Errors in the ADC.

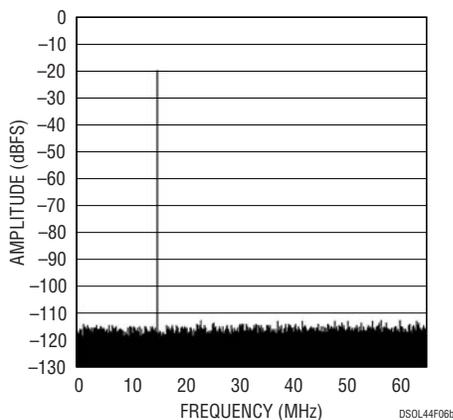


Figure 6b. The Same Conditions with Internal Dither On. Correlated Spurious Tone Energy Has Been Converted to Random Noise

Digital Output Randomizer

Another way to improve dynamic range performance is to eliminate the generation of unwanted tones caused by digital feedback from the ADC outputs. Digital feedback may occur due to capacitive coupling, ground currents or inductive coupling. While good layout can help reduce the effects of digital coupling, it may not be enough to eliminate the problem. One solution is to reduce the digital output voltage swing that will correspondingly reduce digital noise coupled into the analog circuitry. The LTC2208 offers two output modes that have reduced digital output

swing: low voltage CMOS outputs or LVDS outputs. In the CMOS digital output mode, the drivers can operate on supply voltages as low as 0.5V without any speed penalty. In the LVDS output mode each output bit is a differential pair with a 0.35V_{P-P} swing.

In situations where LVDS or low voltage CMOS are still not enough, the LTC2208 provides an optional output digital randomizer to encode the data, the second unique feature offered by the LTC2208. The least significant bit (LSB) is combined using an exclusive-OR function with the other outputs before transmission. The received digital output bus can then be easily decoded by performing the reverse operation in the FPGA. Using this data encode scheme reduces the residual tone caused by digital feedback by 10dB to 15dB.

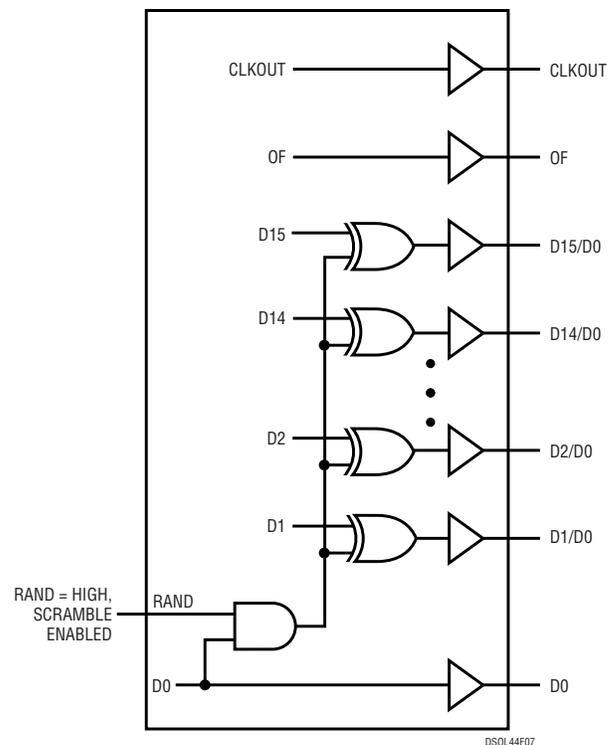


Figure 7. Functional Equivalent of Digital Output Randomizer

Wide Digitizing Bandwidth

In an IF sampling receiver, the sample and hold circuit in the ADC must have enough bandwidth and low distortion at the Intermediate Frequency (IF) to allow the entire band to be converted. By directly sampling an IF signal, the ADC acts like a mixer to eliminate the second analog down conversion stage, improving costs, system reliability and power dissipation. The LTC2208 is designed for high IF sampling, with an analog input bandwidth of 700MHz and can sample IF frequencies up to 250MHz while keeping distortion products below 83dBc.

For wideband receiver applications the LTC2208 can be used to capture and digitize the entire cellular band (30 MHz wide) as a single block of data. This wide-band input is likely to contain unwanted multi-carrier signals transmitted by other wireless systems. The LTC2208’s exceptional distortion performance and wide dynamic range enable it to resolve low level signals in the presence of these large interferers and blockers.

The high sampling rate of the LTC2208 provides an advantage when used in oversampling applications, using processing gain to improve the receiver’s SNR performance. Capturing a signal bandwidth of 30MHz requires an ADC with a sample rate of at least 60MSPs. However if the signal was sampled at a higher rate of 120MSPs the broadband noise floor is reduced by 3dB as given by the following equation

$$SNR \text{ Improvement (dB)} = 10 \times \log (\text{Sampling Rate}/2 \times \text{Signal Bandwidth})$$

This SNR improvement through processing gain is added to the SNR specified by the ADC.

With a sample rate of 130MSPs the LTC2208 is currently the fastest 16-bit ADC, easing stringent anti-aliasing filter requirements and improving system performance through processing gain.

PGA Input Drive

For direct sampled IF receiver systems, the required input drive level is an important consideration. The LTC2208 features a programmable gain amplifier (PGA) front-end that allows the designer to select a 1.5V_{P-P} input range and trade a little reduction in noise performance for lower input drive, which in turn can save substantial power in the input drive circuitry. The PGA allows the ADC reference voltage to remain at a constant voltage so that the input range can be reduced with minimal impact to SNR. Selecting the wider 2.25V_{P-P} range will however maximize the SNR performance of the ADC.

Additional Benefits and Features

Figure 8 shows the basic features of the LTC2208. The part is packaged in a small 9mm x 9mm QFN package and has some integrated bypass capacitance, freeing PCB real estate that would usually be consumed by large and costly decoupling capacitors. In addition, the power dissipation at 130MSPs is at a comparatively low 1250mW, avoiding the need for heat sinking.

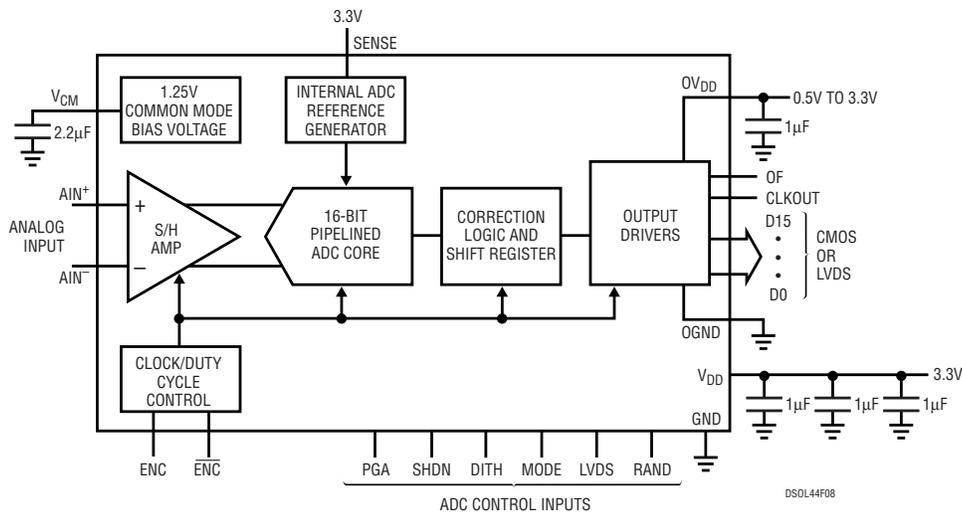


Figure 8. LTC2208 Block Diagram

Design Solutions 44

Designed for ease of use, it requires only a single 3.3V supply for operation and comes with a clock duty cycle stabilizer for maintaining the ADC performance over varying duty cycles. The LTC2208 can accept high frequency, wide dynamic range signals, offering a wide analog input bandwidth of 700MHz.

The LTC2208 family includes speed grades of 130MSPs, 105MSPs, 80MSPs, 65MSPs, 40MSPs, 25MSPs and 10MSPs all with superior SFDR and SNR performance. In addition to the 16-bit ADCs, 14-bit versions of this family will also be available. All devices are supported with demo boards for quick device evaluation. The display from Linear Technology's user friendly PScope ADC software evaluation tool is shown in Figure 9.

Conclusions

We have examined the ADC characteristics that often pose difficulties for high-sensitivity digital receivers and have shown how the LTC2208 delivers the solutions to those problems. The LTC2208 brings a new level of performance and an extensive feature-set that will help make even higher performance digital receivers possible. This new 16-bit family truly simplifies design and provides the flexibility to improve the dynamic range performance of the receiver system.

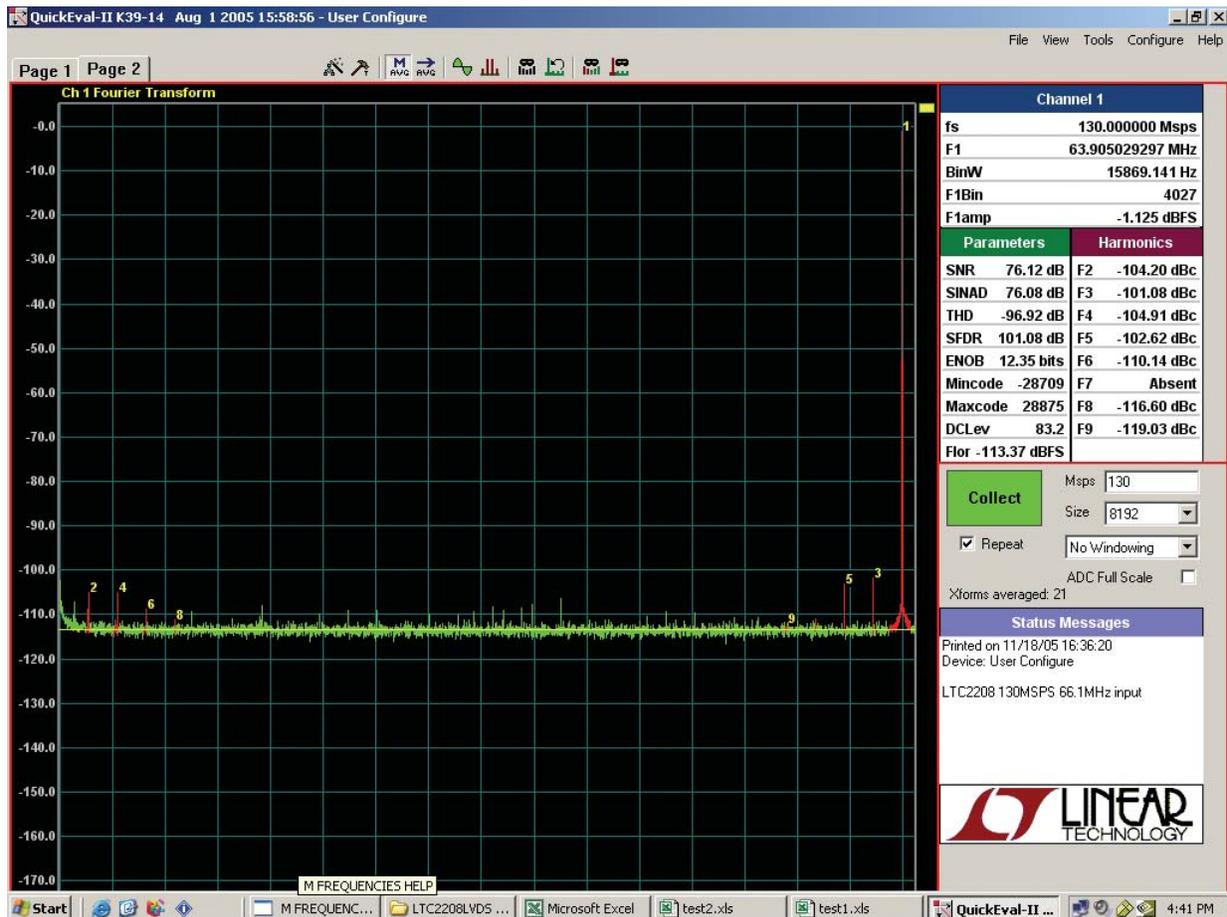


Figure 9. PScope ADC QuickEval Tool–LTC2208 Evaluation

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