Fused Lead Battery Charger ICs Need No Heat Sinks

Design Note 124

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The LT®1510 and LT1511 are high efficiency battery-charging chips capable of output powers up to 25W and 50W, respectively. These chips are intended for fast-charging batteries in modern portable equipment where space is at a premium. They are therefore packaged in low profile surface mount packages and run at a fairly high frequency (200kHz) to minimize the height and footprint of the complete battery charger. To minimize thermal resistance, these packages are specially constructed with the die-attach paddle connected (fused) directly to multiple package leads.

When operating these chips near their maximum power levels, extra care should be taken to minimize chip power dissipation and to keep the overall thermal resistance of the package-board combination as low as possible. Figure 1 shows a simple way to reduce power dissipation with no loss in performance. The LT1510 and LT1511 use an external diode (D2) and capacitor (C_X) to generate a voltage that is higher than the input voltage. This voltage is used to supply the base drive to the internal NPN power switch to allow it to saturate with a forced h_{FE} of about 50. Switching speed and on-resistance losses are minimized with this technique. The *required* boost voltage is only 3V, but with the normal connection of D2, the resulting boost voltage is equal to the battery voltage. Unnecessarily high base drive losses result with high battery voltages. Connecting D2 to a 3.3V or 5V supply (V_X) instead of to the battery reduces chip dissipation by approximately:

$$Power\ reduction = (V_{BAT} - V_X)(I_{CHRG})(V_{BAT})/(50)(V_{IN})$$

With a 20V adapter charging a 12.6V battery at 3A, and V_X = 3.3V, chip power is reduced by 0.35W.

Fused-lead packages conduct most of their heat out the leads. This makes it very important to provide as much PC board copper around the leads as is practical. Total thermal resistance of the package-board combination is dominated by the characteristics of the board in the immediate area of the package. This means both lateral thermal resistance across the board and vertical
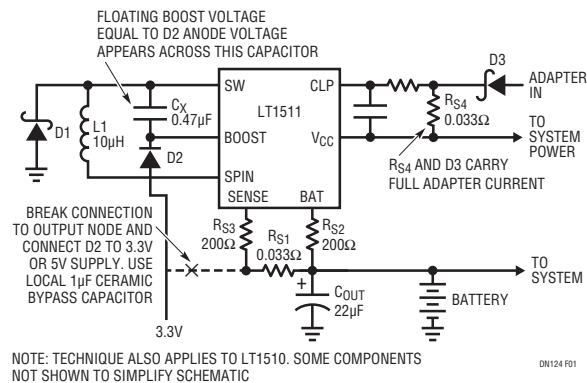

NOTE: TECHNIQUE ALSO APPLIES TO LT1510. SOME COMPONENTS NOT SHOWN TO SIMPLIFY SCHEMATIC

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Figure 1

thermal resistance through the board to other copper layers. Each layer acts as a thermal heat spreader that increases the heat sinking effectiveness of extended areas of the board.

Total board area becomes an important factor when the area of the board drops below about 20 square inches. The graphs in Figures 2 and 3 show thermal resistance versus board area for 2-layer and 4-layer boards. Note that 4-layer boards have significantly lower thermal resistance, but both types show a rapid increase for reduced board areas. Figures 4 and 5 show actual measured lead temperatures for chargers operating at full current. Battery voltage and input voltage will affect device power dissipation, so the data sheet power calculations must be used to extrapolate these readings to other situations.

Vias should be used to connect board layers together. Planes under the charger area can be cut away from the rest of the board and connected with vias to form both a low thermal resistance system and to act as a ground plane for reduced EMI.

Glue-on, chip-mounted heat sinks are effective only in moderate power applications where the PC board copper cannot be used, or where the board size is small.

Figure 2. LT1511 Thermal Resistance

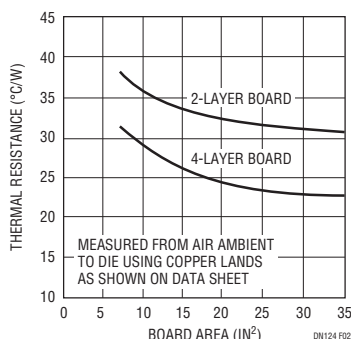**Figure 3. LT1510 Thermal Resistance**
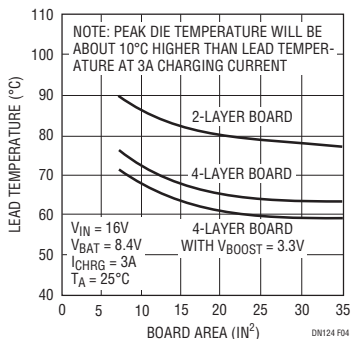

Figure 4. LT1511 Lead Temperature

Figure 5. LT1510 Lead Temperature

They offer very little improvement in a properly laid out multilayer board of reasonable size.

The suggested methods for a final check on chip operating temperature are to solder a small thermocouple on top of one of the IC ground leads or to use an IR sensor on top of the package. Using either method, the temperature measured either way will be about 10°C lower than actual peak die temperature when the charger is delivering full current. The 125°C rating of these charger chips means that lead temperature readings as high as 100°C (with maximum ambient temperature) are still comfortably within the device ratings.

Another consideration is the power dissipation of other parts of the charger and the surrounding circuitry used for other purposes. The catch diode (D1) will dissipate a power equal to:

$$P_{DIODE} = (I_{CHRG})(V_F)(V_{IN} - V_{BAT})/V_{IN}$$

With the V_{IN} = 16V, V_{BAT} = 8.4V, V_F = 0.45V, and I_{CHRG} = 3A, the diode dissipates 0.64W. Unfortunately, it must be located very close to the charger chip to prevent inductive spikes on the Switch pin. Increase in charger chip temperature due to power dissipation in D1 is about 12°C/W. D3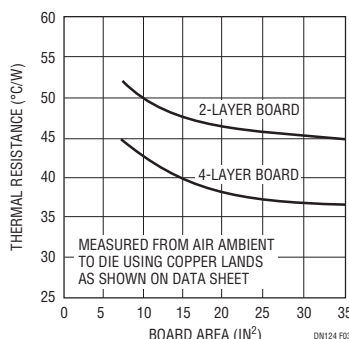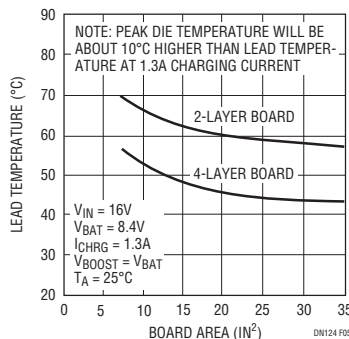 is used for input protection and can also dissipate significant power but it can be located away from the charger. The current sense resistors used with the LT1511 dissipate power equal to:

$$P(R_{S1}) = R_{S1}(I_{CHRG})^2$$

$$P(R_{S4}) = R_{S4}(I_{ADPT})^2$$

R_{S4} power depends only on charger output current, but R_{S1} carries full adapter current. These resistors, which typically dissipate a total of about 0.5W, will also increase chip temperature at about 12°C/W, assuming that they are close to the charger chip.

It is assumed that L1 contributes only slightly to chip temperature rise because its power dissipation is normally fairly low compared to its heat sinking ability. This will be true if a low loss core is used (Kool Mµ, etc.), and the winding resistance is less than $0.2V/I_{CHRG}$. If the charger is located near other high power dissipation circuitry, direct temperature testing may be the only accurate way to ensure safe device temperatures.

Finally, don't forget about losses in PC board trace resistance. A 100mil wide trace is huge by modern standards, but a pair of these traces six inches long, in 1/2oz copper, delivering 3A, would have a resistance of ≈ 0.12Ω, and a power loss of 1.1W!

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