LINEAR TECHNOLOGY

DESIGN NOTES

Hot Swap and Buffer I²C Buses

Design Note 263

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As server systems have grown, the number and complexity of input/output (I/O) cards that contain control circuitry to monitor the servers have grown in proportion. Zero down time systems require users to insert I/O cards into a live backplane. While many IC vendors have developed chips to safely Hot Swap™ the power supply and ground lines, until now no one has developed a monolithic solution to "hot swap" the system data (SDA) and clock (SCL) lines in I²C and SMBus systems. Expansion of these systems have made rise and fall time specifications difficult to meet, as the SDA and SCL capacitances of each I/O card add directly to those of the backplane. The LTC®4300-1 allows the user to plug I/O cards into a live backplane without corrupting the data transaction taking place on the backplane. It also provides bidirectional buffering, keeping the backplane and card capacitances isolated.

Figure 1 shows an application of the LTC4300-1 that safely hot swaps the SDA and SCL lines. The LTC4300 resides on the edge of a peripheral card, with the SCLOUT pin connected to the card's SCL bus, and the SDAOUT connected to the card's SDA bus. When the card is plugged into a live backplane via a staggered connector, ground makes connection first, followed by V_{CC}.

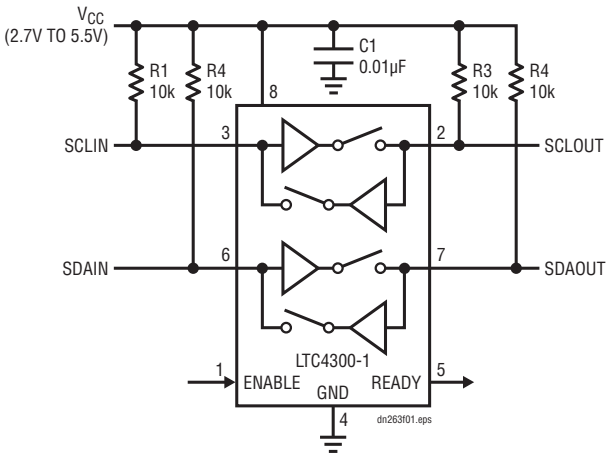

Figure 1. Using the LTC4300-1 to Hot Swap SDA and SCL Lines

After ground and V_{CC} connect, SDAIN and SCLIN make connection with the backplane SDA and SCL lines. During this time, the 1V precharge circuitry is active and forces 1V through 100k nominal resistors to the low capacitance (less than 10pF) SDA and SCL pins, minimizing the worst-case voltage differential these pins will see at the moment of connection. These precharge and low capacitance features result in minimal disturbances on the backplane SDA and SCL busses during hot swapping.

The voltages on the SDA backplane bus and LTC4300-1 SDAIN pin during card insertion are shown in Figure 2. A 100pF capacitor to ground is used to emulate the equivalent SDA bus capacitance. Just before the insertion, the backplane SDA bus is approaching 4V, while the LTC4300-1's SDAIN pin is precharged to 1V. Due to the high resistance and low capacitance of the SDAIN pin, the voltage on the pin rises up to the backplane voltage at the moment of insertion, whereas the backplane voltage is barely affected. The two signals are now shorted together.

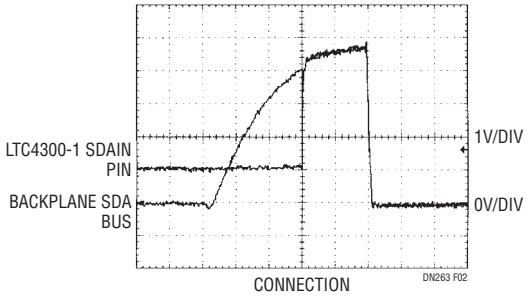

Figure 2. LTC4300-1 SDAIN Pin Connecting to Backplane SDA Bus

Once a Stop Bit or Bus Idle occurs on the backplane without bus contention on the card, the LTC4300-1 disables the precharge circuitry and activates input-to-output connection circuitry, joining the backplane SDA and SCL busses with those on the card.

Capacitance Buffering and Rise Time Accelerator Features

The key feature of the input-to-output connection circuitry is that it provides bidirectional buffering. Figure 3 shows an application that takes advantage of this feature. If the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise and fall time requirements difficult to meet. Placing an LTC4300-1 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the LTC4300-1 drives the capacitance on the card, and the backplane must drive only the low capacitance of the LTC4300-1. The LTC4300-1 further aids in meeting system rise time requirements by providing rise time accelerator circuits on all four SDA and SCL pins. Figure 4 shows the improved rise time provided by the accelerators for 10pF and 100pF equivalent bus capacitances.

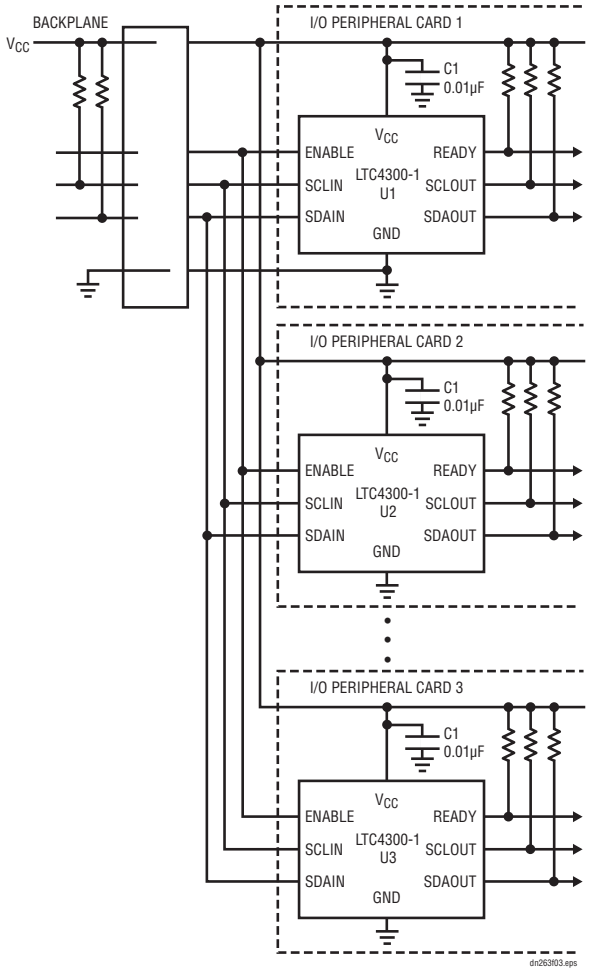

Figure 3. Multiple I/O Cards Plugging into a Backplane

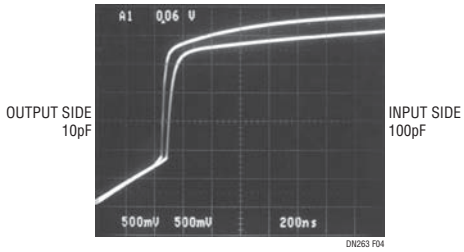

Figure 4. Rise Time Accelerators Pulling Up On 10pF and 100pF Capacitance

Conclusion

The LTC4300-1 allows users to plug an I/O card into a live backplane without corrupting the backplane SDA and SCL signals in 2-wire bus systems. In addition, the connection circuitry provides bidirectional buffering, keeping the backplane and card capacitances isolated. Rise time accelerator circuits provide additional help in meeting rise time requirements.

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dn263f_conv LT/TP 0801 375K • PRINTED IN THE USA