Keywords: MAX2831, WLAN, 802.11b/g, Transmit, Efficiency, Linearity, PA Current, Current

APPLICATION NOTE 4010

MAX2831 Power Amplifier (PA) Output Power and Bias-Current Optimization

Mar 23, 2007

Abstract: This article presents data and register settings for optimized power amplifier (PA) efficiency at various power levels for the MAX2831.

Introduction

Click here for an overview of the wireless components used in a typical radio transceiver.

The MAX2831 is a fully integrated transceiver with power amplifier (PA) for 802.11b/g applications. The bias current and output-matching network for the two-stage PA have been optimized to nominally deliver +18.5dBm while consuming 209mA from a 3.3V supply (at less than 5.6% EVM in 54Mbps (64-QAM) mode) while meeting 802.11g spectral mask requirements. At lower output-power levels, reprogramming the PA Bias Current Registers allows the bias current and overall PA current to be reduced for improved Tx efficiency while still meeting 802.11g requirements. When the PA bias current is optimized for +17dBm transmit power, a current savings of 26mA is achieved as compared with the nominal register setting. When operating at +3dBm transmit power, a current savings of 62mA is achieved as compared with nominal register setting. Further current savings can be achieved for a specific output-power level through optimization of the simple two-capacitor output-matching network.

Programming

Register 10 (A3:A0 = 1010) allows programming of the two-stage PA bias current. Bits D2:D0 allow optimization of the first-stage bias current, and bits D6:D3 allow programming of the second-stage bias current. **Table 1** summarizes the register settings and the equivalent MAX2831 EV kit bias-current settings.

Table 1. MAX2831 PA Bias-Current Register Settings

Power Amplifier First-Stage Bias Current		Power Amplifier Second-Stage Bias Current	
Register 10 (A3:A0 = 1010) Bit D2:D0	Equivalent Bias Current (µA)	Register 10 (A3:A0 = 1010) Bit D6:D3	Equivalent Bias Current (µA)
100	125	0100	160
010	75	0011	120

001	50	0011	120
001	50	0010	80

Results

Figure 1 and **Table 2** summarize the current savings that can be achieved by optimizing the PA bias current. **Table 3** and **Figure 2** summarize the performance for nominal register settings. **Figures 3**, **4**, and **5** summarize performance for register settings optimized for +17dBm and +15dBm and their output spectrums, respectively. **Figure 6** summarizes performance for register settings optimized for +12dBm and +9dBm. **Figure 7** provides the measurement setup.

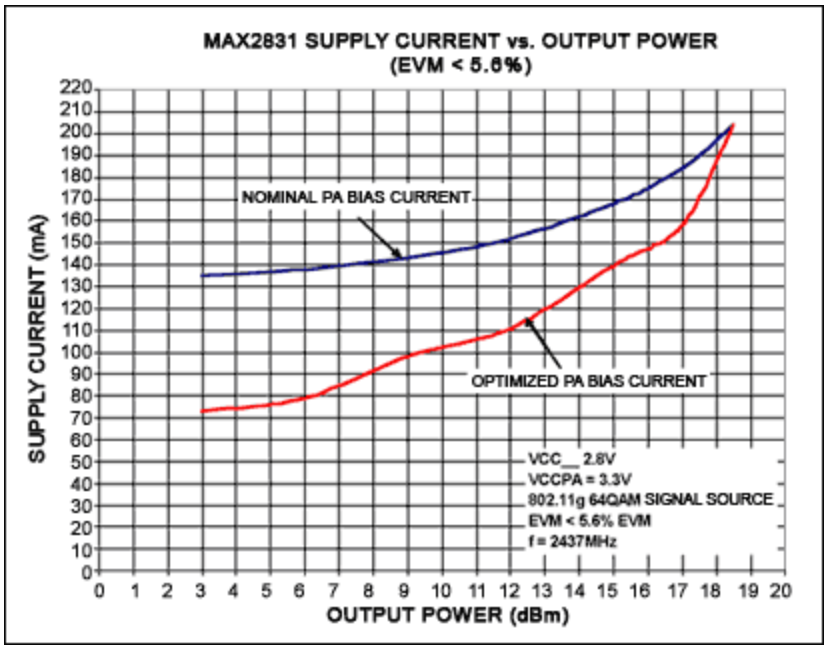

Figure 1. MAX2831 supply current vs. output power for nominal PA bias and PA bias current optimized for specific output-power levels.

Table 2. Register Settings and Measured Results with Bias Current Optimized for Output Power (V_{CCTX} = 2.85V, V_{CCPA} = 3.3V, Signal Source = 90mV_{RMS} 802.11g 64-QAM OFDM (54Mbps), f = 2437MHz, I_{CCTX} = 81mA)

Measured Results				Register Settings (See MAX2831 EV Kit Control Software)		
P_{OUT} (dBm)	EVM (%)	PA Current (mA)	PA Current Savings (mA)	Tx VGA Gain (SPI™) [Register 12 (A3:A0 = 1100) Bit D5:D0]	PA Driver Output Current (µA) [Register 10 (A3:A0 = 1010) Bit D2:D0]	PA Output-Stage Bias (µA) [Register10 (A3:A0 = 1010) Bit D6:D3]
2.9	3.5	73	**61**	35 (100011)	50 (001)	80 (0010)
6.1	5.1	79	**59**	41 (101001)	50 (001)	80 (0010)
9.2	4.4	98	**45**	44 (101100)	50 (001)	120 (0011)
12.1	5.6	111	**41**	50 (110010)	50 (001)	120 (0011)

15.2	5.0	140	**28**	53 (110101)	75 (010)	120 (0011)
17.0	5.3	158	**26**	57 (111001)	75 (010)	120 (0011)
18.7	5.5	204	**—**	57 (111001)	125 (100)	160 (0100)

Table 3. MAX2831 Output Power, Supply Current, EVM and Register Settings Optimized for +18.5dBm (Nominal)

(V_{CCTX} = 2.85V, V_{CCPA} = 3.3V, Signal Source = 90mV_{RMS} 802.11g 64-QAM OFDM (54Mbps), f = 2437MHz, I_{CCTX} = 81mA)

Measured Results			Register Settings (See MAX2831 EV Kit Control Software)		
P_{OUT} (dBm)	EVM (%)	PA Current (mA)	Tx VGA Gain (SPI) [Register 12 (A3:A0 = 1100) Bit D5:D0]	PA Driver Output Current (µA) [Register 10 (A3:A0 = 1010) Bit D2:D0]	PA Output-Stage Bias (µA) [Register10 (A3:A0 = 1010) Bit D6:D3]
3.3	2.1	135	24 (011000)	125 (100)	160 (0100)
6.3	2.3	138	30 (011110)	125 (100)	160 (0100)
9.2	2.6	143	36 (100100)	125 (100)	160 (0100)
12.2	2.9	152	43 (101011)	125 (100)	160 (0100)
15.1	3.4	168	49 (110001)	125 (100)	160 (0100)
17.1	4.1	184	53 (110101)	125 (100)	160 (0100)
18.7	5.5	204	57 (111001)	125 (100)	160 (0100)

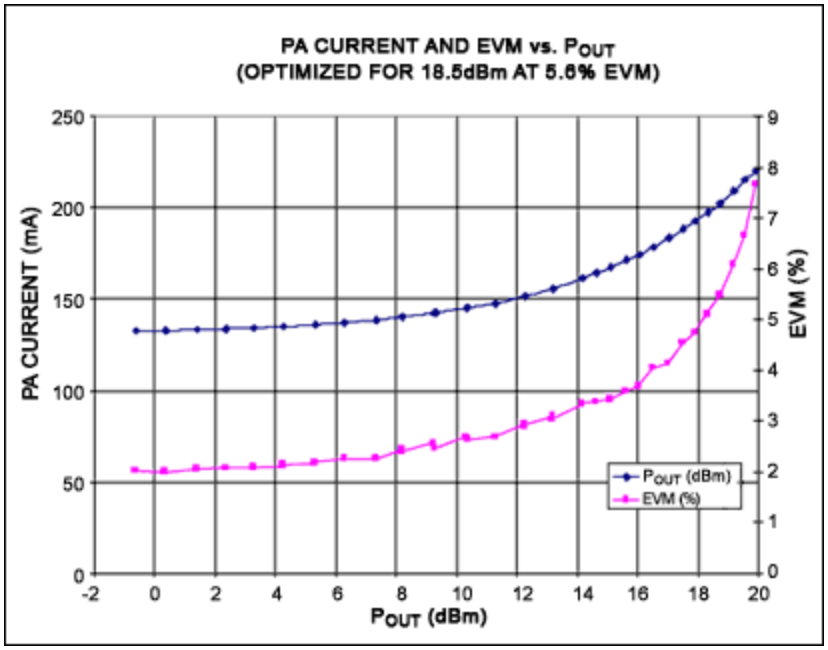

Figure 2. MAX2831 output power, supply current, and EVM optimized for +18.5dBm. (A3:A0 = 1010, D6:D3 = 0100, D2:D0 = 100)

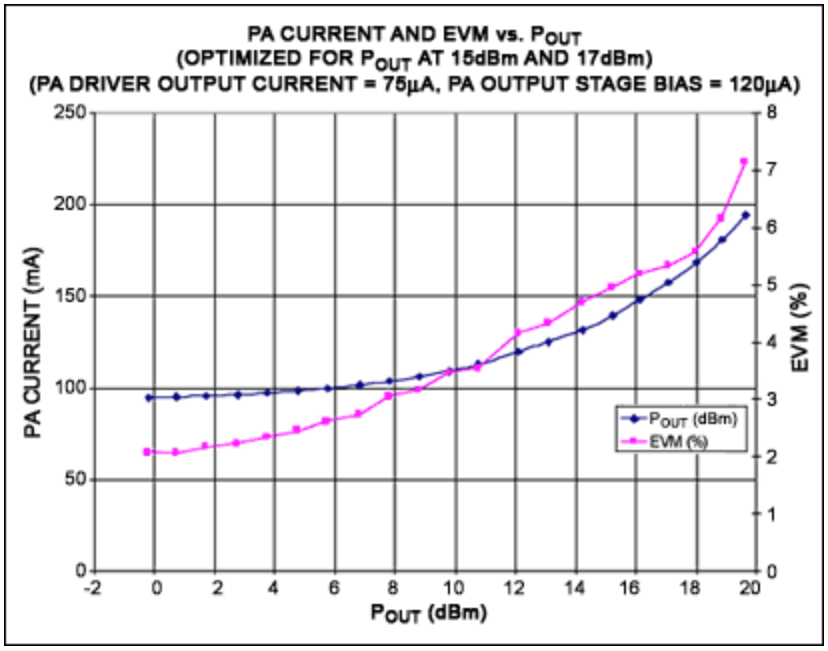

Figure 3. MAX2831 output power, supply current, and EVM with register settings optimized for +17dBm and +15dBm. (A3:A0 = 1010, D6:D3 = 0011, D2:D0 = 010)

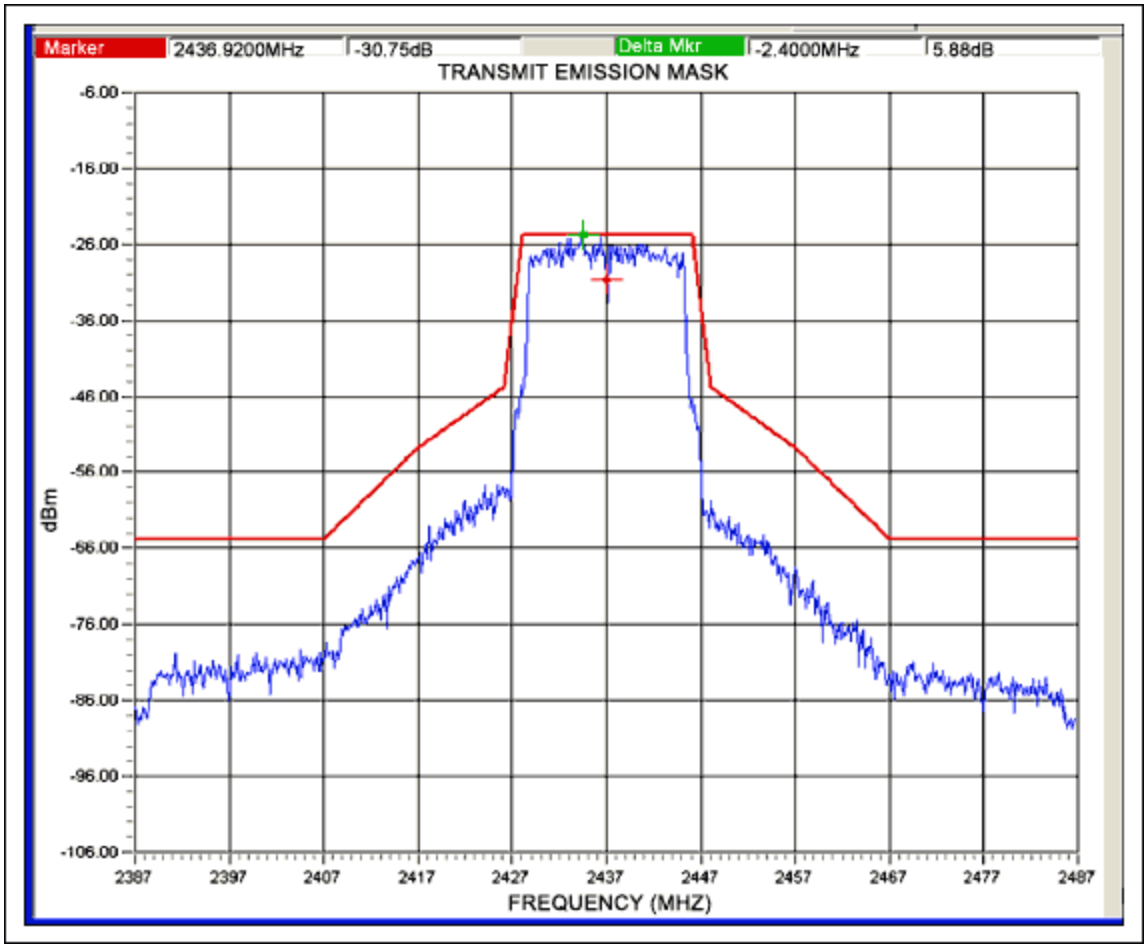

Figure 4. Output spectrum at +17dBm (red line denotes 11g spectral mask requirements). (A3:A0 = 1010, D6:D3 = 0011, D2:D0 = 010)

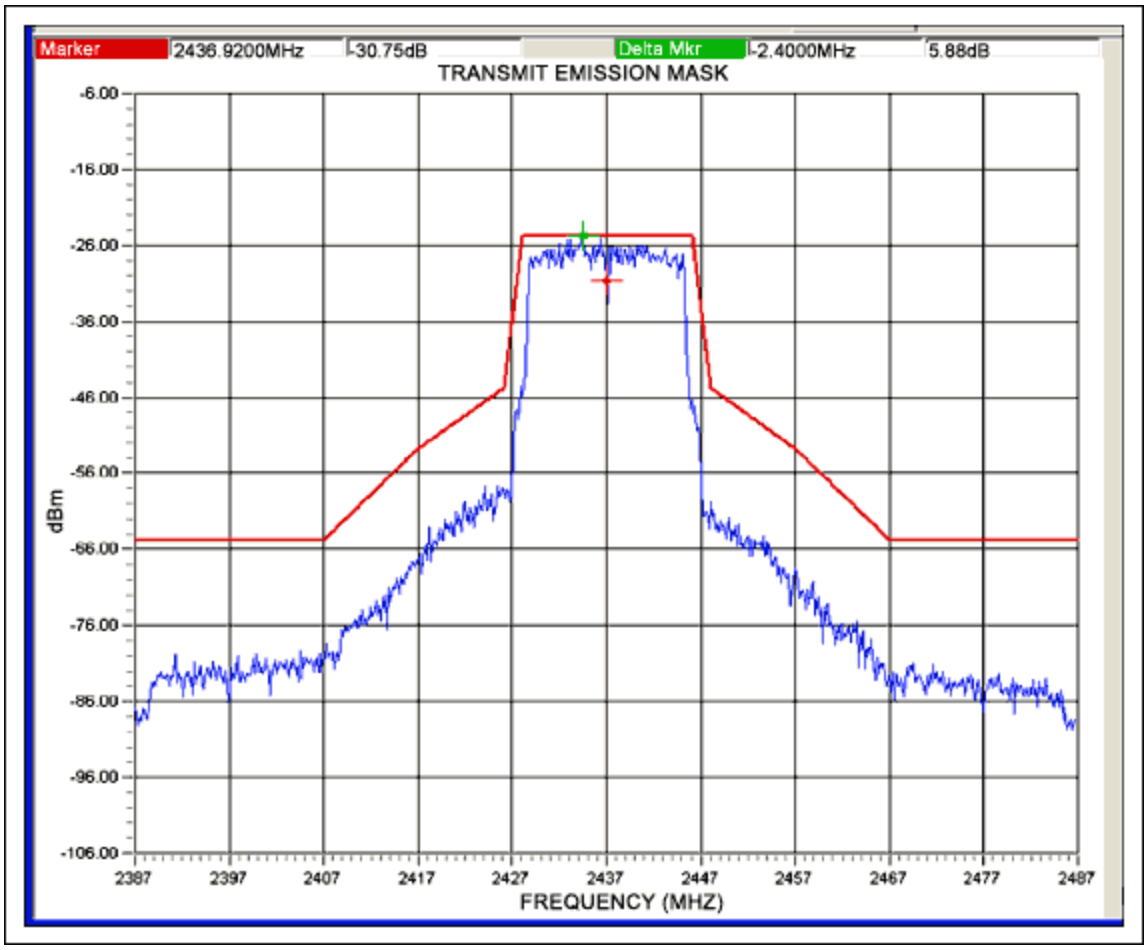

Figure 5. Output spectrum at +15dBm (red line denotes 11g spectral mask requirements). (A3:A0 = 1010, D6:D3 = 0011, D2:D0 = 010)

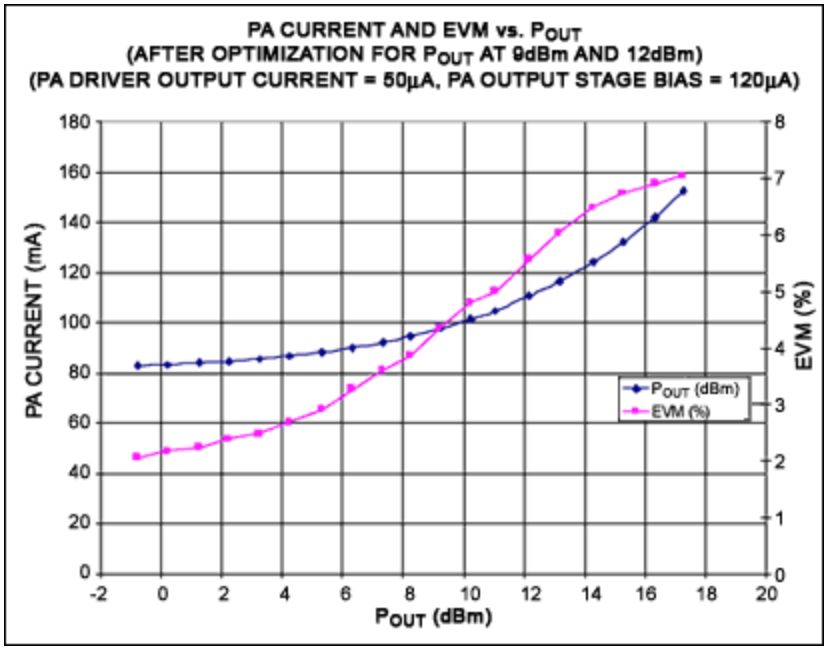

Figure 6. MAX2831 output power, supply current, and EVM with register settings optimized for +12dBm and +9dBm. (A3:A0 = 1010, D6:D3 = 0011, D2:D0 = 001)

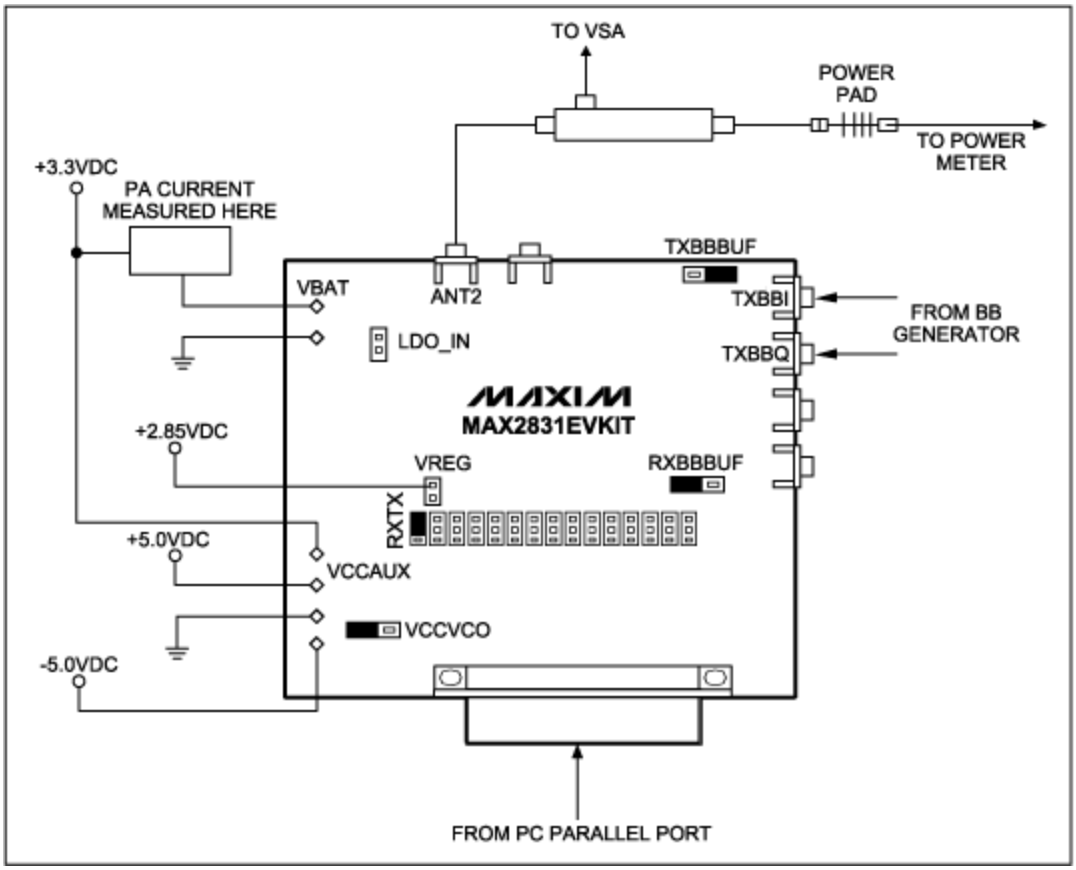

Figure 7. Test setup diagram for the MAX2831 wireless LAN transceiver.

Related Parts	
MAX2831	2.4GHz to 2.5GHz, 802.11g RF Transceivers with Integrated PA

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