NOTES:

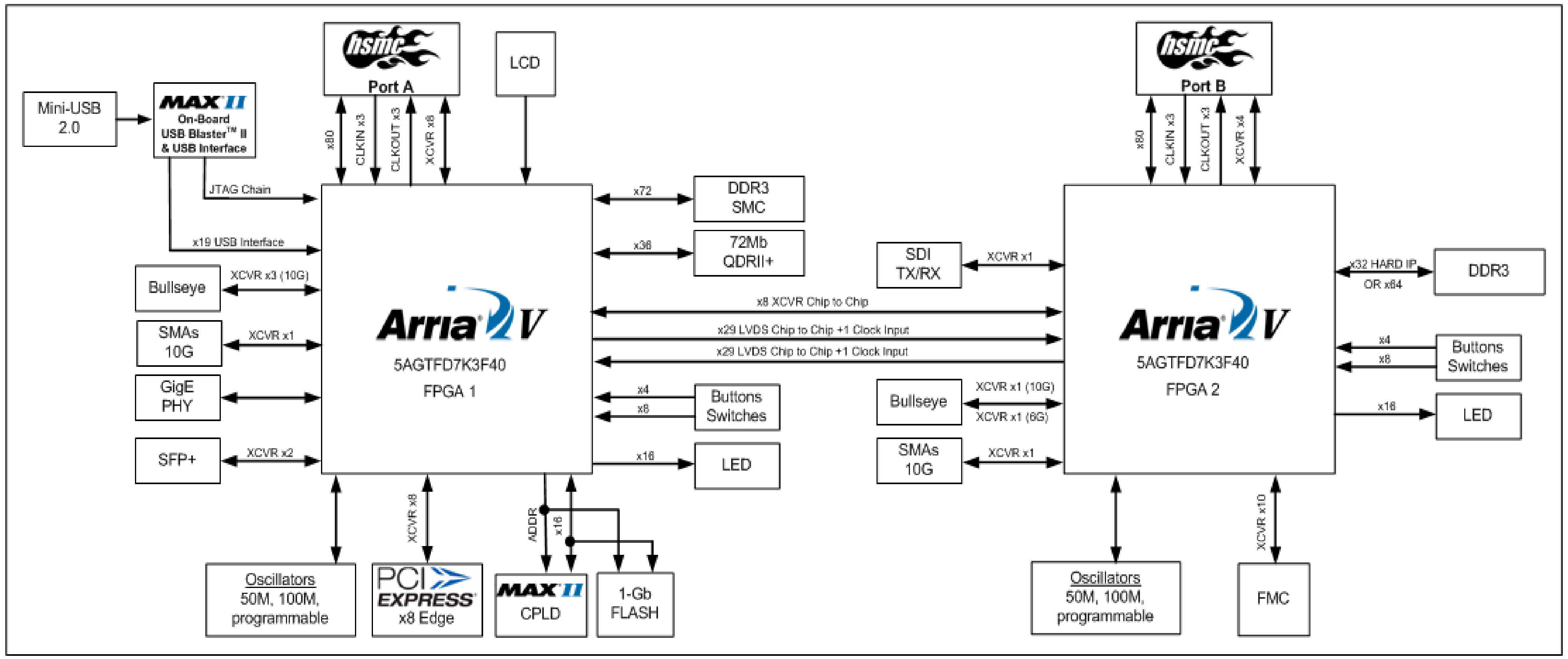
1. Project Drawing Numbers:

Raw PCB	100-0320804-C1
Gerber Files	110-0320804-C1
PCB Design Files	120-0320804-C1
Assembly Drawing	130-0320804-C1
Fab Drawing	140-0320804-C1
Schematic Drawing	150-0320804-C1
PCB Film	160-0320804-C1
Bill of Materials	170-0320804-C1
Schematic Design Files	180-0320804-C1
Functional Specification	210-0320804-C1
PCB Layout Guidelines	220-0320804-C1
Assembly Rework	320-0320804-C1

2. 1709 Parts, 88 Library Parts, 1966 Nets, 9887 Pins
3. This board was designed for either the Arria V GX or GT devices

REV	DATE	PAGES	DESCRIPTION
A	12/14/2011	All	Initial Released Rev A
B	5/16/2012	Many	1. Separated VCC into 2 power rails (VCC and VCCP) including decoupling caps. 2. A5_VCCIO_FMC power pin correction 3. Added FM_A26 to MAX II device 4. Corrected FPGA 2 config bus 5. hardwired CLKIN50 to enabled on power up 6. Constrain MSEL pins to known states for both FPGAs 7. Tie FPGA pin N6 to GND 8. Mini-USB pin 5 coonected to board GND 9. Correct reverse power diode pin connections 10. Add CLOCK_SDA and CLOCK_SCL to FPGA1 11. Removed FPGA2 and MAXII devices from JTAG chain 12. Removed unused PCIe JTAG circuit 13. Added x2 clock buffer for eye measurement via Bullseye cables 14. C2C_DIN_P/N9 pin swapped 15. Reduced C2C to x29 and added C2C clock inputs 16. PCIE_PERSTn moved to pin N9 17. MAX3378 decoupling added 18. Moved DDR3*_CKE to discrete 4.7K pulldown 19. Moved DDR3*_RESET to discrete 51 Ohm to 1.5V 20. Moved SMA AC-coupling from TX pins to RX pins 21. Removed backplane interface
C	12/19/2012	Many	1. Added 2 caps in parallel with R23 and R28 in LTC3880 2. Added Resistors and caps in line with the pins on the LTM4628 and LT3855 for Future debugging (U27.J7,U26.J7,U3.24) 3.Changes C118 to 1206, Cap change to 10V rating for C138, C334, C929, C930.

Arria V GT FPGA Development Kit Board



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Title **Arria V GT FPGA Development Kit Board**

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FPGA 1 Package Top View

BANK 7A
BANK 7B
BANK 7C
BANK 7D
VCCIO = 2.5V
Chip-to-Chip (LVDS)
LCD, USER IO

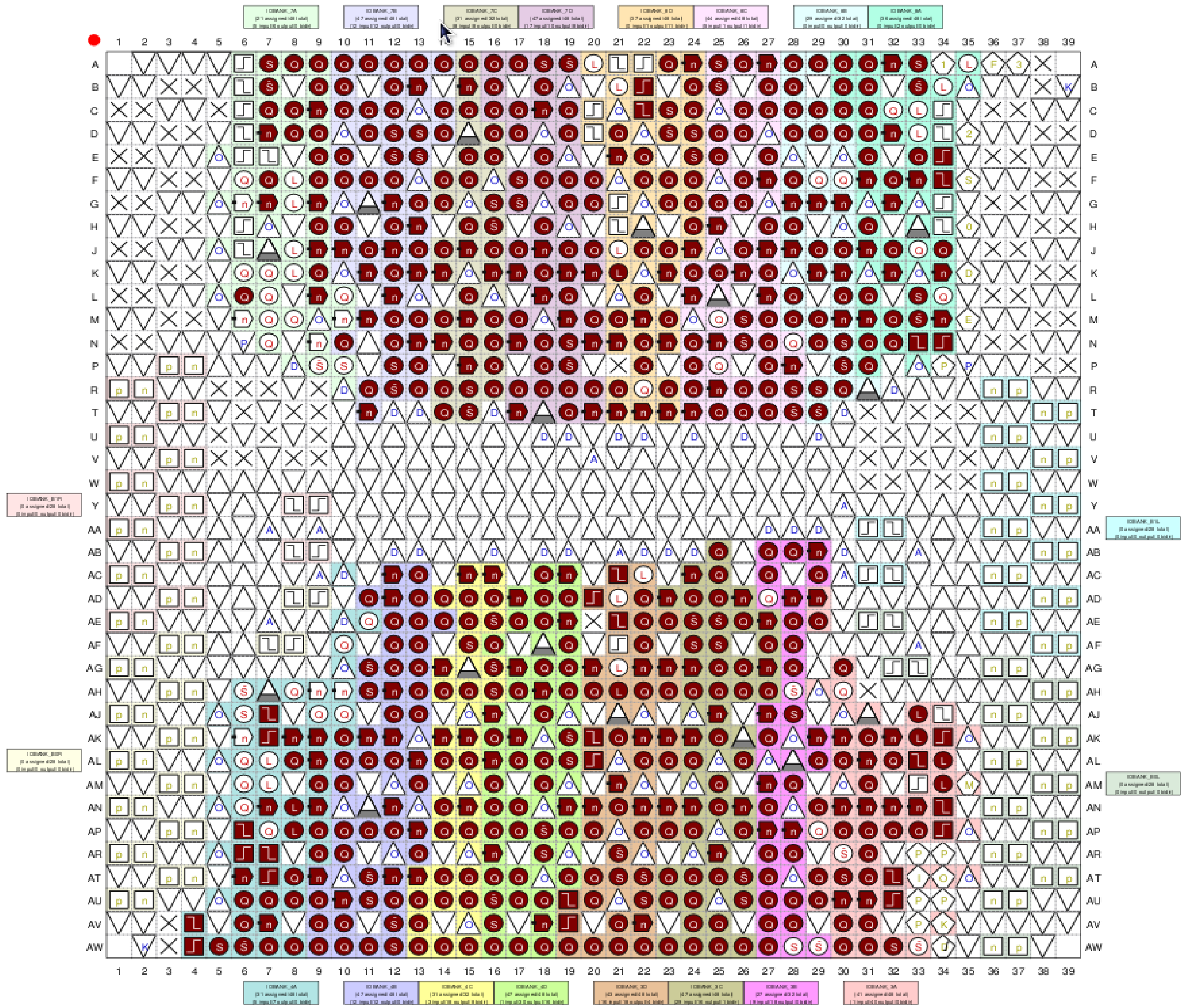
BANK 8A
BANK 8B
BANK 8C
BANK 8D
VCCIO = 1.5V
DDR3, Embedded USB Blaster II

Top View - Flip Chip

Arria V - 5AGXFB3H4F40C5

XCVR BANK QR2 (GT option only)
HSMC Port x4 (Total XCVR x8)
Bullseye SMAs (6G) x2
Bullseye SMA (10G)

XCVR BANKS QR0, QR1
HSMC Port A x4
Chip-to-Chip x8



XCVR BANK QL2 (GT option only)
SFP+ x1
Bullseye SMA (10G)

XCVR BANKS: QL0, QL1
PCI Express x8
SFP+ x1
SMA (6G)

BANK 4A
BANK 4B
BANK 4C
BANK 4D
VCCIO = 2.5V
HSMA,
SFP+ control,
User IO
Ethernet, PCIe,
SFP+ control

BANK 3A
BANK 3B
BANK 3C
BANK 3D
VCCIO = 1.8V
QDRII+, FM
FLASH, FM bus

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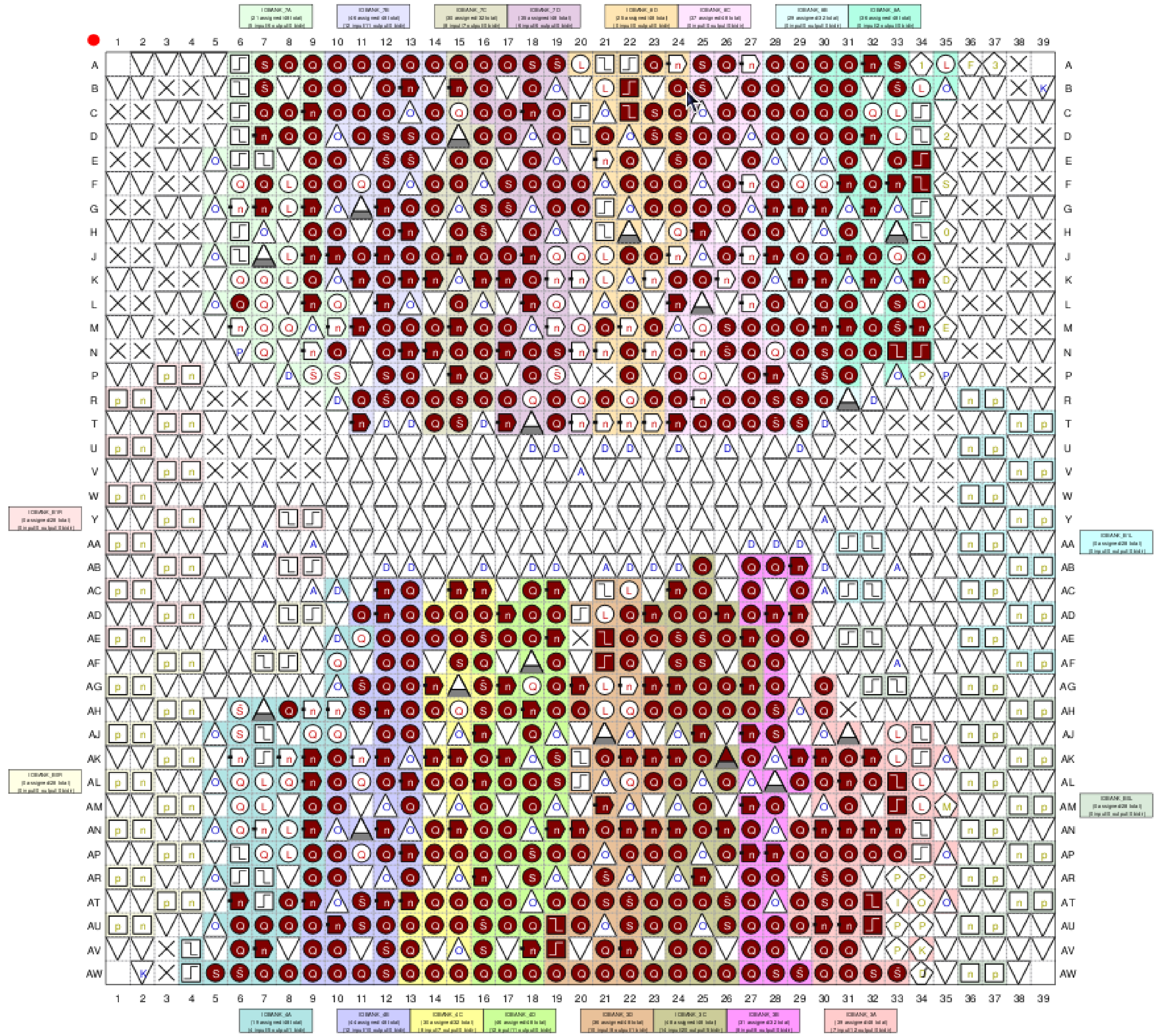
FPGA 2 Package Top View

BANK 7A
BANK 7B
BANK 7C
BANK 7D
VCCIO = 2.5V
Chip-to-Chip (LVDS)

BANK 8A
BANK 8B
BANK 8C
BANK 8D
VCCIO = 1.5V
DDR3 x32 (2 Individual Interfaces)

Top View - Flip Chip

Arria V - 5AGXFB3H4F40C5



XCVR BANK QR2 (GT option only)
FMC x6 (Total FMC x10)

XCVR BANK QL2 (GT option only)
Bullseye SMA (10G)

XCVR BANKS QR0, QR1

HSMC Port B x4
SDI
FMC x4
Bullseye SMA (6G)
SMA (10G)

XCVR BANKS: QL0, QL1

Chip-to-Chip x8

BANK 4A
BANK 4B
BANK 4C
BANK 4D
BANK 3D
VCCIO = 2.5V
FMC

BANK 3A
BANK 3B
BANK 3C
VCCIO = 2.5V
HSMC Port B
SDI
USER I/O

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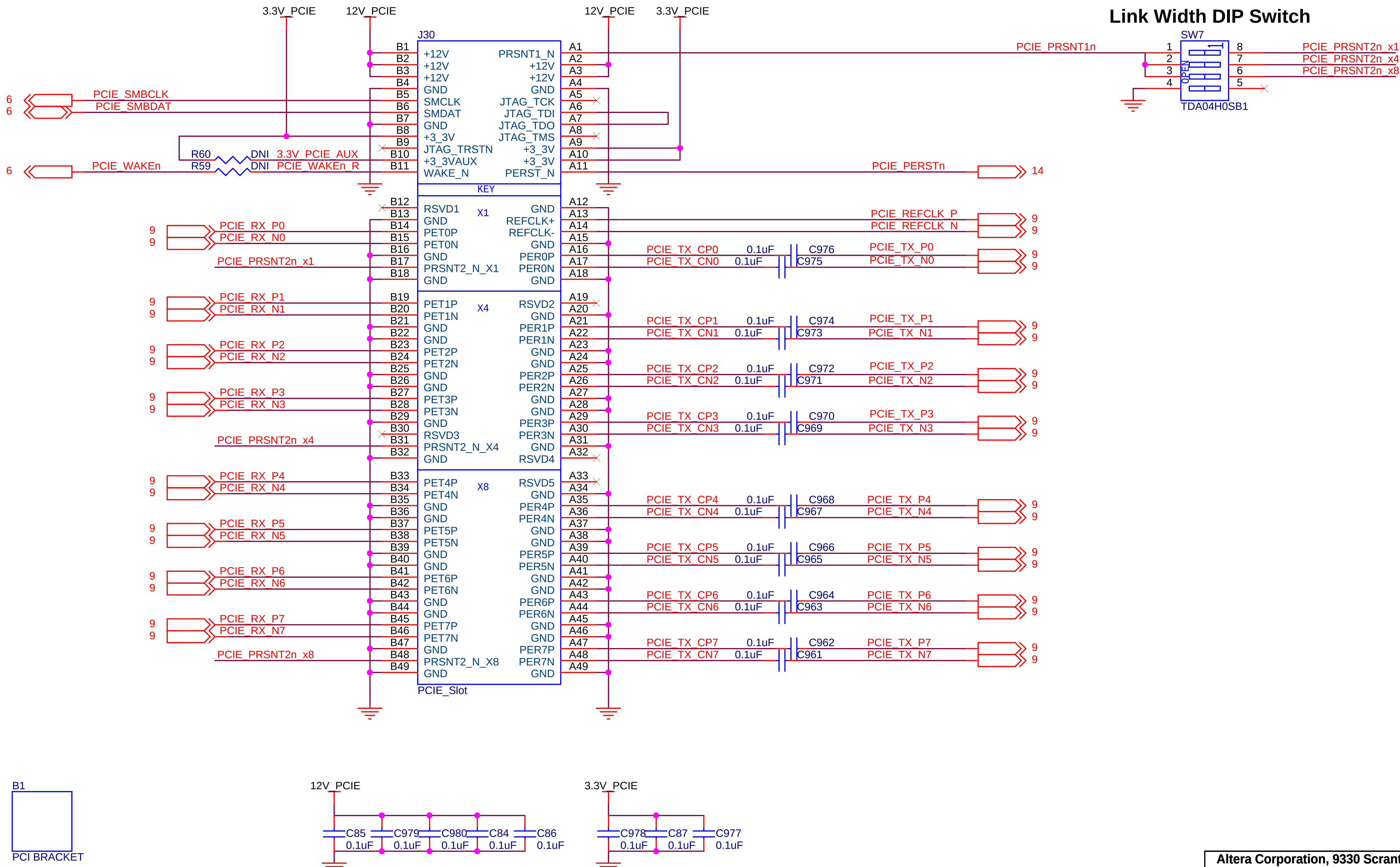
PCI Express Edge Connector



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Arria V GT FPGA 1, Bank 3

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Size: B | Document Number: 150-0320804-C1 (6XX-44164R) | Rev: C

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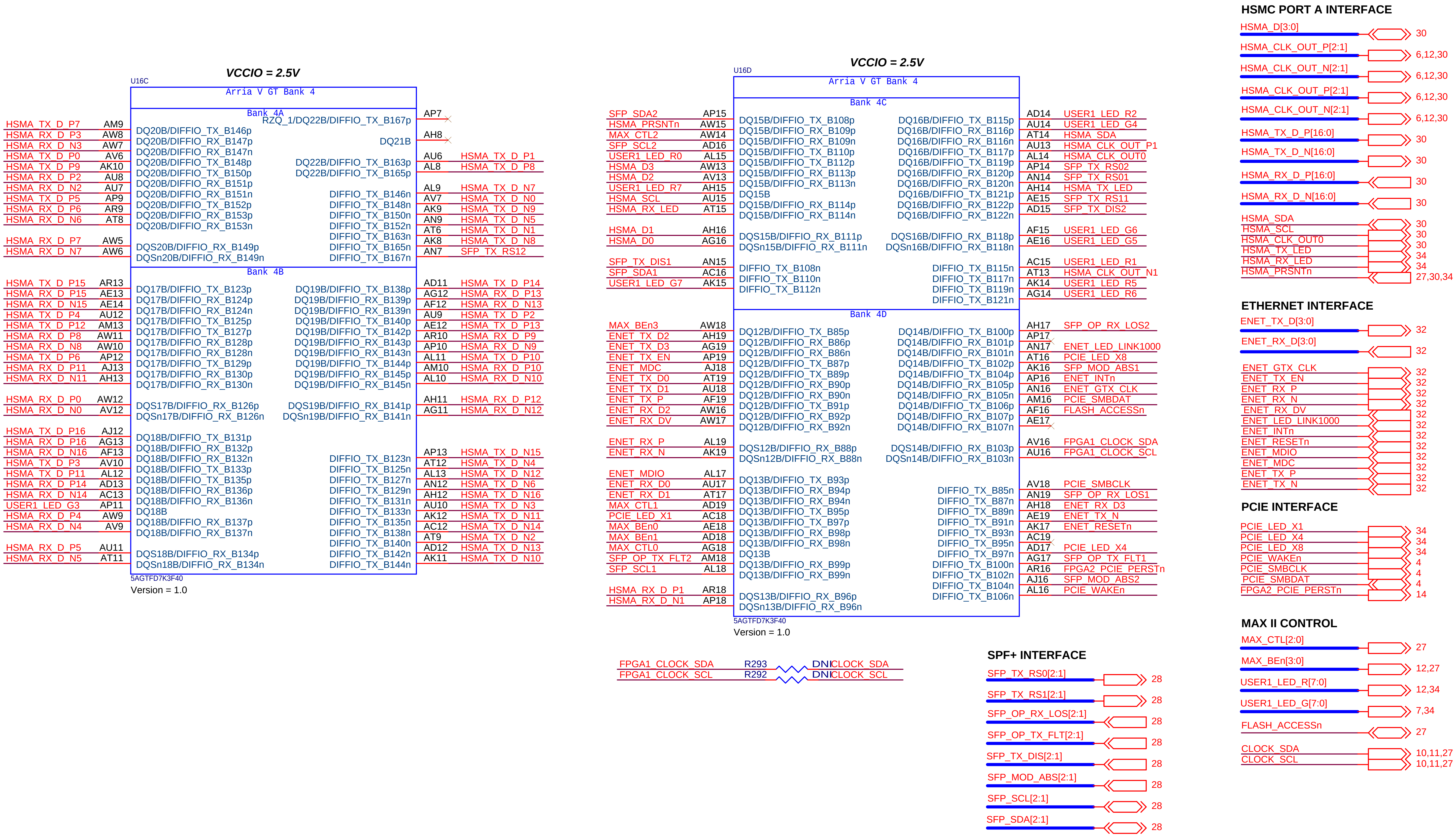
Arria V GT FPGA 1, Bank 4



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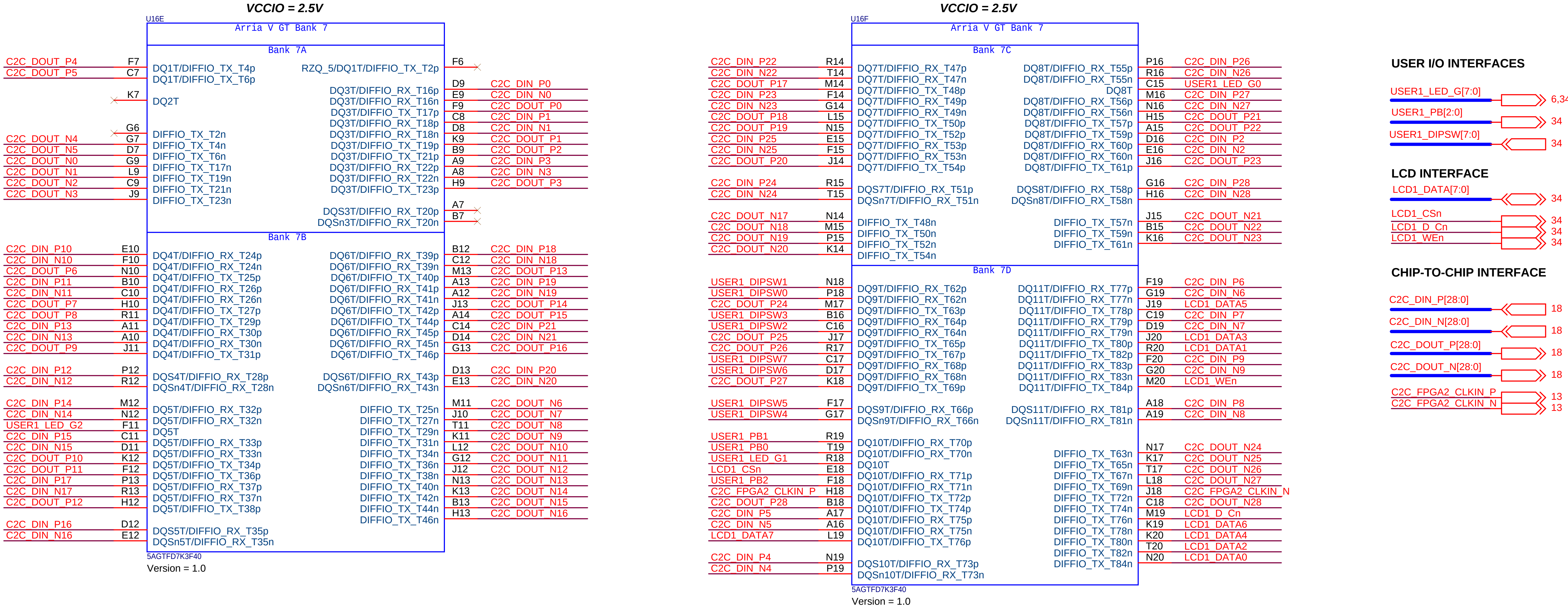
Arria V GT FPGA 1, Bank 7



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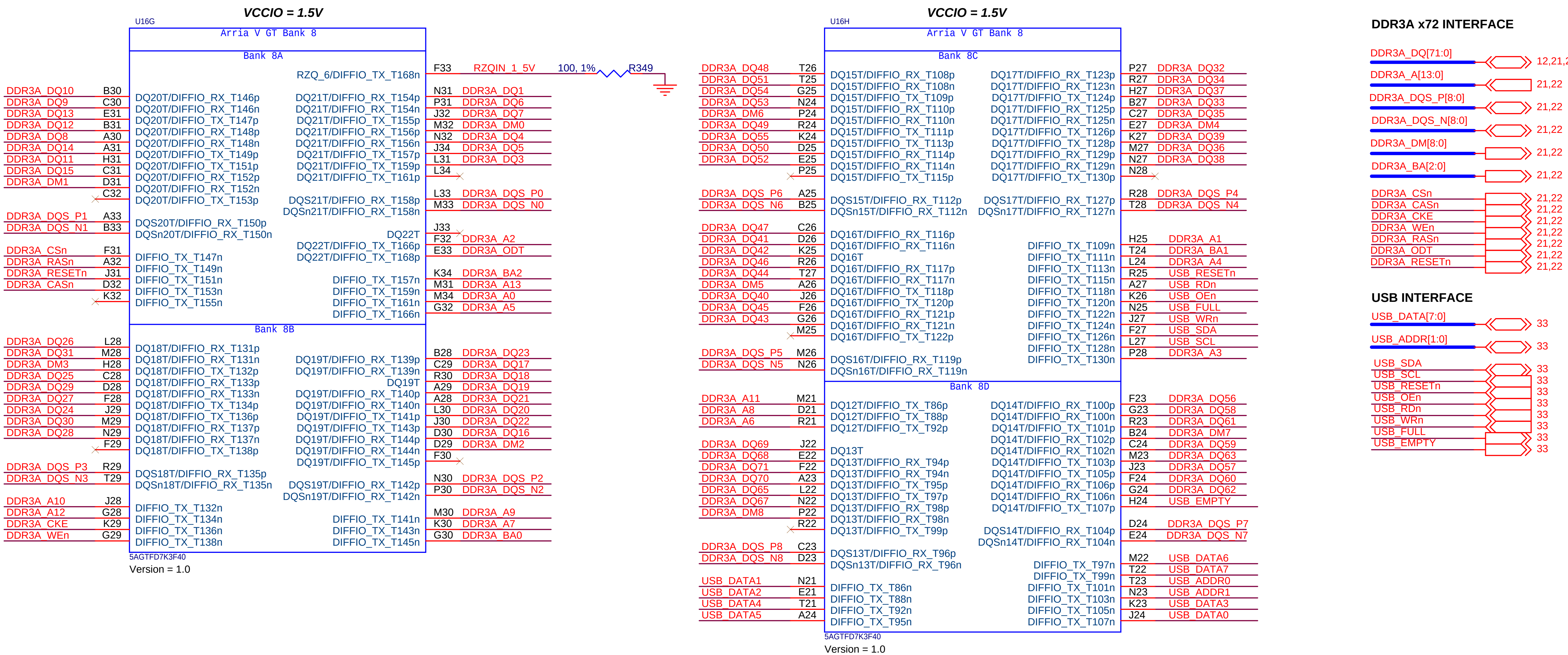
Arria V GT FPGA 1, Bank 8



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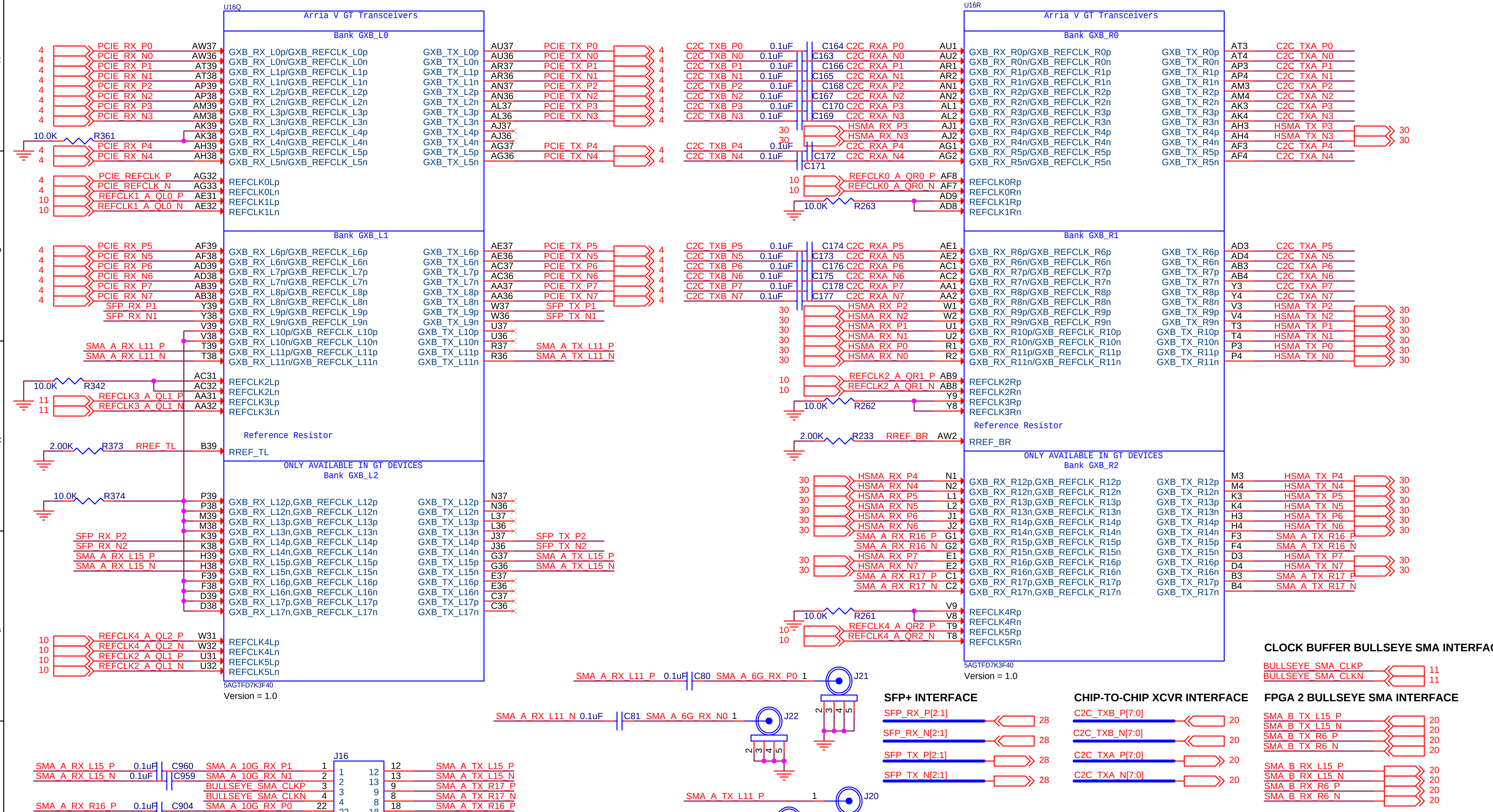
Arria V GT Transceivers and Power (FPGA 1)



CLOCK BUFFER BULLSEYE SMA INTERFACE

SFP+ INTERFACE

CHIP-TO-CHIP XCVR INTERFACE

FPGA 2 BULLSEYE SMA INTERFACE

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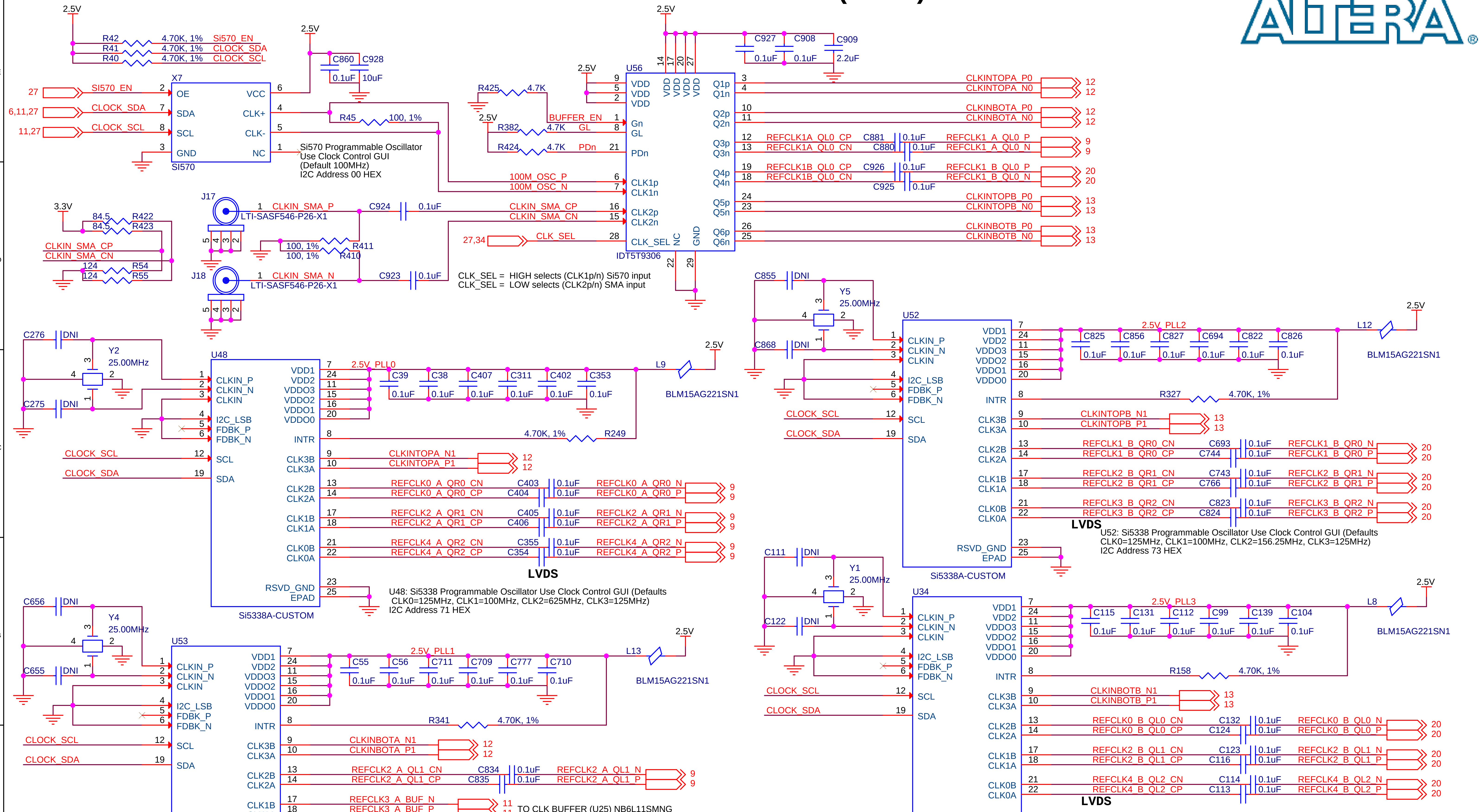
Clocks/Oscillators (1 of 2)



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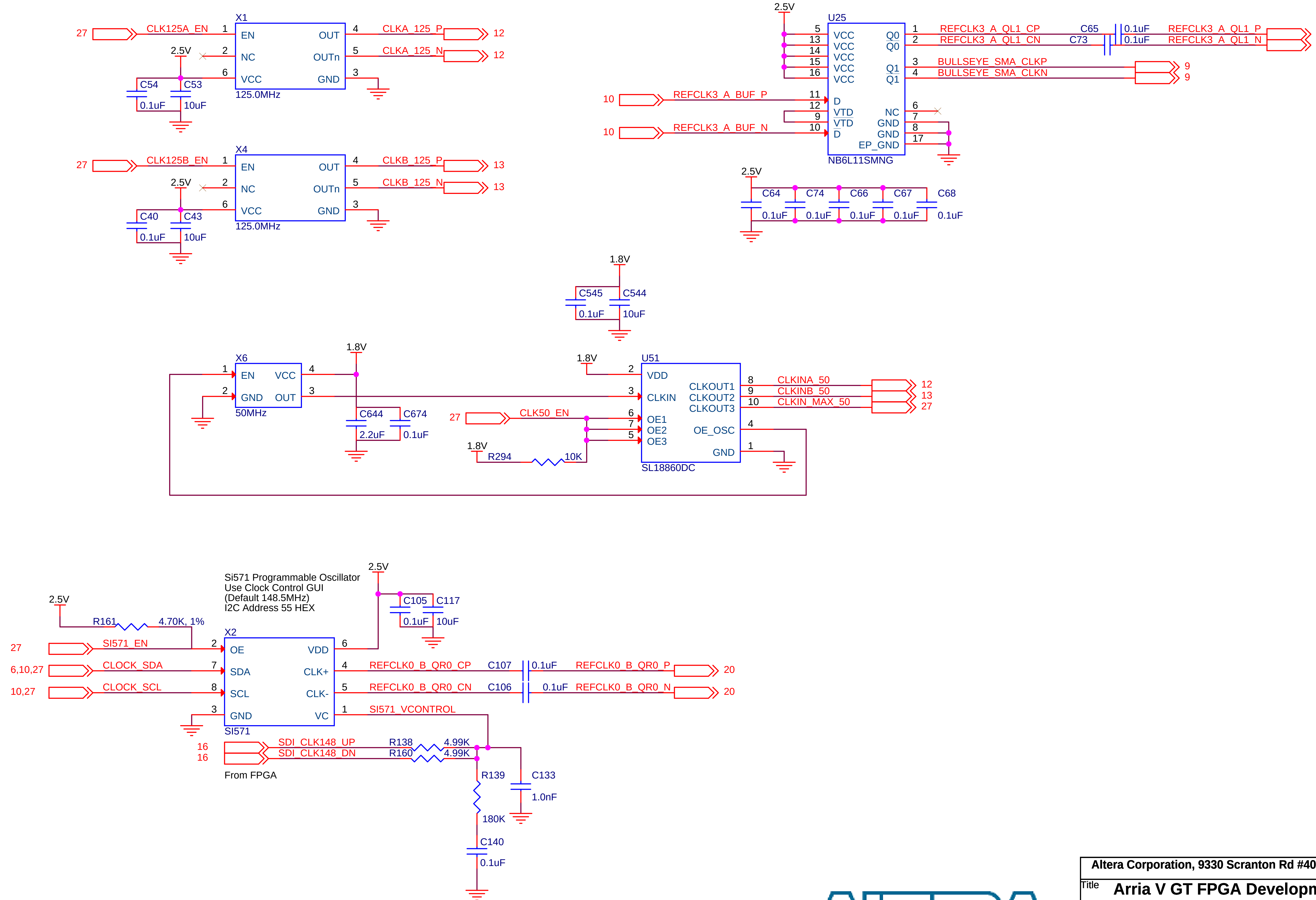
Clocks/Oscillators (2 of 2)



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Arria V GT Clocks (FPGA 1)

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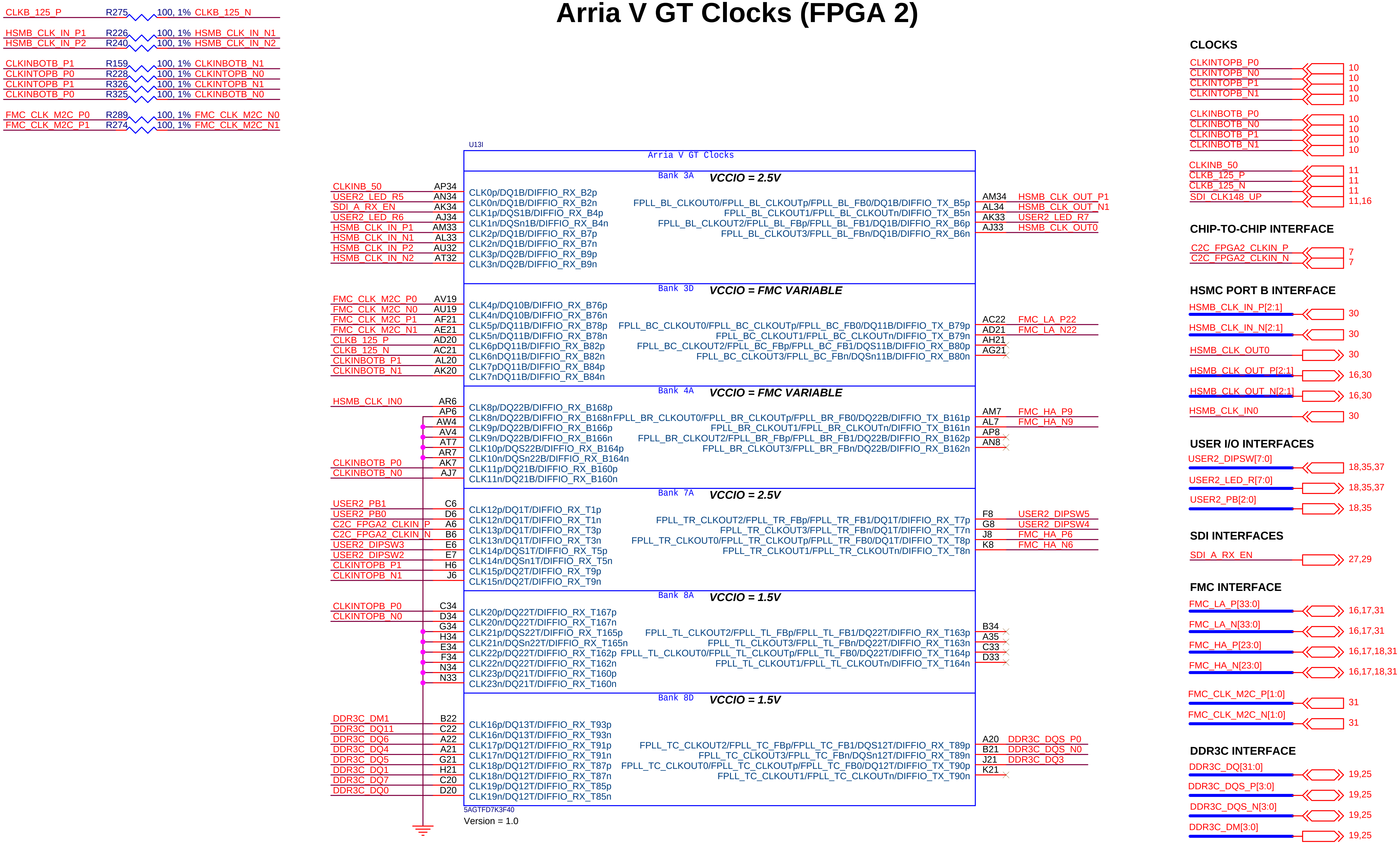
Arria V GT Clocks (FPGA 2)



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Arria V GT Configuration

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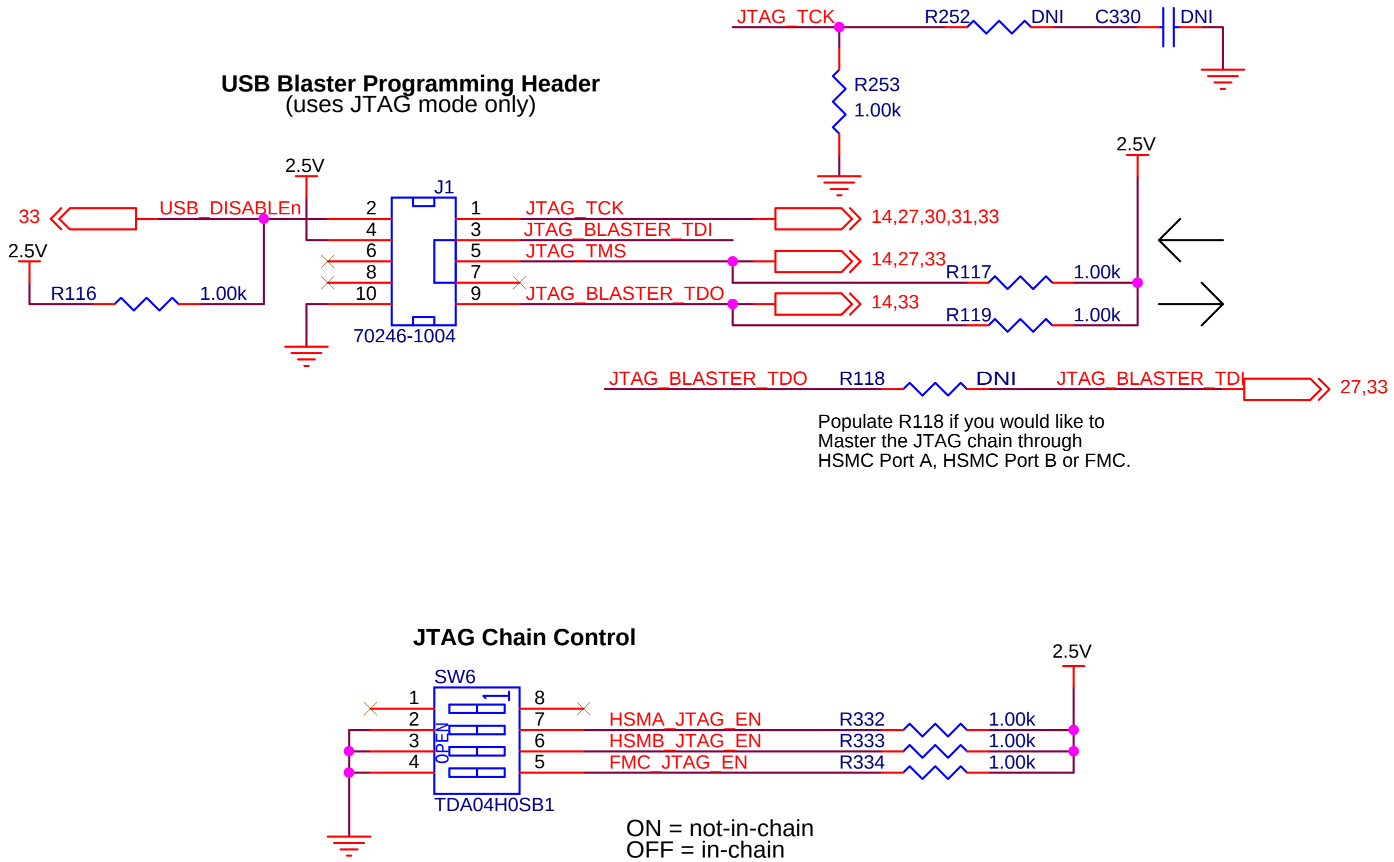
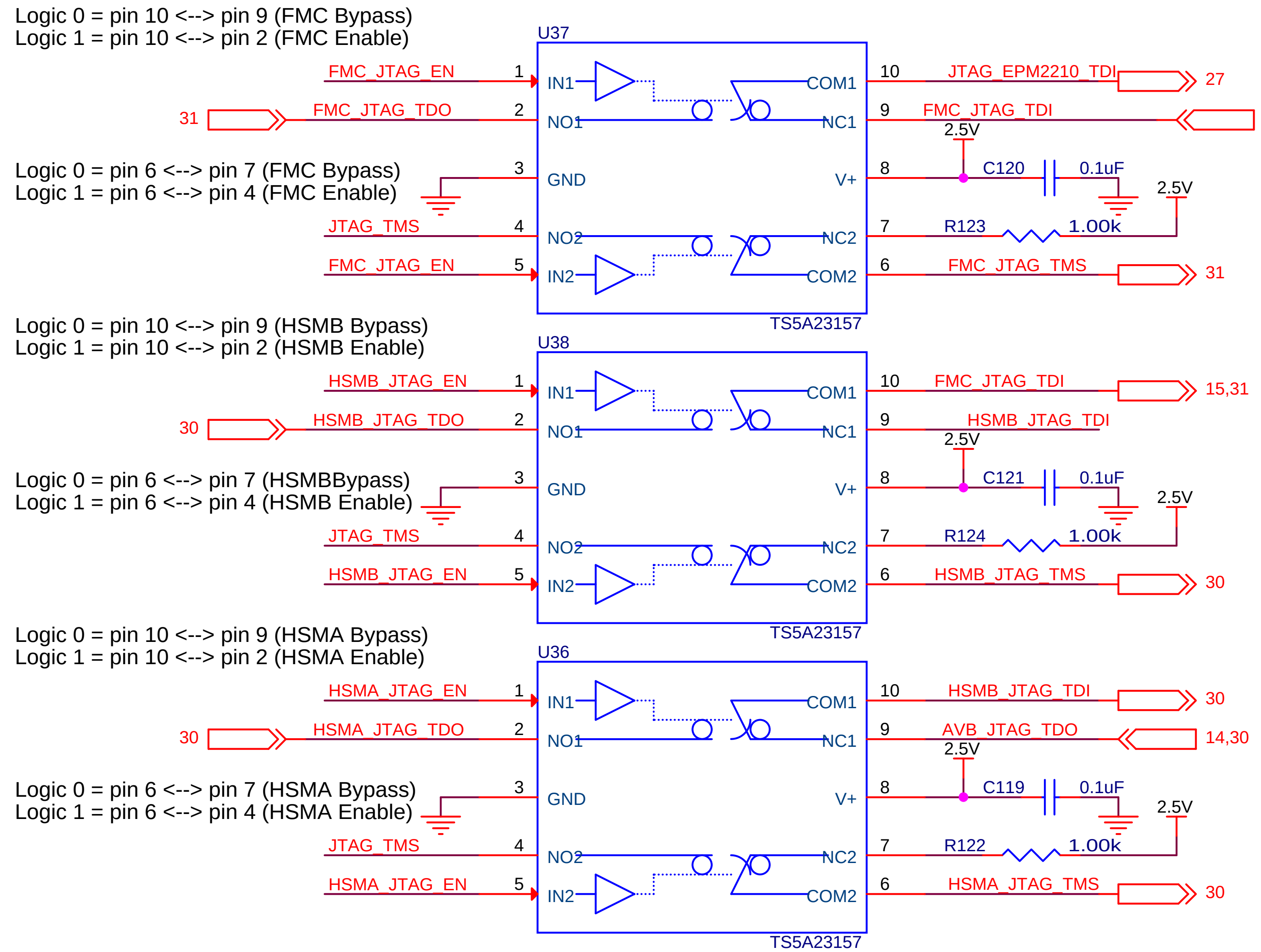
JTAG

TS5A23157 Switch Functions
When Pins 1 & 5 are:
LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON





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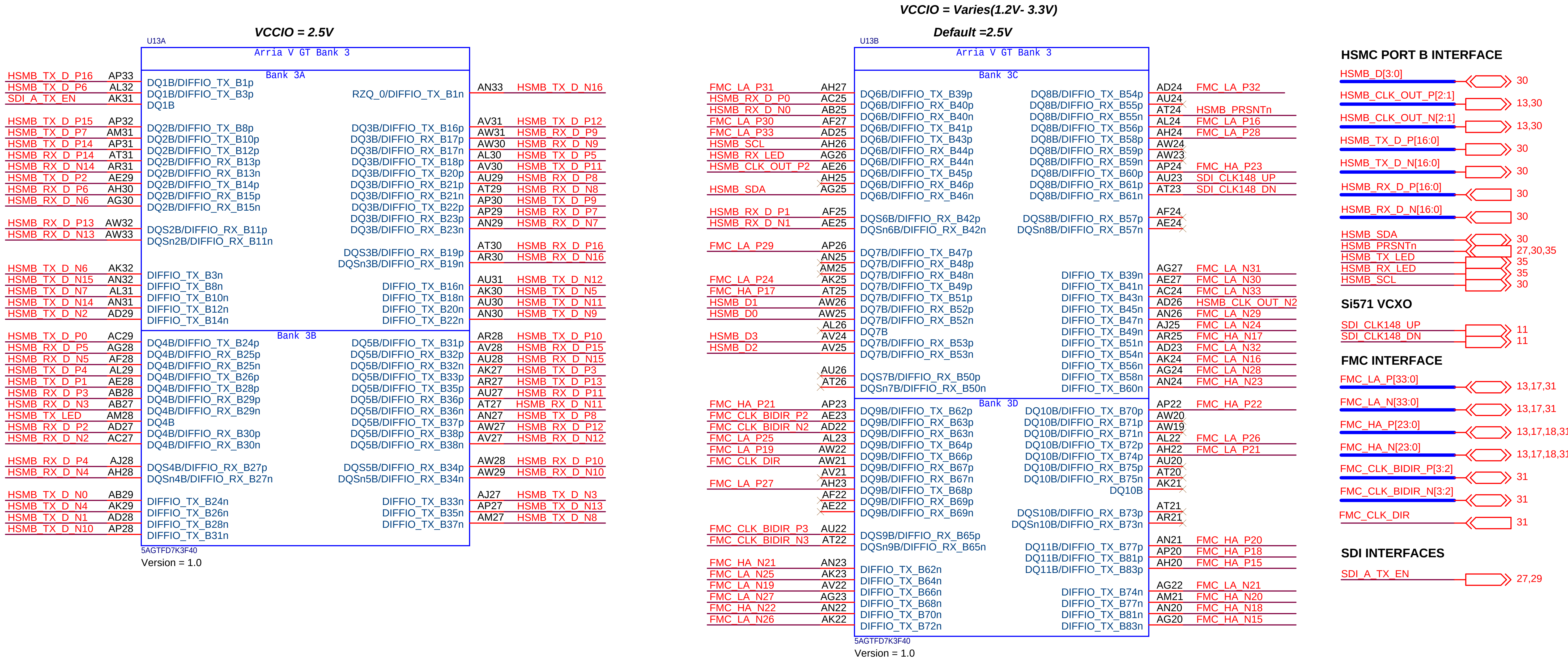
Arria V GT FPGA 2, Bank 3

NOTE: HSMB, SDI AND FMC CAN ONLY BE USED AT THE SAME TIME WHEN A5_VCCIO_FMC = 2.5V



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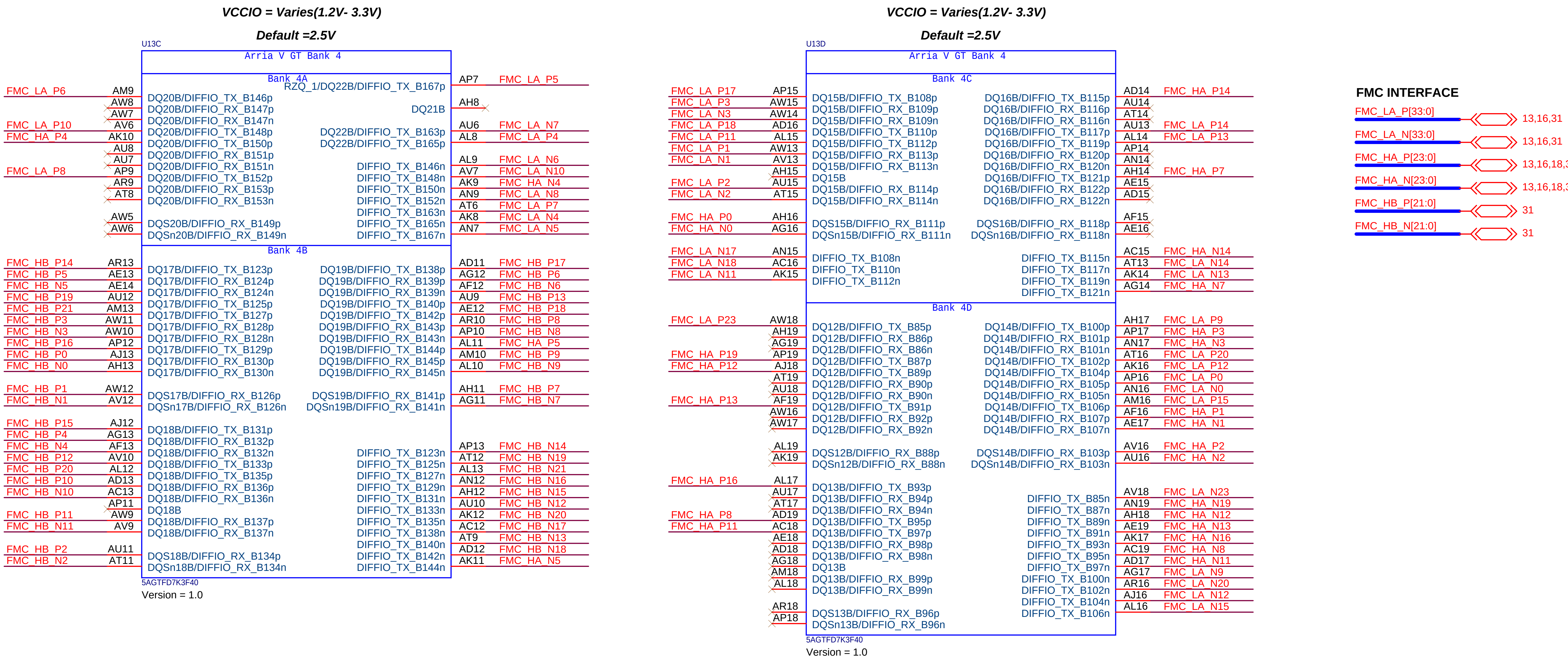
Arria V GT FPGA 2, Bank 4

NOTE: HSMB, SDI AND FMC CAN ONLY BE USED AT THE SAME TIME WHEN A5_VCCIO_FMC = 2.5V



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Title **Arria V GT FPGA Development Kit Board**

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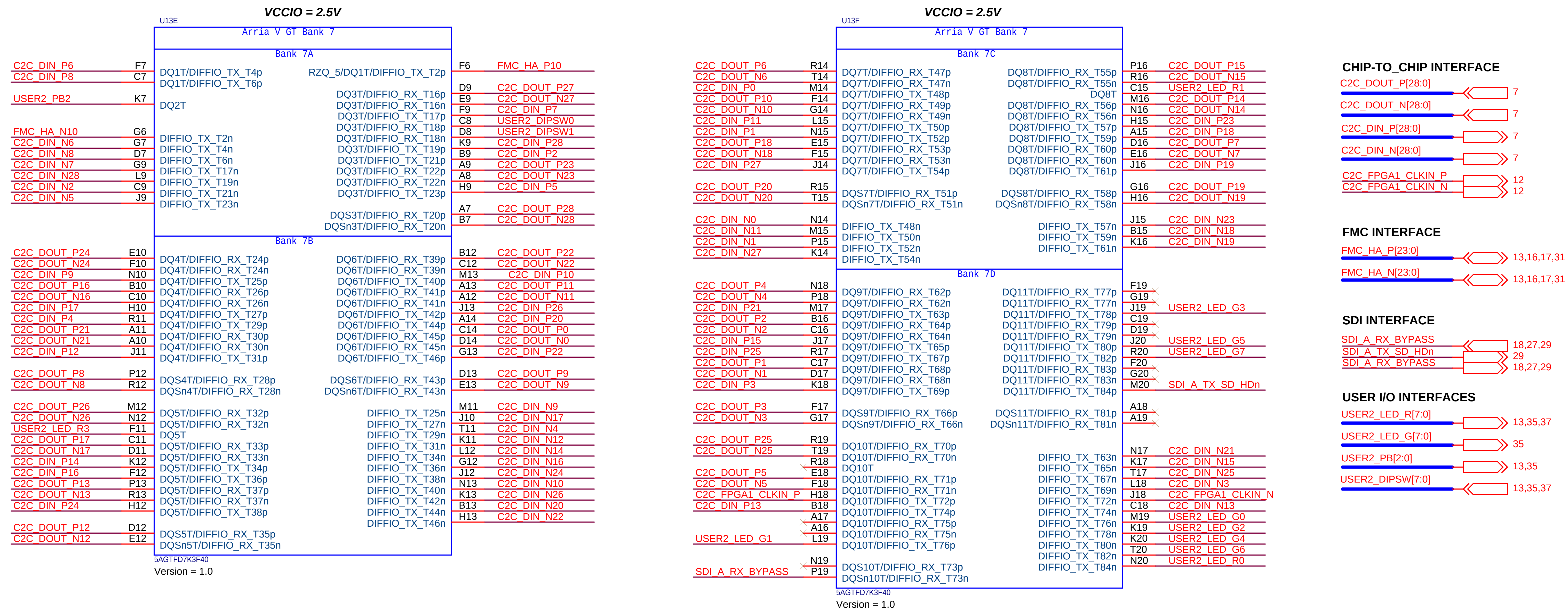
Arria V GT FPGA 2, Bank 7



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Arria V GT FPGA 2, Bank 8

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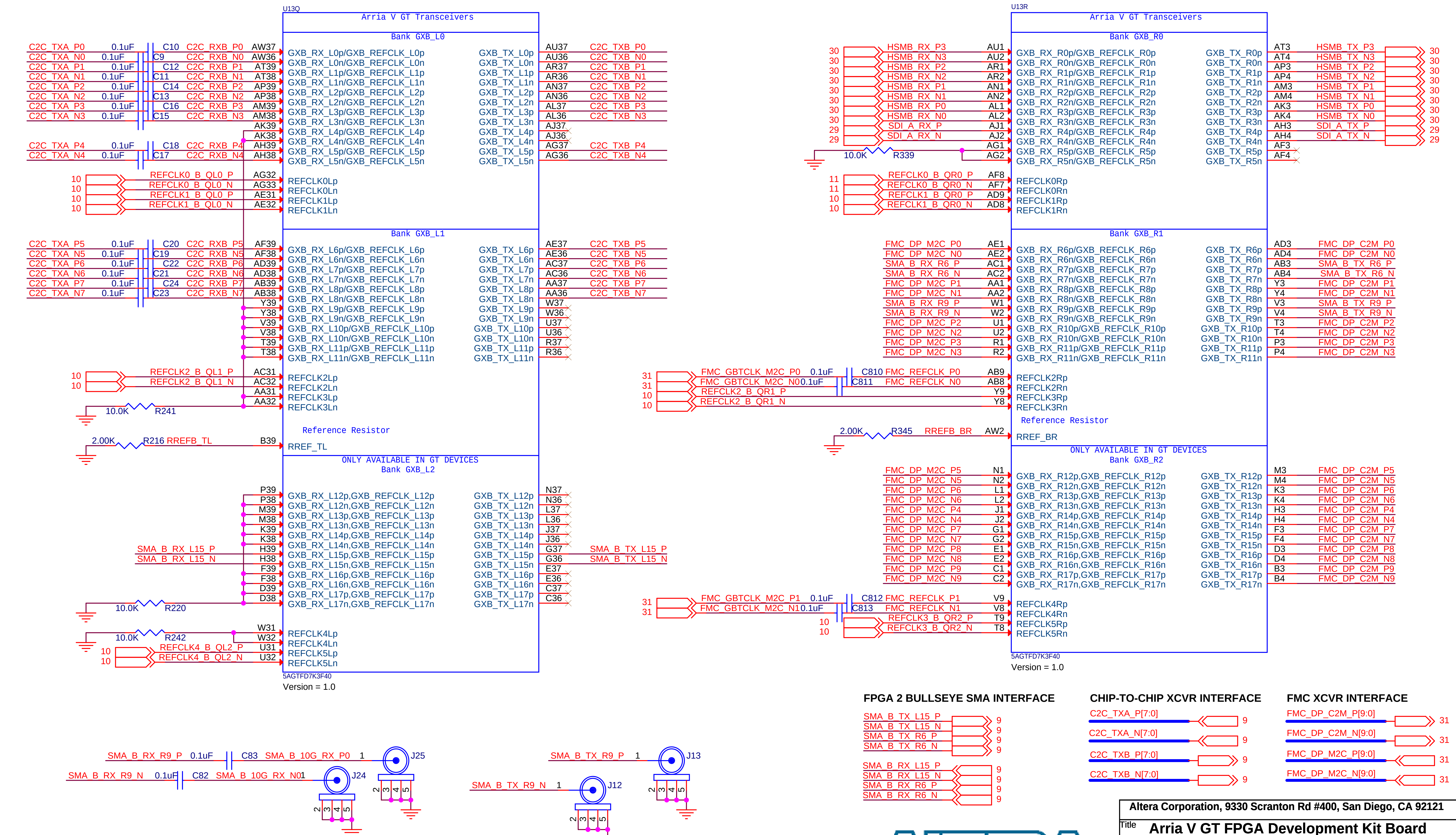
Arria V GT Transceivers and Power (FPGA 2)



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Title: Arria V GT FPGA Development Kit Board

Size	Document Number	Rev
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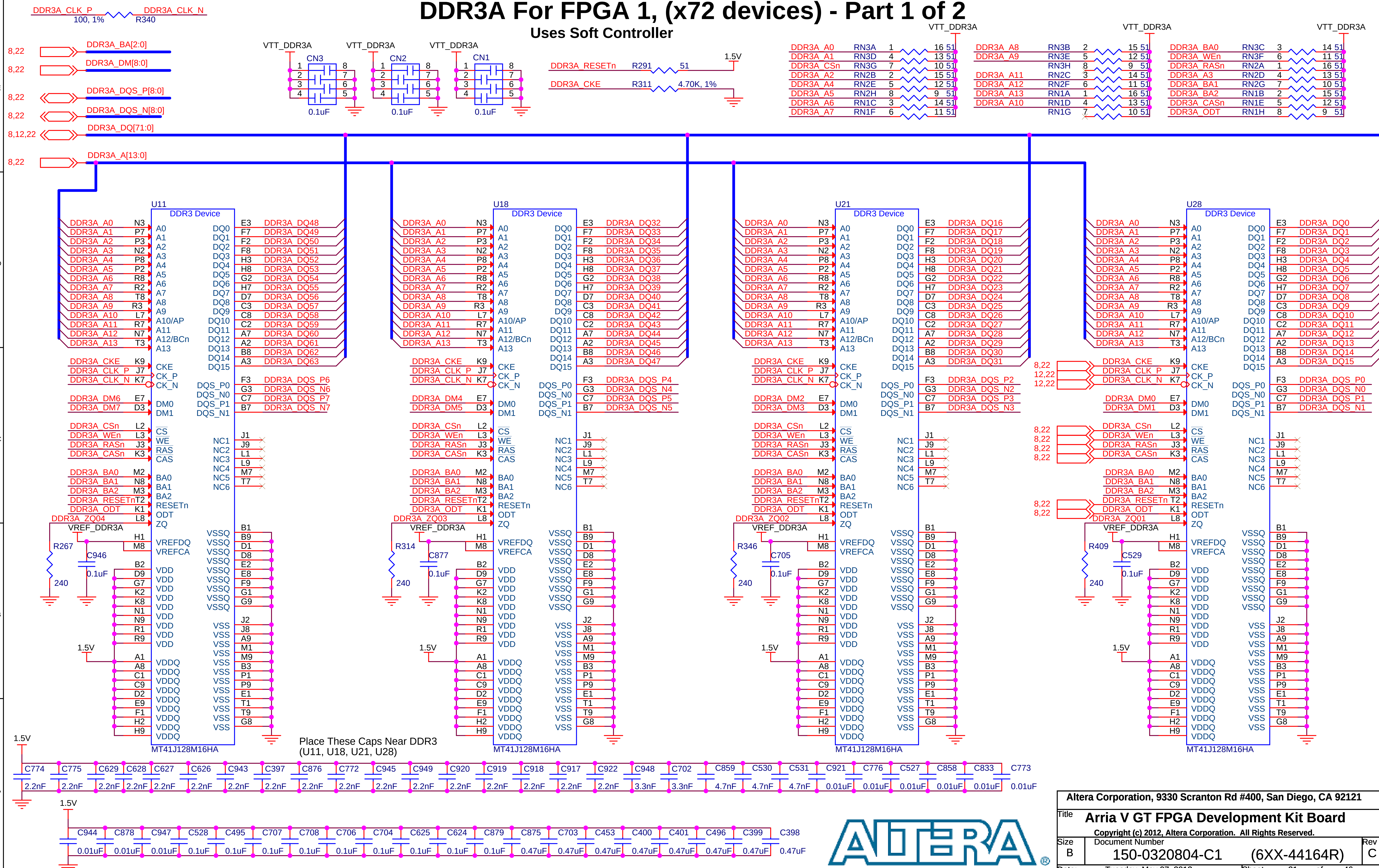
Date: Tuesday, May 07, 2013

DDR3A For FPGA 1, (x72 devices) - Part 1 of 2

Uses Soft Controller



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Title: **Arria V GT FPGA Development Kit Board**

Size	Document Number		Rev
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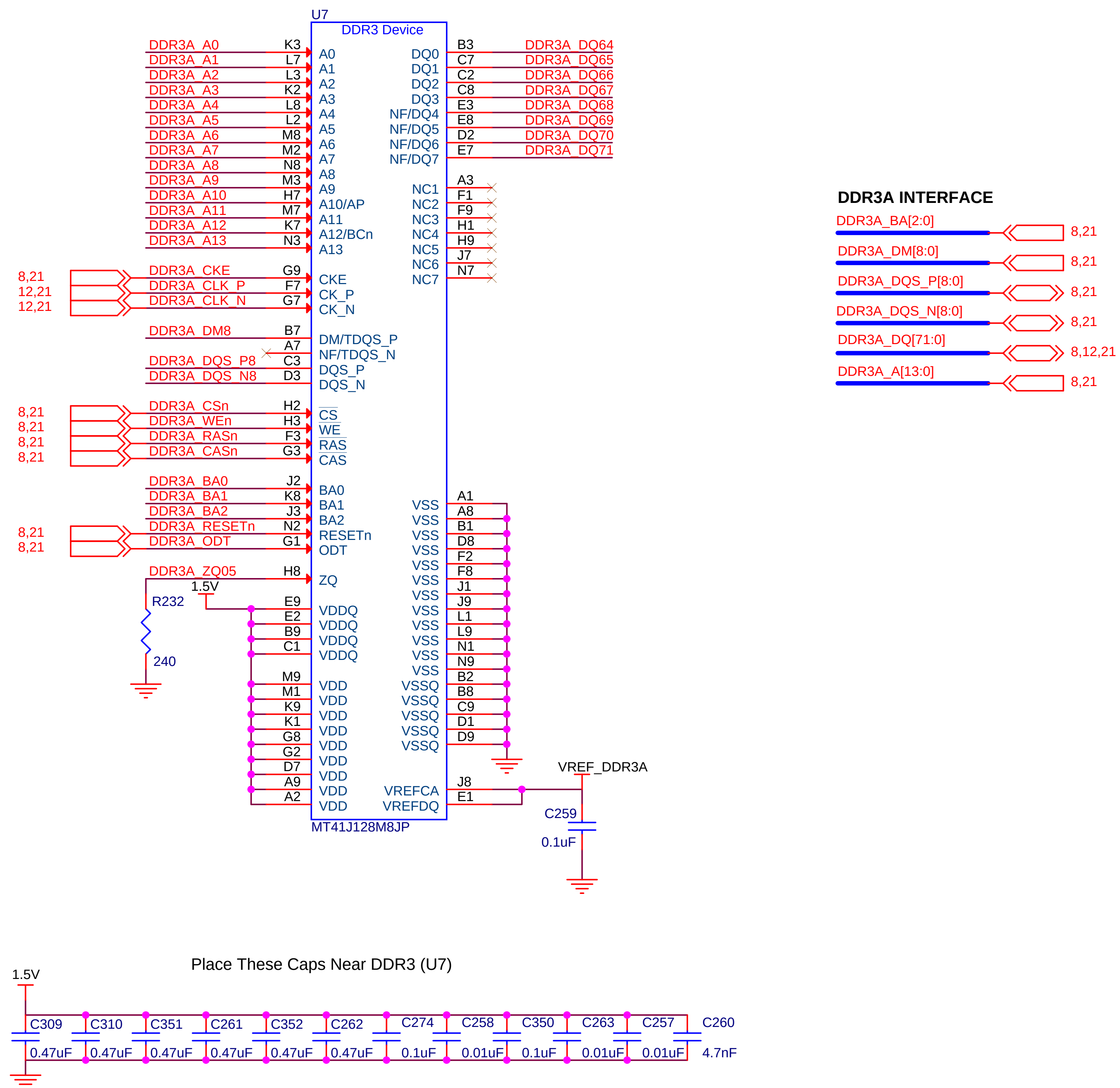
DDR3A For FPGA 1, (x72 devices) - Part 2 of 2

Uses Soft Controller



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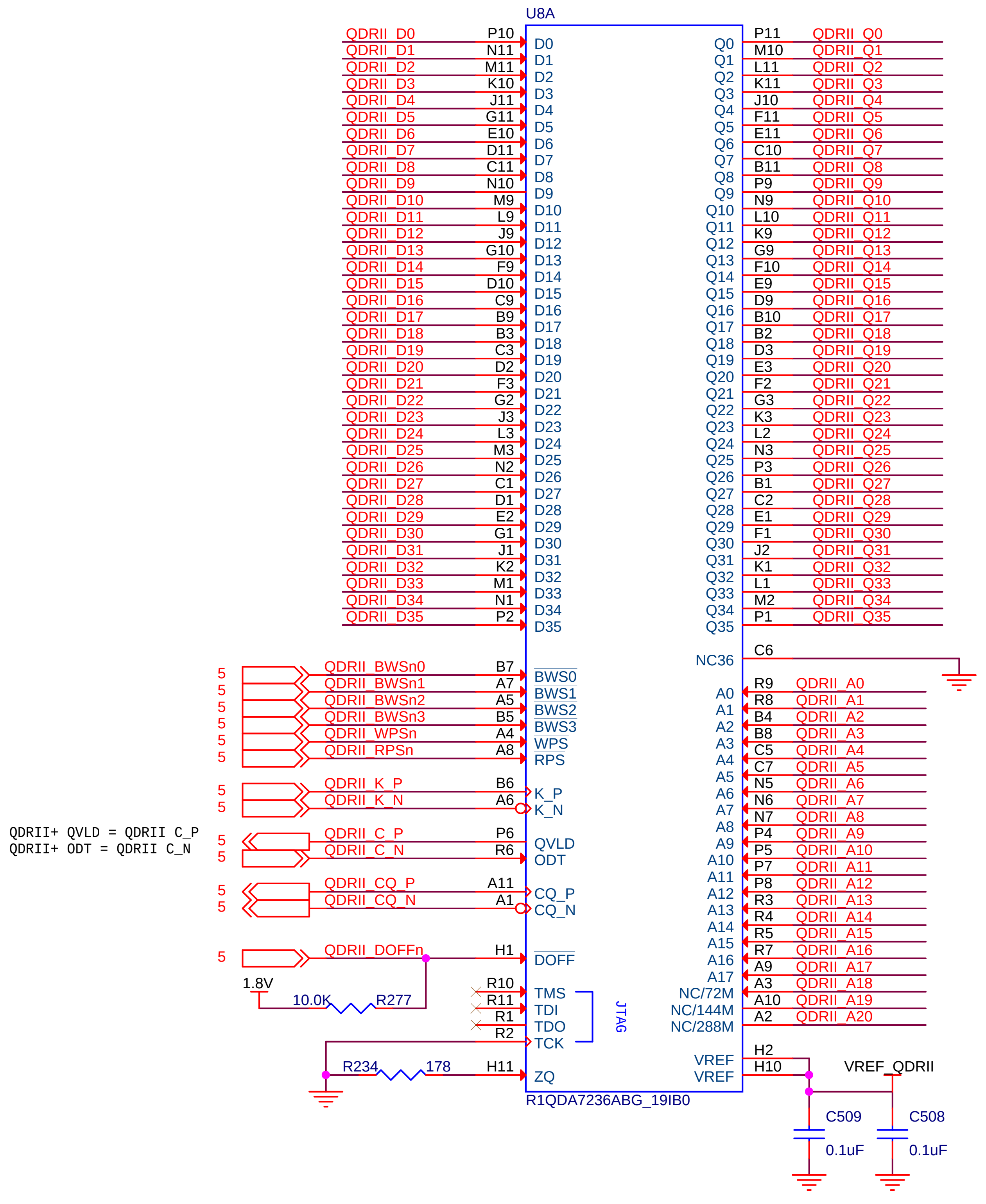
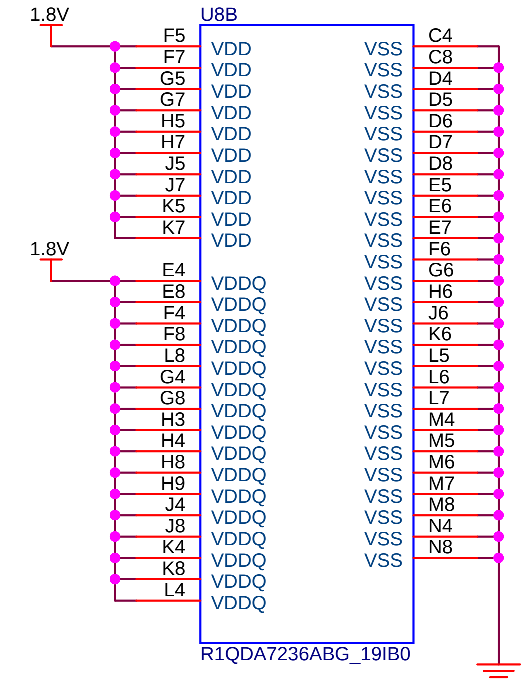
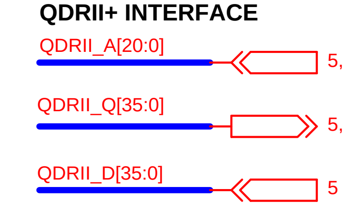
QDRII+

Altera recomends to use external termination for QDRII/+ address and command signals. In this case external termination was not used, because simulations showed that with the short trace length and a point to point connection the external temination was not necessary. As a result since there is limited board space external termination is not used.

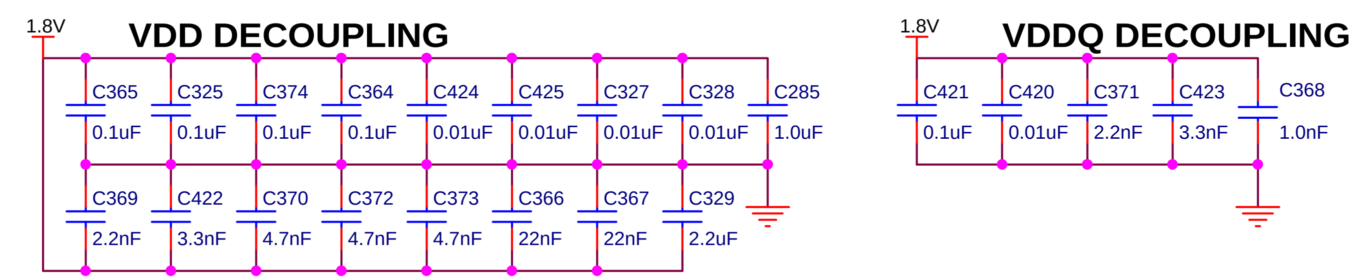




QDRII+ INTERFACE



Place These Caps Near QDRII+



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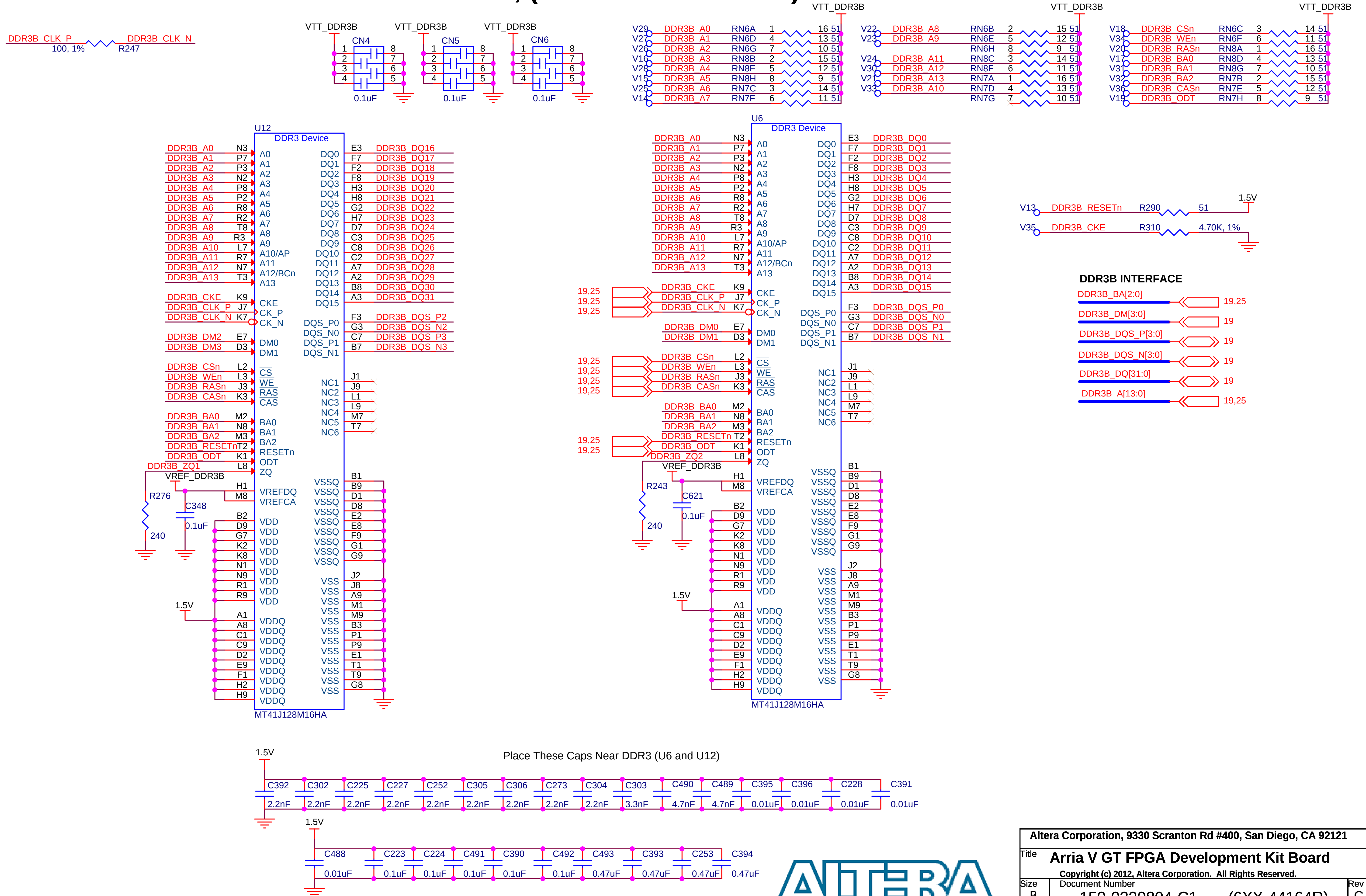
DDR3 For FPGA 2, (x32 Hard IP devices)



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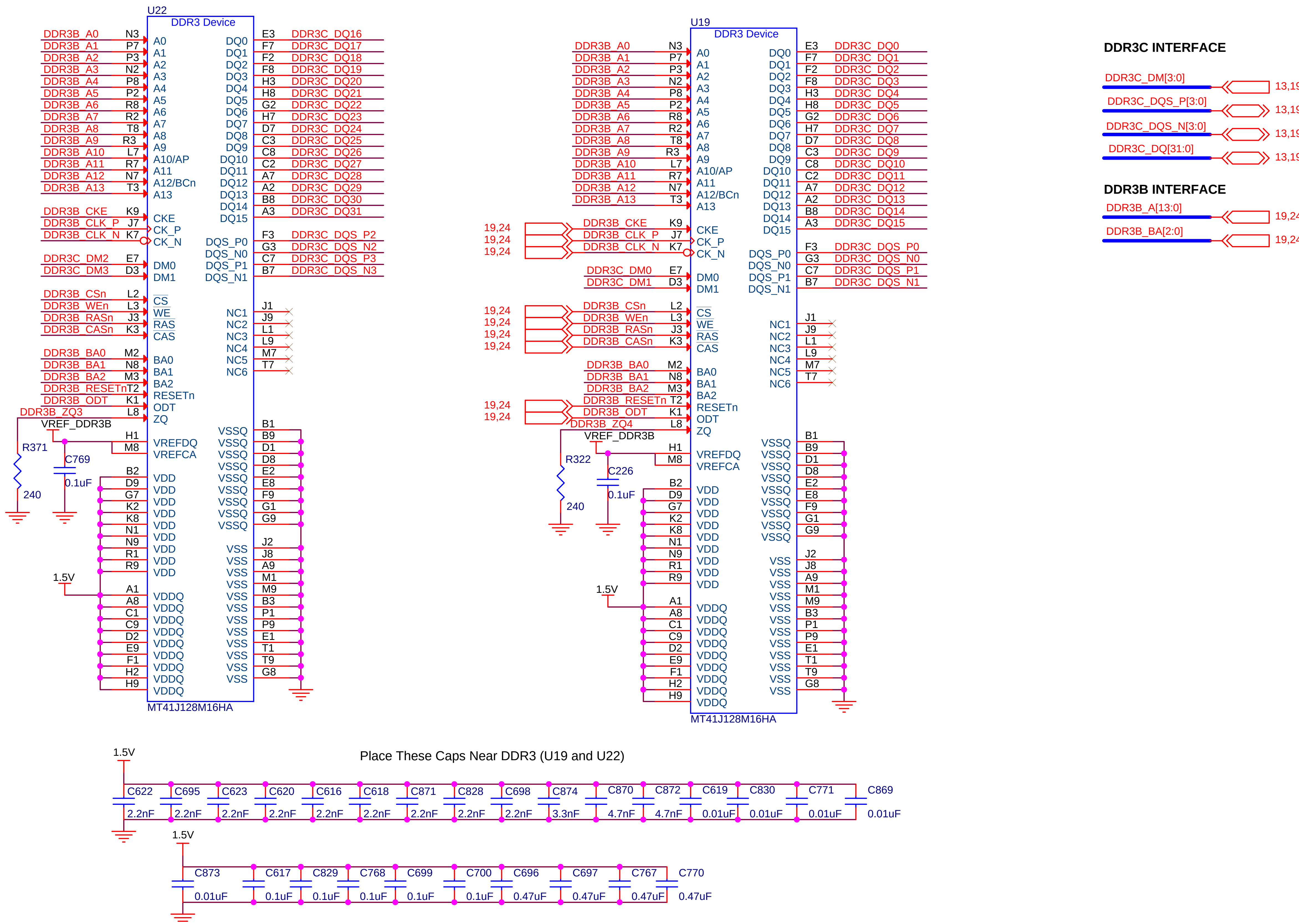
DDR3C For FPGA 2, (x64 Using Soft Controller Option)



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Title: **Arria V GT FPGA Development Kit Board**

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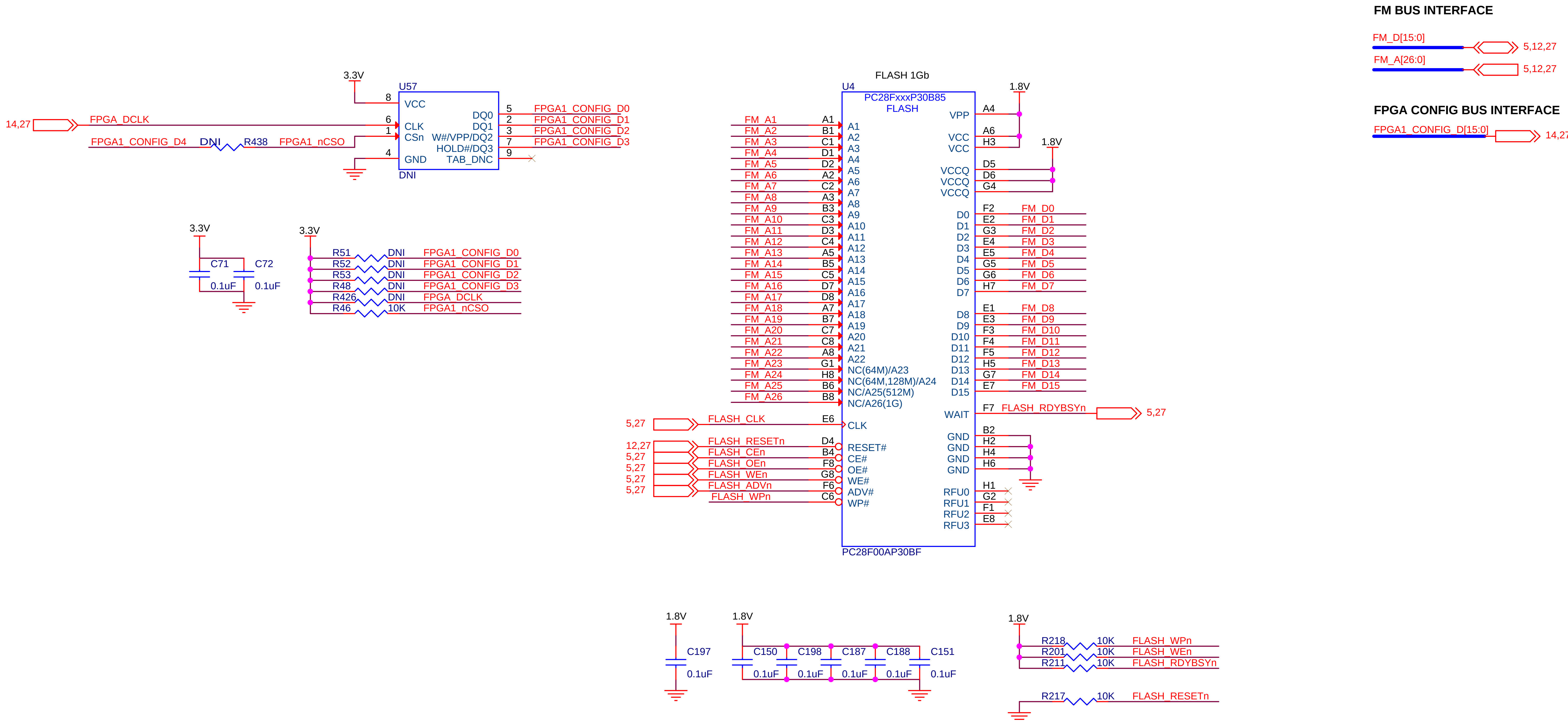
FLASH



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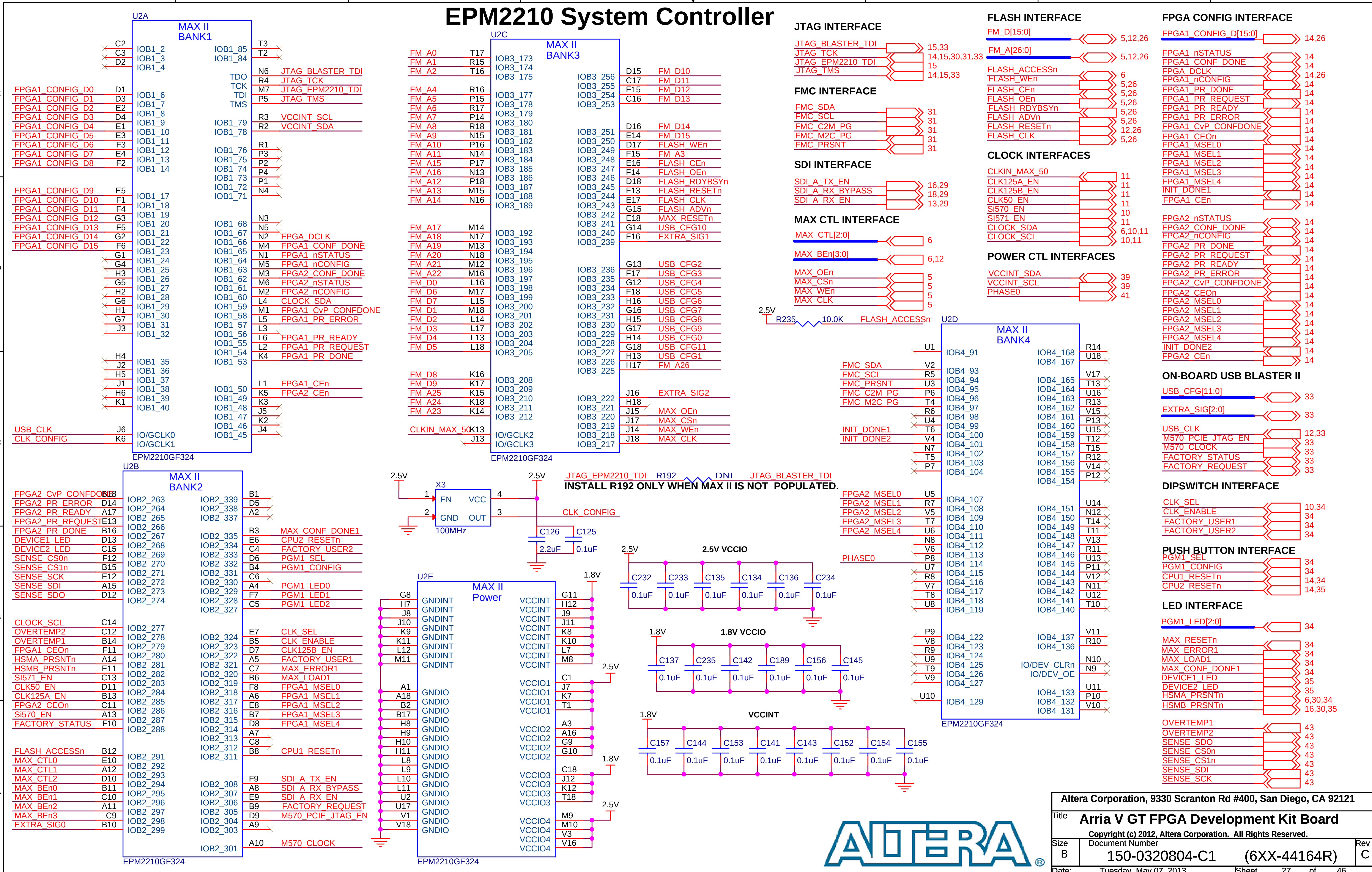
EPM2210 System Controller



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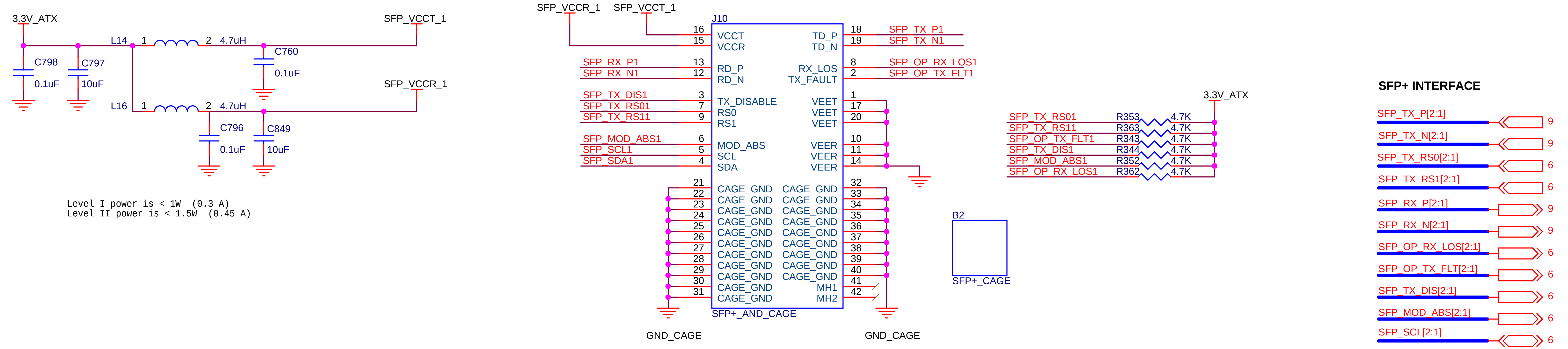
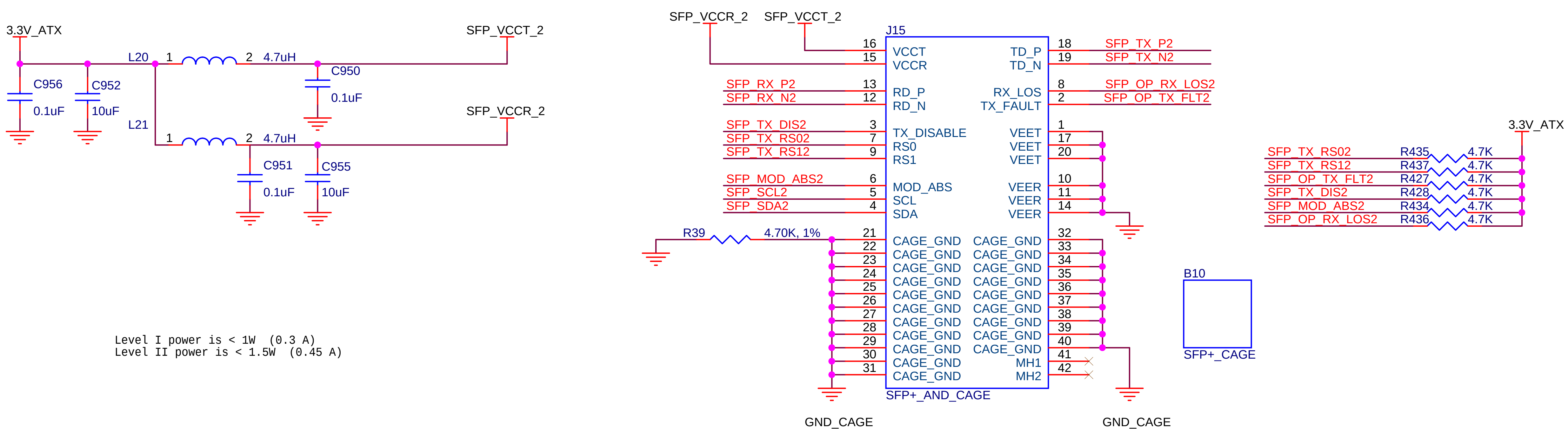
Small Form Factor Pluggable Plus (SFP+) Connector



Optical (SFP+) Transceiver Cage & Connector 1

THIS SFP+ INTERFACE IS ONLY AVAILABLE WITH ARRIA GT DEV KITS



Optical (SFP+) Transceiver Cage & Connector 2

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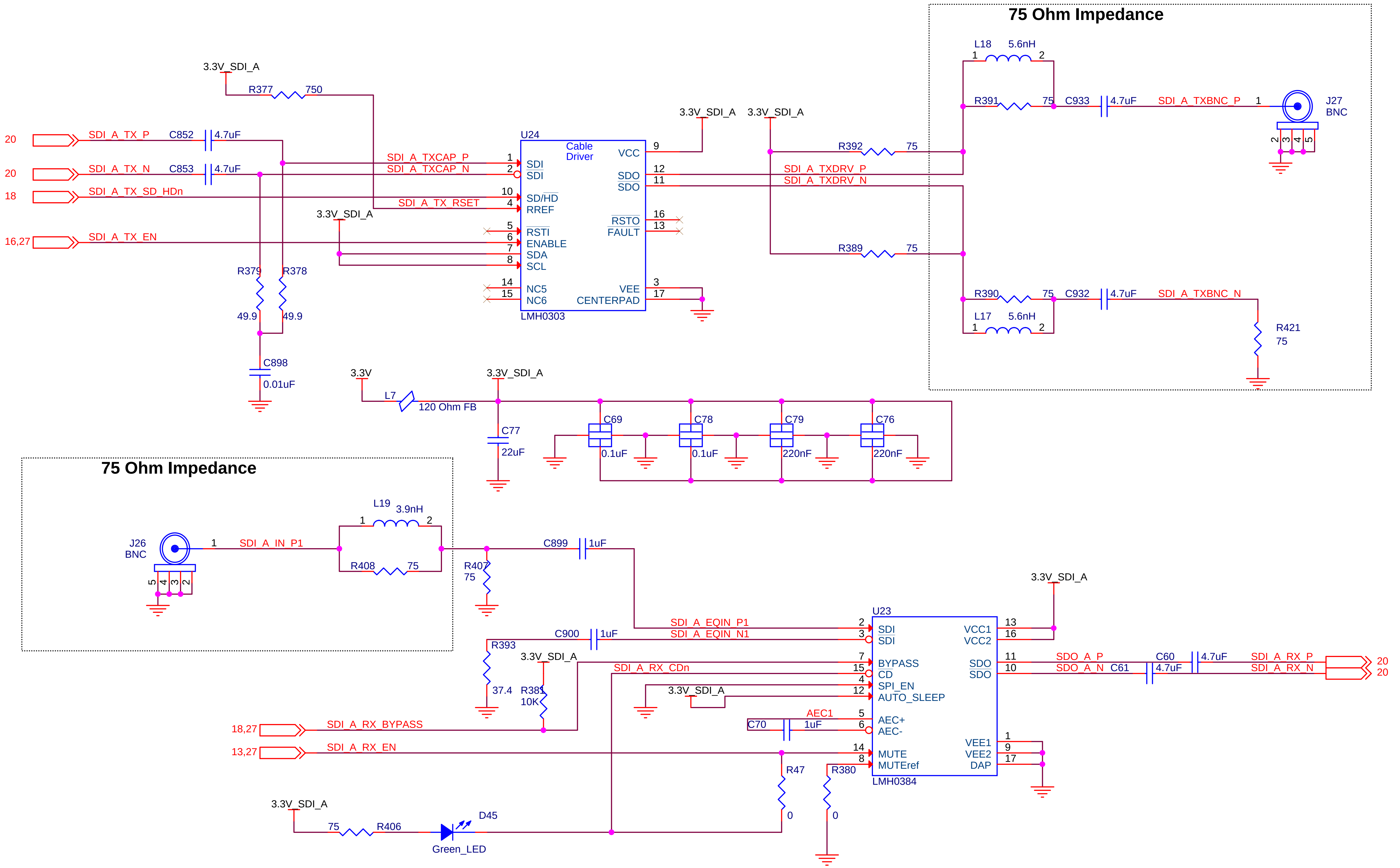
SDI Cable Driver, Equalizer, and SMB



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Title: **Arria V GT FPGA Development Kit Board**		
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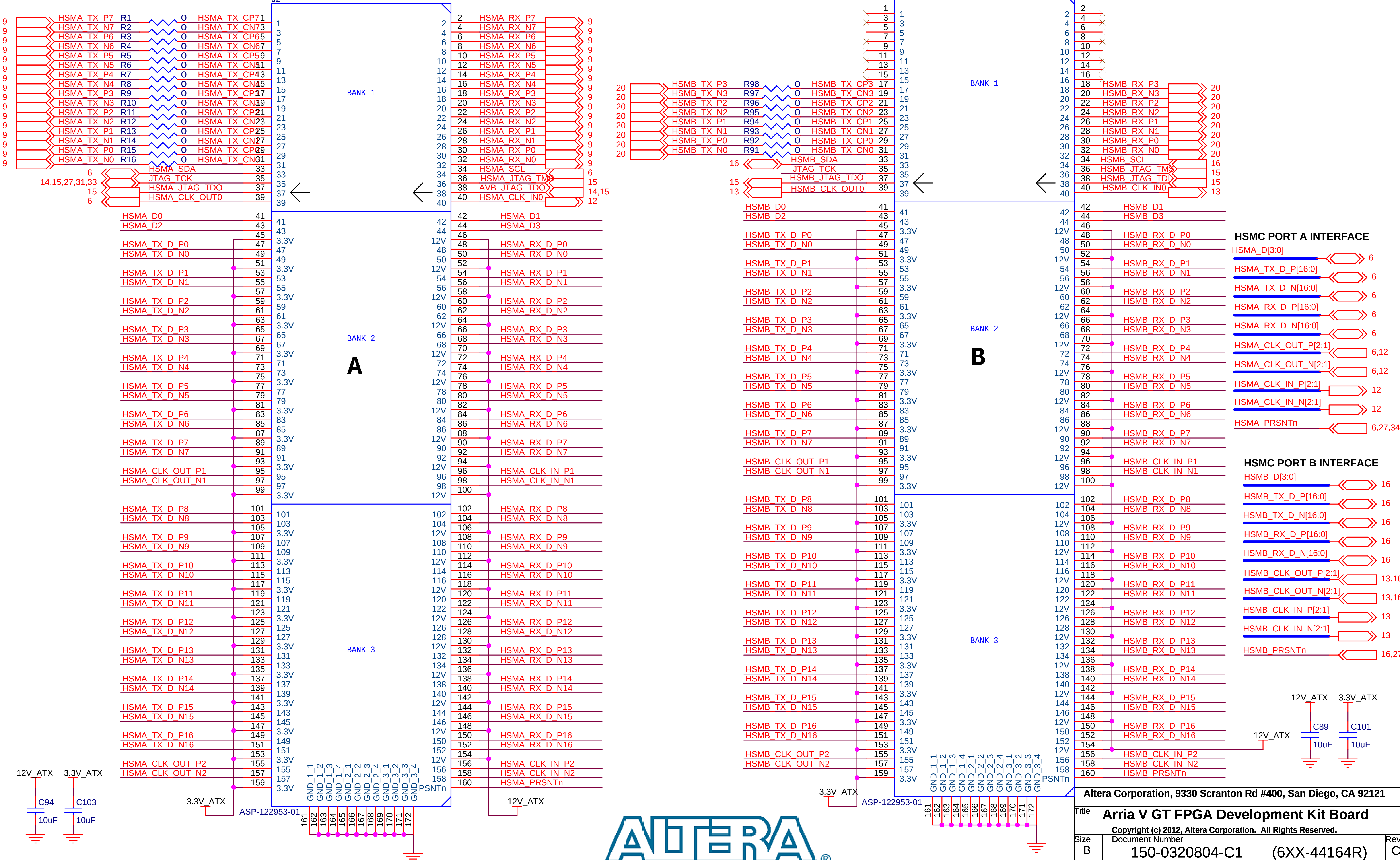
HSMC Port A & Port B



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Size B	Document Number 150-0320804-C1	(6XX-44164R)	Rev C
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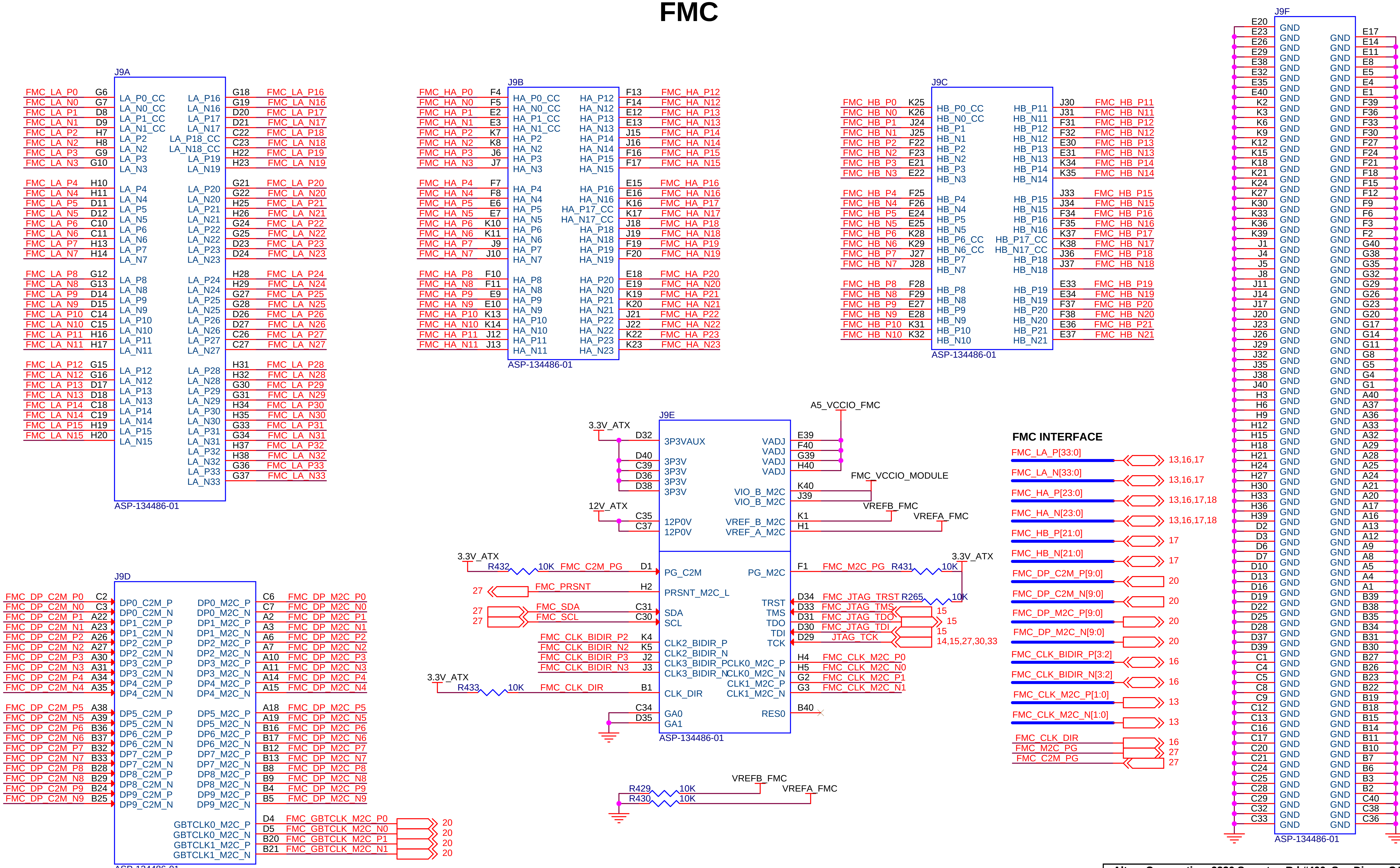
FMC



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Title: **Arria V GT FPGA Development Kit Board**

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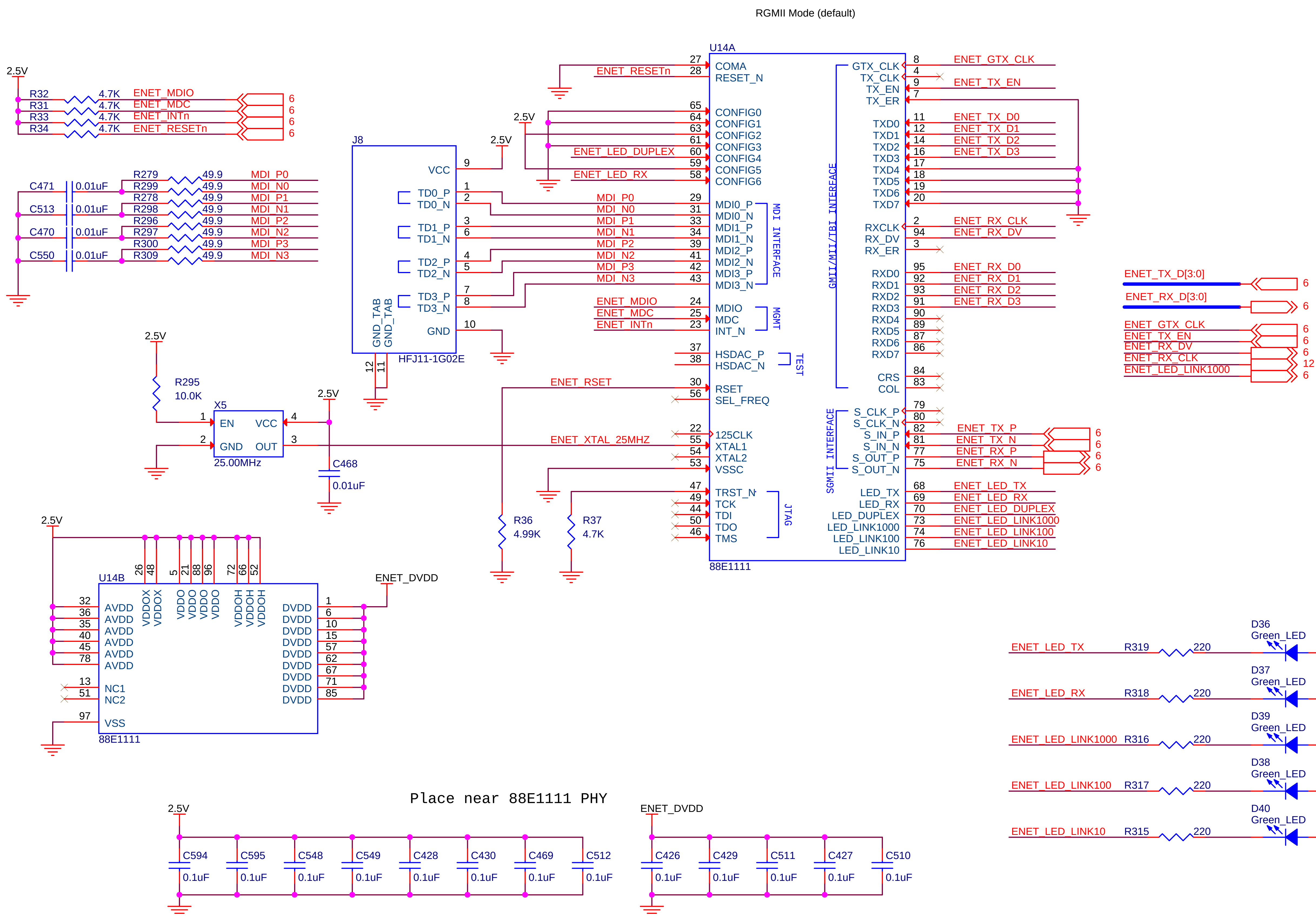
10/100/1000 Ethernet



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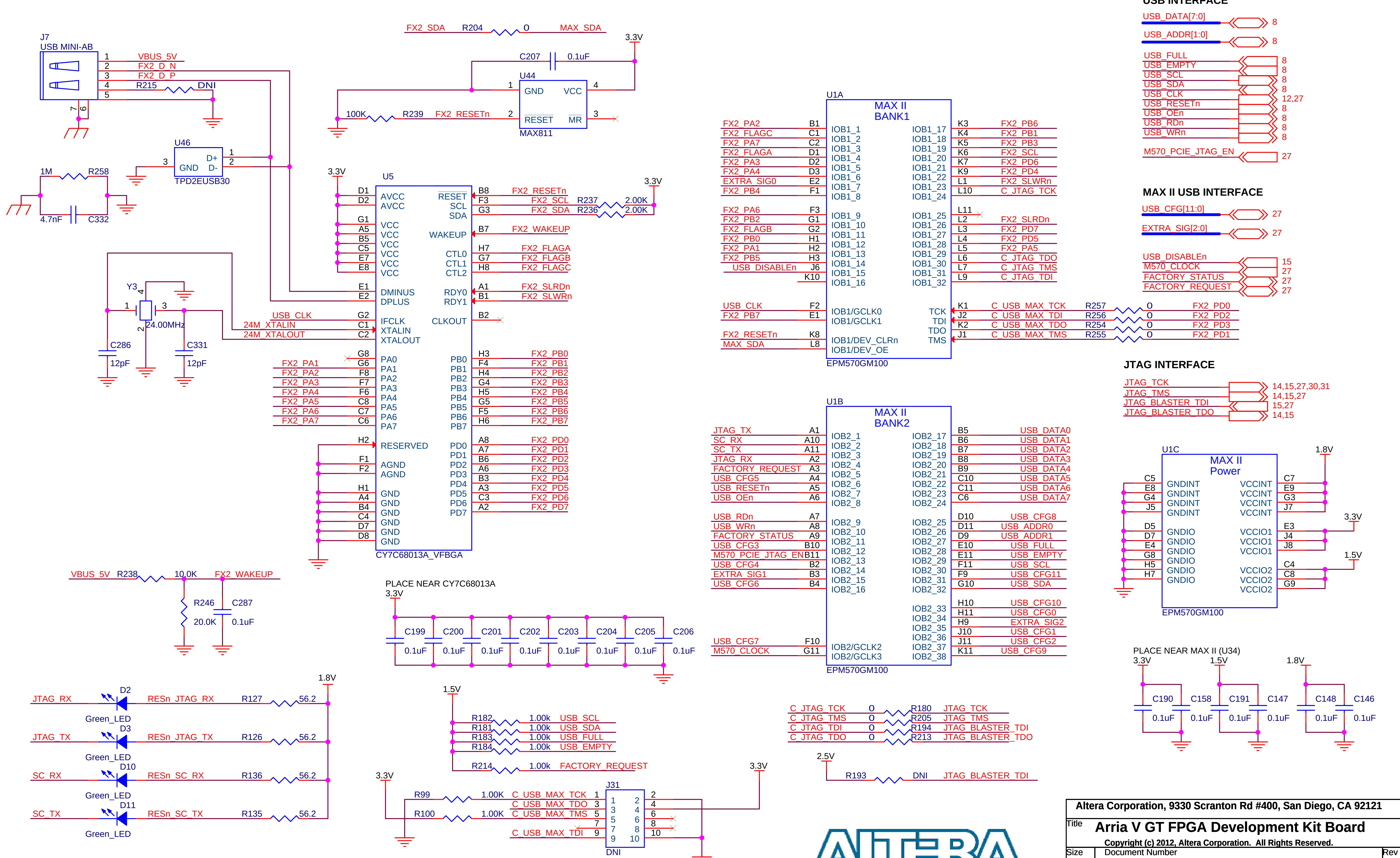
On-Board USB Blaster II



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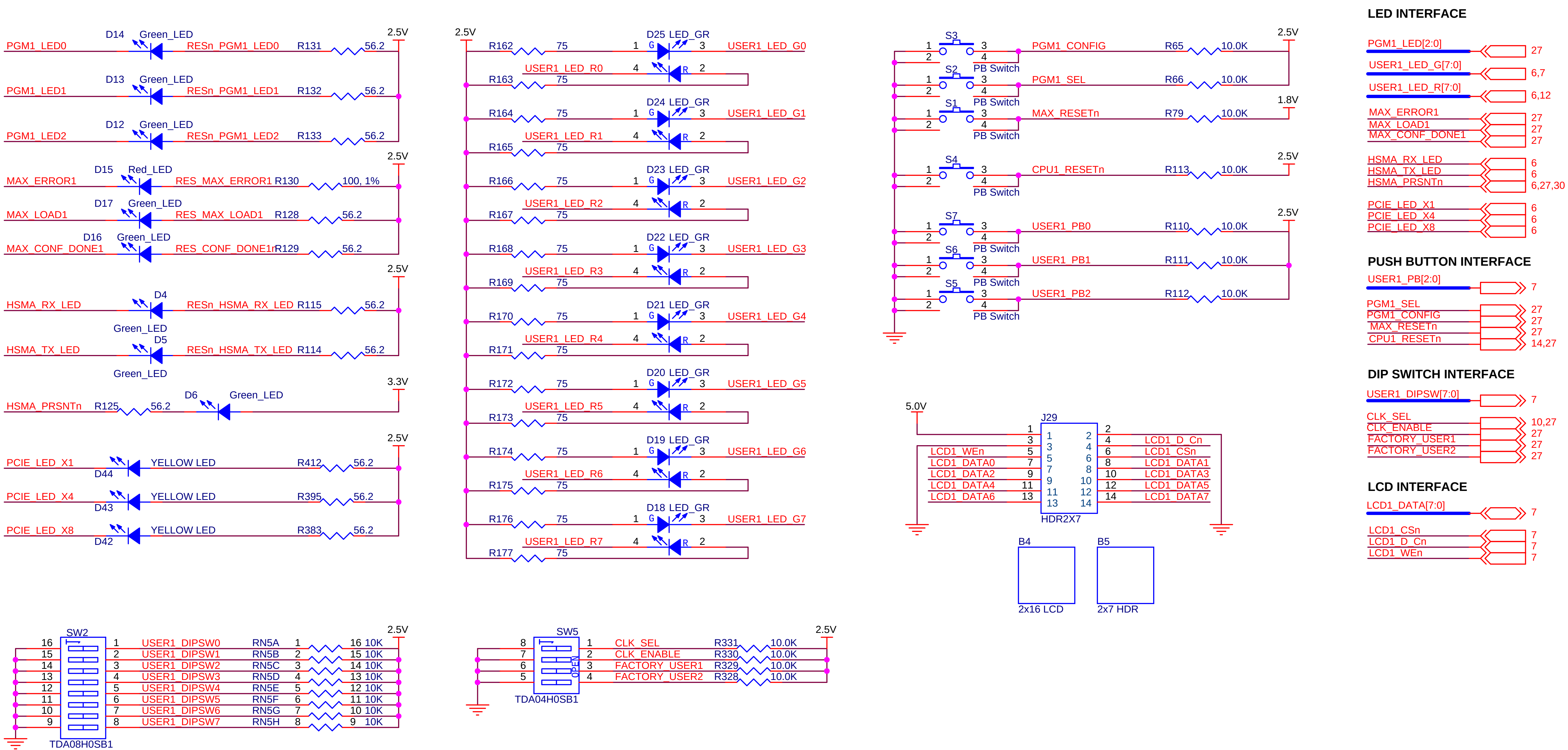
User I/O - (For Arria V GT FPGA 1)



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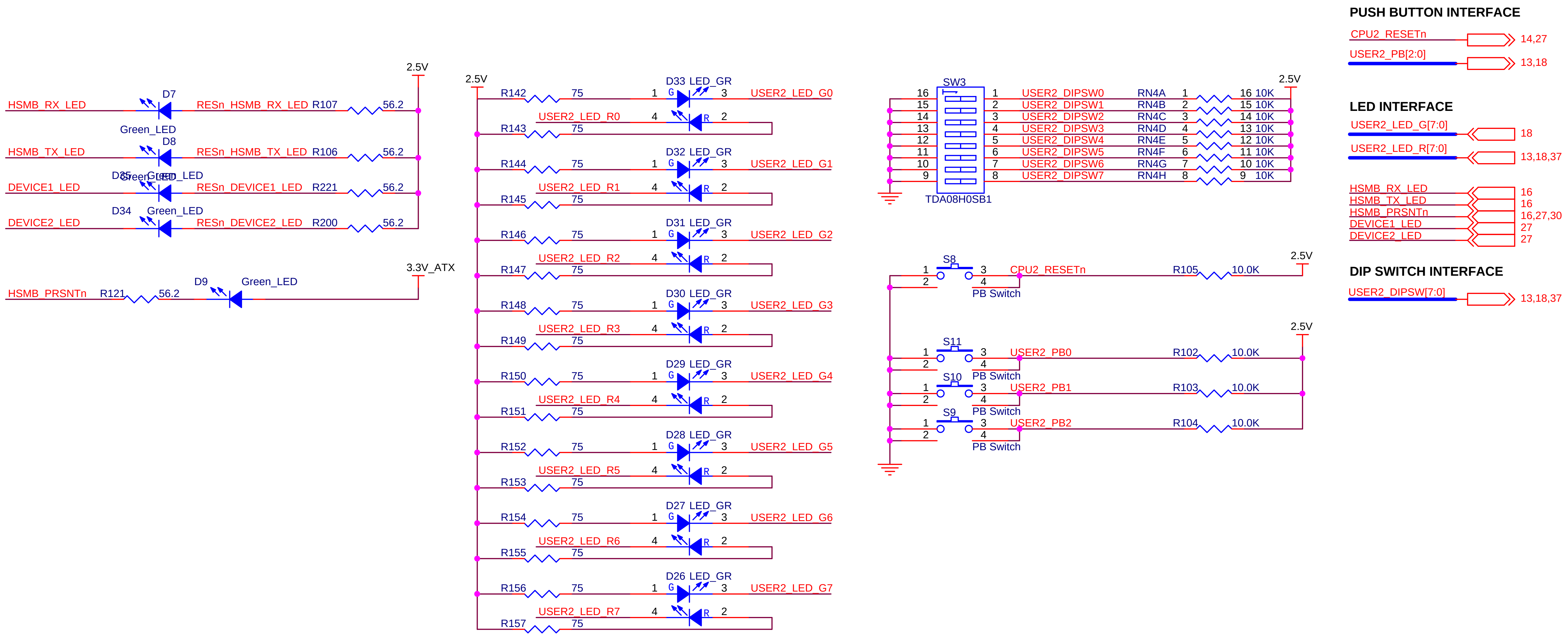
User I/O - (For Arria V GT FPGA 2)



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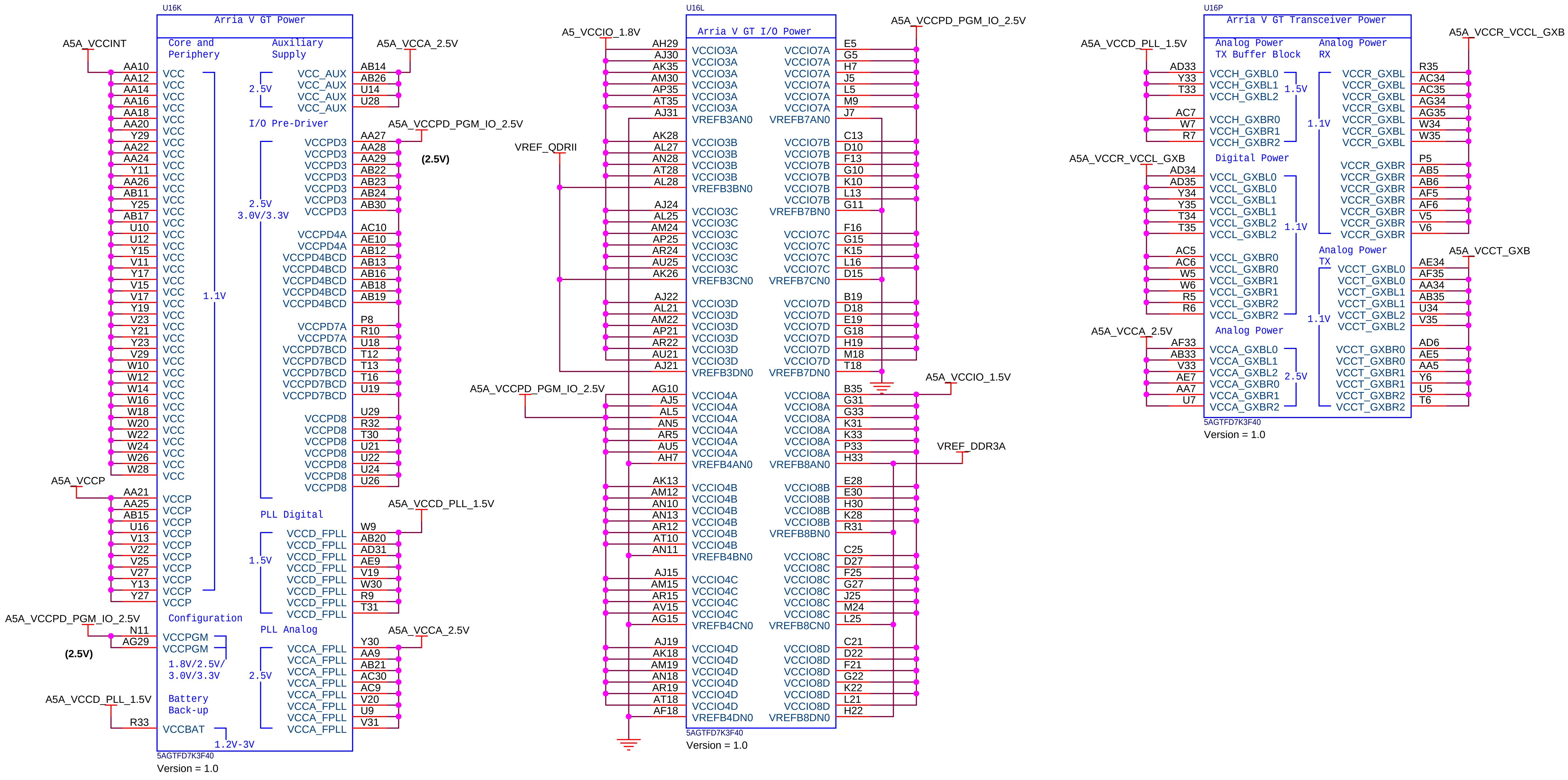
Power - Arria V GT Power (FPGA 1)



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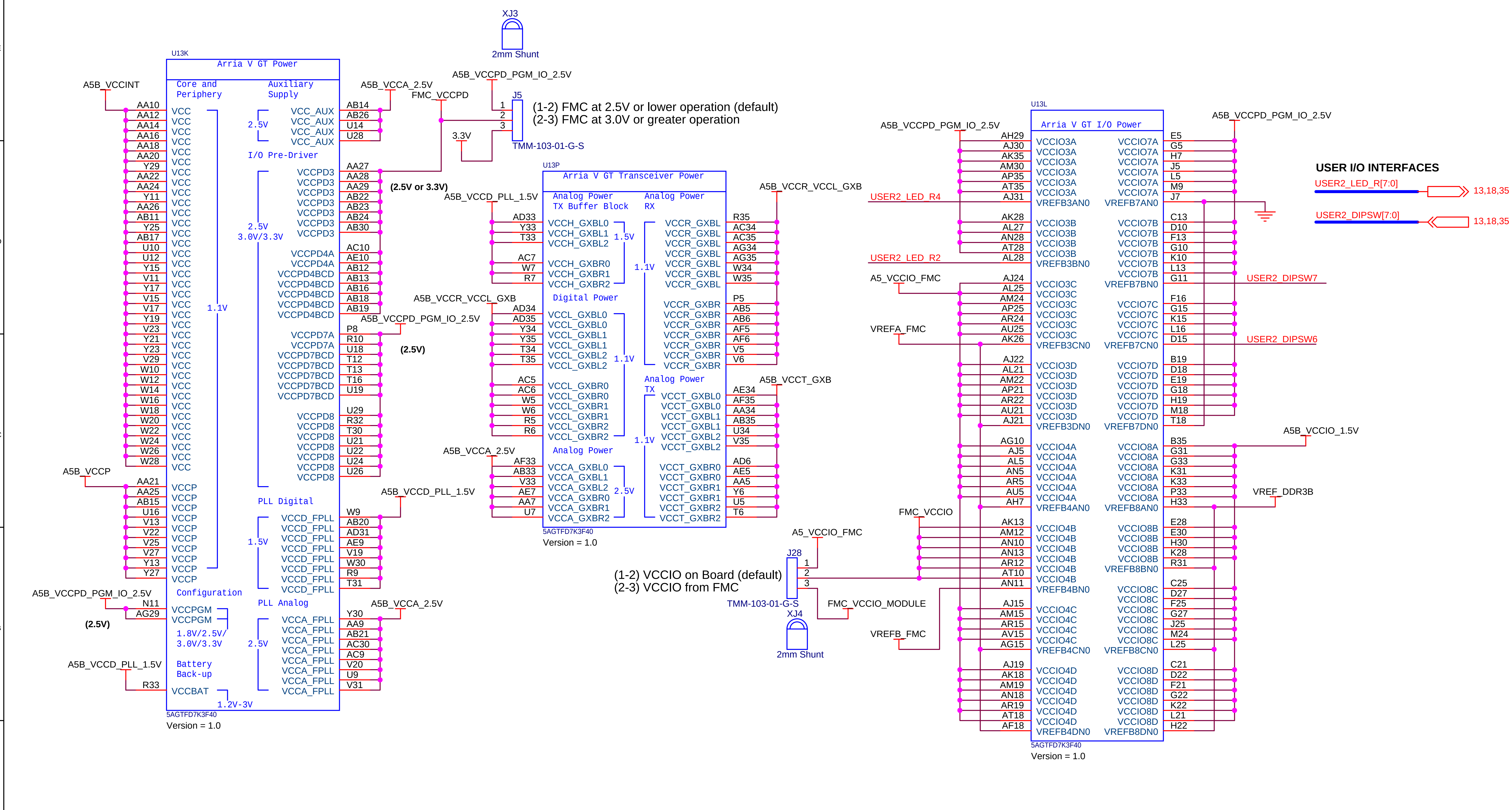
Power - Arria V GT Power (FPGA 2)



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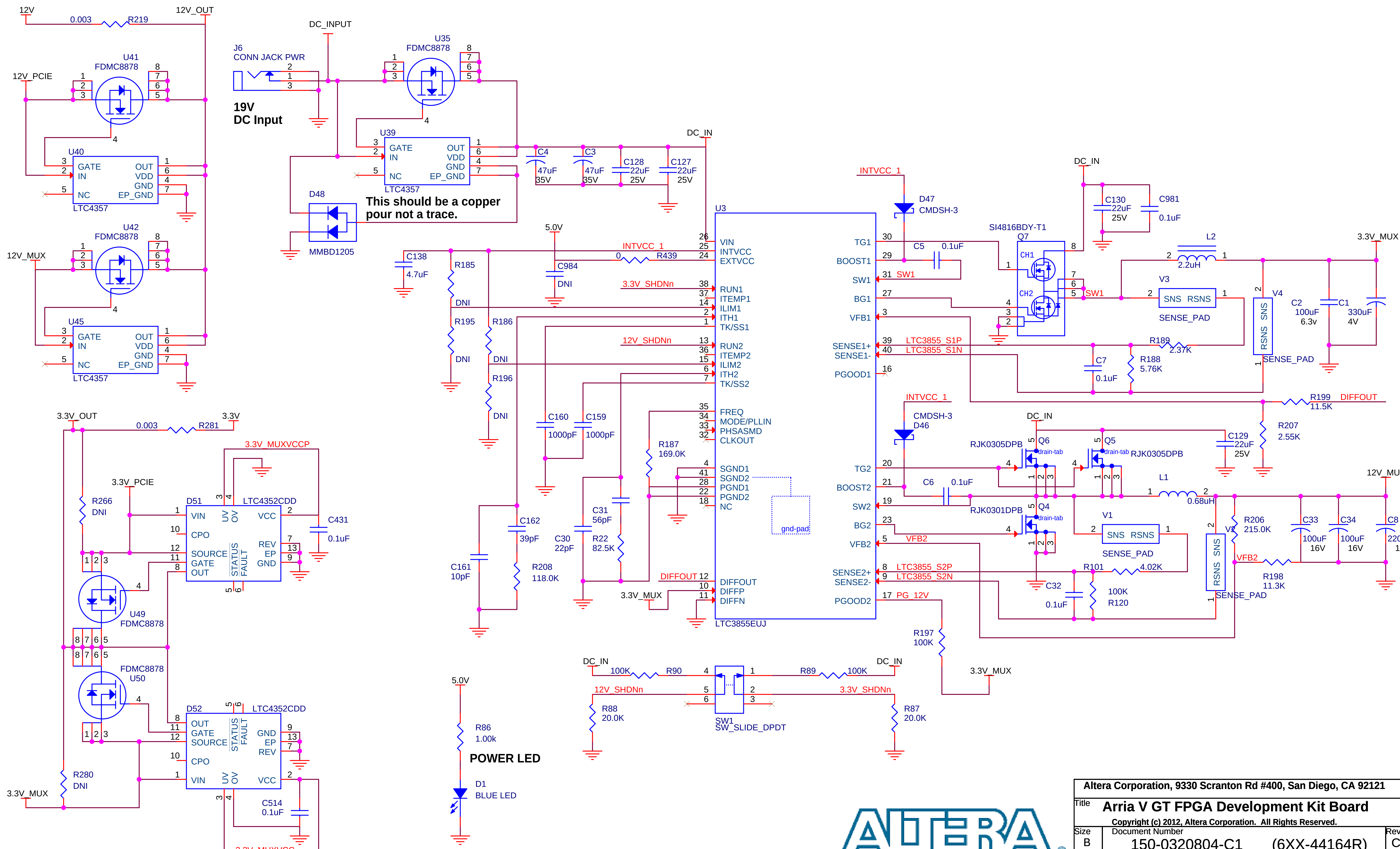
Power 1 - DC Input & 12V, 3.3V Output



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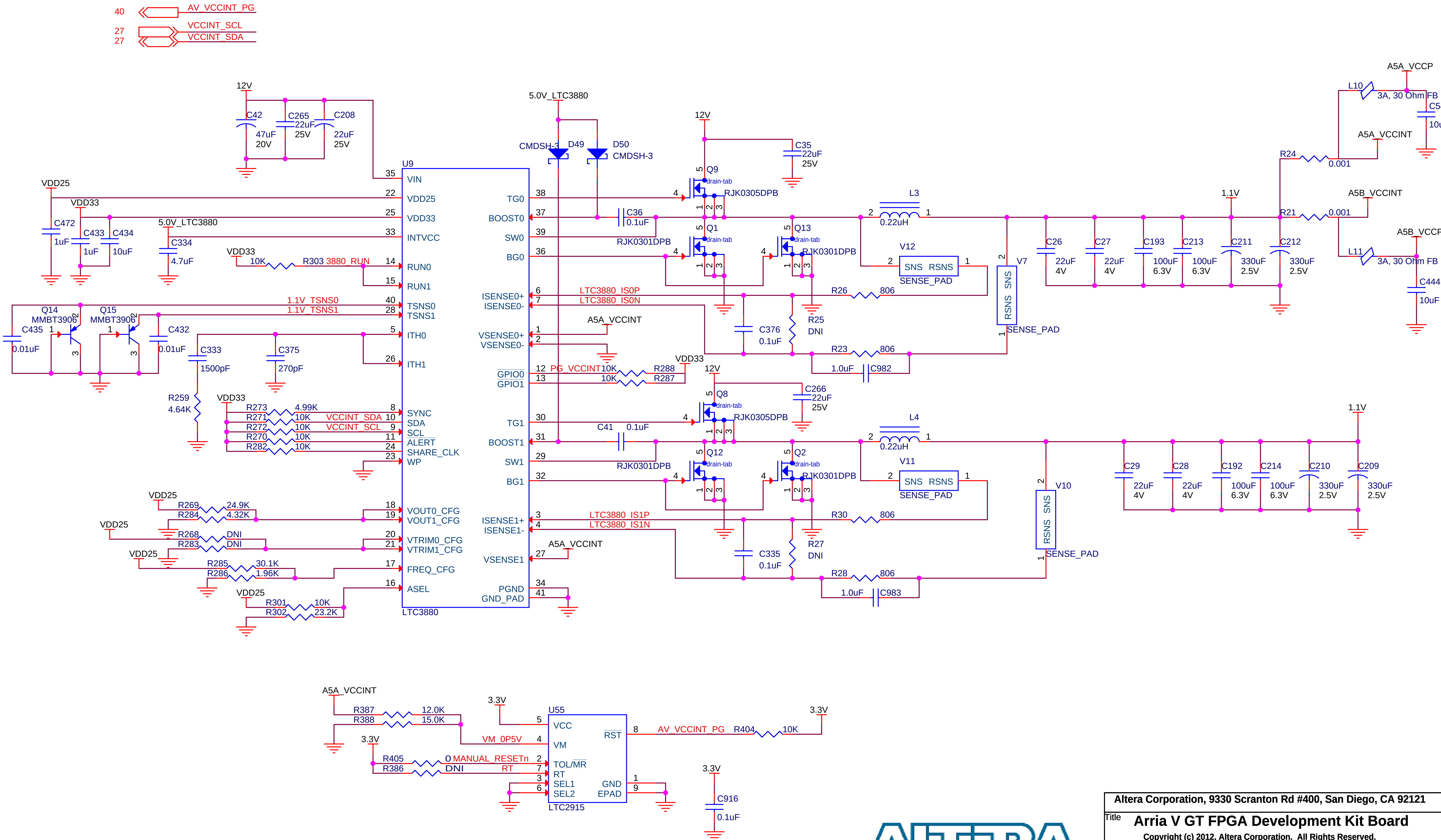
Power 2 - 1.1V (VCCINT)



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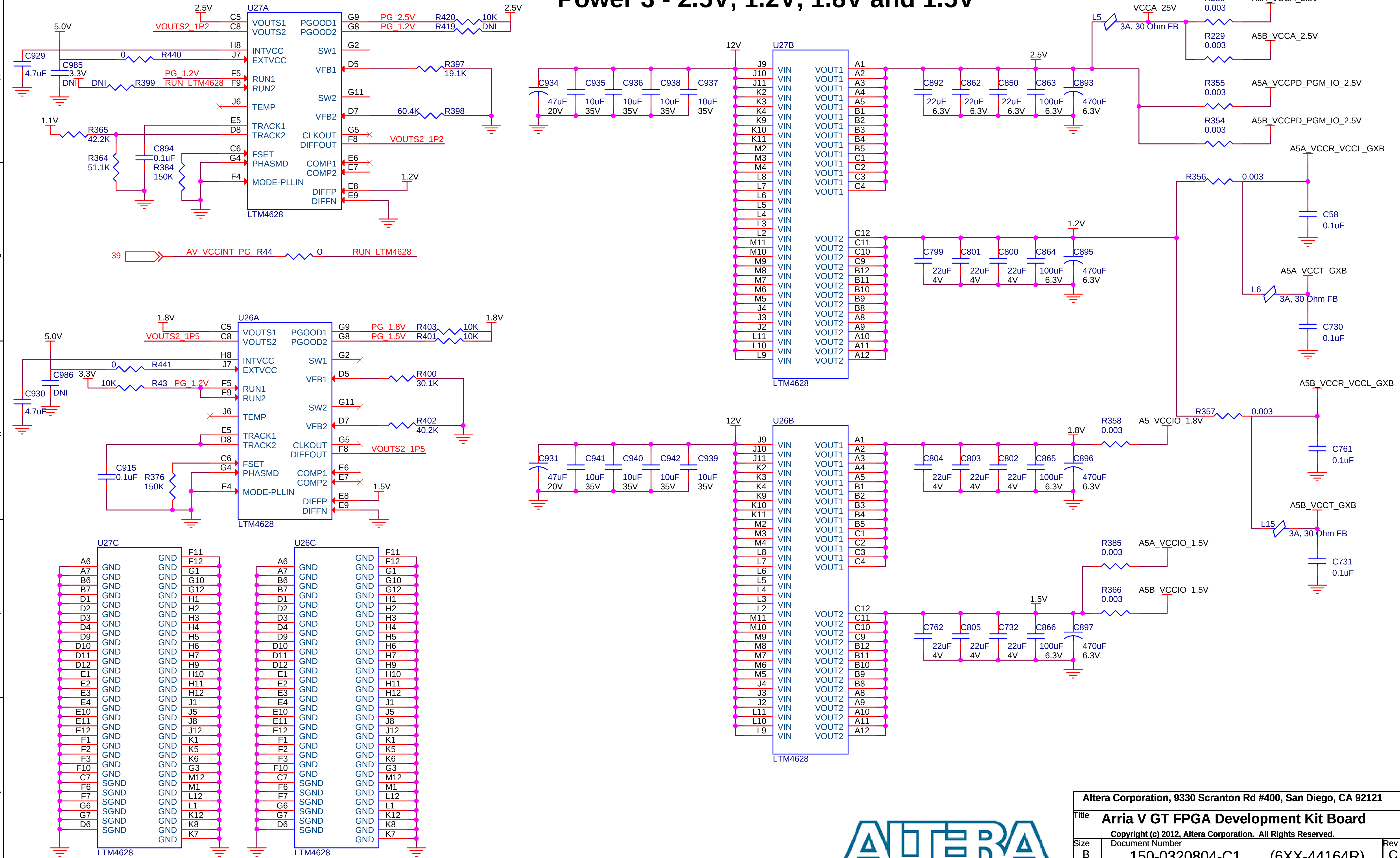
Power 3 - 2.5V, 1.2V, 1.8V and 1.5V



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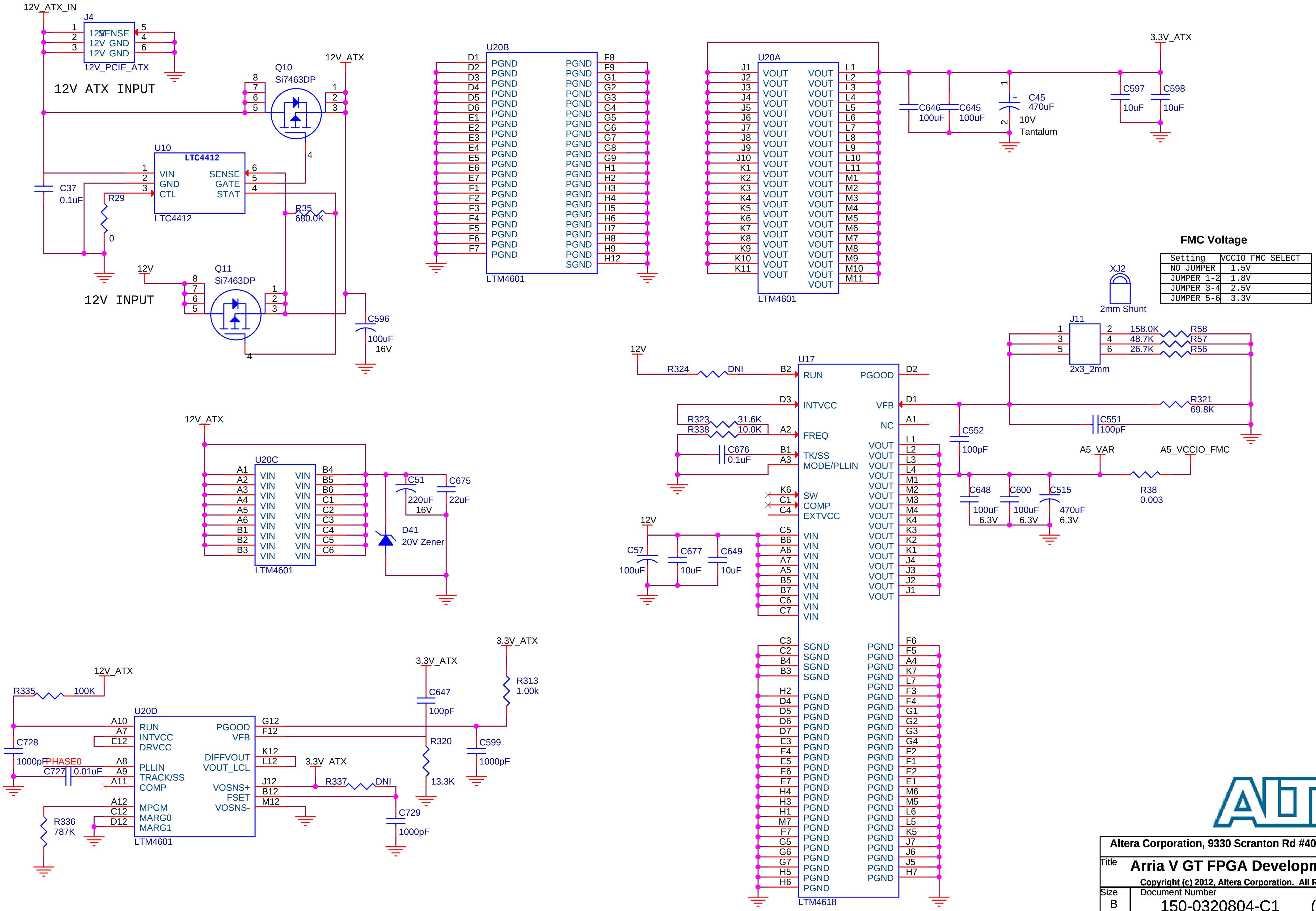
Power 3 - 3.3V_ATX and FMC Variable



FMC Voltage

Setting	VCCIO FMC SELECT
NO JUMPER	1.5V
JUMPER 1-2	1.8V
JUMPER 3-4	2.5V
JUMPER 5-6	3.3V

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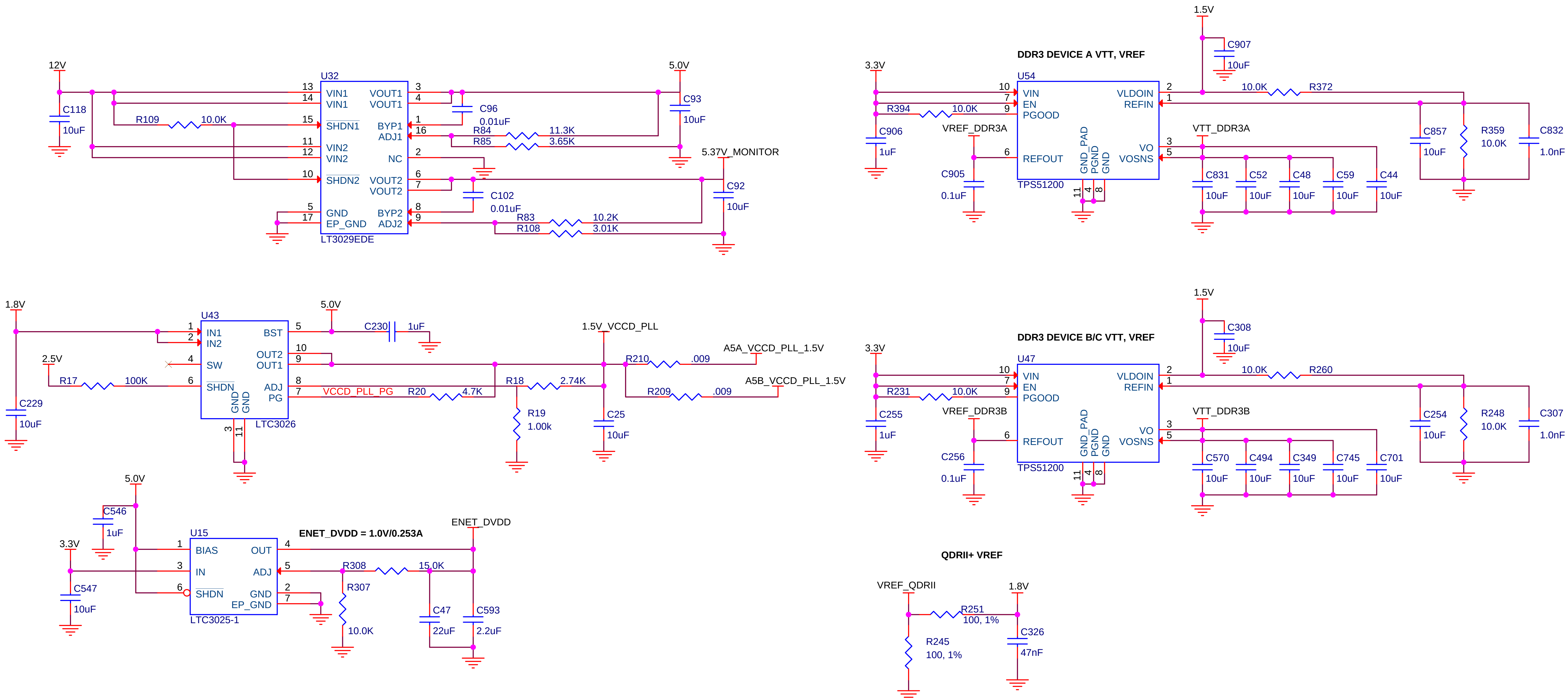
Power 4 - Linear Regulators



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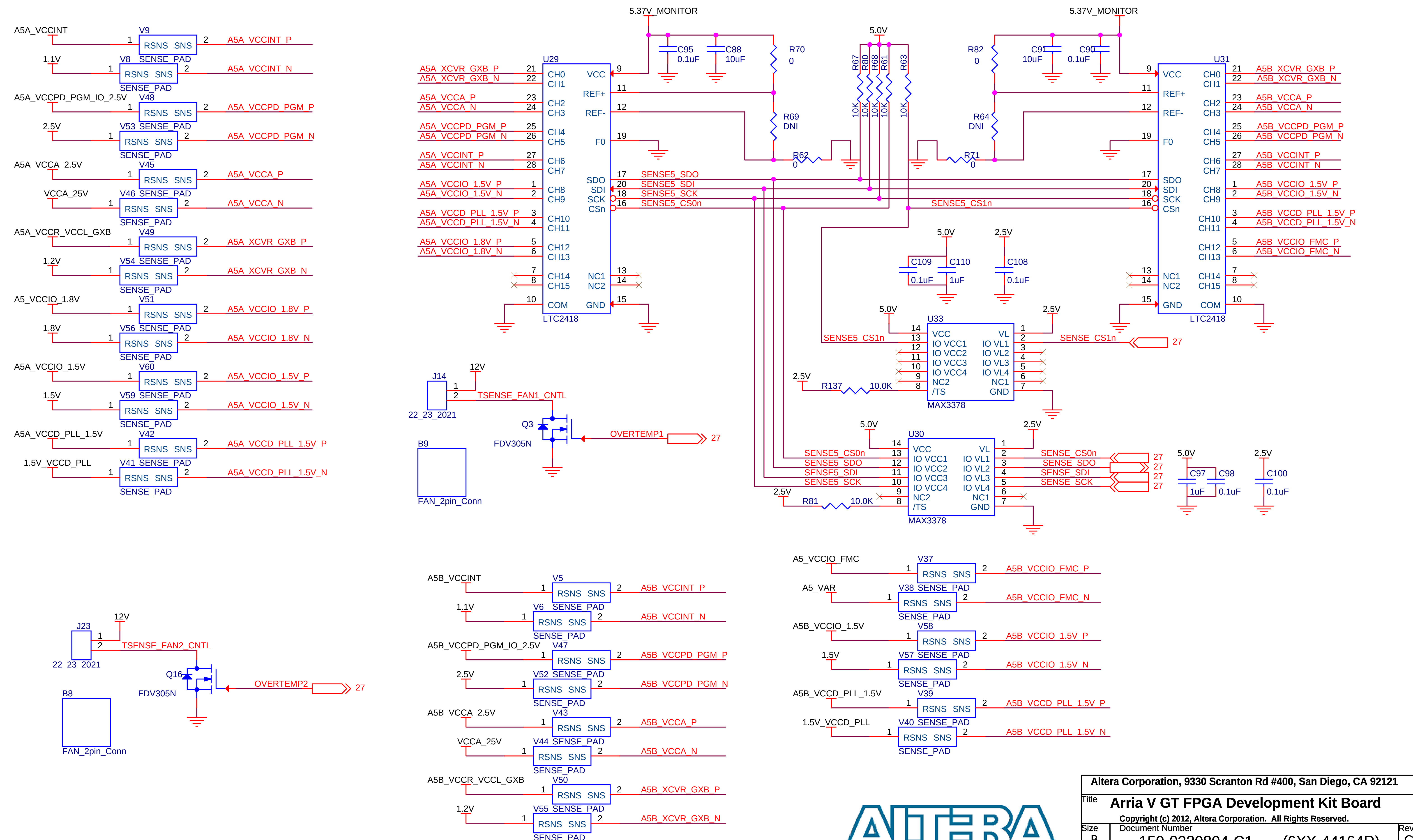
Power 6 - Power Monitor



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Decoupling - FPGA 1

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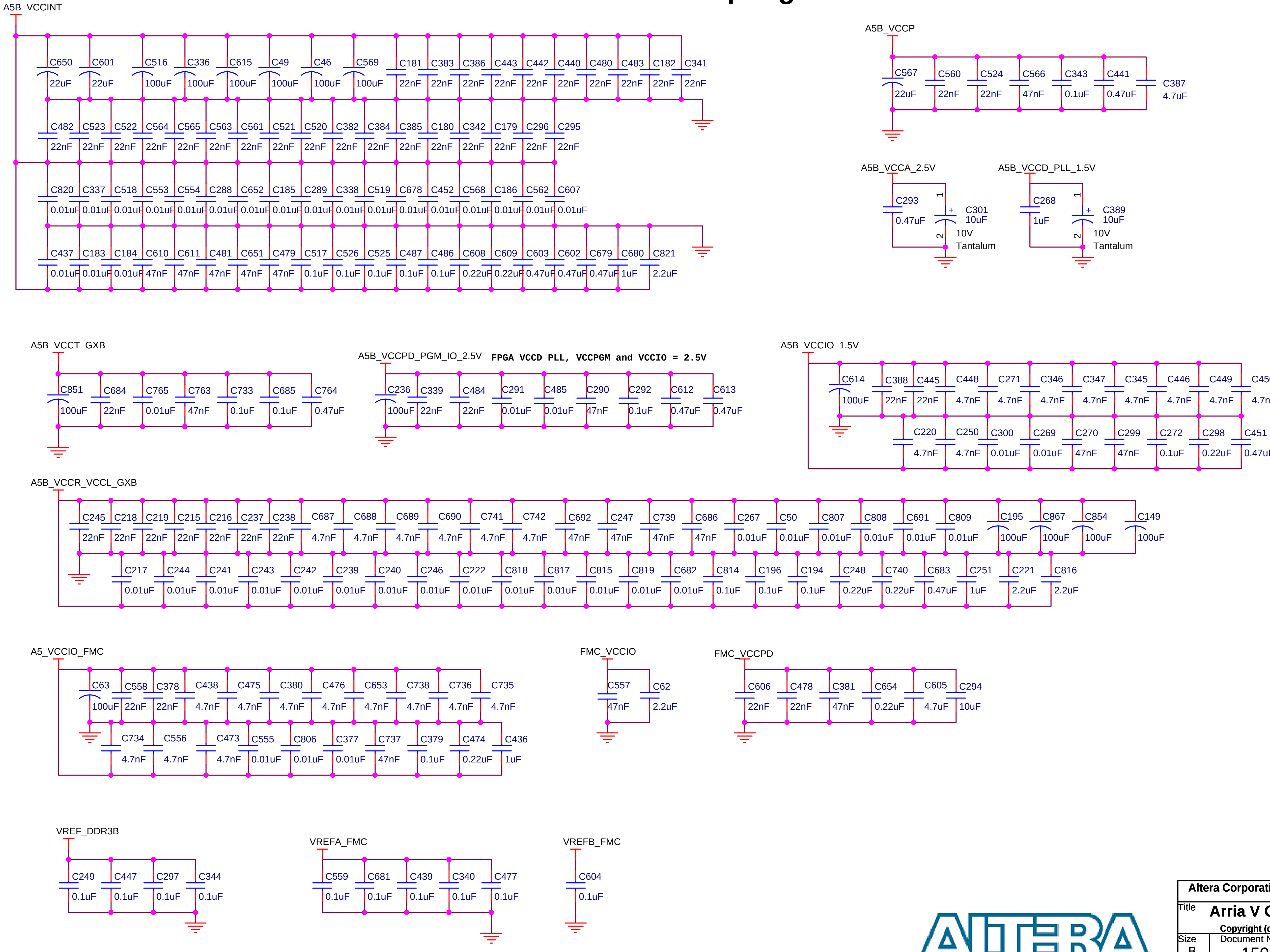
Decoupling - FPGA 2



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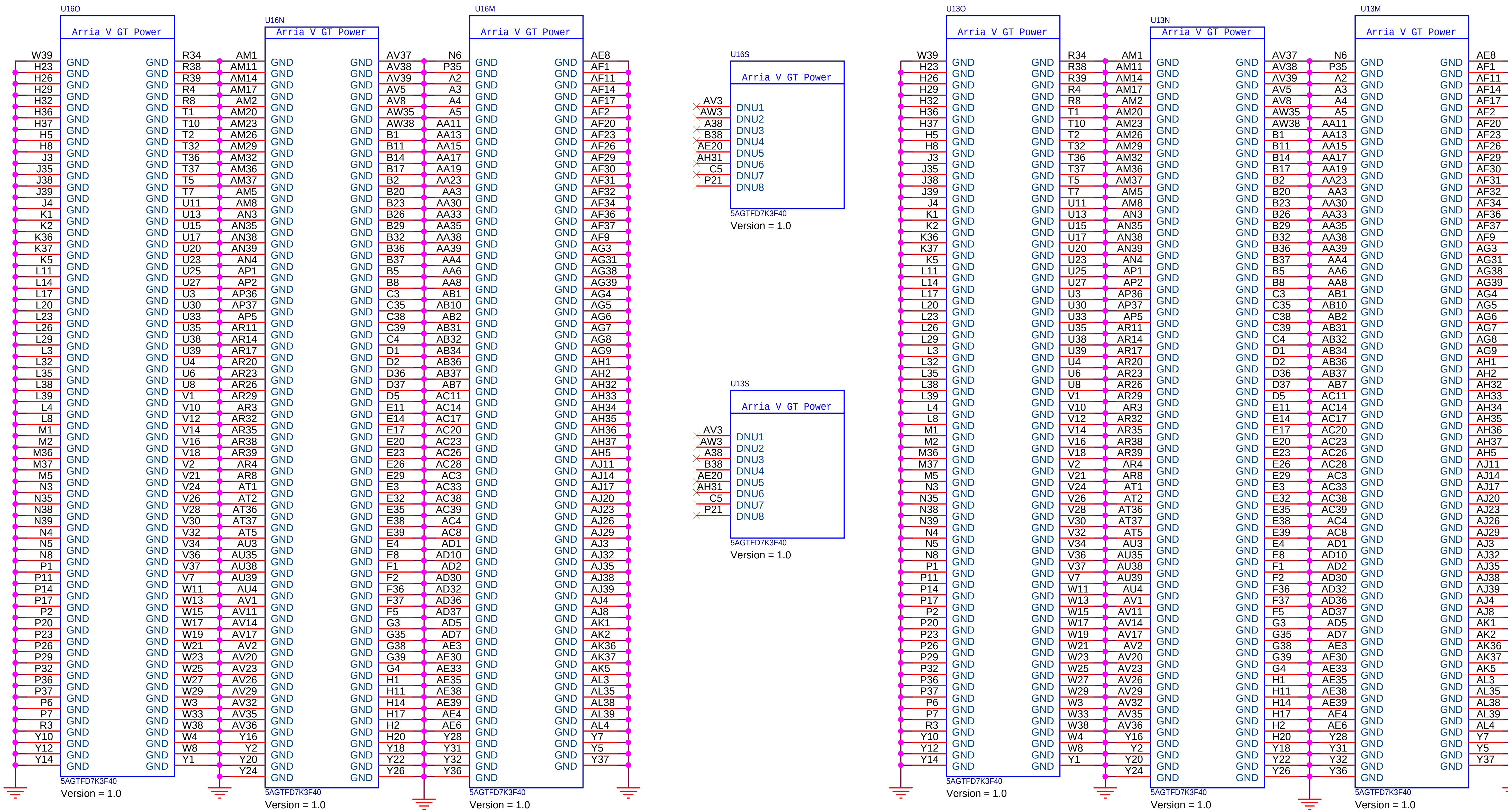
Power - Arria V GT Ground Power



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