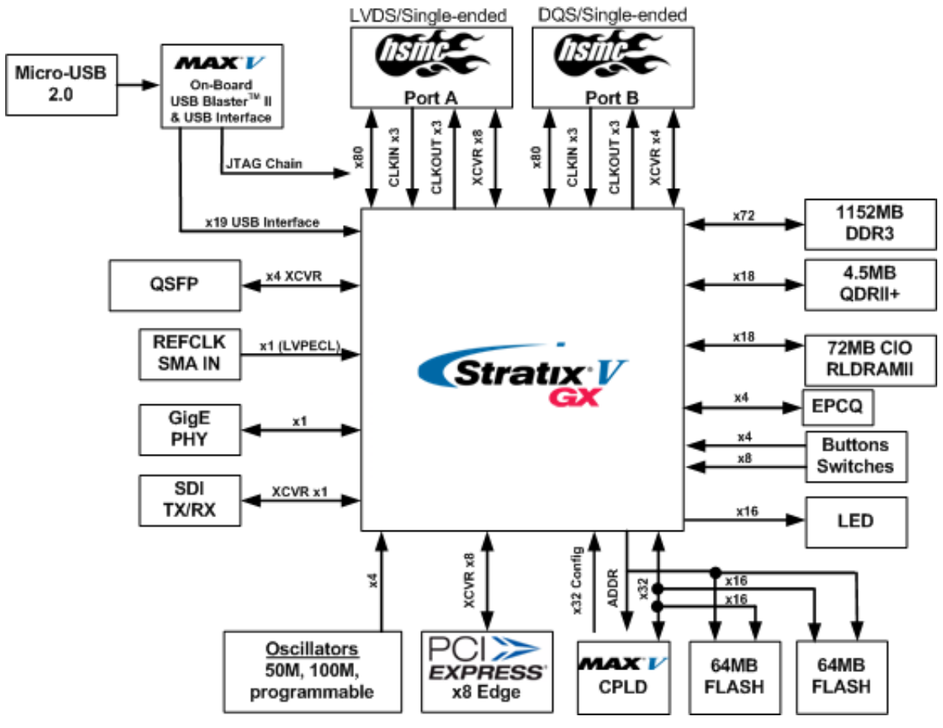
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0320202-D1
Gerber Files	110-0320202-D1
PCB Design Files	120-0320202-D1
Assembly Drawing	130-0320202-D1
Fab Drawing	140-0320202-D1
Schematic Drawing	150-0320202-D1
PCB Film	160-0320202-D1
Bill of Materials	170-0320202-D1
Schematic Design Files	180-0320202-D1
Functional Specification	210-0320202-D1
PCB Layout Guidelines	220-0320202-D1
Assembly Rework	320-0320202-D1

2. 1148 Parts, 88 Library Parts, 1306 Nets, 6595 Pins

Stratix V GX FPGA Development Kit Board



REV	DATE	PAGES	DESCRIPTION
D1	09/11/2012	22	REMOVE HSMC RESISTORS (AC CAP PLACEHOLDERS) R3-R18, R28-35. CHANGE MAX_RESETn TO 2.5V PULLUP, FROM 1.8V FOR LAYOUT IMPROVEMENT.
D1.1	05/16/2013	12	DNI U22

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 1 of 34

FPGA Package Top View

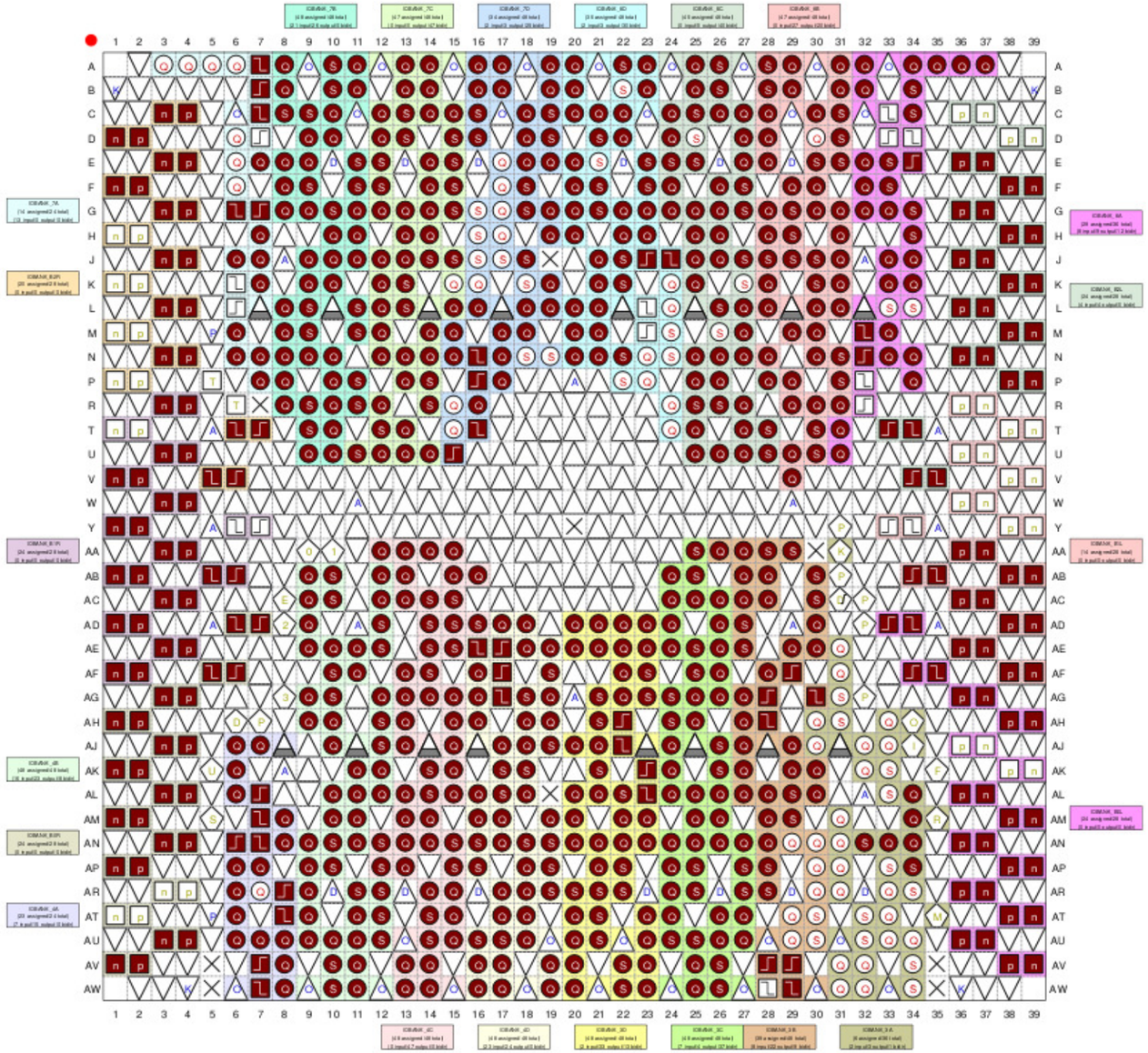
BANK 7B **VCCIO = 2.5V**
HSMA, QSFP CTL, DisplayPort CTL

BANK 7A
BANK 7C **VCCIO = 2.5V default/Variable**
HSMB, USER IO
BANK 7D

BANK 8A
BANK 8B **VCCIO = 1.5V**
DDR3, Embedded USB Blaster II
BANK 8C
BANK 8D

Top View - Flip Chip

Stratix V - 5SGXEA7K2F40C2ES



XCVR BANK QR2
HSMC Port B x2 (of 4 XCVRS)
DisplayPort (x4)

XCVR BANK QR3
QSFP
SDI

XCVR BANKS QR0, QR1
HSMC Port A x8
HSMC Port B x2 (of 4 XCVRS)

XCVR BANKS QR0, QR2
PCI Express x8

BANK 4B **VCCIO = 2.5V**
HSMA, USER IO
BANK 4A FLASH, USER IO **VCCIO = 1.8V**

BANK 4C QDRII+, FLASH **VCCIO = 1.8V**
BANK 4D

BANK 3A **VCCIO = 2.5V**
BANK 3B CONFIG, ENET, USER IO

BANK 3C **VCCIO = 1.8V**
BANK 3D RLDRAM II, FLASH

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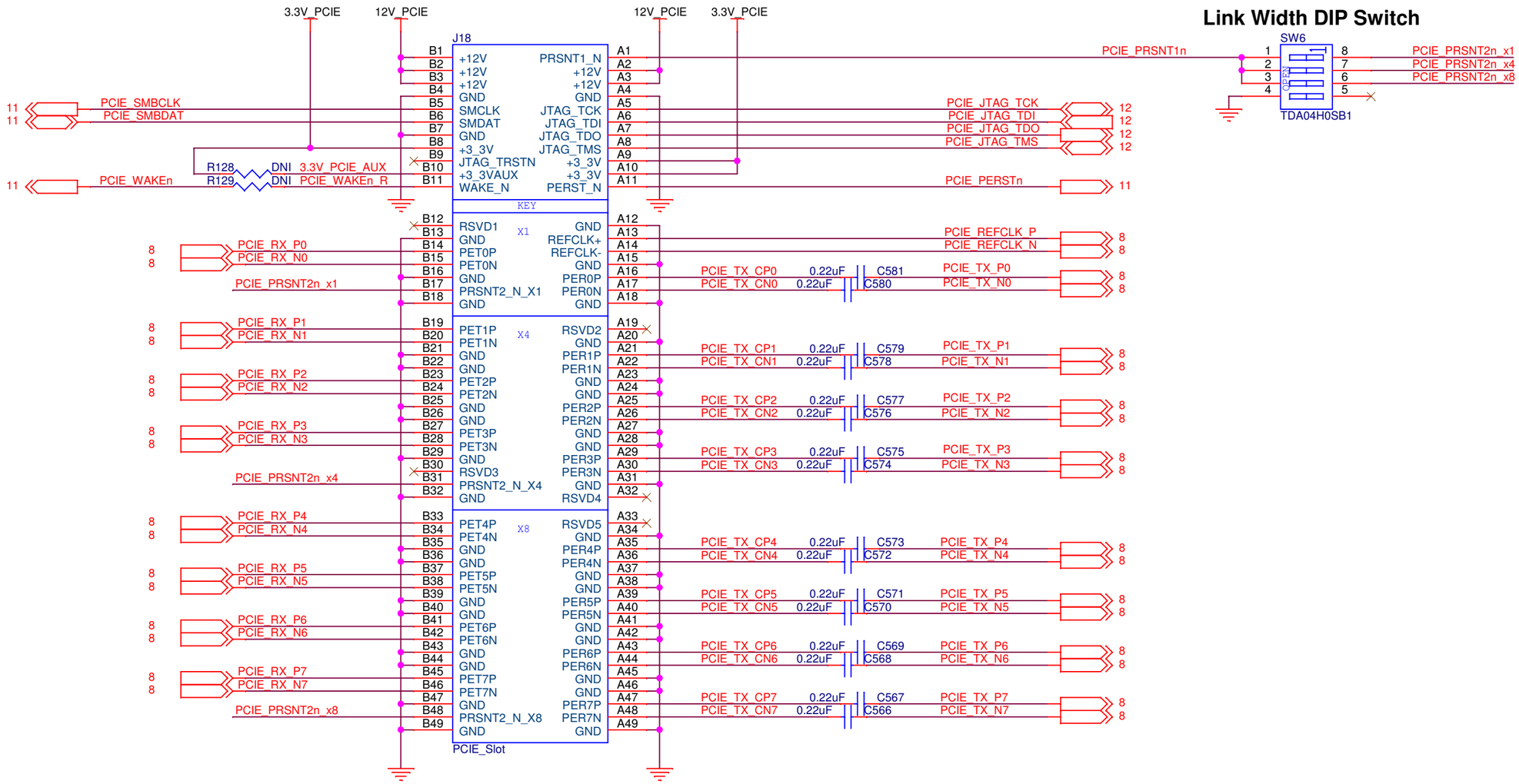
Title **Stratix V GX FPGA Development Kit Board**

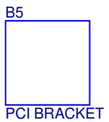
Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

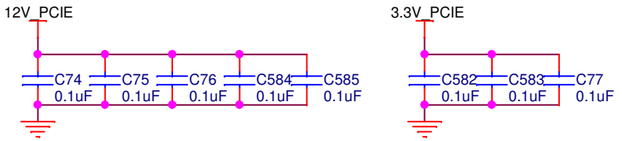
Date: Monday, June 03, 2013 Sheet 2 of 34

PCI Express Edge Connector



Link Width DIP Switch





Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 3 of 34

Stratix V Bank 3

U15A

Stratix V GX Bank 3

Bank 3A

VCCIO = 2.5V

		RZQ_0/DQSN1B/DIFFIO_RX_B2N	AR34	ENET_RX_N	See Stratix V GX Config sheet for ENET_RX_P

Bank 3B

VCCIO = 2.5V

HSMB_SDA	AK30	DQ11B/DIFFIO_TX_B31P	DQ13B/DIFFIO_TX_B37P	AA26	ENET_MDC
HSMB_SCL	AL30	DQ11B/DIFFIO_TX_B31N	DQ13B/DIFFIO_TX_B37N	AA27	ENET_MDIO
HSMA_D1	AK29	DQ11B/DIFFIO_TX_B33P	DQ13B/DIFFIO_TX_B39P	AB27	ENET_TX_P
HSMA_D0	AJ29	DQ11B/DIFFIO_TX_B33N	DQ13B/DIFFIO_TX_B39N	AC27	ENET_TX_N
PCIE_LED_X1	AL27	DQ12B/DIFFIO_TX_B35P	DQ14B/DIFFIO_TX_B41P	AG27	QSFP_MOD_SELn
PCIE_LED_G2	AL28	DQ12B/DIFFIO_TX_B35N	DQ14B/DIFFIO_TX_B41N	AH27	QSFP_MOD_PRSn
PCIE_LED_X8	AM28	DQ12B/DIFFIO_RX_B36P	DQ14B/DIFFIO_RX_B42P	AJ27	SDI_TX_SD_HDn
PCIE_LED_X4	AN28	DQ12B/DIFFIO_RX_B36N	DQ14B/DIFFIO_RX_B42N	AK27	SDI_TX_EN
HSMA_SDA	AL29			AA28	ENET_RESETn
HSMA_SCL	AM29	DQS11B/DIFFIO_RX_B32P	DQS13B/DIFFIO_RX_B38P	AA29	ENET_INTn
HSMA_D3	AP28	DQSN11B/DIFFIO_RX_B32N	DQSN13B/DIFFIO_RX_B38N	AD27	QSFP_LP_MODE
HSMA_D2	AR28	DQS12B/DIFFIO_RX_B34P	DQS14B/DIFFIO_RX_B40P	AE27	QSFP_INTERRUPTn
		DQSN12B/DIFFIO_RX_B34N	DQSN14B/DIFFIO_RX_B40N		

5SGXA7KF40

Version = 1.0 Pin-out

U15B

Stratix V GX Bank 3

Bank 3C

VCCIO = 1.8V

RLDC_DQ8	AT27	DQ15B/DIFFIO_TX_B43P	DQ19B/DIFFIO_TX_B55P	AV25	FM_D30
RLDC_DQ6	AU27	DQ15B/DIFFIO_TX_B43N	DQ19B/DIFFIO_TX_B55N	AW25	FM_D29
RLDC_DQ7	AT26	DQ15B/DIFFIO_TX_B45P	DQ19B/DIFFIO_TX_B57P	AR24	USER_LED_R3
RLDC_DQ5	AU26	DQ15B/DIFFIO_TX_B45N	DQ19B/DIFFIO_TX_B57N	AT24	FM_D31
RLDC_QVLD	AL26	DQ16B/DIFFIO_TX_B47P	DQ20B/DIFFIO_TX_B59P	AM25	FM_D14
RLDC_DQ3	AM26	DQ16B/DIFFIO_TX_B47N	DQ20B/DIFFIO_TX_B59N	AN25	FM_D13
RLDC_DQ2	AN26	DQ16B/DIFFIO_RX_B48P	DQ20B/DIFFIO_RX_B60P	AN24	FM_D16
RLDC_DQ1	AN27	DQ16B/DIFFIO_RX_B48N	DQ20B/DIFFIO_RX_B60N	AP24	FM_D15
RLDC_DQ4	AV26			AU24	USER_LED_G3
RLDC_DQ0	AW26	DQS15B/DIFFIO_RX_B44P	DQS19B/DIFFIO_RX_B56P	AU25	
RLDC_QK_P0	AP27	DQSN15B/DIFFIO_RX_B44N	DQSN19B/DIFFIO_RX_B56N	AP25	RLDC_DK_P
RLDC_QK_N0	AR27	DQS16B/DIFFIO_RX_B46P	DQS20B/DIFFIO_RX_B58P	AR25	RLDC_DK_N
		DQSN16B/DIFFIO_RX_B46N	DQSN20B/DIFFIO_RX_B58N		
RLDC_DQ11	AD26			AB24	FM_D18
RLDC_DQ12	AE26	DQ17B/DIFFIO_TX_B49P	DQ21B/DIFFIO_TX_B61P	AC24	FM_D17
RLDC_DQ9	AC25	DQ17B/DIFFIO_TX_B49N	DQ21B/DIFFIO_TX_B61N	AD24	FM_D22
RLDC_DQ10	AC26	DQ17B/DIFFIO_TX_B51P	DQ21B/DIFFIO_TX_B63P	AE24	FM_D21
RLDC_DQ13	AF26	DQ17B/DIFFIO_TX_B51N	DQ21B/DIFFIO_TX_B63N	AJ24	FM_D26
RLDC_DQ15	AG26	DQ18B/DIFFIO_TX_B53P	DQ22B/DIFFIO_TX_B65P	AK24	FM_D25
RLDC_DQ16	AG25	DQ18B/DIFFIO_TX_B53N	DQ22B/DIFFIO_TX_B65N	AL25	FM_D28
RLDC_DQ17	AH25	DQ18B/DIFFIO_RX_B54P	DQ22B/DIFFIO_RX_B66P	AL24	FM_D27
		DQ18B/DIFFIO_RX_B54N	DQ22B/DIFFIO_RX_B66N		
RLDC_DM	AB25			AE25	FM_D20
RLDC_DQ14	AA25	DQS17B/DIFFIO_RX_B50P	DQS21B/DIFFIO_RX_B62P	AF25	FM_D19
RLDC_QK_P1	AJ26	DQSN17B/DIFFIO_RX_B50N	DQSN21B/DIFFIO_RX_B62N	AH24	FM_D24
RLDC_QK_N1	AK26	DQS18B/DIFFIO_RX_B52P	DQS22B/DIFFIO_RX_B64P	AG24	FM_D23
		DQSN18B/DIFFIO_RX_B52N	DQSN22B/DIFFIO_RX_B64N		

Bank 3D

VCCIO = 1.8V

RLDC_A21	AV23	DQ23B/DIFFIO_TX_B67P	DQ27B/DIFFIO_TX_B79P	AV20	RLDC_A12
RLDC_A2	AW23	DQ23B/DIFFIO_TX_B67N	DQ27B/DIFFIO_TX_B79N	AW20	RLDC_A11
RLDC_A6	AT23	DQ23B/DIFFIO_TX_B69P	DQ27B/DIFFIO_TX_B81P	AT20	RLDC_A7
RLDC_A5	AU23	DQ23B/DIFFIO_TX_B69N	DQ27B/DIFFIO_TX_B81N	AU20	RLDC_A20
RLDC_REFn	AM22	DQ24B/DIFFIO_TX_B71P	DQ28B/DIFFIO_TX_B83P	AN20	RLDC_A19
RLDC_WEn	AN22	DQ24B/DIFFIO_TX_B71N	DQ28B/DIFFIO_TX_B83N	AM20	RLDC_A10
RLDC_A9	AM23	DQ24B/DIFFIO_RX_B72P	DQ28B/DIFFIO_RX_B84P	AN21	FM_D0
RLDC_CSn	AN23	DQ24B/DIFFIO_RX_B72N	DQ28B/DIFFIO_RX_B84N	AP21	FM_A25
RLDC_A22	AV22			AT21	RLDC_CK_P
RLDC_A1	AW22	DQS23B/DIFFIO_RX_B68P	DQS27B/DIFFIO_RX_B80P	AU21	RLDC_CK_N
RLDC_A16	AP22	DQSN23B/DIFFIO_RX_B68N	DQSN27B/DIFFIO_RX_B80N	AR20	RLDC_A17
RLDC_A18	AR22	DQS24B/DIFFIO_RX_B70P	DQS28B/DIFFIO_RX_B82P	AR21	RLDC_A15
		DQSN24B/DIFFIO_RX_B70N	DQSN28B/DIFFIO_RX_B82N		
RLDC_A3	AD23			AD20	FM_D2
RLDC_BA0	AE23	DQ25B/DIFFIO_TX_B73P	DQ29B/DIFFIO_TX_B85P	AD21	FM_D1
RLDC_A0	AD22	DQ25B/DIFFIO_TX_B73N	DQ29B/DIFFIO_TX_B85N	AE20	FM_D6
RLDC_A4	AE22	DQ25B/DIFFIO_TX_B75P	DQ29B/DIFFIO_TX_B87P	AE21	FM_D5
RLDC_BA1	AF22	DQ25B/DIFFIO_TX_B75N	DQ29B/DIFFIO_TX_B87N	AJ20	FM_D10
RLDC_A13	AG22	DQ26B/DIFFIO_TX_B77P	DQ30B/DIFFIO_TX_B89P	AJ21	FM_D9
		DQ26B/DIFFIO_TX_B77N	DQ30B/DIFFIO_TX_B89N	AL20	FM_D12
			DQ30B/DIFFIO_RX_B90P	AL21	FM_D11
			DQ30B/DIFFIO_RX_B90N		
RLDC_A14	AF23			AH21	FM_D4
RLDC_A8	AG23	DQS25B/DIFFIO_RX_B74P	DQS29B/DIFFIO_RX_B86P	AG21	FM_D3
		DQSN25B/DIFFIO_RX_B74N	DQSN29B/DIFFIO_RX_B86N	AK21	FM_D8
			DQS30B/DIFFIO_RX_B88P	AL22	FM_D7
			DQSN30B/DIFFIO_RX_B88N		

5SGXA7KF40

Version = 1.0 Pin-out

FLASH & MAX BUS INTERFACE

FM_D[31:0] 17,18

FM_A[26:0] 17,18,5,9

LCD & USER I/O INTERFACES

USER_LED_R[7:0] 24,9

USER_LED_G3 24

ETHERNET INTERFACE

ENET_RX_N 23
ENET_INTn 23
ENET_RESETn 23
ENET_MDIO 23
ENET_MDC 23
ENET_TX_P 23
ENET_TX_N 23

HSMC INTERFACE

HSMA_D[3:0] 22

HSMA_SDA 22
HSMA_SCL 22

HSMB_SDA 22
HSMB_SCL 22

PCIE INTERFACE

PCIE_LED_G2 24
PCIE_LED_X1 24
PCIE_LED_X4 24
PCIE_LED_X8 24

SDI INTERFACE

SDI_TX_SD_HDn 21
SDI_TX_EN 18,21

RLDRAM II INTERFACE

RLDC_DQ[17:0] RLDC_DQ[17:0] 16

RLDC_QK_P[1:0] RLDC_QK_P[1:0] 16

RLDC_QK_N[1:0] RLDC_QK_N[1:0] 16

RLDC_A[22:0] RLDC_A[22:0] 16

RLDC_BA[2:0] RLDC_BA[2:0] 16,9

RLDC_CK_P RLDC_CK_P 16
RLDC_CK_N RLDC_CK_N 16

RLDC_DK_P RLDC_DK_P 16
RLDC_DK_N RLDC_DK_N 16

RLDC_CSn RLDC_CSn 16,4
RLDC_WEn RLDC_WEn 16
RLDC_REFn RLDC_REFn 16
RLDC_CSn RLDC_CSn 16,4
RLDC_DM RLDC_DM 16
RLDC_QVLD RLDC_QVLD 16

QSFP INTERFACE

QSFP_MOD_SELn QSFP_MOD_SELn 19
QSFP_LP_MODE QSFP_LP_MODE 19
QSFP_INTERRUPTn QSFP_INTERRUPTn 19
QSFP_MOD_PRSn QSFP_MOD_PRSn 19

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 4 of 34

Stratix V Bank 4

U15C

Stratix V GX Bank 4

Bank 4A

VCCIO = 1.8V

HSMA_RX_LED	AV8	DQ67B/DIFFIO_TX_B199P	DQ70B/DIFFIO_RX_B210N	AL6	FLASH_RDYBSYn0
HSMA_PRSNTn	AW8	DQ67B/DIFFIO_TX_B199N	DQ70B/DIFFIO_TX_B209P	AJ6	FLASH_RESETn
HSMB_PRSNTn	AU7	DQ67B/DIFFIO_TX_B201P	DQ70B/DIFFIO_TX_B209N	AJ7	FLASH_OEn
HSMA_TX_LED	AU8	DQ67B/DIFFIO_TX_B201N			
HSMB_TX_LED	AP6	DQ69B/DIFFIO_TX_B205P	RZQ_1/DQ70B/DIFFIO_RX_B210P	AK6	R199 100, 1%
HSMB_RX_LED	AR6	DQ69B/DIFFIO_TX_B205N			
FLASH_WEn	AN8	DQ69B/DIFFIO_TX_B207P			
FLASH_CLK	AM8	DQ69B/DIFFIO_TX_B207N			

Bank 4B

VCCIO = 2.5V

HSMA_TX_D_P7	AB12	DQ59B/DIFFIO_TX_B175P	DQ63B/DIFFIO_TX_B187P	AB9	HSMA_TX_D_P6
HSMA_TX_D_N7	AC12	DQ59B/DIFFIO_TX_B175N	DQ63B/DIFFIO_TX_B187N	AC9	HSMA_TX_D_N6
HSMA_TX_D_P4	AE10	DQ59B/DIFFIO_TX_B177P	DQ63B/DIFFIO_TX_B189P	AD9	HSMA_TX_D_P5
HSMA_TX_D_N4	AE11	DQ59B/DIFFIO_TX_B177N	DQ63B/DIFFIO_TX_B189N	AE9	HSMA_TX_D_N5
HSMA_TX_D_P3	AG12	DQ60B/DIFFIO_TX_B179P	DQ64B/DIFFIO_TX_B191P	AG9	HSMA_CLK_OUT_P1
HSMA_TX_D_N3	AF11	DQ60B/DIFFIO_TX_B179N	DQ64B/DIFFIO_TX_B191N	AH9	HSMA_CLK_OUT_N1
HSMA_RX_D_P3	AL12	DQ60B/DIFFIO_RX_B180P	DQ64B/DIFFIO_RX_B192P	AH10	LCD_D_Cn
HSMA_RX_D_N3	AK12	DQ60B/DIFFIO_RX_B180N	DQ64B/DIFFIO_RX_B192N	AJ10	HSMA_CLK_OUT0
HSMA_RX_D_P6	AD12	DQS59B/DIFFIO_RX_B176P	DQS63B/DIFFIO_RX_B188P	AB10	HSMA_RX_D_P7
HSMA_RX_D_N6	AE12	DQSN59B/DIFFIO_RX_B176N	DQSN63B/DIFFIO_RX_B188N	AC10	HSMA_RX_D_N7
HSMA_RX_D_P4	AH12	DQS60B/DIFFIO_RX_B178P	DQS64B/DIFFIO_RX_B190P	AF10	HSMA_RX_D_P5
HSMA_RX_D_N4	AJ12	DQSN60B/DIFFIO_RX_B178N	DQSN64B/DIFFIO_RX_B190N	AG10	HSMA_RX_D_N5
HSMA_TX_D_P2	AK11	DQ61B/DIFFIO_TX_B181P	DQ65B/DIFFIO_TX_B193P	AL10	LCD_DATA3
HSMA_TX_D_N2	AL11	DQ61B/DIFFIO_TX_B181N	DQ65B/DIFFIO_TX_B193N	AM10	LCD_DATA2
HSMA_TX_D_P1	AM11	DQ61B/DIFFIO_TX_B183P	DQ65B/DIFFIO_TX_B195P	AN9	LCD_DATA5
HSMA_TX_D_N1	AN11	DQ61B/DIFFIO_TX_B183N	DQ65B/DIFFIO_TX_B195N	AP9	LCD_DATA4
HSMA_TX_D_P0	AT11	DQ62B/DIFFIO_TX_B185P	DQ66B/DIFFIO_TX_B197P	AR9	LCD_DATA7
HSMA_TX_D_N0	AU11	DQ62B/DIFFIO_TX_B185N	DQ66B/DIFFIO_TX_B197N	AT9	LCD_DATA6
HSMA_RX_D_P0	AV11	DQ62B/DIFFIO_RX_B186P	DQ66B/DIFFIO_RX_B198P	AU9	LCD_CSn
HSMA_RX_D_N0	AW11	DQ62B/DIFFIO_RX_B186N	DQ66B/DIFFIO_RX_B198N	AU10	SDI_CLK148_DN
HSMA_RX_D_P2	AR11	DQS61B/DIFFIO_RX_B182P	DQS65B/DIFFIO_RX_B194P	AN10	LCD_DATA1
HSMA_RX_D_N2	AR12	DQSN61B/DIFFIO_RX_B182N	DQSN65B/DIFFIO_RX_B194N	AP10	LCD_DATA0
HSMA_RX_D_P1	AT12	DQS62B/DIFFIO_RX_B184P	DQS66B/DIFFIO_RX_B196P	AV10	USER_LED_G7
HSMA_RX_D_N1	AU12	DQSN62B/DIFFIO_RX_B184N	DQSN66B/DIFFIO_RX_B196N	AW10	LCD_WEn

5SGXA7KF40

Version = 1.0 Pin-out

QDRII+ QVLD = QDRII C_P
QDRII+ ODT = QDRII C_N

U15D

Stratix V GX Bank 4

Bank 4C

VCCIO = 1.8V

QDRII_D1	AB16	DQ51B/DIFFIO_TX_B151P	DQ55B/DIFFIO_TX_B163P	AB13	QDRII_A13
QDRII_D2	AB15	DQ51B/DIFFIO_TX_B151N	DQ55B/DIFFIO_TX_B163N	AC13	QDRII_A14
QDRII_D5	AA14	DQ51B/DIFFIO_TX_B153P	DQ55B/DIFFIO_TX_B165P	AA12	QDRII_A18
QDRII_D4	AA15	DQ51B/DIFFIO_TX_B153N	DQ55B/DIFFIO_TX_B165N	AA13	QDRII_A20
QDRII_BWSn0	AH15	DQ52B/DIFFIO_TX_B155P	DQ56B/DIFFIO_TX_B167P	AH13	QDRII_A7
QDRII_BWSn1	AJ15	DQ52B/DIFFIO_TX_B155N	DQ56B/DIFFIO_TX_B167N	AJ13	QDRII_A8
QDRII_RPSn	AG15	DQ52B/DIFFIO_RX_B156P	DQ56B/DIFFIO_RX_B168P	AF13	QDRII_A2
QDRII_D8	AG14	DQ52B/DIFFIO_RX_B156N	DQ56B/DIFFIO_RX_B168N	AG13	QDRII_A4
QDRII_D3	AC15	DQS51B/DIFFIO_RX_B152P	DQS55B/DIFFIO_RX_B164P	AC14	QDRII_A9
QDRII_D7	AD16	DQSN51B/DIFFIO_RX_B152N	DQSN55B/DIFFIO_RX_B164N	AD14	QDRII_A6
QDRII_D0	AD15	DQS52B/DIFFIO_RX_B154P	DQS56B/DIFFIO_RX_B166P	AE14	QDRII_A10
QDRII_D6	AE15	DQSN52B/DIFFIO_RX_B154N	DQSN56B/DIFFIO_RX_B166N	AF14	QDRII_A15
QDRII_WPSn	AK15	DQ53B/DIFFIO_TX_B157P	DQ57B/DIFFIO_TX_B169P	AL13	QDRII_A16
QDRII_D9	AL15	DQ53B/DIFFIO_TX_B157N	DQ57B/DIFFIO_TX_B169N	AM13	QDRII_A11
QDRII_D10	AM14	DQ53B/DIFFIO_TX_B159P	DQ57B/DIFFIO_TX_B171P	AN13	QDRII_A5
QDRII_D12	AN14	DQ53B/DIFFIO_TX_B159N	DQ57B/DIFFIO_TX_B171N	AP13	QDRII_A1
QDRII_D15	AR14	DQ54B/DIFFIO_TX_B161P	DQ58B/DIFFIO_TX_B173P	AV14	FLASH_CEn0
QDRII_D16	AR15	DQ54B/DIFFIO_TX_B161N	DQ58B/DIFFIO_TX_B173N	AW14	QDRII_A12
QDRII_D13	AT15	DQ54B/DIFFIO_RX_B162P	DQ58B/DIFFIO_RX_B174P	AV13	QDRII_DOFFn
QDRII_D17	AU15	DQ54B/DIFFIO_RX_B162N	DQ58B/DIFFIO_RX_B174N	AW13	FLASH_CEn1
QDRII_K_P	AK14	DQS53B/DIFFIO_RX_B158P	DQS57B/DIFFIO_RX_B170P	AN12	QDRII_A17
QDRII_K_N	AL14	DQSN53B/DIFFIO_RX_B158N	DQSN57B/DIFFIO_RX_B170N	AP12	QDRII_A19
QDRII_D11	AN15	DQS54B/DIFFIO_RX_B160P	DQS58B/DIFFIO_RX_B172P	AT14	QDRII_A3
QDRII_D14	AP15	DQSN54B/DIFFIO_RX_B160N	DQSN58B/DIFFIO_RX_B172N	AU14	QDRII_A0

Bank 4D

VCCIO = 1.8V

QDRII_Q5	AG19	DQ43B/DIFFIO_TX_B127P	DQ47B/DIFFIO_TX_B141P	AL16	FM_A3
QDRII_Q8	AH19	DQ43B/DIFFIO_TX_B127N	DQ47B/DIFFIO_TX_B141N	AM16	FM_A2
QDRII_Q6	AH18	DQ43B/DIFFIO_TX_B129P			
QDRII_Q7	AJ18	DQ43B/DIFFIO_TX_B129N			
QDRII_Q1	AE18	DQ44B/DIFFIO_TX_B131P	DQ48B/DIFFIO_TX_B143P	AF16	FM_A4
QDRII_Q3	AE19	DQ44B/DIFFIO_TX_B131N	DQ48B/DIFFIO_TX_B143N	AG16	FM_A5
QDRII_Q2	AD18	DQ44B/DIFFIO_RX_B132P			
QDRII_Q0	AD17	DQ44B/DIFFIO_RX_B132N			
QDRII_Q9	AJ19	DQS43B/DIFFIO_RX_B128P			
QDRII_Q10	AK18	DQSN43B/DIFFIO_RX_B128N			
QDRII_CQ_N	AF19	DQS44B/DIFFIO_RX_B130P			
QDRII_Q4	AG18	DQSN44B/DIFFIO_RX_B130N			
QDRII_Q11	AL18	DQ45B/DIFFIO_TX_B133P	DQ49B/DIFFIO_TX_B145P	AM17	FM_A7
QDRII_Q17	AM19	DQ45B/DIFFIO_TX_B133N	DQ49B/DIFFIO_TX_B145N	AN17	FM_A6
QDRII_Q13	AP18	DQ45B/DIFFIO_TX_B135P	DQ49B/DIFFIO_TX_B147P	AR17	FM_A11
QDRII_Q14	AR18	DQ45B/DIFFIO_TX_B135N	DQ49B/DIFFIO_TX_B147N	AT17	FM_A10
QDRII_C_P	AT18	DQ46B/DIFFIO_TX_B137P	DQ50B/DIFFIO_TX_B149P	AV16	FM_A15
QDRII_C_N	AU18	DQ46B/DIFFIO_TX_B137N	DQ50B/DIFFIO_TX_B149N	AW16	FM_A14
FM_A1	AV19	DQ46B/DIFFIO_RX_B138P	DQ50B/DIFFIO_RX_B150P	AV17	FM_A17
FM_A0	AW19	DQ46B/DIFFIO_RX_B138N	DQ50B/DIFFIO_RX_B150N	AW17	FM_A16
QDRII_CQ_P	AN19	DQS45B/DIFFIO_RX_B134P	DQS49B/DIFFIO_RX_B146P	AN16	FM_A9
QDRII_Q16	AN18	DQSN45B/DIFFIO_RX_B134N	DQSN49B/DIFFIO_RX_B146N	AP16	FM_A8
QDRII_Q15	AP19	DQS46B/DIFFIO_RX_B136P	DQS50B/DIFFIO_RX_B148P	AU17	FM_A13
QDRII_Q12	AR19	DQSN46B/DIFFIO_RX_B136N	DQSN50B/DIFFIO_RX_B148N	AU16	FM_A12

5SGXA7KF40

Version = 1.0 Pin-out

QDRII INTERFACE

QDRII_A[20:0] — 15
QDRII_D[17:0] — 15
QDRII_Q[17:0] — 15
QDRII_C_P — 15
QDRII_CQ_P — 15
QDRII_CQ_N — 15
QDRII_K_P — 15
QDRII_K_N — 15
QDRII_BWSn0 — 15
QDRII_BWSn1 — 15
QDRII_WPSn — 15
QDRII_RPSn — 15
QDRII_C_N — 15
QDRII_DOFFn — 15

FLASH INTERFACE

FM_A[26:0] — 17,18,4,9
FLASH_OEn — 17,18
FLASH_CLK — 17,18
FLASH_WEn — 17,18
FLASH_RDYBSYn0 — 17,18
FLASH_RESETn — 17,18
FLASH_CEn0 — 17,18
FLASH_CEn1 — 17,18

LCD & USER I/O INTERFACES

LCD_DATA[7:0] — 24
LCD_CSn — 24
LCD_D_Cn — 24
LCD_WEn — 24
USER_LED_G[7:0] — 11,24,4,6,9

HSMC INTERFACE

HSMB_TX_LED — 24
HSMA_CLK_OUT0 — 22
HSMA_TX_LED — 24
HSMA_RX_LED — 24
HSMA_PRSNTn — 18,22,24
HSMB_PRSNTn — 18,22,24
HSMB_RX_LED — 24
HSMA_CLK_OUT_P[2:1] — 22,6
HSMA_CLK_OUT_N[2:1] — 22,6
HSMA_TX_D_P[16:0] — 22,6
HSMA_TX_D_N[16:0] — 22,6
HSMA_RX_D_P[16:0] — 22,6
HSMA_RX_D_N[16:0] — 22,6

Si571 VCXO

SDI_CLK148_DN — 10

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Stratix V GX FPGA Development Kit Board

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 5 of 34

Stratix V Bank 7

U15E

Stratix V GX Bank 7

Bank 7A

VCCIO = HSMB VARIABLE
1.2V/1.5V/1.8V/2.5V

USER_DIPSW1	H7	DQ1T/DIFFIO_RX_T1N	DQ4T/DIFFIO_TX_T10P	E6	
USER_DIPSW2	J7	DQ1T/DIFFIO_TX_T2P	DQ4T/DIFFIO_TX_T10N	D6	
USER_DIPSW3	K7	DQ1T/DIFFIO_TX_T2N	DQ4T/DIFFIO_TX_T12P	F6	
USER_DIPSW4	M6	DQ2T/DIFFIO_TX_T4P	DQ4T/DIFFIO_TX_T12N	E7	USER_DIPSW0
USER_DIPSW5	N6	DQ2T/DIFFIO_TX_T4N	RZQ_4/DQ1T/DIFFIO_RX_T1P	J6	R197 100, 1%
USER_DIPSW6	P7	DQ2T/DIFFIO_TX_T6P			
USER_DIPSW7	N7	DQ2T/DIFFIO_TX_T6N			

Bank 7B

VCCIO = 2.5V

HSMA_RX_D_P13	F8	DQ5T/DIFFIO_RX_T13P	DQ9T/DIFFIO_RX_T25P	H11	HSMA_RX_D_P11
HSMA_RX_D_N13	E8	DQ5T/DIFFIO_RX_T13N	DQ9T/DIFFIO_RX_T25N	G11	HSMA_RX_D_N11
HSMA_CLK_OUT_P2	G9	DQ5T/DIFFIO_TX_T14P	DQ9T/DIFFIO_TX_T26P	J10	HSMA_TX_D_P12
HSMA_CLK_OUT_N2	G8	DQ5T/DIFFIO_TX_T14N	DQ9T/DIFFIO_TX_T26N	H10	HSMA_TX_D_N12
HSMA_TX_D_P16	A8	DQ6T/DIFFIO_TX_T16P	DQ10T/DIFFIO_TX_T28P	D10	HSMA_TX_D_P14
HSMA_TX_D_N16	B8	DQ6T/DIFFIO_TX_T16N	DQ10T/DIFFIO_TX_T28N	C10	HSMA_TX_D_N14
HSMA_TX_D_P13	E9	DQ6T/DIFFIO_TX_T18P	DQ10T/DIFFIO_TX_T30P	B11	HSMA_TX_D_P15
HSMA_TX_D_N13	D9	DQ6T/DIFFIO_TX_T18N	DQ10T/DIFFIO_TX_T30N	A11	HSMA_TX_D_N15
HSMA_RX_D_P12	G10	DQS5T/DIFFIO_RX_T15P	DQS9T/DIFFIO_RX_T27P	F11	HSMA_RX_D_P14
HSMA_RX_D_N12	F9	DQSN5T/DIFFIO_RX_T15N	DQSN9T/DIFFIO_RX_T27N	E11	HSMA_RX_D_N14
HSMA_RX_D_P15	C8	DQS6T/DIFFIO_RX_T17P	DQS10T/DIFFIO_RX_T29P	B10	HSMA_RX_D_P16
HSMA_RX_D_N15	C9	DQSN6T/DIFFIO_RX_T17N	DQSN10T/DIFFIO_RX_T29N	A10	HSMA_RX_D_N16
HSMA_RX_D_P10	M8	DQ7T/DIFFIO_RX_T19P	DQ11T/DIFFIO_RX_T31P	K10	DP_DIRECTION
HSMA_RX_D_N10	L8	DQ7T/DIFFIO_RX_T19N	DQ11T/DIFFIO_RX_T31N	J11	USER_LED_G0
HSMA_TX_D_P11	K9	DQ7T/DIFFIO_TX_T20P	DQ11T/DIFFIO_TX_T32P	P10	HSMA_TX_D_P9
HSMA_TX_D_N11	J9	DQ7T/DIFFIO_TX_T20N	DQ11T/DIFFIO_TX_T32N	N10	HSMA_TX_D_N9
HSMA_TX_D_P10	N8	DQ8T/DIFFIO_TX_T22P	DQ12T/DIFFIO_TX_T34P	T10	DP_AUX_TX_P
HSMA_TX_D_N10	N9	DQ8T/DIFFIO_TX_T22N	DQ12T/DIFFIO_TX_T34N	R10	DP_AUX_TX_N
HSMA_TX_D_P8	R8	DQ8T/DIFFIO_TX_T24P	DQ12T/DIFFIO_TX_T36P	U10	USER_LED_G1
HSMA_TX_D_N8	P8	DQ8T/DIFFIO_TX_T24N	DQ12T/DIFFIO_TX_T36N	U9	USER_LED_G2
HSMA_RX_D_P9	M9	DQS7T/DIFFIO_RX_T21P	DQS11T/DIFFIO_RX_T33P	M11	DP_RETURN
HSMA_RX_D_N9	L9	DQSN7T/DIFFIO_RX_T21N	DQSN11T/DIFFIO_RX_T33N	L11	DP_HOT_PLUG
HSMA_RX_D_P8	T9	DQS8T/DIFFIO_RX_T23P	DQS12T/DIFFIO_RX_T35P	R11	DP_AUX_P
HSMA_RX_D_N8	R9	DQSN8T/DIFFIO_RX_T23N	DQSN12T/DIFFIO_RX_T35N	P11	DP_AUX_N

5SGXA7KF40 Version = 1.0 Pin-out

U15F

Stratix V GX Bank 7

Bank 7C

VCCIO = HSMB VARIABLE
1.2V/1.5V/1.8V/2.5V

HSMB_DQ14	B13	DQ13T/DIFFIO_RX_T37P	DQ17T/DIFFIO_RX_T49P	C14	HSMB_DQ30
HSMB_DQ15	A13	DQ13T/DIFFIO_RX_T37N	DQ17T/DIFFIO_RX_T49N	C15	HSMB_DQ31
HSMB_DQ12	D12	DQ13T/DIFFIO_TX_T38P	DQ17T/DIFFIO_TX_T50P	B14	HSMB_DQ28
HSMB_DQ13	C12	DQ13T/DIFFIO_TX_T38N	DQ17T/DIFFIO_TX_T50N	A14	HSMB_DQ29
HSMB_DQ8	G12	DQ14T/DIFFIO_TX_T40P	DQ18T/DIFFIO_TX_T52P	F14	HSMB_DQ25
HSMB_DQ9	G13	DQ14T/DIFFIO_TX_T40N	DQ18T/DIFFIO_TX_T52N	E14	HSMB_DQ27
HSMB_DM1	J13	DQ14T/DIFFIO_TX_T42P	DQ18T/DIFFIO_TX_T54P	H14	HSMB_DM3
HSMB_A2	H13	DQ14T/DIFFIO_TX_T42N	DQ18T/DIFFIO_TX_T54N	G14	HSMB_A3
HSMB_DQS_P1	D13	DQS13T/DIFFIO_RX_T39P	DQS17T/DIFFIO_RX_T51P	E15	HSMB_DQS_P3
HSMB_DQS_N1	C13	DQSN13T/DIFFIO_RX_T39N	DQSN17T/DIFFIO_RX_T51N	D15	HSMB_DQS_N3
HSMB_DQ10	F12	DQS14T/DIFFIO_RX_T41P	DQS18T/DIFFIO_RX_T53P	G15	HSMB_DQ24
HSMB_DQ11	E12	DQSN14T/DIFFIO_RX_T41N	DQSN18T/DIFFIO_RX_T53N	F15	HSMB_DQ26
HSMB_DQ4	M12	DQ15T/DIFFIO_RX_T43P	DQ19T/DIFFIO_RX_T55P	U13	HSMB_DQ16
HSMB_DQ5	L12	DQ15T/DIFFIO_RX_T43N	DQ19T/DIFFIO_RX_T55N	U12	HSMB_DM2
HSMB_DQ6	K12	DQ15T/DIFFIO_TX_T44P	DQ19T/DIFFIO_TX_T56P	T13	HSMB_DQ17
HSMB_DQ7	J12	DQ15T/DIFFIO_TX_T44N	DQ19T/DIFFIO_TX_T56N	U14	HSMB_DQ20
HSMB_DQ3	N13	DQ16T/DIFFIO_TX_T46P	DQ20T/DIFFIO_TX_T58P	N14	HSMB_DQ18
HSMB_DQ2	N12	DQ16T/DIFFIO_TX_T46N	DQ20T/DIFFIO_TX_T58N	M14	HSMB_DQ19
HSMB_DQ1	R12	DQ16T/DIFFIO_TX_T48P	DQ20T/DIFFIO_TX_T60P	L15	HSMB_DQ21
HSMB_RASn	P13	DQ16T/DIFFIO_TX_T48N	DQ20T/DIFFIO_TX_T60N	K15	
HSMB_DQS_P0	L13	DQS15T/DIFFIO_RX_T45P	DQS19T/DIFFIO_RX_T57P	R14	HSMB_DQS_P2
HSMB_DQS_N0	K13	DQSN15T/DIFFIO_RX_T45N	DQSN19T/DIFFIO_RX_T57N	P14	HSMB_DQS_N2
HSMB_DM0	U11	DQS16T/DIFFIO_RX_T47P	DQS20T/DIFFIO_RX_T59P	J14	HSMB_DQ22
HSMB_DQ0	T12	DQSN16T/DIFFIO_RX_T47N	DQSN20T/DIFFIO_RX_T59N	J15	HSMB_DQ23

Bank 7D

VCCIO = HSMB VARIABLE
1.2V/1.5V/1.8V/2.5V

HSMB_A9	B17	DQ21T/DIFFIO_RX_T61P	DQ25T/DIFFIO_RX_T73P	B19	HSMB_A14
HSMB_A8	A17	DQ21T/DIFFIO_RX_T61N	DQ25T/DIFFIO_RX_T73N	A19	HSMB_A13
HSMB_CLK_OUT_P2	B16	DQ21T/DIFFIO_TX_T62P	DQ25T/DIFFIO_TX_T74P	D18	HSMB_A12
HSMB_CLK_OUT_N2	A16	DQ21T/DIFFIO_TX_T62N	DQ25T/DIFFIO_TX_T74N	C18	HSMB_A11
	F17	DQ22T/DIFFIO_TX_T64P	DQ26T/DIFFIO_TX_T76P	E18	HSMB_BA0
	E17	DQ22T/DIFFIO_TX_T64N	DQ26T/DIFFIO_TX_T76N	E19	HSMB_BA3
	H17	DQ22T/DIFFIO_TX_T66P	DQ26T/DIFFIO_TX_T78P	H19	HSMB_CSn
	G17	DQ22T/DIFFIO_TX_T66N	DQ26T/DIFFIO_TX_T78N	G19	HSMB_CKE
HSMB_CLK_OUT_P1	D16	DQS21T/DIFFIO_RX_T63P	DQS25T/DIFFIO_RX_T75P	D19	HSMB_BA1
HSMB_CLK_OUT_N1	C16	DQSN21T/DIFFIO_RX_T63N	DQSN25T/DIFFIO_RX_T75N	C19	HSMB_A15
	H16	DQS22T/DIFFIO_RX_T65P	DQS26T/DIFFIO_RX_T77P	G18	HSMB_A10
	G16	DQSN22T/DIFFIO_RX_T65N	DQSN26T/DIFFIO_RX_T77N	F18	HSMB_BA2
	T15	DQ23T/DIFFIO_TX_T68P	DQ27T/DIFFIO_RX_T79P	N17	HSMB_A0
	R15	DQ23T/DIFFIO_TX_T68N	DQ27T/DIFFIO_RX_T79N	M17	HSMB_WEn
			DQ27T/DIFFIO_TX_T80P	R16	HSMB_CASn
			DQ27T/DIFFIO_TX_T80N	P17	HSMB_A1
HSMB_C_P	N15	DQ24T/DIFFIO_TX_T70P	DQ28T/DIFFIO_TX_T82P	M18	HSMB_ADDR_CMD0
DDR ODT HSMB_C_N	M15	DQ24T/DIFFIO_TX_T70N	DQ28T/DIFFIO_TX_T82N	L18	HSMB_A4
			DQ28T/DIFFIO_TX_T84P	K19	HSMB_A6
			DQ28T/DIFFIO_TX_T84N	L19	HSMB_A5
				N18	
		DQS27T/DIFFIO_RX_T81P		N19	
		DQSN27T/DIFFIO_RX_T81N		K18	
		DQS28T/DIFFIO_RX_T83P		J18	HSMB_A7
		DQSN28T/DIFFIO_RX_T83N			

5SGXA7KF40 Version = 1.0 Pin-out

FLASH INTERFACES

FM_A[26:0] 17,18,4,5,9

USER I/O INTERFACES

USER_DIPSW[7:0] 24
USER_LED_R[7:0] 24,4,9
USER_LED_G[7:0] 11,24,4,5,9

HSMC INTERFACE

HSMA_TX_D_P[16:0] 22,5
HSMA_TX_D_N[16:0] 22,5
HSMA_RX_D_P[16:0] 22,5
HSMA_RX_D_N[16:0] 22,5
HSMA_CLK_OUT_P[2:1] 22,5
HSMA_CLK_OUT_N[2:1] 22,5

HSMB INTERFACE

HSMB_A[15:0] 22
HSMB_BA[3:0] 22
HSMB_DM[3:0] 22
HSMB_DQ[31:0] 22
HSMB_DQS_P[3:0] 22
HSMB_DQS_N[3:0] 22
HSMB_CLK_IN_P[2:1] 22,9
HSMB_CLK_IN_N[2:1] 22,9
HSMB_CLK_OUT_P[2:1] 22
HSMB_CLK_OUT_N[2:1] 22
HSMB_WEn 22
HSMB_CSn 22
HSMB_CKE 22
HSMB_CASn 22
HSMB_RASn 22
HSMB_CLK_IN0 22,9
HSMB_CLK_OUT0 22,9
HSMB_C_P 22
HSMB_C_N 22
HSMB_ADDR_CMD0 22

DISPLAYPORT INTERFACE

DP_HOT_PLUG — DP_HOT_PLUG 20
DP_DIRECTION — DP_DIRECTION 20
DP_RETURN — DP_RETURN 20
DP_AUX_P — DP_AUX_P 20
DP_AUX_N — DP_AUX_N 20
DP_AUX_TX_P — DP_AUX_TX_P 20
DP_AUX_TX_N — DP_AUX_TX_N 20

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 6 of 34

Stratix V Bank 8

U15G

Stratix V GX Bank 8

Bank 8A

VCCIO = 1.5V

MAX5_BEn0	U31	DQ65T/DIFFIO_TX_T194P	DQ68T/DIFFIO_TX_T202P	A34	MAX5_WEn
MAX5_BEn1	T31	DQ65T/DIFFIO_TX_T194N	DQ68T/DIFFIO_TX_T202N	A35	USB_DATA0
			DQ68T/DIFFIO_TX_T204P	A36	USB_DATA2
MAX5_BEn2	N33		DQ68T/DIFFIO_TX_T204N	A37	USB_DATA3
MAX5_BEn3	M33	DQ66T/DIFFIO_TX_T196P	DQ69T/DIFFIO_RX_T205P	E32	USB_DATA4
		DQ66T/DIFFIO_TX_T196N	DQ69T/DIFFIO_RX_T205N	F32	USB_DATA5
			DQ69T/DIFFIO_TX_T206P	G33	USB_DATA6
			DQ69T/DIFFIO_TX_T206N	G32	USB_DATA7
			DQS68T/DIFFIO_RX_T203P	C34	USB_DATA1
			DQS69T/DIFFIO_RX_T207P	F33	USB_SDA
			DQSN69T/DIFFIO_RX_T207N	E33	USB_OEn
			RZQ_5/DQSN68T/DIFFIO_RX_T203N	B34	100, 1% R297
MAX5_CSn	B32	DQ67T/DIFFIO_TX_T200P	DQ70T/DIFFIO_TX_T208P	K33	USB_RDn
MAX5_OEn	A32	DQ67T/DIFFIO_TX_T200N	DQ70T/DIFFIO_TX_T208N	J33	USB_WRn
			DQ70T/DIFFIO_TX_T210P	K34	USB_ADDR1
			DQ70T/DIFFIO_TX_T210N	J34	USB_SCL
			DQS70T/DIFFIO_RX_T209P	H34	USB_RESETn
			DQSN70T/DIFFIO_RX_T209N	G34	USB_ADDR0

Bank 8B

VCCIO = 1.5V

DDR3_DQ13	V29	DQ57T/DIFFIO_RX_T169P	DQ61T/DIFFIO_RX_T181P	N30	DDR3_CLK_P
DDR3_DQ15	U29	DQ57T/DIFFIO_RX_T169N	DQ61T/DIFFIO_RX_T181N	M30	DDR3_CLK_N
DDR3_DQ11	R29	DQ57T/DIFFIO_TX_T170P	DQ61T/DIFFIO_TX_T182P	R30	DDR3_A12
DDR3_DQ12	P29	DQ57T/DIFFIO_TX_T170N	DQ61T/DIFFIO_TX_T182N	R31	DDR3_CKE
DDR3_DQ14	N28	DQ58T/DIFFIO_TX_T172P	DQ62T/DIFFIO_TX_T184P	L31	DDR3_A11
DDR3_DQ9	M29	DQ58T/DIFFIO_TX_T172N	DQ62T/DIFFIO_TX_T184N	L30	DDR3_A4
DDR3_DQ10	L28	DQ58T/DIFFIO_TX_T174P	DQ62T/DIFFIO_TX_T186P	K31	DDR3_A1
DDR3_DQ8	K28	DQ58T/DIFFIO_TX_T174N	DQ62T/DIFFIO_TX_T186N	J31	DDR3_A13
DDR3_DQS_P1	U30	DQS57T/DIFFIO_RX_T171P	DQS61T/DIFFIO_RX_T183P	P31	DDR3_A8
DDR3_DQS_N1	T30	DQSN57T/DIFFIO_RX_T171N	DQSN61T/DIFFIO_RX_T183N	N31	DDR3_A6
DDR3_A9	J29	DQS58T/DIFFIO_RX_T173P	DQS62T/DIFFIO_RX_T185P	K30	DDR3_BA1
DDR3_DM1	J28	DQSN58T/DIFFIO_RX_T173N	DQSN62T/DIFFIO_RX_T185N	J30	DDR3_A10
DDR3_DQ3	F29	DQ59T/DIFFIO_RX_T175P	DQ63T/DIFFIO_RX_T187P	B31	DDR3_CSn
DDR3_DQ1	E28	DQ59T/DIFFIO_RX_T175N	DQ63T/DIFFIO_RX_T187N	A31	DDR3_ODT
DDR3_DQ5	H28	DQ59T/DIFFIO_TX_T176P	DQ63T/DIFFIO_TX_T188P	D30	
DDR3_DQ7	G28	DQ59T/DIFFIO_TX_T176N	DQ63T/DIFFIO_TX_T188N	C30	DDR3_WEn
DDR3_DQ4	D28	DQ60T/DIFFIO_TX_T178P	DQ64T/DIFFIO_TX_T190P	G30	DDR3_RESETn
DDR3_DQ6	C28	DQ60T/DIFFIO_TX_T178N	DQ64T/DIFFIO_TX_T190N	F30	DDR3_A7
DDR3_DQ2	B29	DQ60T/DIFFIO_TX_T180P	DQ64T/DIFFIO_TX_T192P	H31	DDR3_A2
DDR3_DM0	A29	DQ60T/DIFFIO_TX_T180N	DQ64T/DIFFIO_TX_T192N	G31	DDR3_A0
DDR3_DQS_P0	H29	DQS59T/DIFFIO_RX_T177P	DQS63T/DIFFIO_RX_T189P	D31	DDR3_A3
DDR3_DQS_N0	G29	DQSN59T/DIFFIO_RX_T177N	DQSN63T/DIFFIO_RX_T189N	C31	DDR3_BA0
DDR3_CASn	B28	DQS60T/DIFFIO_RX_T179P	DQS64T/DIFFIO_RX_T191P	E30	DDR3_BA2
DDR3_DQ0	A28	DQSN60T/DIFFIO_RX_T179N	DQSN64T/DIFFIO_RX_T191N	E31	DDR3_A5

5SGXA7KF40

Version = 1.0 Pin-out

U15H

Stratix V GX Bank 8

Bank 8C

VCCIO = 1.5V

DDR3_DQ44	P25	DQ49T/DIFFIO_RX_T145P	DQ53T/DIFFIO_RX_T157P	U26	DDR3_DQ28
DDR3_DQ46	N25	DQ49T/DIFFIO_RX_T145N	DQ53T/DIFFIO_RX_T157N	U27	DDR3_DQ30
DDR3_DQ47	U25	DQ49T/DIFFIO_TX_T146P	DQ53T/DIFFIO_TX_T158P	T27	DDR3_DQ26
DDR3_DQ45	T25	DQ49T/DIFFIO_TX_T146N	DQ53T/DIFFIO_TX_T158N	R27	DDR3_DQ31
DDR3_DQ43	P26	DQ50T/DIFFIO_TX_T148P	DQ54T/DIFFIO_TX_T160P	N27	DDR3_DQ25
DDR3_DQ41	N26	DQ50T/DIFFIO_TX_T148N	DQ54T/DIFFIO_TX_T160N	P28	DDR3_DQ29
DDR3_DM5	K25	DQ50T/DIFFIO_TX_T150P	DQ54T/DIFFIO_TX_T162P	M27	DDR3_DQ27
DDR3_DQ40	J25	DQ50T/DIFFIO_TX_T150N	DQ54T/DIFFIO_TX_T162N	L27	DDR3_DM3
DDR3_DQS_P5	R25	DQS49T/DIFFIO_RX_T147P	DQS53T/DIFFIO_RX_T159P	U28	DDR3_DQS_P3
DDR3_DQS_N5	R26	DQSN49T/DIFFIO_RX_T147N	DQSN53T/DIFFIO_RX_T159N	T28	DDR3_DQS_N3
	M26	DQS50T/DIFFIO_RX_T149P	DQS54T/DIFFIO_RX_T161P	K27	
DDR3_DQ42	L26	DQSN50T/DIFFIO_RX_T149N	DQSN54T/DIFFIO_RX_T161N	J27	DDR3_DQ24
DDR3_DQ35	G24	DQ51T/DIFFIO_RX_T151P	DQ55T/DIFFIO_RX_T163P	G26	DDR3_DQ16
DDR3_DQ33	F24	DQ51T/DIFFIO_RX_T151N	DQ55T/DIFFIO_RX_T163N	F26	DDR3_DQ18
DDR3_DQ37	H25	DQ51T/DIFFIO_TX_T152P	DQ55T/DIFFIO_TX_T164P	J26	DDR3_DQ21
DDR3_DQ39	G25	DQ51T/DIFFIO_TX_T152N	DQ55T/DIFFIO_TX_T164N	H26	DDR3_DQ23
DDR3_DQ36	D24	DQ52T/DIFFIO_TX_T154P	DQ56T/DIFFIO_TX_T166P	E27	DDR3_DQ22
DDR3_DQ38	C24	DQ52T/DIFFIO_TX_T154N	DQ56T/DIFFIO_TX_T166N	D27	DDR3_DQ17
DDR3_DQ32	B25	DQ52T/DIFFIO_TX_T156P	DQ56T/DIFFIO_TX_T168P	C26	DDR3_DQ20
DDR3_DM4	A25	DQ52T/DIFFIO_TX_T156N	DQ56T/DIFFIO_TX_T168N	C27	DDR3_DQ19
DDR3_DQS_P4	E24	DQS51T/DIFFIO_RX_T153P	DQS55T/DIFFIO_RX_T165P	G27	DDR3_DQS_P2
DDR3_DQS_N4	E25	DQSN51T/DIFFIO_RX_T153N	DQSN55T/DIFFIO_RX_T165N	F27	DDR3_DQS_N2
	D25	DQS52T/DIFFIO_RX_T155P	DQS56T/DIFFIO_RX_T167P	B26	DDR3_RASn
DDR3_DQ34	C25	DQSN52T/DIFFIO_RX_T155N	DQSN56T/DIFFIO_RX_T167N	A26	DDR3_DM2

Bank 8D

VCCIO = 1.5V

DDR3_DQ69	K21	DQ41T/DIFFIO_RX_T121P	DQ45T/DIFFIO_TX_T134P	L24	
DDR3_DQ67	J21	DQ41T/DIFFIO_RX_T121N	DQ45T/DIFFIO_TX_T134N	K24	
DDR3_DQ64	M20	DQ41T/DIFFIO_TX_T122P			
DDR3_DQ65	L20	DQ41T/DIFFIO_TX_T122N			
DDR3_DM8	M21	DQ42T/DIFFIO_TX_T124P	DQ46T/DIFFIO_TX_T136P	P23	
DDR3_DQ71	L21	DQ42T/DIFFIO_TX_T124N	DQ46T/DIFFIO_TX_T136N	N23	
DDR3_DQ70	N20	DQ42T/DIFFIO_TX_T126P	DQ46T/DIFFIO_TX_T138P	T24	
DDR3_DQ68	N21	DQ42T/DIFFIO_TX_T126N	DQ46T/DIFFIO_TX_T138N	R24	
DDR3_DQS_P8	K22	DQS41T/DIFFIO_RX_T123P	DQS46T/DIFFIO_RX_T137P	N24	
DDR3_DQS_N8	J22	DQSN41T/DIFFIO_RX_T123N	DQSN46T/DIFFIO_RX_T137N	M24	
	P22	DQS42T/DIFFIO_RX_T125P			
DDR3_DQ66	N22	DQSN42T/DIFFIO_RX_T125N			
DDR3_DQ58	F20	DQ43T/DIFFIO_RX_T127P	DQ47T/DIFFIO_RX_T139P	H23	DDR3_DQ53
DDR3_DQ63	E20	DQ43T/DIFFIO_RX_T127N	DQ47T/DIFFIO_RX_T139N	G23	DDR3_DQ51
DDR3_DQ60	H20	DQ43T/DIFFIO_TX_T128P	DQ47T/DIFFIO_TX_T140P	H22	DDR3_DQ48
DDR3_DQ62	G20	DQ43T/DIFFIO_TX_T128N	DQ47T/DIFFIO_TX_T140N	G22	DDR3_DQ50
DDR3_DQ57	C20	DQ44T/DIFFIO_TX_T130P	DQ48T/DIFFIO_TX_T142P	C22	DDR3_DQ54
DDR3_DQ59	C21	DQ44T/DIFFIO_TX_T130N	DQ48T/DIFFIO_TX_T142N	D22	DDR3_DQ52
DDR3_DM7	B20	DQ44T/DIFFIO_TX_T132P	DQ48T/DIFFIO_TX_T144P	B23	DDR3_DQ49
DDR3_DQ56	A20	DQ44T/DIFFIO_TX_T132N	DQ48T/DIFFIO_TX_T144N	A23	DDR3_DQ55
DDR3_DQS_P7	G21	DQS43T/DIFFIO_RX_T129P	DQS47T/DIFFIO_RX_T141P	F23	DDR3_DQS_P6
DDR3_DQS_N7	F21	DQSN43T/DIFFIO_RX_T129N	DQSN47T/DIFFIO_RX_T141N	E23	DDR3_DQS_N6
	E21	DQS44T/DIFFIO_RX_T131P	DQS48T/DIFFIO_RX_T143P	B22	
DDR3_DQ61	D21	DQSN44T/DIFFIO_RX_T131N	DQSN48T/DIFFIO_RX_T143N	A22	DDR3_DM6

5SGXA7KF40

Version = 1.0 Pin-out

In order to operate DDR3 at 1066MHz Altera requires all DDR3 address and command signals to be in the same sub-bank. With the current DDR3 pin out this board only supports DDR3 up to 800MHz. In order to support DDR3 at 1066MHz in the future DDR3_RASn would need to move to sub-bank 8B, pin U15.D30.

DDR3 x72 INTERFACE

DDR3_DQ[71:0]	13,14	
DDR3_A[13:0]	13,14	
DDR3_DQS_P[8:0]	13,14	
DDR3_DQS_N[8:0]	13,14	
DDR3_DM[8:0]	13,14	
DDR3_BA[2:0]	13,14	
DDR3_CSn	13,14	
DDR3_CASn	13,14	
DDR3_CKE	13,14	
DDR3_WEn	13,14	
DDR3_RASn	13,14	
DDR3_CLK_P	13,14	
DDR3_CLK_N	13,14	
DDR3_ODT	13,14	
DDR3_RESETn	13,14	

MAX V CONTROL

MAX5_BEn[3:0]	18	
MAX5_OEn	18	
MAX5_CSn	18	
MAX5_WEn	18	

STRATIX V USB INTERFACE

USB_DATA[7:0]	USB_DATA[7:0]	25
USB_ADDR[1:0]	USB_ADDR[1:0]	25
USB_SCL	USB_SCL	25
USB_SDA	USB_SDA	25
USB_RESETn	USB_RESETn	25
USB_OEn	USB_OEn	25
USB_RDn	USB_RDn	25
USB_WRn	USB_WRn	25

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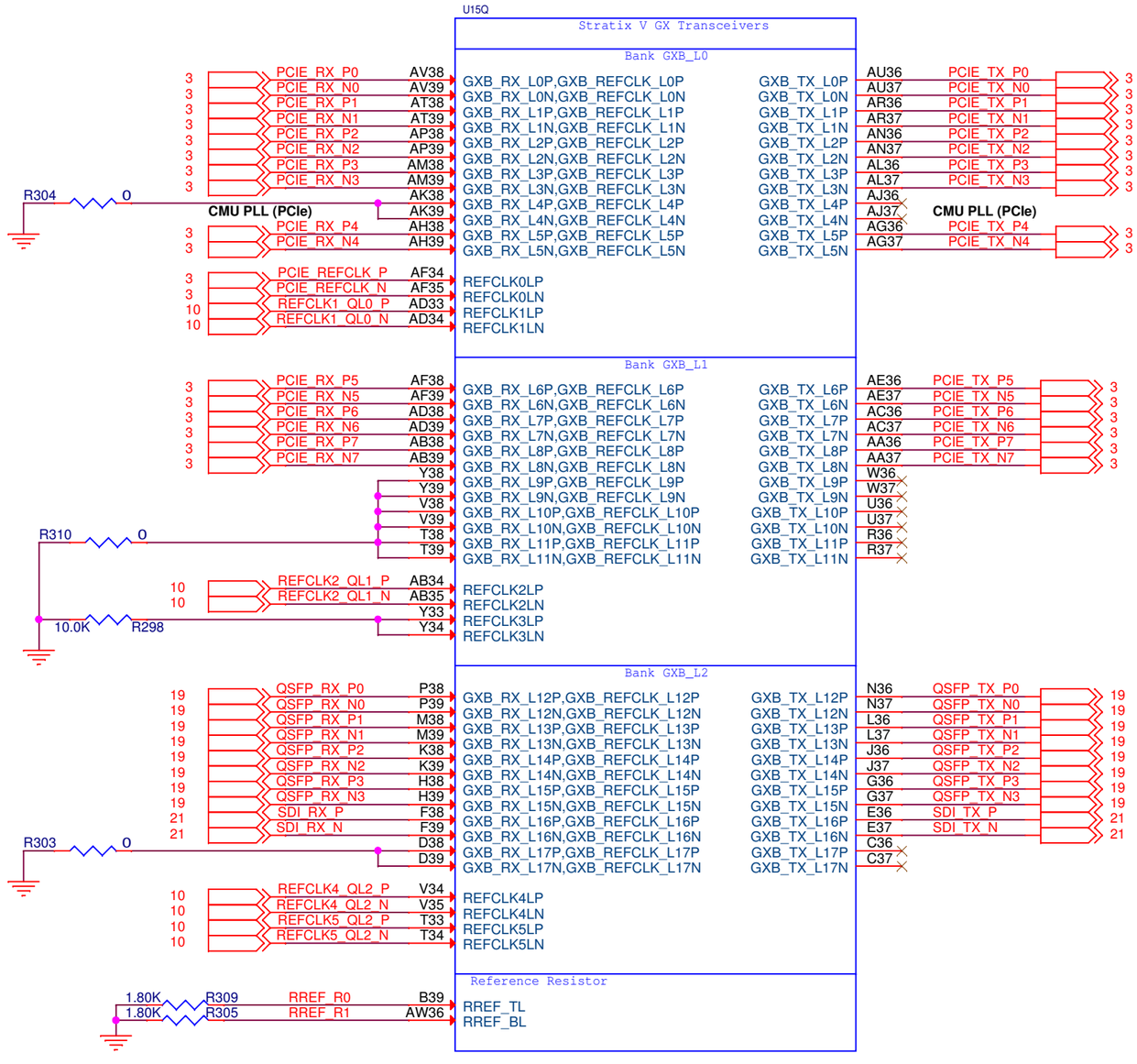
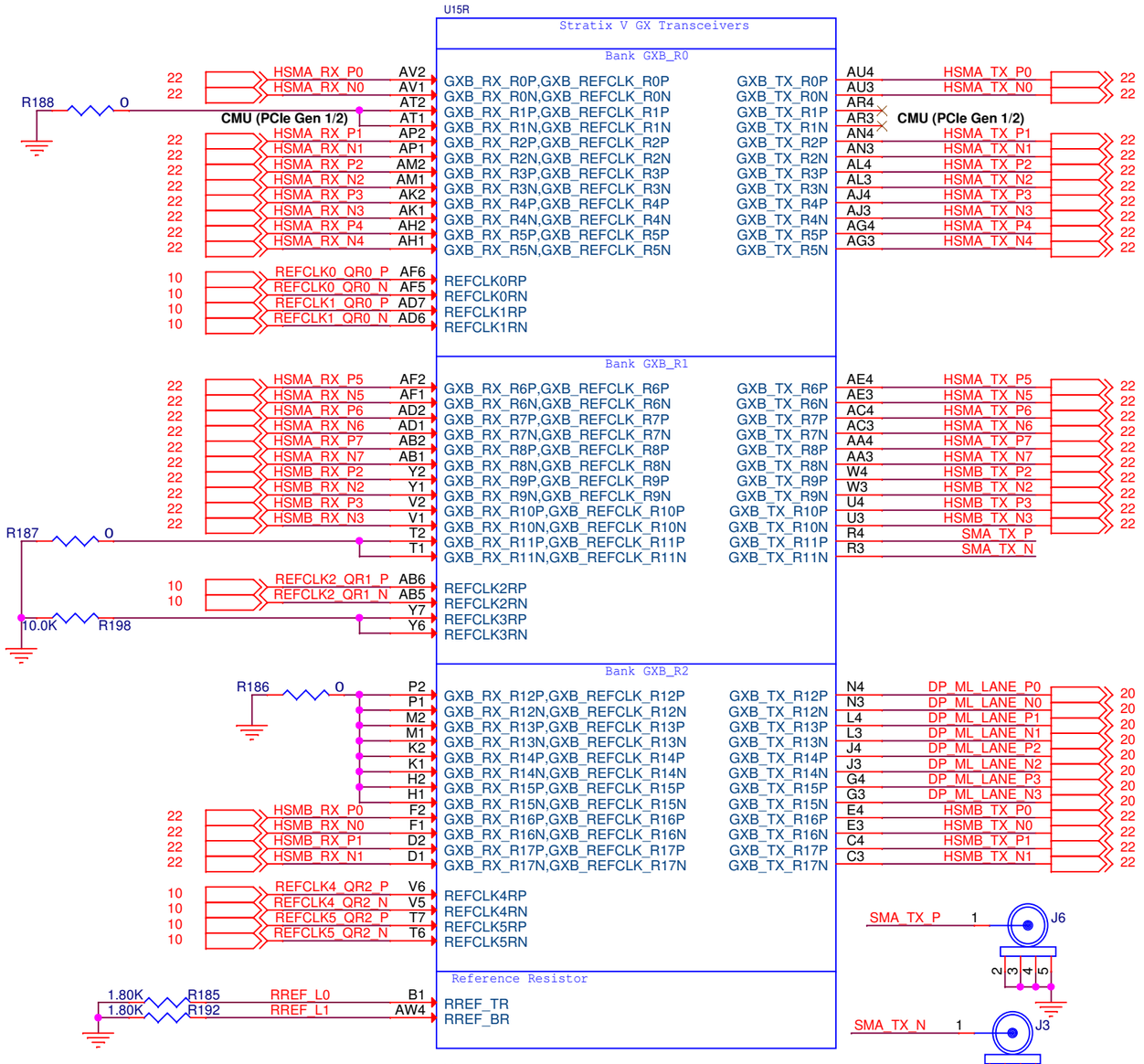
Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 7 of 34

Stratix V GX Transceivers and Power





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B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 8 of 34

Stratix V GX Clocks

HSMA_CLK_IN_P1	R202	100, 1%	HSMA_CLK_IN_N1
HSMA_CLK_IN_P2	R196	100, 1%	HSMA_CLK_IN_N2
HSMB_CLK_IN_P1	R224	100, 1%	HSMB_CLK_IN_N1
HSMB_CLK_IN_P2	R223	100, 1%	HSMB_CLK_IN_N2
CLKINBOT_P1	R225	100, 1%	CLKINBOT_N1
CLKINTOP_P0	R261	100, 1%	CLKINTOP_N0
CLKINTOP_P1	R286	100, 1%	CLKINTOP_N1
CLKINBOT_P0	R253	100, 1%	CLKINBOT_N0

U15I

Stratix V GX Clocks

Bank 3B ***VCCIO = 2.5V***

CLK_125_P	AV29	CLK0P/DQS8B/DIFFIO_RX_B22P	FPLL_BL_CLKOUTP/DQ9B/DIFFIO_TX_B25P	AD30	QSFP_SCL
CLK_125_N	AW29	CLK0N/DQSN8B/DIFFIO_RX_B22N	FPLL_BL_CLKOUTN/DQ9B/DIFFIO_TX_B25N	AE30	QSFP_RSTn
USB_CLK	AV28	CLK1P/DQ8B/DIFFIO_RX_B24P	FPLL_BL_FB/CLKOUTP/DQS9B/DIFFIO_RX_B26P	AB30	SDI_RX_BYPASS
SDI_CLK148_UP	AW28	CLK1N/DQ8B/DIFFIO_RX_B24N	FPLL_BL_FB/CLKOUTN/DQSN9B/DIFFIO_RX_B26N	AC30	QSFP_SDA
HSMB_CLK_IN0	AF29	CLK2P/DQS10B/DIFFIO_RX_B28P			
USER_LED_R1	AG30	CLK2N/DQSN10B/DIFFIO_RX_B28N			
HSMA_CLK_IN0	AG28	CLK3P/DQ10B/DIFFIO_RX_B30P			
USER_LED_R0	AH28	CLK3N/DQ10B/DIFFIO_RX_B30N			

Bank 3D ***VCCIO = 1.8V***

CLKINBOT_P0	AH22	CLK4P/DQS26B/DIFFIO_RX_B76P			
CLKINBOT_N0	AJ22	CLK4N/DQSN26B/DIFFIO_RX_B76N			
RLDC_BA2	AK23	CLK5P/DQ26B/DIFFIO_RX_B78P			
USER_LED_R6	AL23	CLK5N/DQ26B/DIFFIO_RX_B78N			

Bank 4A ***VCCIO = 1.8V***

USER_LED_R2	AL7	CLK8P/DQS70B/DIFFIO_RX_B208P	FPLL_BR_CLKOUTP/DQ68B/DIFFIO_TX_B203P	AT6	FM_A19
USER_LED_R4	AM7	CLK8N/DQSN70B/DIFFIO_RX_B208N	FPLL_BR_CLKOUTN/DQ68B/DIFFIO_TX_B203N	AU6	FM_A18
CLKIN_50	AN6	CLK9P/DQS69B/DIFFIO_RX_B206P	FPLL_BR_FB/CLKOUTP/DQ68B/DIFFIO_RX_B204P	AP7	FLASH_ADVn
FLASH_RDYBSYn1	AN7	CLK9N/DQSN69B/DIFFIO_RX_B206N	FPLL_BR_FB/CLKOUTN/DQ68B/DIFFIO_RX_B204N	AR7	USER_LED_G6
HSMA_CLK_IN_P1	AR8	CLK10P/DQS68B/DIFFIO_RX_B202P			
HSMA_CLK_IN_N1	AT8	CLK10N/DQSN68B/DIFFIO_RX_B202N			
USER_LED_R7	AV7	CLK11P/DQS67B/DIFFIO_RX_B200P			
USER_LED_R5	AW7	CLK11N/DQSN67B/DIFFIO_RX_B200N			

Bank 4D ***VCCIO = 1.8V***

CLKINBOT_P1	AF17	CLK6P/DQS48B/DIFFIO_RX_B142P	FPLL_BC_CLKOUTP/DQ47B/DIFFIO_TX_B139P	AH16	FM_A24
CLKINBOT_N1	AG17	CLK6N/DQSN48B/DIFFIO_RX_B142N	FPLL_BC_CLKOUTN/DQ47B/DIFFIO_TX_B139N	AJ17	FM_A26
FM_A23	AE17	CLK7P/DQ48B/DIFFIO_RX_B144P	FPLL_BC_FB/CLKOUTP/DQS47B/DIFFIO_RX_B140P	AK17	FM_A21
FM_A22	AE16	CLK7N/DQ48B/DIFFIO_RX_B144N	FPLL_BC_FB/CLKOUTN/DQSN47B/DIFFIO_RX_B140N	AL17	FM_A20

Bank 7A ***VCCIO = HSMB VARIABLE***

HSMA_CLK_IN_P2	G7	CLK12P/DQS1T/DIFFIO_RX_T3P	FPLL_TR_FB/CLKOUTP/DQ3T/DIFFIO_RX_T7P	A3	
HSMA_CLK_IN_N2	G6	CLK12N/DQSN1T/DIFFIO_RX_T3N	FPLL_TR_FB/CLKOUTN/DQ3T/DIFFIO_RX_T7N	A4	
	L6	CLK13P/DQS2T/DIFFIO_RX_T5P	FPLL_TR_CLKOUTP/DQ3T/DIFFIO_TX_T8P	A6	
	K6	CLK13N/DQSN2T/DIFFIO_RX_T5N	FPLL_TR_CLKOUTN/DQ3T/DIFFIO_TX_T8N	A5	
USER_PB1	B7	CLK14P/DQS3T/DIFFIO_RX_T9P			
USER_PB0	A7	CLK14N/DQSN3T/DIFFIO_RX_T9N			
	D7	CLK15P/DQS4T/DIFFIO_RX_T11P			
USER_PB2	C7	CLK15N/DQSN4T/DIFFIO_RX_T11N			

Bank 7D ***VCCIO = HSMB VARIABLE***

HSMB_CLK_IN_P2	P16	CLK18P/DQS23T/DIFFIO_RX_T69P	FPLL_TC_FB/CLKOUTP/DQS24T/DIFFIO_RX_T71P	J16	
HSMB_CLK_IN_N2	N16	CLK18N/DQSN23T/DIFFIO_RX_T69N	FPLL_TC_FB/CLKOUTN/DQSN24T/DIFFIO_RX_T71N	J17	
HSMB_CLK_IN_P1	U15	CLK19P/DQ23T/DIFFIO_RX_T67P	FPLL_TC_CLKOUTP/DQ24T/DIFFIO_TX_T72P	L16	HSMB_CLK_OUT0
HSMB_CLK_IN_N1	T16	CLK19N/DQ23T/DIFFIO_RX_T67N	FPLL_TC_CLKOUTN/DQ24T/DIFFIO_TX_T72N	K16	

Bank 8A ***VCCIO = 1.5V***

MAX5_CLK	E34	CLK20P/DQS67T/DIFFIO_RX_T201P	FPLL_TL_FB/CLKOUTP/DQS66T/DIFFIO_RX_T197P	L33	
	D34	CLK20N/DQSN67T/DIFFIO_RX_T201N	FPLL_TL_FB/CLKOUTN/DQSN66T/DIFFIO_RX_T197N	L34	
	D33	CLK21P/DQ67T/DIFFIO_RX_T199P	FPLL_TL_CLKOUTP/DQ66T/DIFFIO_TX_T198P	P34	USB_EMPTY
	C33	CLK21N/DQ67T/DIFFIO_RX_T199N	FPLL_TL_CLKOUTN/DQ66T/DIFFIO_TX_T198N	N34	USB_FULL
CLKINTOP_P1	N32	CLK22P/DQS65T/DIFFIO_RX_T195P			
CLKINTOP_N1	M32	CLK22N/DQSN65T/DIFFIO_RX_T195N			
	R32	CLK23P/DQ65T/DIFFIO_RX_T193P			
	P32	CLK23N/DQ65T/DIFFIO_RX_T193N			

Bank 8D ***VCCIO = 1.5V***

CLKINTOP_P0	J23	CLK16P/DQS45T/DIFFIO_RX_T135P	
CLKINTOP_N0	J24	CLK16N/DQSN45T/DIFFIO_RX_T135N	
	M23	CLK17P/DQ45T/DIFFIO_RX_T133P	
	L23	CLK17N/DQ45T/DIFFIO_RX_T133N	

5SGXA7KF40

Version = 1.0 Pin-out

STRATIX V CLOCKS

CLKINTOP_P[1:0]	CLKINTOP_P[1:0]	10
CLKINTOP_N[1:0]	CLKINTOP_N[1:0]	10
CLKINBOT_P[1:0]	CLKINBOT_P[1:0]	10
CLKINBOT_N[1:0]	CLKINBOT_N[1:0]	10
CLKIN_50	CLKIN_50	10,18
CLK_125_P	CLK_125_P	10
CLK_125_N	CLK_125_N	10
SDI_CLK148_UP	SDI_CLK148_UP	10

STRATIX V USB INTERFACE

USB_CLK	USB_CLK	18,25
USB_FULL	USB_FULL	25
USB_EMPTY	USB_EMPTY	25

HSMC INTERFACE

HSMA_CLK_IN_P[2:1]		22
HSMA_CLK_IN_N[2:1]		22
HSMB_CLK_IN_P[2:1]		22
HSMB_CLK_IN_N[2:1]		22
HSMA_CLK_IN0		22
HSMB_CLK_IN0		22
HSMB_CLK_OUT0		22

QSFP INTERFACE

QSFP_RSTn	QSFP_RSTn	19
QSFP_SCL	QSFP_SCL	19
QSFP_SDA	QSFP_SDA	19

FLASH INTERFACE

FLASH_ADVn		17,18
FLASH_RDYBSYn1		17,18
FM_A[26:0]		17,18,4,5

MAX V CONTROL

MAX5_CLK		18
USER_PB[2:0]		24

LCD & USER I/O INTERFACES

USER_LED_R[7:0]		24,4
USER_LED_G[7:0]		11,24,4,5,6

SDI INTERFACES

SDI_RX_BYPASS	SDI_RX_BYPASS	18,21

RLDRAM II INTERFACE

RLDC_BA[2:0]	RLDC_BA[2:0]	16,4

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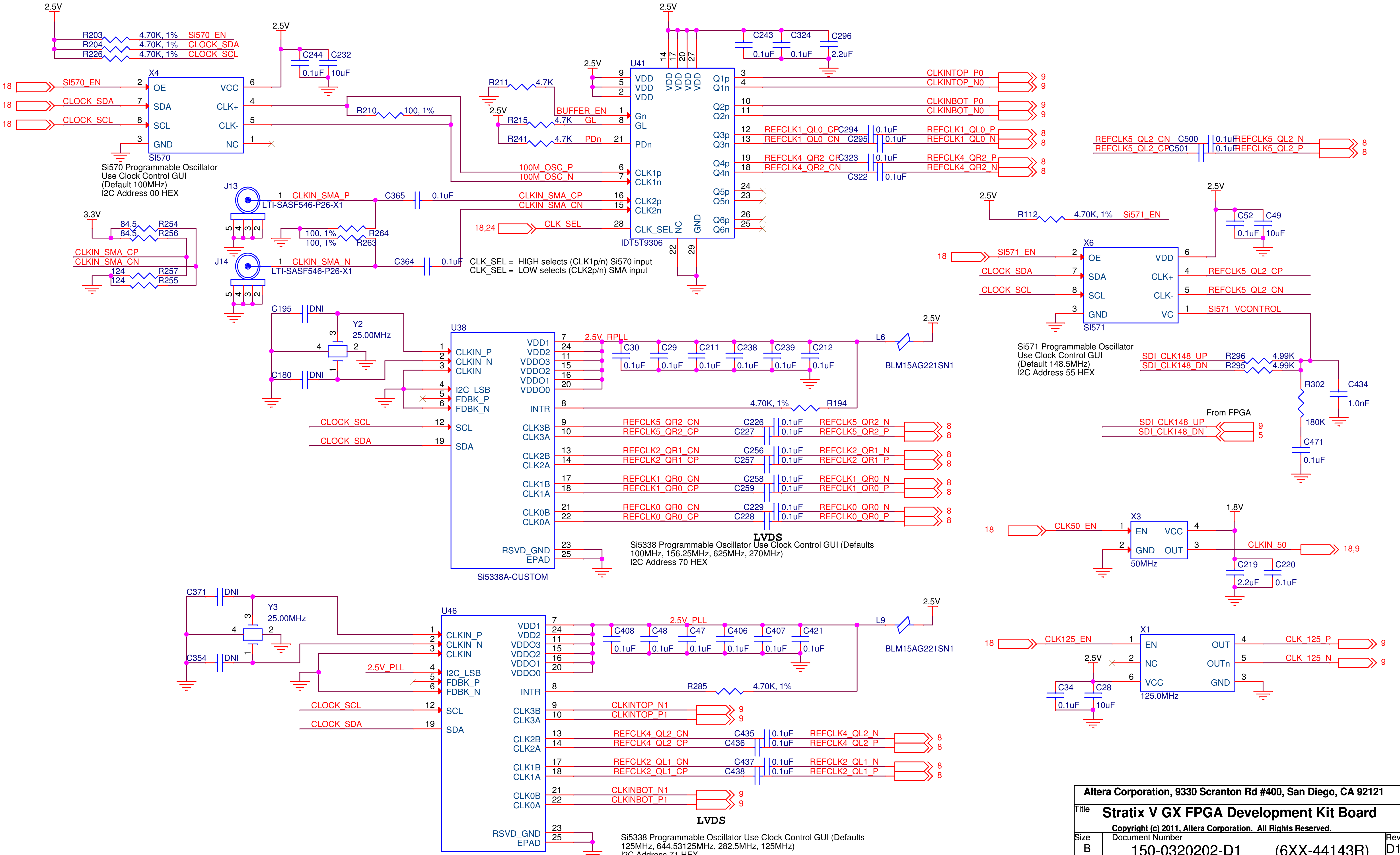
Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 9 of 34

PLL



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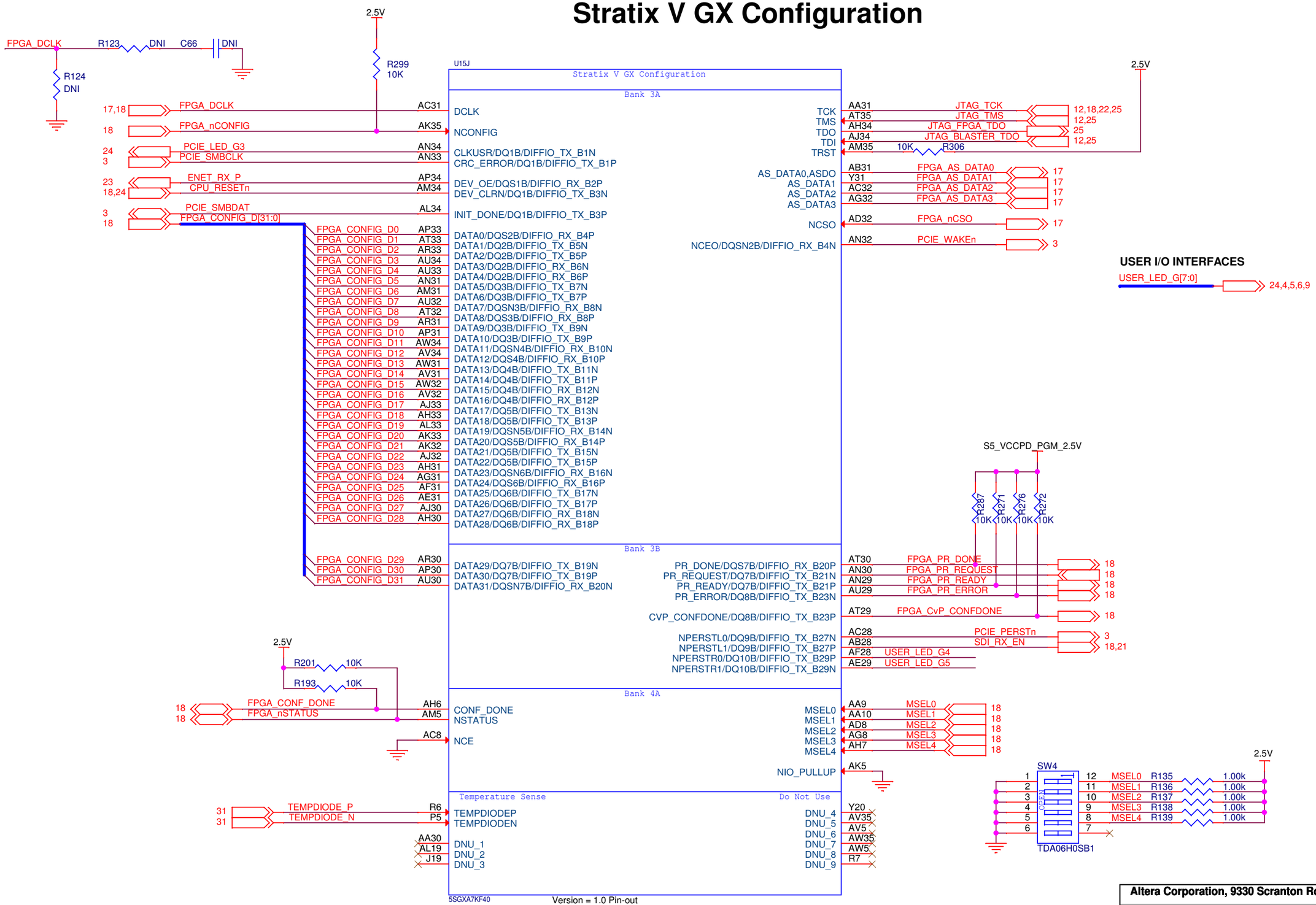
Title **Stratix V GX FPGA Development Kit Board**

Size B | Document Number 150-0320202-D1 (6XX-44143R) | Rev D1.1

Date: Monday, June 03, 2013 | Sheet 10 of 34

Stratix V GX Configuration



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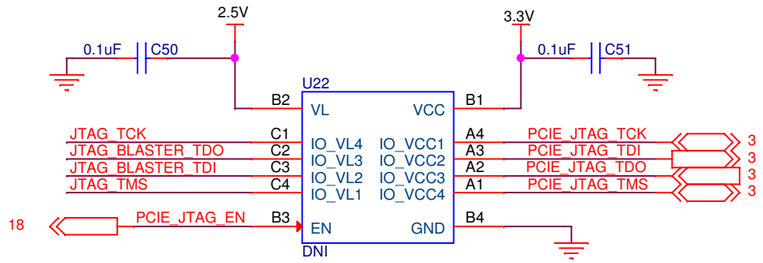
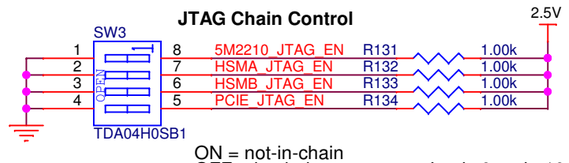
Title: **Stratix V GX FPGA Development Kit Board**

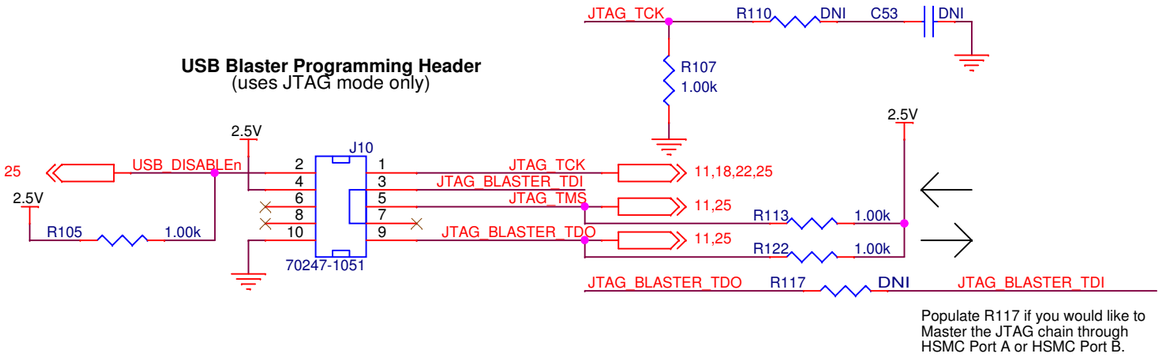
Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 11 of 34

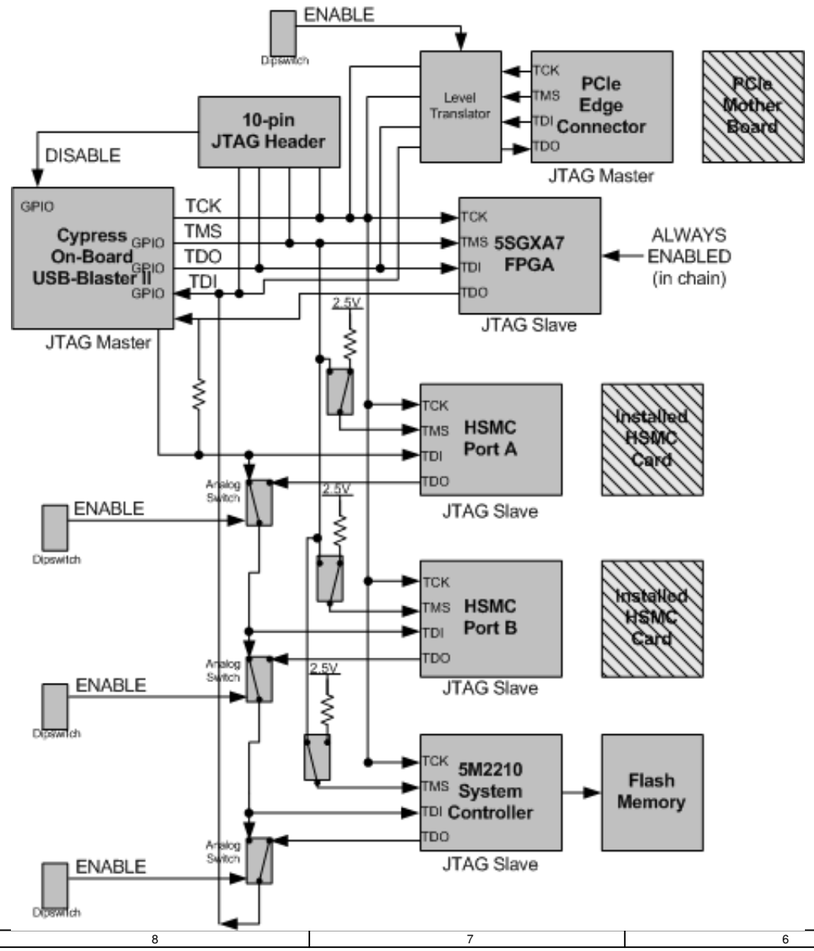
JTAG





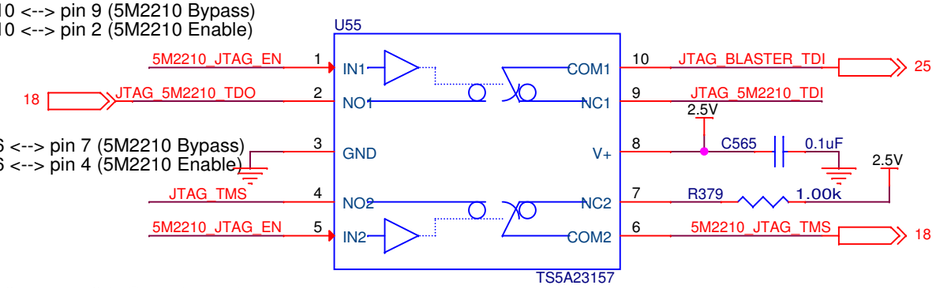


Populate R117 if you would like to Master the JTAG chain through HSMC Port A or HSMC Port B.

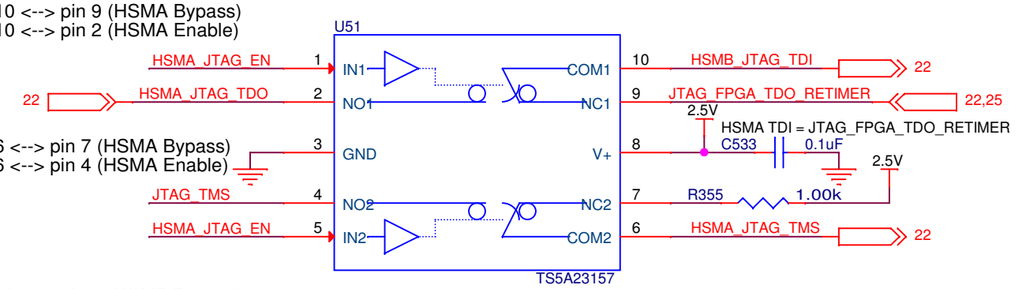


TS5A23157 Switch Functions
When Pins 1 & 5 are:
LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON

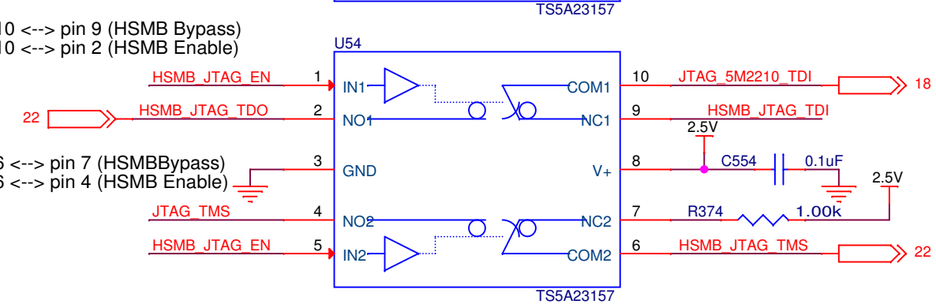
Logic 0 = pin 10 <--> pin 9 (5M2210 Bypass)
Logic 1 = pin 10 <--> pin 2 (5M2210 Enable)



Logic 0 = pin 10 <--> pin 9 (HSMA Bypass)
Logic 1 = pin 10 <--> pin 2 (HSMA Enable)



Logic 0 = pin 10 <--> pin 9 (HSMB Bypass)
Logic 1 = pin 10 <--> pin 2 (HSMB Enable)



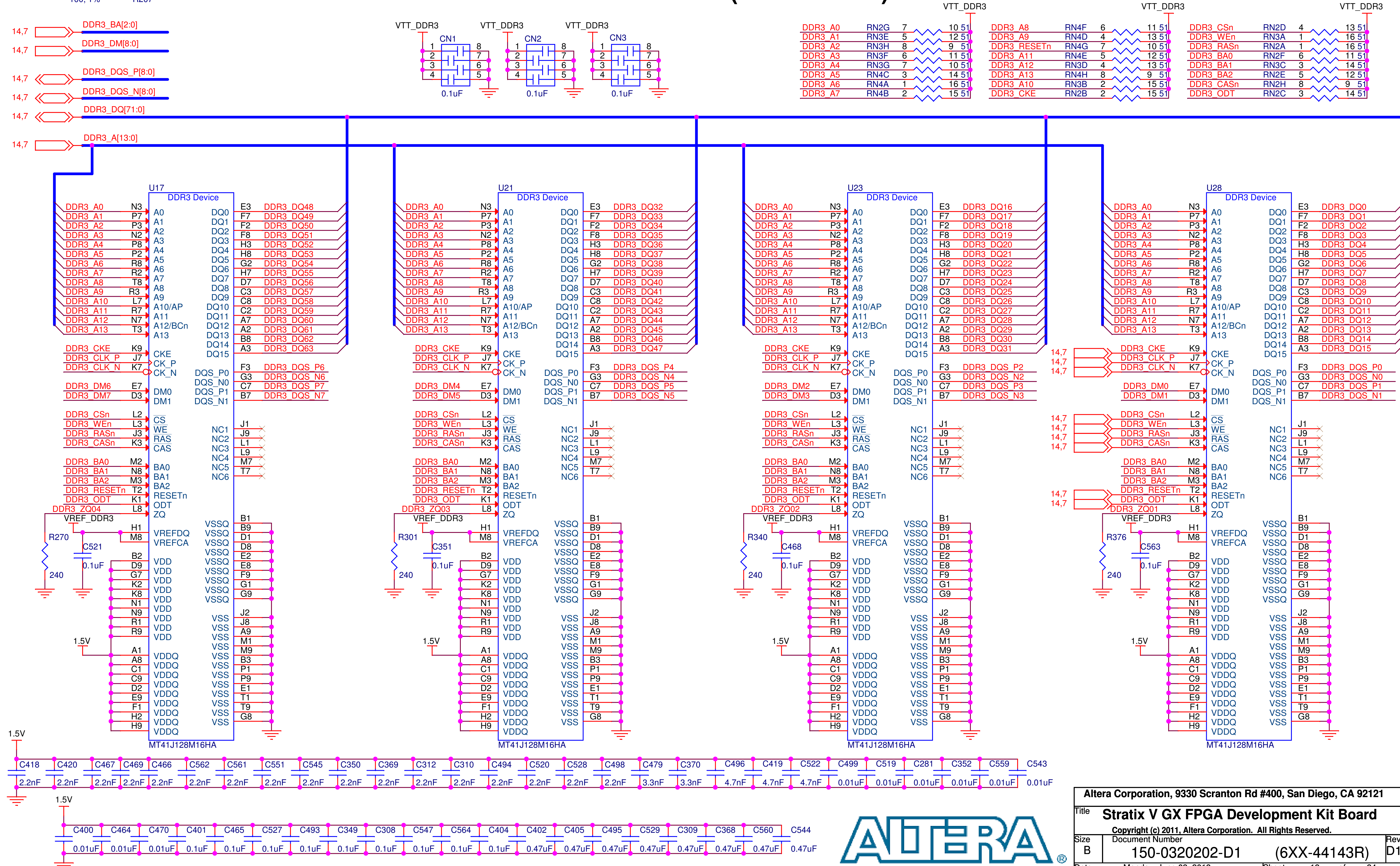
Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 12 of 34

512MB DDR3 (x72 devices) - Part 1 of 2



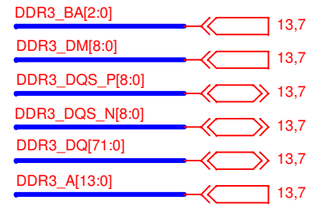
Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

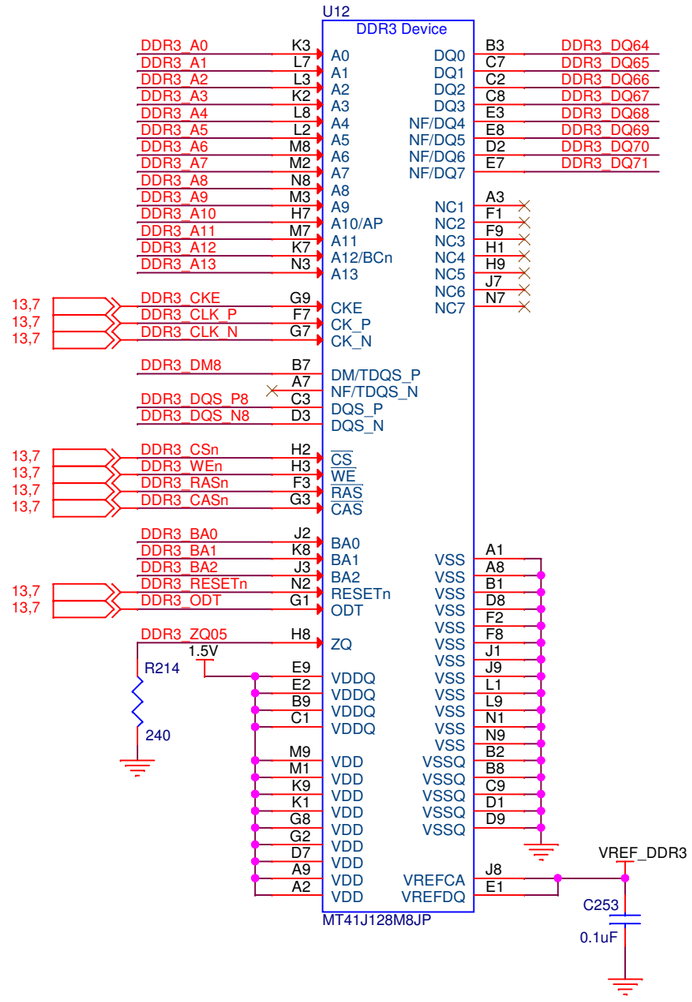
Title: Stratix V GX FPGA Development Kit Board

Size	Document Number		Rev
B	150-0320202-D1	(6XX-44143R)	D1.1

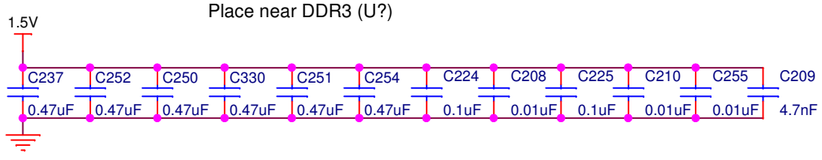
Date: Monday, June 03, 2013 Sheet 13 of 34

1152MB DDR3 - Part 2 of 2





Place near DDR3 (U?)



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title: Stratix V GX FPGA Development Kit Board		
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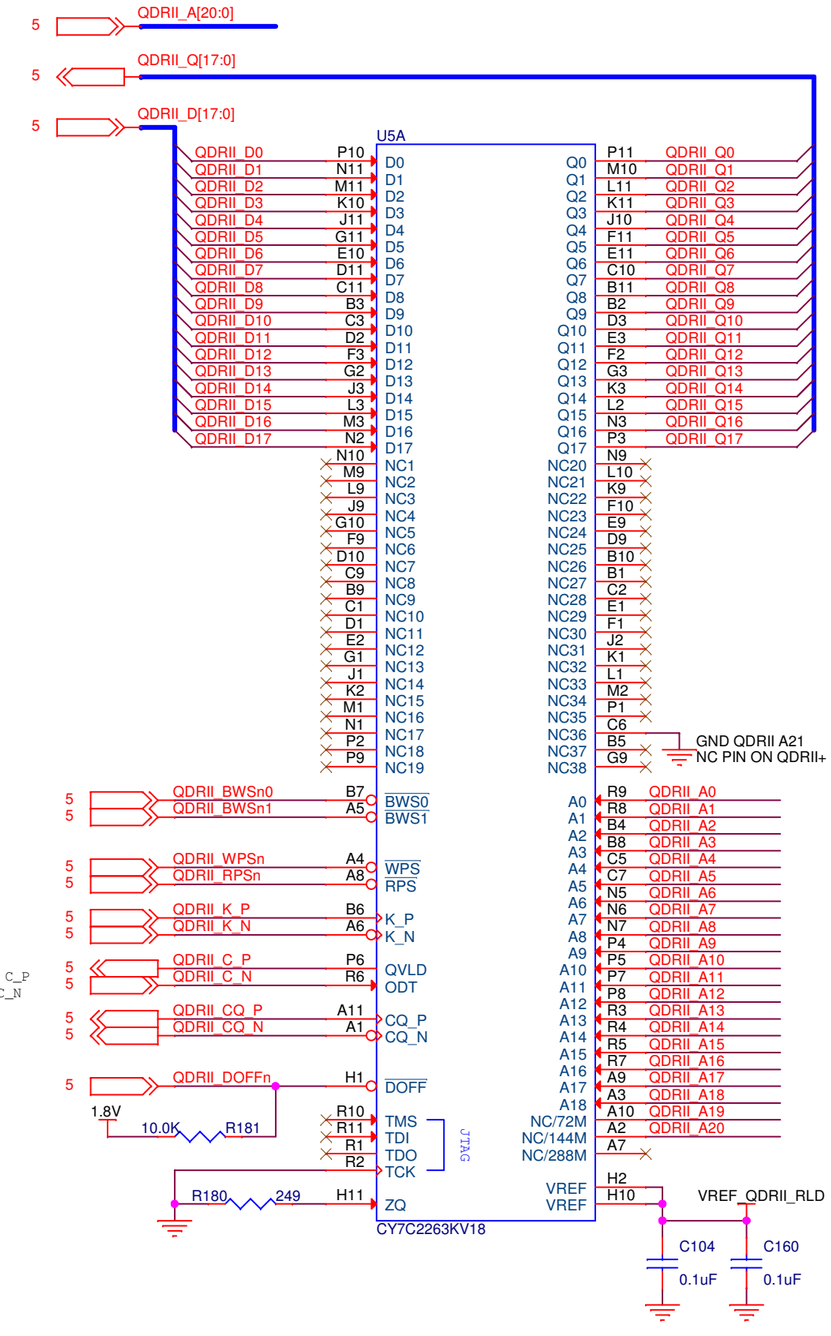
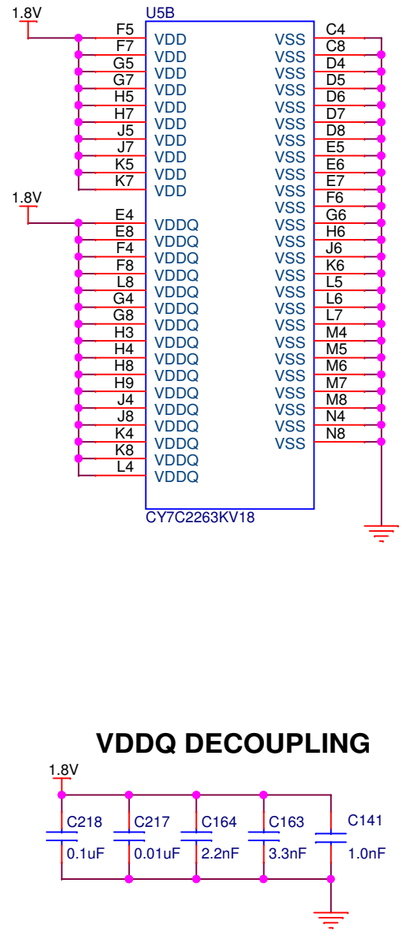
Size: B	Document Number: 150-0320202-D1 (6XX-44143R)	Rev: D1.1
Date: Monday, June 03, 2013	Sheet 14 of 34	

QDRII+

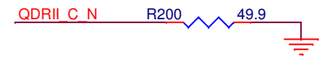
Altera recommends to use external termination for QDRII/+ address and command signals. In this case external termination was not used, because simulations showed that with the short trace length and a point to point connection the external termination was not necessary. As a result since there is limited board space external termination is not used.



QDRII+ QVLD = QDRII C_P
QDRII+ ODT = QDRII C_N

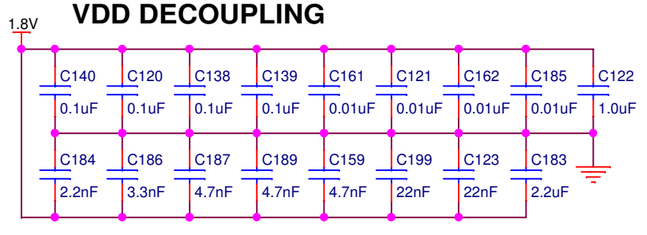


Place Near QDRII+



VDDQ DECOUPLING

VDD DECOUPLING



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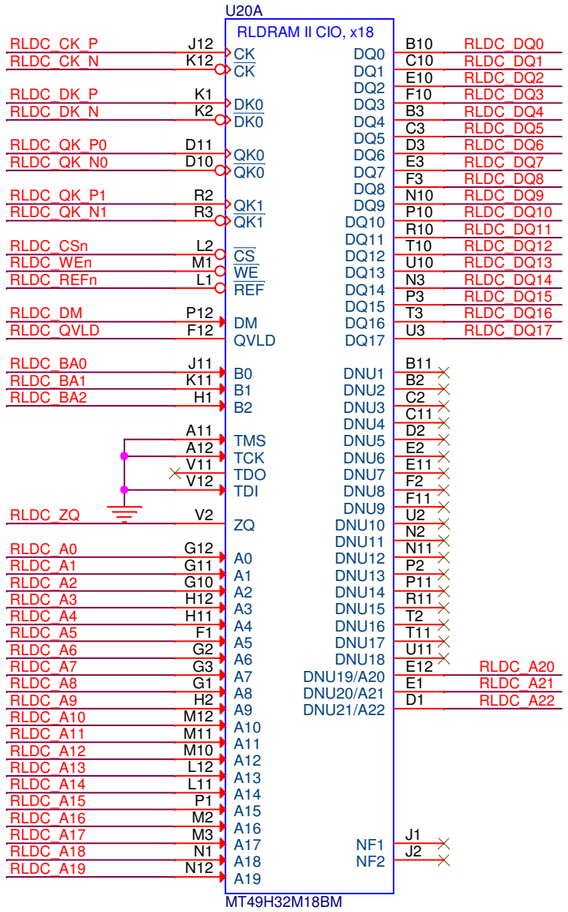
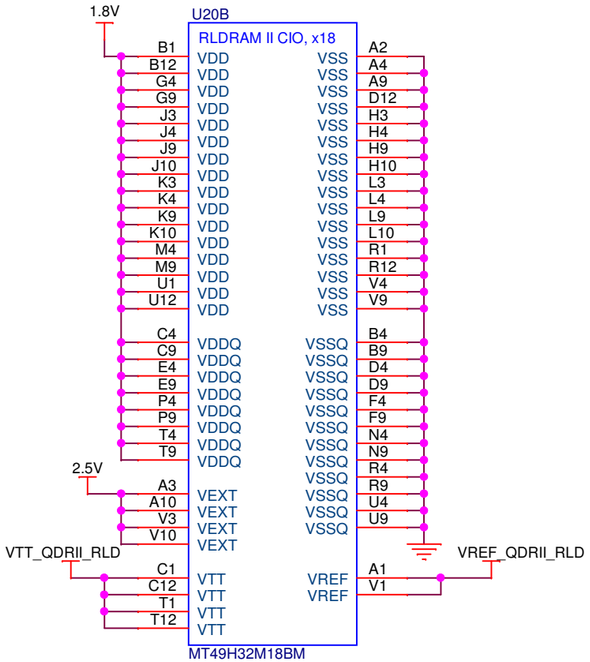
Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 15 of 34

RLDRAM II, CIO

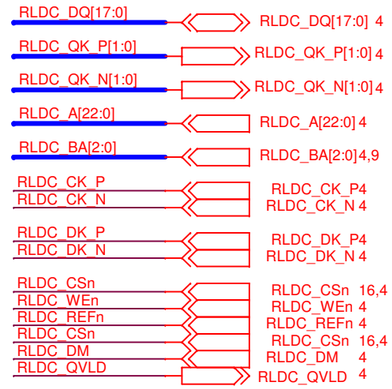




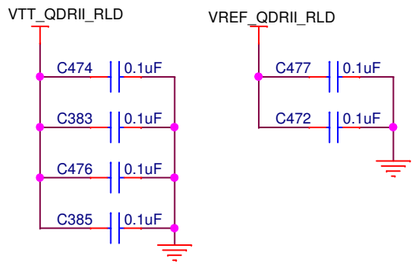
Altera recommends to use external termination for RLDRAM II address and command signals. In this case external termination was not used, because simulations showed that with the short trace length and a point to point connection the external termination was not necessary. As a result since there is limited board space external termination is not used.

On-die termination (ODT) is enabled by setting A9 to "1" during an MRS command.

RLDRAM II INTERFACE

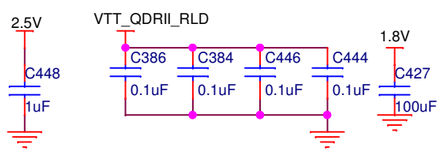


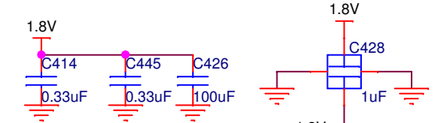
PLACE THESE CAPACITORS AS CLOSE AS POSSIBLE TO THE RLDRAM II

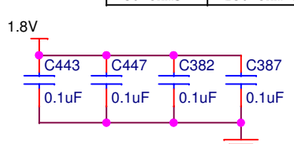


HSTL1

BYPASS CAPS FOR RLDRAM II CIO



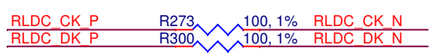




Output Impedence

Setting	RLDC_ZQ
MAX Drive	1.8V
60 Ohms	301 Ohm to GND
50 Ohms	250 Ohm to GND

PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM II



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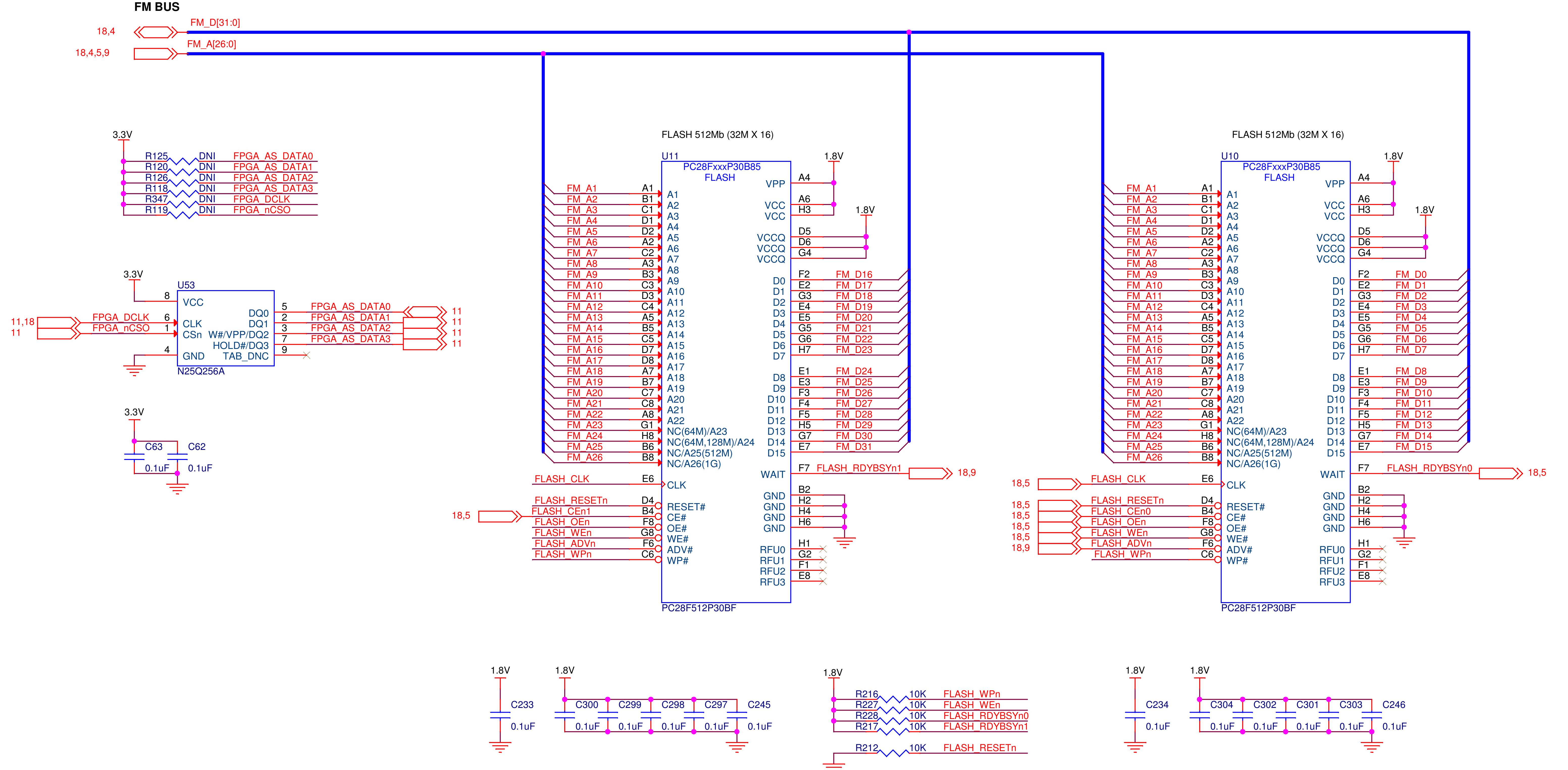
Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 16 of 34

FLASH



- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.
- When using dual x16 flash devices for an equivalent x32 (x16||x16) flash device a word consists of 32 data bits so addressing starts with FM_A1 mapped to address bit 2 in software.

5M2210 System Controller

U4A — MAX V BANK1 — 5M2210ZF256

FPGA_CONFIG_D0	D3	DIFFIO_L1P	DIFFIO_L13P	J4	FPGA_nSTATUS
FPGA_CONFIG_D1	C2	DIFFIO_L1N	DIFFIO_L13N	K1	FPGA_CONF_DONE
FPGA_CONFIG_D2	C3	DIFFIO_L2P	DIFFIO_L14P	J3	FPGA_DCLK
FPGA_CONFIG_D3	E3	DIFFIO_L2N	DIFFIO_L14N	K2	FPGA_CONFIG_D24
FPGA_CONFIG_D4	D2	DIFFIO_L3P	DIFFIO_L15P	K5	FPGA_CONFIG_D25
FPGA_CONFIG_D5	E4	DIFFIO_L3N	DIFFIO_L15N	L1	FPGA_CONFIG_D26
FPGA_CONFIG_D6	D1	DIFFIO_L4P	DIFFIO_L16P	L2	FPGA_CONFIG_D27
FPGA_CONFIG_D7	E5	DIFFIO_L4N	DIFFIO_L16N	K3	FPGA_CONFIG_D28
FPGA_CONFIG_D8	F3	DIFFIO_L5P	DIFFIO_L17P	M1	EXTRA_SIG0
FPGA_CONFIG_D9	E1	DIFFIO_L5N	DIFFIO_L17N	M2	FPGA_CONFIG_D29
FPGA_CONFIG_D10	F4	DIFFIO_L6P	DIFFIO_L18P	L4	FPGA_CONFIG_D30
FPGA_CONFIG_D11	F2	DIFFIO_L6N	DIFFIO_L18N	L3	FPGA_CONFIG_D31
FPGA_CONFIG_D12	F1	DIFFIO_L7P	DIFFIO_L19P	N1	FPGA_nCONFIG
FPGA_CONFIG_D13	F6	DIFFIO_L7N	DIFFIO_L19N	M4	
FPGA_CONFIG_D14	G2	DIFFIO_L8P	DIFFIO_L20P	N2	VCCINT_SCL
FPGA_CONFIG_D15	G3	DIFFIO_L8N	DIFFIO_L20N	M3	VCCINT_SDA
FPGA_CONFIG_D16	G1	DIFFIO_L9P	DIFFIO_L21P	N3	FPGA_CvP_CONFDONE
FPGA_CONFIG_D17	G4	DIFFIO_L9N	DIFFIO_L21N	P2	FPGA_PR_ERROR
FPGA_CONFIG_D18	H2	DIFFIO_L10P			
FPGA_CONFIG_D19	G5	DIFFIO_L10N	IOB1_1	E2	FPGA_PR_READY
FPGA_CONFIG_D20	H3	DIFFIO_L11P	IOB1_2	F5	FPGA_PR_REQUEST
FPGA_CONFIG_D21	J1	DIFFIO_L11N	IOB1_3	H1	FPGA_PR_DONE
FPGA_CONFIG_D23	H4	DIFFIO_L12P	IOB1_4	K4	
FPGA_CONFIG_D22	J2	DIFFIO_L12N	IOB1_5	L5	
USB_CLK	H5	IOB1/CLK0	TCK	P3	JTAG_TCK
CLK_CONFIG	J5	IOB1/CLK1	TDI	L6	JTAG_5M2210_TDI
			TDO	M5	JTAG_5M2210_TDO
			TMS	N4	5M2210_JTAG_TMS

JTAG_TCK → 11,12,22,25; JTAG_5M2210_TDI → 12; JTAG_5M2210_TDO → 12; 5M2210_JTAG_TMS → 12

U4B — MAX V BANK2 — 5M2210ZF256

SI571_EN	D4	DIFFIO_T1P	DIFFIO_T13P	E10	
	B1	DIFFIO_T1N	DIFFIO_T13N	A11	
	C5	DIFFIO_T2P	DIFFIO_T14P	B11	
	C4	DIFFIO_T2N	DIFFIO_T14N	A12	
	B4	DIFFIO_T3P	DIFFIO_T15P	E11	MAX_CONF_DONE
	D6	DIFFIO_T3N	DIFFIO_T15N	B12	
	E6	DIFFIO_T4P	DIFFIO_T16P	C11	
TSENSE_ALERTn	B5	DIFFIO_T4N	DIFFIO_T16N	B13	PGM_SEL
SENSE_SCK	A5	DIFFIO_T5P	DIFFIO_T17P	D12	PGM_CONFIG
SENSE_SDI	D7	DIFFIO_T5N	DIFFIO_T17N	B14	PGM_LED0
SENSE_SDO	B6	DIFFIO_T6P	DIFFIO_T18P	C13	PGM_LED1
SENSE_CS0n	E7	DIFFIO_T6N	DIFFIO_T18N	B16	PGM_LED2
OVERTEMPn	C8	DIFFIO_T7P			
OVERTEMP	B7	DIFFIO_T7N			
SENSE_SMB_CLK	D8	DIFFIO_T8P	IOB2_6	A13	CLK_SEL
SENSE_SMB_DATA	A7	DIFFIO_T8N	IOB2_7	A15	CLK_ENABLE
HSMA_PRSNTn	B8	DIFFIO_T9P	IOB2_8	A2	FACTORY_LOAD
HSMB_PRSNTn	A8	DIFFIO_T9N	IOB2_9	A4	MAX_ERROR
	A9	DIFFIO_T10P	IOB2_10	A6	MAX_LOAD
CLK50_EN	E9	DIFFIO_T10N	IOB2_11	B10	MSEL0
CLK125_EN	B9	DIFFIO_T11P	IOB2_12	B3	MSEL1
CLOCK_SDA	D9	DIFFIO_T11N	IOB2_13	C10	MSEL2
Si570_EN	A10	DIFFIO_T12P	IOB2_14	C12	MSEL3
CLOCK_SCL	C9	DIFFIO_T12N	IOB2_15	C6	MSEL4
			IOB2_16	C7	PCIE_JTAG_EN
			IOB2_17	D10	CPU_RESETn
			IOB2_18	D11	SDI_TX_EN
			IOB2_19	D5	SDI_RX_BYPASS
			IOB2_20	E8	SDI_RX_EN

FPGA_CONFIG_D[31:0] → 11
FPGA_nSTATUS → 11
FPGA_CONF_DONE → 11
FPGA_DCLK → 11,17
FPGA_nCONFIG → 11
FPGA_PR_DONE → 11
FPGA_PR_REQUEST → 11
FPGA_PR_READY → 11
FPGA_PR_ERROR → 11
FPGA_CvP_CONFDONE → 11
SENSE_SDO → 31
SENSE_SDI → 31
SENSE_SCK → 31
SENSE_CS0n → 31
TSENSE_ALERTn → 31
OVERTEMPn → 24,31
OVERTEMP → 31
SENSE_SMB_CLK → 31
SENSE_SMB_DATA → 31
SDI_TX_EN → 21,4
SDI_RX_BYPASS → 21,9
SDI_RX_EN → 11,21
VCCINT_SCL → 27
VCCINT_SDA → 27

FM_D[31:0] → 17,4
FM_A[26:0] → 17,4,5,9
FLASH_WEn → 17,5
FLASH_CEn0 → 17,5
FLASH_CEn1 → 17,5
FLASH_OEn → 17,5
FLASH_RDYBSYn0 → 17,5
FLASH_RDYBSYn1 → 17,9
FLASH_RESETn → 17,5
FLASH_CLK → 17,5
FLASH_ADVn → 17,9
CLK125_EN → 10
CLK50_EN → 10
Si570_EN → 10
Si571_EN → 10
CLOCK_SDA → 10
CLOCK_SCL → 10
MSEL0 → 11
MSEL1 → 11
MSEL2 → 11
MSEL3 → 11
MSEL4 → 11
MAX5_BEn[3:0] → 7
MAX5_OEn → 7
MAX5_CSn → 7
MAX5_WEn → 7
MAX5_CLK → 9
HSMA_PRSNTn → 22,24,5
HSMB_PRSNTn → 22,24,5
CPU_RESETn → 11,24
CLKIN_50 → 10,9

U4C — MAX V BANK3 — 5M2210ZF256

FM_A0	E14	DIFFIO_R1P	DIFFIO_R13P	J14	FM_D0
FM_A1	C14	DIFFIO_R1N	DIFFIO_R13N	J15	FM_D1
FM_A2	C15	DIFFIO_R2P	DIFFIO_R14P	K16	FM_D2
FM_A3	E13	DIFFIO_R2N	DIFFIO_R14N	K13	FM_D3
FM_A4	E12	DIFFIO_R3P	DIFFIO_R15P	K15	FM_D4
FM_A5	D15	DIFFIO_R3N	DIFFIO_R15N	K14	FM_D5
FM_A6	F14	DIFFIO_R4P	DIFFIO_R16P	L16	FM_D6
FM_A7	D16	DIFFIO_R4N	DIFFIO_R16N	L11	FM_D7
FM_A8	F13	DIFFIO_R5P	DIFFIO_R17P	L15	FM_D8
FM_A9	E15	DIFFIO_R5N	DIFFIO_R17N	L12	FM_D9
FM_A10	E16	DIFFIO_R6P	DIFFIO_R18P	M16	FM_D10
FM_A11	F15	DIFFIO_R6N	DIFFIO_R18N	L13	FM_D11
FM_A12	G14	DIFFIO_R7P	DIFFIO_R19P	M15	FM_D12
FM_A13	F16	DIFFIO_R7N	DIFFIO_R19N	L14	FM_D13
FM_A14	G13	DIFFIO_R8P	DIFFIO_R20P	N16	FM_D14
FM_A15	G15	DIFFIO_R8N	DIFFIO_R20N	M13	FM_D15
FM_A16	G12	DIFFIO_R9P	DIFFIO_R21P	N15	FM_D16
FM_A17	G16	DIFFIO_R9N	DIFFIO_R21N	N14	FM_D17
FM_A18	H14	DIFFIO_R10P	DIFFIO_R22P	P15	FM_D18
FM_A19	H15	DIFFIO_R10N	DIFFIO_R22N	P14	FM_D19
FM_A20	H13	DIFFIO_R11P			
FM_A21	H16	DIFFIO_R11N	IOB3_21	D13	FM_D20
FM_A22	J13	DIFFIO_R12P	IOB3_22	D14	FM_D21
FM_D23	J16	DIFFIO_R12N	IOB3_23	F11	FM_D22
			IOB3_24	F12	FM_D24
			IOB3_25	K12	FM_D25
CLKIN_50	J12		IOB3_26	M14	FM_D26
	H12	IOB3/CLK2	IOB3_27	N13	FM_D27
		IOB3/CLK3			

U4D — MAX V BANK4 — 5M2210ZF256

FM_D28	R1	DIFFIO_B1P	DIFFIO_B14P	M10	MAX5_OEn
FM_D29	P4	DIFFIO_B1N	DIFFIO_B14N	R10	MAX5_CSn
FM_A25	T2	DIFFIO_B2P	DIFFIO_B15P	N10	MAX5_WEn
FM_A24	P5	DIFFIO_B2N	DIFFIO_B15N	T11	MAX5_CLK
FM_A23	R3	DIFFIO_B3P	DIFFIO_B16P	P10	MAX5_BEn0
FM_D30	N5	DIFFIO_B3N	DIFFIO_B16N	R11	MAX5_BEn1
FM_D31	P6	DIFFIO_B4P	DIFFIO_B17P	T12	MAX5_BEn2
FLASH_WEn	N6	DIFFIO_B4N	DIFFIO_B17N	N11	MAX5_BEn3
FLASH_CEn0	R5	DIFFIO_B5P	DIFFIO_B19P	T13	EXTRA_SIG1
FLASH_OEn	M6	DIFFIO_B5N	DIFFIO_B19N	R13	
FLASH_RDYBSYn0	T5	DIFFIO_B6P	DIFFIO_B18P	R12	SECURITY_MODE
FLASH_RESETn	P7	DIFFIO_B6N	DIFFIO_B18N	P11	M570_CLOCK
FLASH_CLK	R6	DIFFIO_B7P	DIFFIO_B20P	N12	FACTORY_STATUS
FLASH_ADVn	N7	DIFFIO_B7N	DIFFIO_B20N	R14	FACTORY_REQUEST
FLASH_CEn1	M7	DIFFIO_B8P	DIFFIO_B21P	P12	M570_PCIE_JTAG_EN
FLASH_RDYBSYn1	R7	DIFFIO_B8N	DIFFIO_B21N	T15	EXTRA_SIG2
USB_CFG2	P8	DIFFIO_B9P	DIFFIO_B22P	R16	
USB_CFG3	T7	DIFFIO_B9N	DIFFIO_B22N	P13	
USB_CFG4	N8	DIFFIO_B10P	IOB4_28	M11	
USB_CFG5	R8	DIFFIO_B10N	IOB4_29	M12	
USB_CFG6	T8	DIFFIO_B11P	IOB4_30	N9	
USB_CFG7	T9	DIFFIO_B11N	IOB4_31	R4	USB_CFG0
USB_CFG8	R9	DIFFIO_B12P	IOB4_32	T10	USB_CFG11
USB_CFG9	P9	DIFFIO_B12N	IOB4_33	T4	USB_CFG1
MAX_RESETn	M9	DIFFIO_B13N/DEV_CLRn			
USB_CFG10	M8	DIFFIO_B13P/DEV_OE			

U4E — MAX V Power — 5M2210ZF256

	F7	GNDINT	VCCINT	F10	1.8V
	G6	GNDINT	VCCINT	G11	
	H7	GNDINT	VCCINT	H10	
	H9	GNDINT	VCCINT	H8	
	J10	GNDINT	VCCINT	J7	
	J8	GNDINT	VCCINT	J9	
	K11	GNDINT	VCCINT	K6	
	L10	GNDINT	VCCINT	L7	
	A1	GNDIO	VCCIO1	C1	2.5V
	A16	GNDIO	VCCIO1	H6	
	B15	GNDIO	VCCIO1	J6	
	B2	GNDIO	VCCIO1	P1	
	G10	GNDIO			
	G7	GNDIO	VCCIO2	A14	
	G8	GNDIO	VCCIO2	A3	
	G9	GNDIO	VCCIO2	F8	
	K10	GNDIO	VCCIO2	F9	
	K7	GNDIO			
	K8	GNDIO	VCCIO3	C16	1.8V
	K9	GNDIO	VCCIO3	H11	
	R15	GNDIO	VCCIO3	J11	
	R2	GNDIO	VCCIO3	P16	
	T1	GNDIO			
	T16	GNDIO	VCCIO4	L8	
	T6	GNDIO	VCCIO4	L9	
			VCCIO4	T14	
			VCCIO4	T3	

ON-BOARD USB BLASTER II

USB_CFG[11:0] → USB_CFG[11:0] 25
EXTRA_SIG[2:0] → EXTRA_SIG[2:0] 25
USB_CLK → 25,9
PCIE_JTAG_EN → 12
M570_PCIE_JTAG_EN → 25
M570_CLOCK → 25
FACTORY_STATUS → 25
FACTORY_REQUEST → 25

MAXV DIPSWITCH

CLK_SEL → 10,24
CLK_ENABLE → 24
FACTORY_LOAD → 24
SECURITY_MODE → 24

PUSH BUTTON INTERFACE

PGM_SEL → PGM_SEL 24
PGM_CONFIG → PGM_CONFIG 24
MAX_RESETn → MAX_RESETn 24

LED INTERFACE

PGM_LED[2:0] → PGM_LED[2:0] 24
MAX_ERROR → MAX_ERROR 24
MAX_LOAD → MAX_LOAD 24
MAX_CONF_DONE → MAX_CONF_DONE 24

X2 — 100MHz — 2.5V — EN, GND, VCC, OUT → CLK_CONFIG

C96 2.2uF, C92 0.1uF

VCCINT (1.8V): C201, C200, C190, C107, C147, C142, C165, C168 — 0.1uF

2.5V VCCIO (2.5V): C146, C126, C108, C191, C109, C125 — 0.1uF

1.8V VCCIO (1.8V): C167, C166, C143, C124, C144, C145 — 0.1uF

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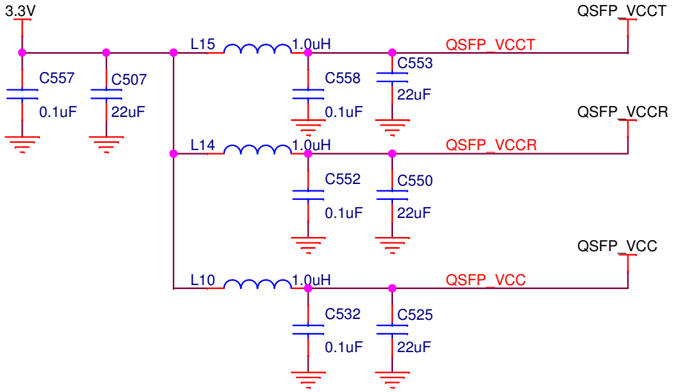
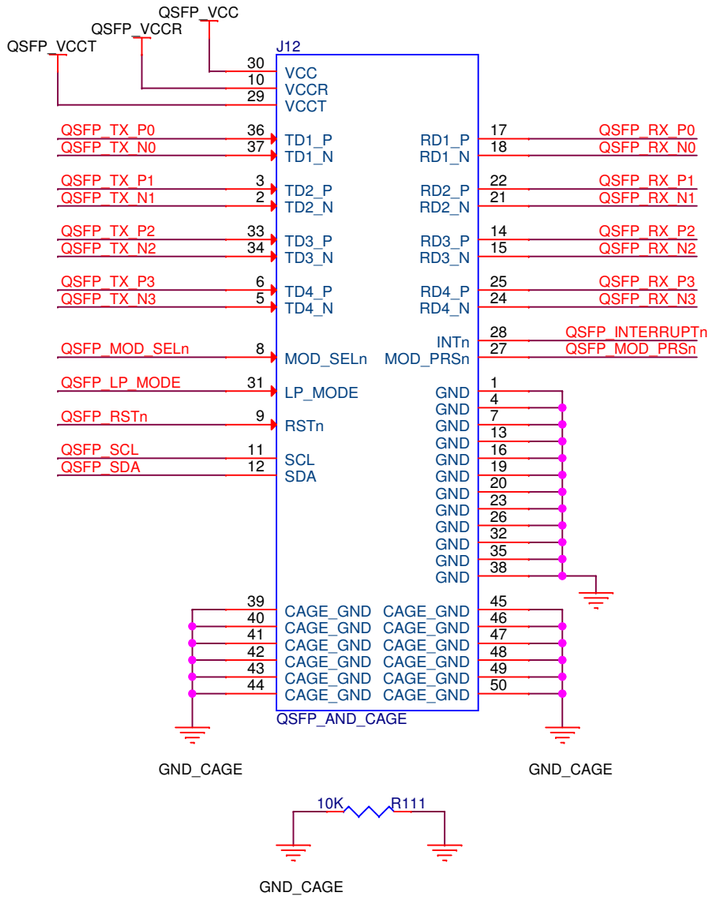
Title: **Stratix V GX FPGA Development Kit Board**

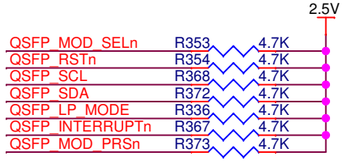
Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

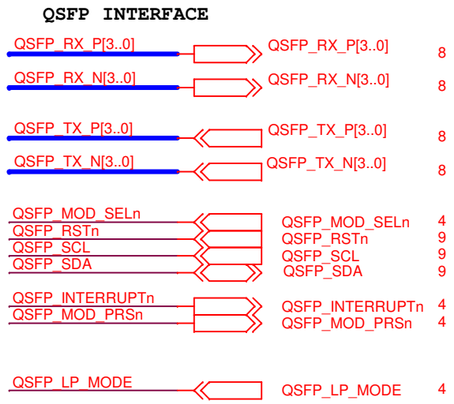
Date: Monday, June 03, 2013 Sheet 18 of 34

Quad Small Form-factor Pluggable (QSFP) Interface









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Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

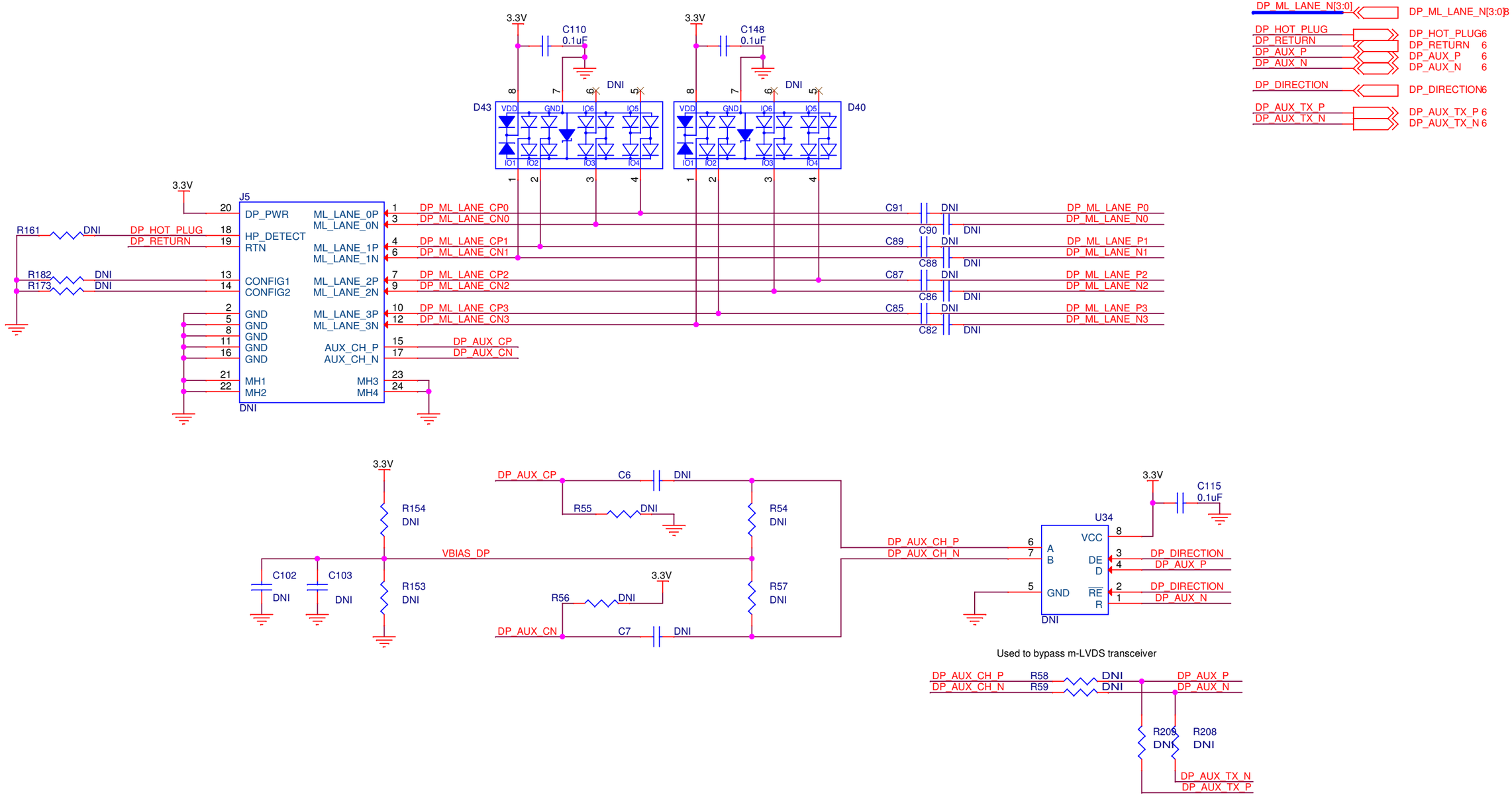
Date: Monday, June 03, 2013 Sheet 19 of 34

Display Port (x4)

UNTESTED AND UNPOPULATED.

DISPLAYPORT INTERFACE

DP_ML_LANE_P[3:0] — DP_ML_LANE_P[3:0]8
DP_ML_LANE_N[3:0] — DP_ML_LANE_N[3:0]8
DP_HOT_PLUG — DP_HOT_PLUG6
DP_RETURN — DP_RETURN 6
DP_AUX_P — DP_AUX_P 6
DP_AUX_N — DP_AUX_N 6
DP_DIRECTION — DP_DIRECTION6
DP_AUX_TX_P — DP_AUX_TX_P 6
DP_AUX_TX_N — DP_AUX_TX_N 6



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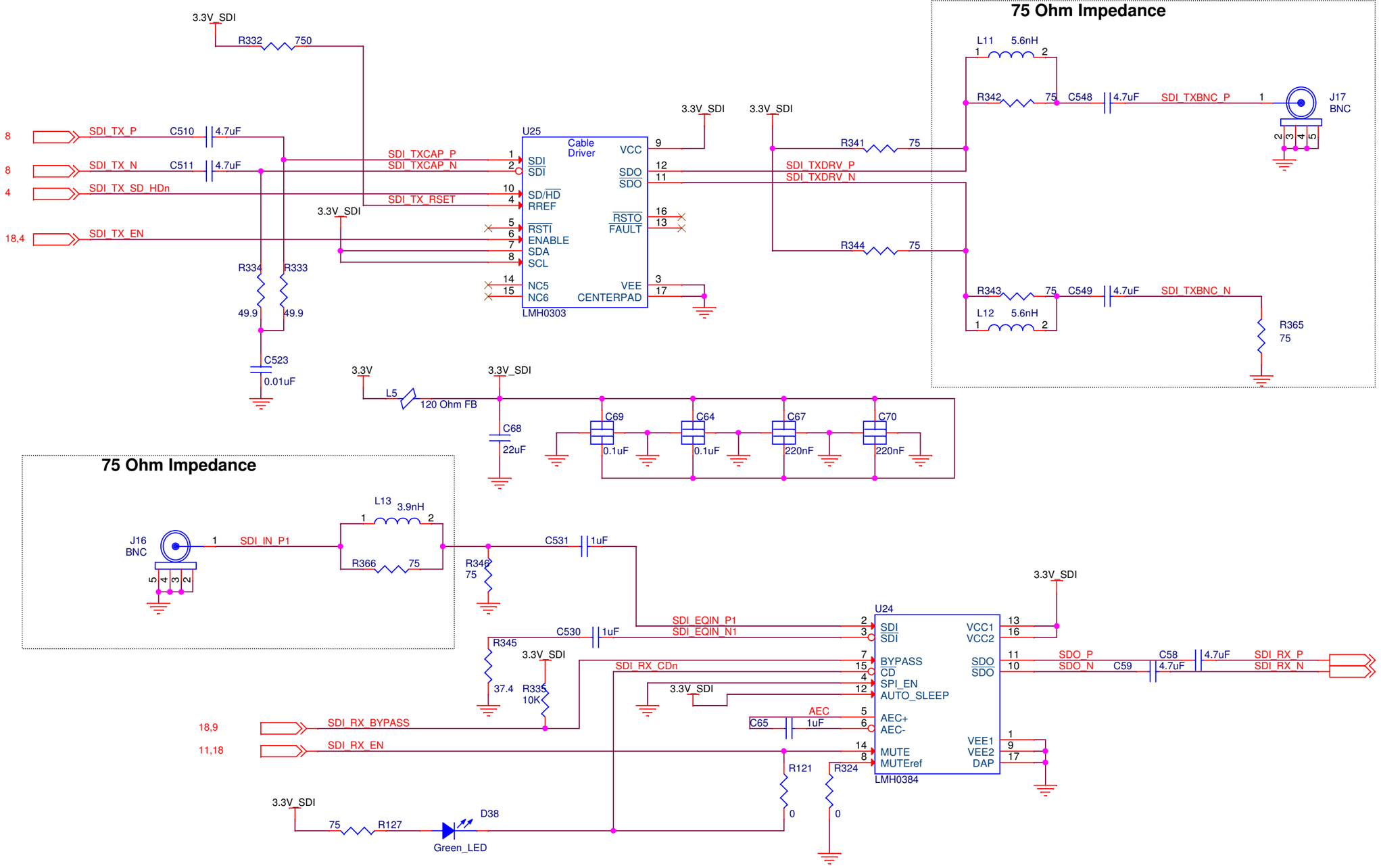
Size: B	Document Number: 150-0320202-D1 (6XX-44143R)	Rev: D1.1
Date: Monday, June 03, 2013	Sheet 20 of 34	

SDI Cable Driver, Equalizer, and SMB



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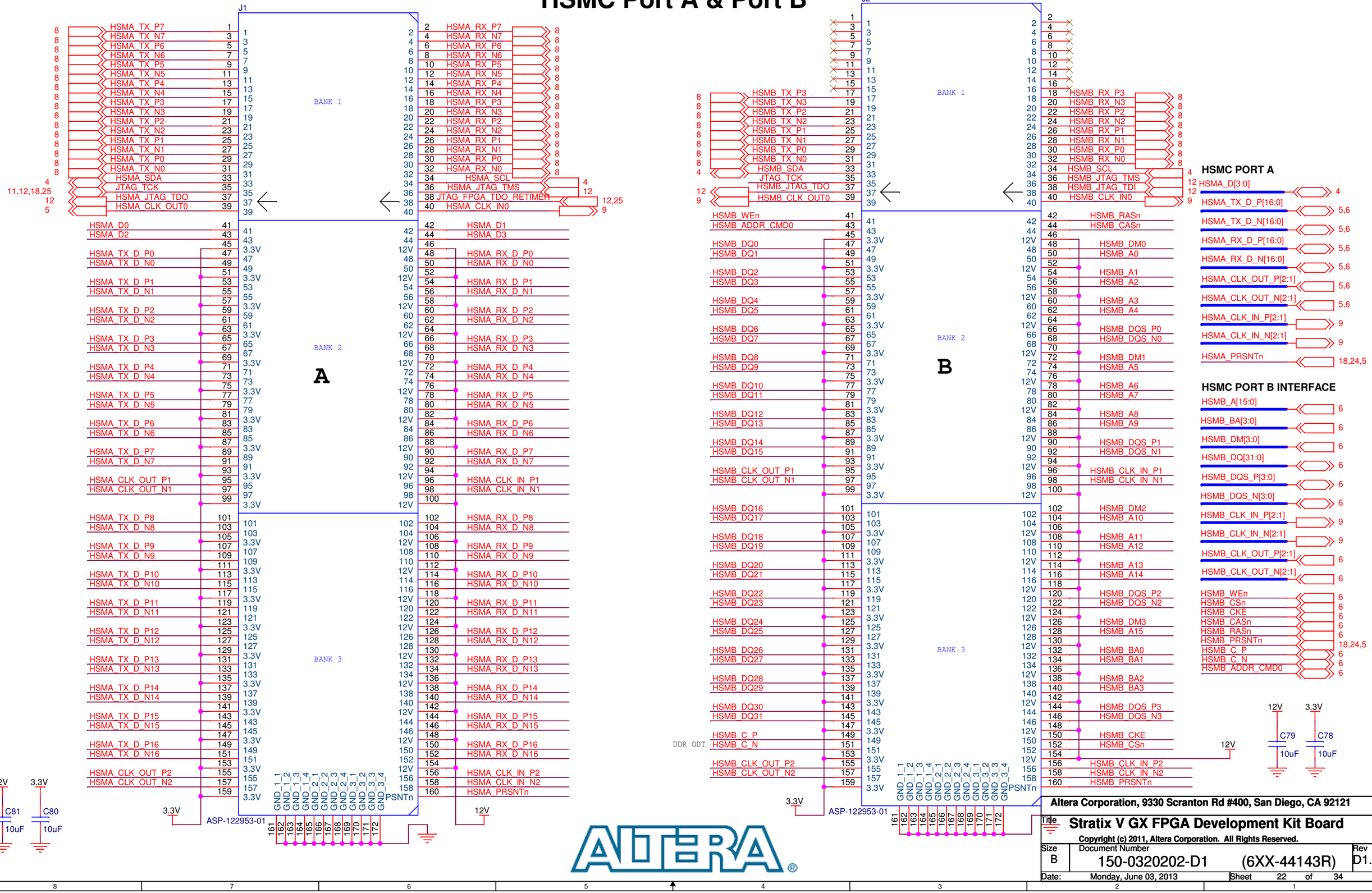
Title: Stratix V GX FPGA Development Kit Board

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 21 of 34

HSMC Port A & Port B



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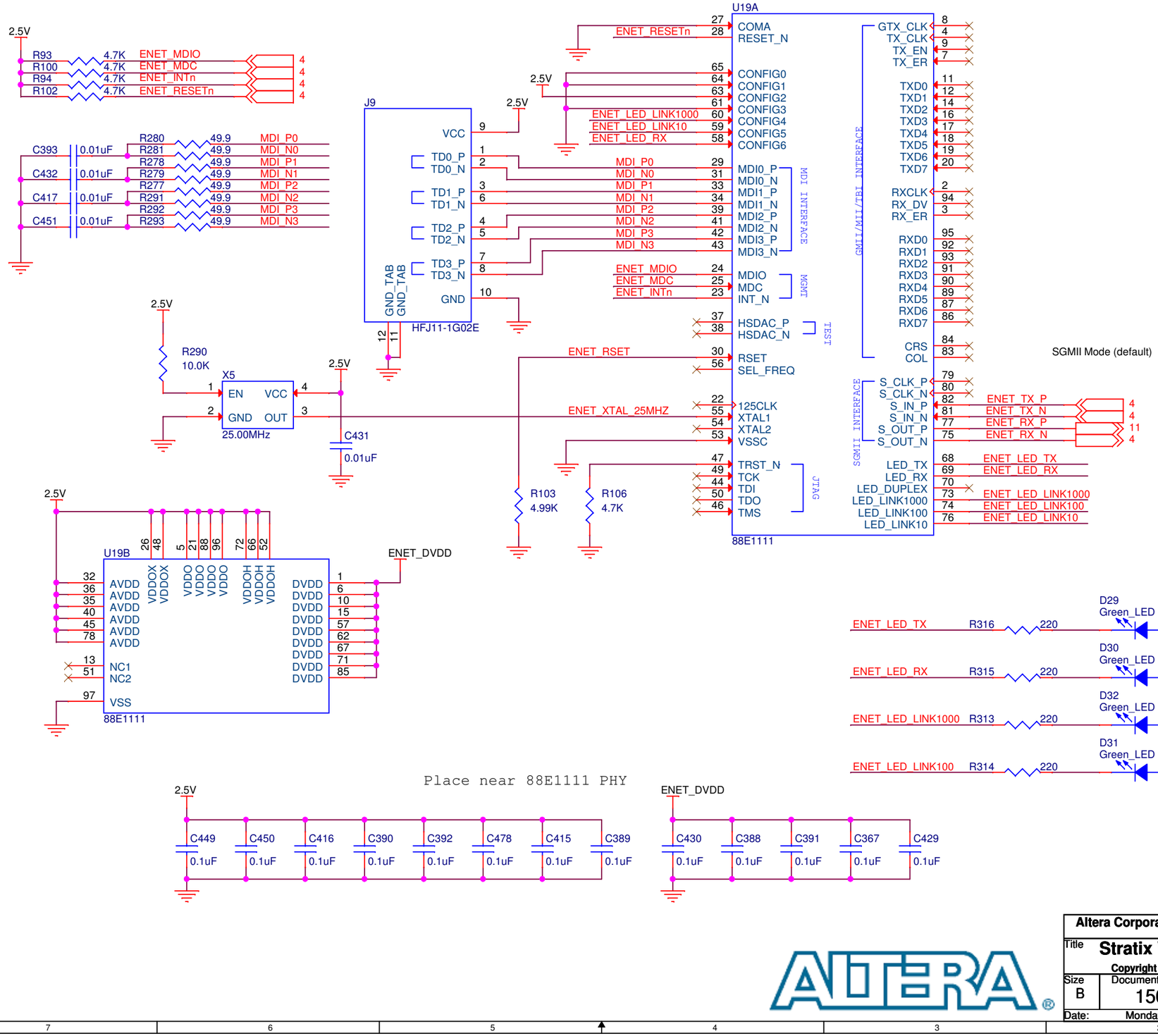
Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 22 of 34

10/100/1000 Ethernet



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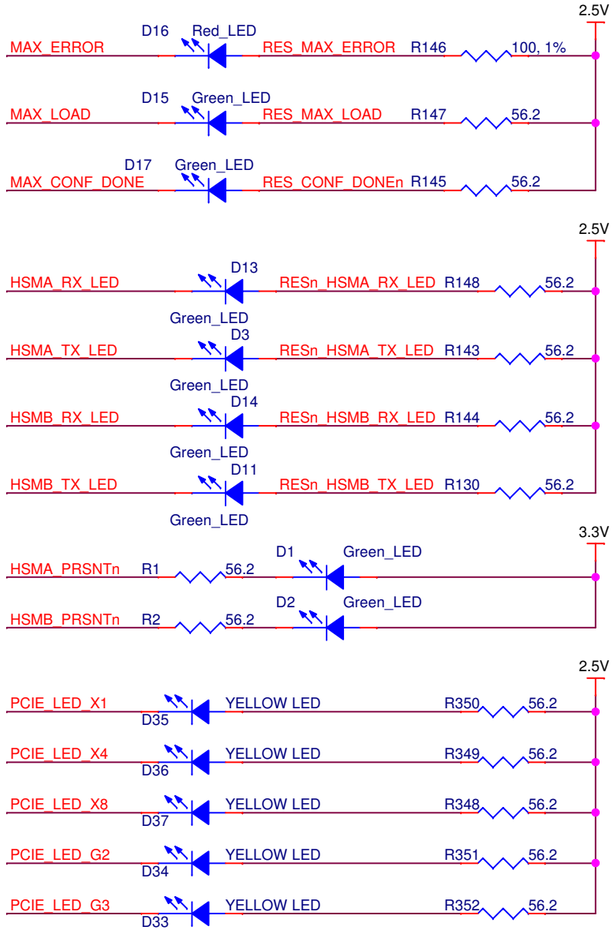
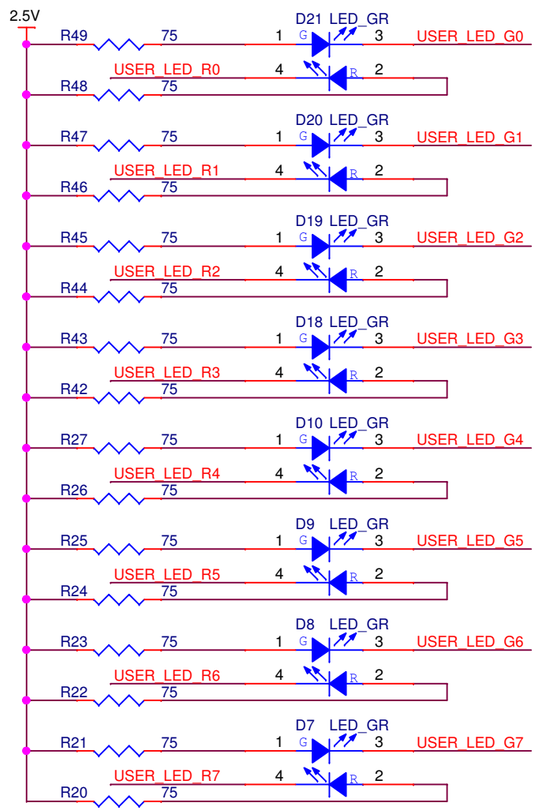
Title: **Stratix V GX FPGA Development Kit Board**

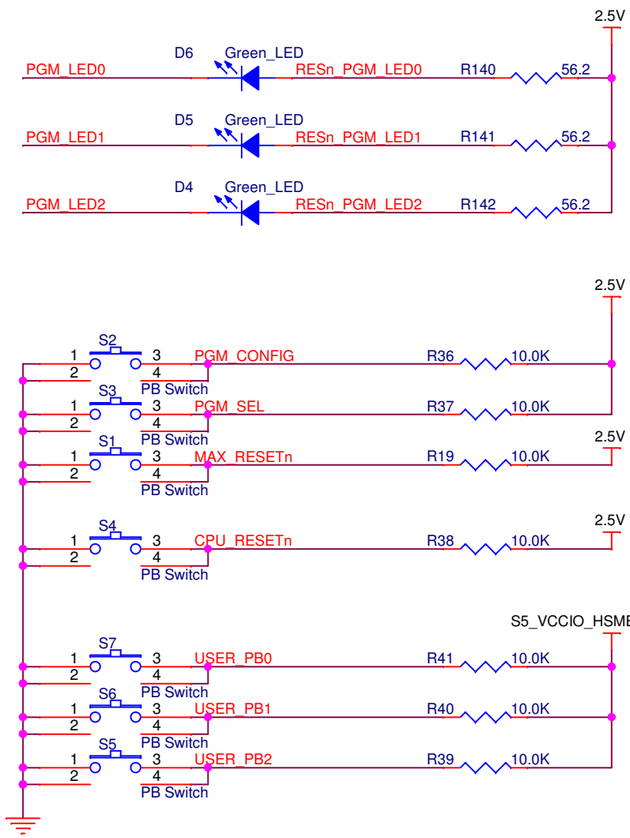
Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

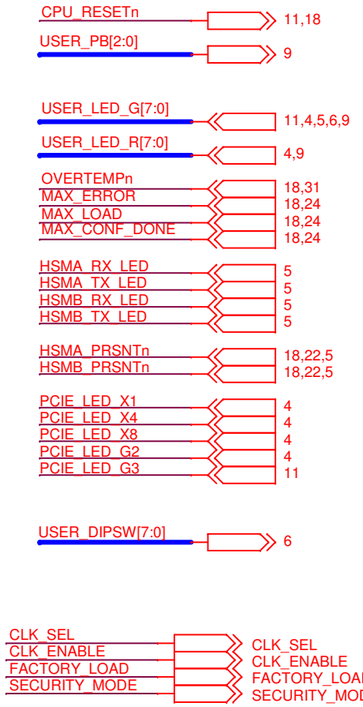
Date: Monday, June 03, 2013 Sheet 23 of 34

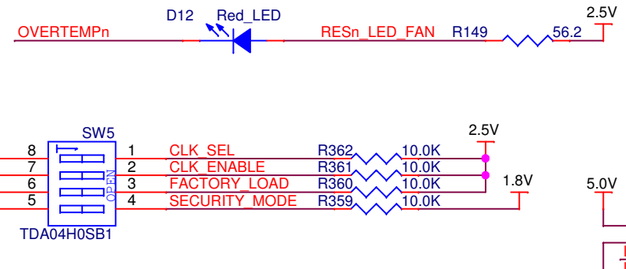
User I/O

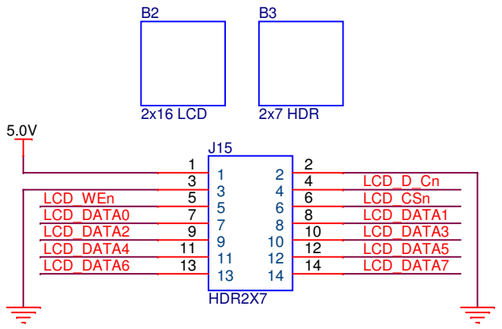


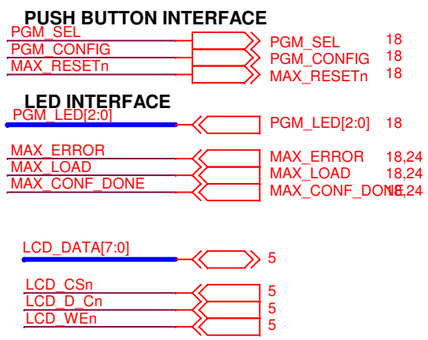












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Title: Stratix V GX FPGA Development Kit Board		
Size: B	Document Number: 150-0320202-D1 (6XX-44143R)	Rev: D1.1
Date: Monday, June 03, 2013	Sheet 24 of 34	

On-Board USB Blaster II

J7
MICRO_USB_CONN
VBUS 1 VBUS_5V
D- 2 FX2_D_N
D+ 3 FX2_D_P
ID 4 R246 DNI
5
9 8 7 6

U43
TPD2EUSB30
GND 3
D+ 1
D- 2

1M R260
4.7nF C346

Y1
24.00MHz
C205 12pF
C204 12pF

FX2_SDA R72 0 MAX_SDA

3.3V
C247 0.1uF
U9
MAX811
GND 1
VCC 4
RESET 2
MR 3
100K R205 FX2_RESETn

3.3V
U8
CY7C68013A_VFBGA

D1	AVCC	RESET	B8	FX2_RESETn	
D2	AVCC	SCL	F3	FX2_SCL	R206 2.00K 3.3V
		SDA	G3	FX2_SDA	R71 2.00K
G1	VCC				
A5	VCC	WAKEUP	B7	FX2_WAKEUP	
B5	VCC				
C5	VCC	CTL0	H7	FX2_FLAGA	
E7	VCC	CTL1	G7	FX2_FLAGB	
E8	VCC	CTL2	H8	FX2_FLAGC	
E1	DMINUS	RDY0	A1	FX2_SLRDn	
E2	DPLUS	RDY1	B1	FX2_SLWRn	
G2	IFCLK	CLKOUT	B2		
C1	XTALIN				
C2	XTALOUT				
G8	PA0	PB0	H3	FX2_PB0	
G6	PA1	PB1	F4	FX2_PB1	
F8	PA2	PB2	H4	FX2_PB2	
F7	PA3	PB3	G4	FX2_PB3	
F6	PA4	PB4	H5	FX2_PB4	
C8	PA5	PB5	G5	FX2_PB5	
C7	PA6	PB6	F5	FX2_PB6	
C6	PA7	PB7	H6	FX2_PB7	
H2	RESERVED	PD0	A8	FX2_PD0	
		PD1	A7	FX2_PD1	
F1	AGND	PD2	B6	FX2_PD2	
F2	AGND	PD3	A6	FX2_PD3	
		PD4	B3	FX2_PD4	
H1	GND	PD5	A3	FX2_PD5	
A4	GND	PD6	C3	FX2_PD6	
B4	GND	PD7	A2	FX2_PD7	
C4	GND				
D7	GND				
D8	GND				

USB_CLK
24M_XTALIN
24M_XTALOUT

VBUS_5V R190 10.0K FX2_WAKEUP
R189 20.0K C192 0.1uF

PLACE NEAR CY7C68013A
3.3V
C221 C193 C222 C203 C202 C326 C235 C248
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

1.8V
D28 JTAG_RX RESn_JTAG_RX R242 56.2 Green_LED
D27 JTAG_TX RESn_JTAG_TX R243 56.2 Green_LED
D26 SC_RX RESn_SC_RX R244 56.2 Green_LED
D25 SC_TX RESn_SC_TX R245 56.2 Green_LED

1.5V
R77 1.00k USB_SCL
R80 1.00k USB_SDA
R75 1.00k USB_FULL
R76 1.00k USB_EMPTY
R73 1.00k FACTORY_REQUEST

3.3V
R155 1.00K C_USB_MAX_TCK
R172 1.00K C_USB_MAX_TMS
C_USB_MAX_TDI
J19
DNI

U14A
MAX II BANK1
EPM570GM100

FX2_PA2	B1	IOB1_1	IOB1_17	K3	FX2_PB6
FX2_FLAGC	C1	IOB1_2	IOB1_18	K4	FX2_PB1
FX2_PA7	C2	IOB1_3	IOB1_19	K5	FX2_PB3
FX2_FLAGA	D1	IOB1_4	IOB1_20	K6	FX2_SCL
FX2_PA3	D2	IOB1_5	IOB1_21	K7	FX2_PD6
FX2_PA4	D3	IOB1_6	IOB1_22	K9	FX2_PD4
EXTRA_SIG0	E2	IOB1_7	IOB1_23	L1	FX2_SLWRn
FX2_PB4	F1	IOB1_8	IOB1_24	L10	C_JTAG_TCK
FX2_PA6	F3	IOB1_9	IOB1_25	L11	JTAG_FPGA_TDO_RETIMER
FX2_PB2	G1	IOB1_10	IOB1_26	L2	FX2_SLRDn
FX2_FLAGB	G2	IOB1_11	IOB1_27	L3	FX2_PD7
FX2_PB0	H1	IOB1_12	IOB1_28	L4	FX2_PD5
FX2_PA1	H2	IOB1_13	IOB1_29	L5	FX2_PA5
FX2_PB5	H3	IOB1_14	IOB1_30	L6	C_JTAG_TDO
USB_DISABLEn	J6	IOB1_15	IOB1_31	L7	C_JTAG_TMS
JTAG_FPGA_TDO	K10	IOB1_16	IOB1_32	L9	C_JTAG_TDI
USB_CLK	F2	IOB1/GCLK0	TCK	K1	C_USB_MAX_TCK R86 0 FX2_PD0
FX2_PB7	E1	IOB1/GCLK1	TDI	J2	C_USB_MAX_TDI R87 0 FX2_PD2
			TDO	K2	C_USB_MAX_TDO R88 0 FX2_PD3
FX2_RESETn	K8	IOB1/DEV_CLRn	TMS	J1	C_USB_MAX_TMS R85 0 FX2_PD1
MAX_SDA	L8	IOB1/DEV_OE			

JTAG_FPGA_TDO_RETIMER 0 R259 JTAG_FPGA_TDO 1,11

U14B
MAX II BANK2
EPM570GM100

JTAG_TX	A1	IOB2_1	IOB2_17	B5	USB_DATA0
SC_RX	A10	IOB2_2	IOB2_18	B6	USB_DATA1
SC_TX	A11	IOB2_3	IOB2_19	B7	USB_DATA2
JTAG_RX	A2	IOB2_4	IOB2_20	B8	USB_DATA3
FACTORY_REQUEST	A3	IOB2_5	IOB2_21	B9	USB_DATA4
USB_CFG5	A4	IOB2_6	IOB2_22	C10	USB_DATA5
USB_RESETn	A5	IOB2_7	IOB2_23	C11	USB_DATA6
USB_OEn	A6	IOB2_8	IOB2_24	C6	USB_DATA7
USB_RDn	A7	IOB2_9	IOB2_25	D10	USB_CFG8
USB_WRn	A8	IOB2_10	IOB2_26	D11	USB_ADDR0
FACTORY_STATUS	A9	IOB2_11	IOB2_27	D9	USB_ADDR1
USB_CFG3	B10	IOB2_12	IOB2_28	E10	USB_FULL
M570_PCIE_JTAG_EN	B11	IOB2_13	IOB2_29	E11	USB_EMPTY
USB_CFG4	B2	IOB2_14	IOB2_30	F11	USB_SCL
EXTRA_SIG1	B3	IOB2_15	IOB2_31	F9	USB_CFG11
USB_CFG6	B4	IOB2_16	IOB2_32	G10	USB_SDA
			IOB2_33	H10	USB_CFG10
			IOB2_34	H11	USB_CFG0 V13
			IOB2_35	H9	EXTRA_SIG2
			IOB2_36	J10	USB_CFG1 V15
USB_CFG7	F10	IOB2/GCLK2	IOB2_37	J11	USB_CFG2 V14
M570_CLOCK	G11	IOB2/GCLK3	IOB2_38	K11	USB_CFG9

C_JTAG_TCK 0 R266 JTAG_TCK
C_JTAG_TMS 0 R275 JTAG_TMS
C_JTAG_TDI 0 R265 JTAG_BLASTER_TDI
C_JTAG_TDO 0 R274 JTAG_BLASTER_TDO

2.5V
R308 DNI JTAG_BLASTER_TDI

U14C
MAX II Power
EPM570GM100

C5	GNDINT	VCCINT	C7	1.8V
E8	GNDINT	VCCINT	E9	
G4	GNDINT	VCCINT	G3	
J5	GNDINT	VCCINT	J7	
D5	GNDIO	VCCIO1	E3	3.3V
D7	GNDIO	VCCIO1	J4	
E4	GNDIO	VCCIO1	J8	
G8	GNDIO			
H5	GNDIO	VCCIO2	C4	1.5V
H7	GNDIO	VCCIO2	C8	
		VCCIO2	G9	

PLACE NEAR MAX II (U14)
3.3V 1.5V 1.8V
C327 C306 C269 C268 C305 C270
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

STRATIX V USB INTERFACE

USB_DATA[7:0]	USB_DATA[7:0]	7
USB_ADDR[1:0]	USB_ADDR[1:0]	7
USB_FULL	USB_FULL	9
USB_EMPTY	USB_EMPTY	9
USB_SCL	USB_SCL	7
USB_SDA	USB_SDA	7
USB_CLK	USB_CLK	18,9
USB_RESETn	USB_RESETn	7
USB_OEn	USB_OEn	7
USB_RDn	USB_RDn	7
USB_WRn	USB_WRn	7
M570_PCIE_JTAG_EN	M570_PCIE_JTAG_EN	18
JTAG_FPGA_TDO_RETIMER		12,22

MAX V USB INTERFACE

USB_CFG[11:0]	USB_CFG[11:0]	18
EXTRA_SIG[2:0]	EXTRA_SIG[2:0]	18
USB_DISABLEn	USB_DISABLEn	12
M570_CLOCK	M570_CLOCK	18
FACTORY_STATUS	FACTORY_STATUS	18
FACTORY_REQUEST	FACTORY_REQUEST	18

JTAG INTERFACE

JTAG_TCK	JTAG_TCK	11,12,18,22
JTAG_TMS	JTAG_TMS	11,12
JTAG_BLASTER_TDI	JTAG_BLASTER_TDI	12
JTAG_BLASTER_TDO	JTAG_BLASTER_TDO	11,12

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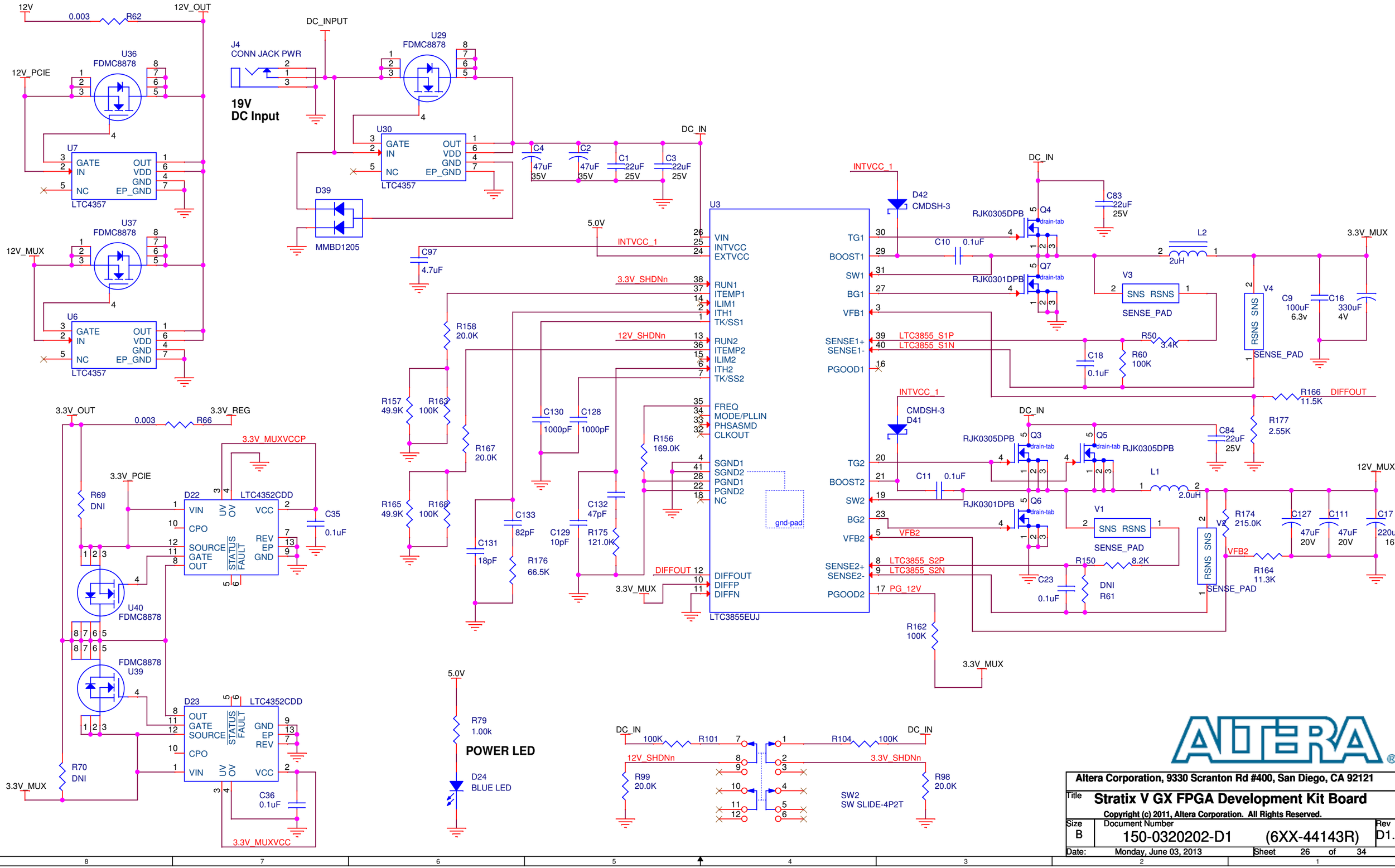
Title: Stratix V GX FPGA Development Kit Board

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 25 of 34

Power 1 - DC Input & 12V, 3.3V Output



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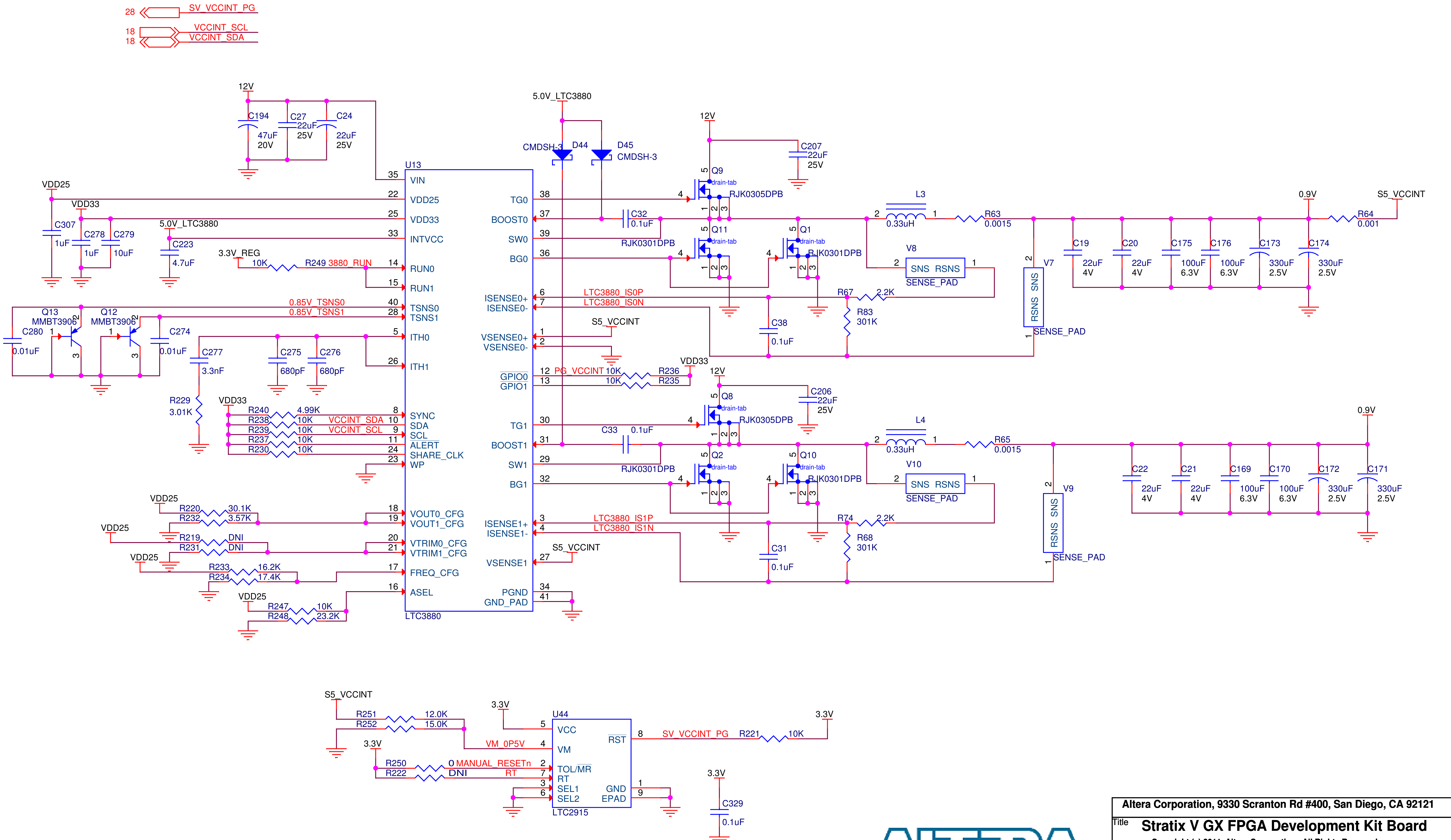
Title: Stratix V GX FPGA Development Kit Board

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 26 of 34

Power 2 - 0.90V


SV_VCCINT_PG
VCCINT_SCL
VCCINT_SDA
28
18
18
12V
C194 47uF 20V
C27 22uF 25V
C24 22uF 25V
VDD25
VDD33
C307 1uF
C278 1uF
C279 10uF
5.0V_LTC3880
C223 4.7uF
3.3V_REG
10K R249 3880_RUN
Q13 MMBT3906
Q12 MMBT3906
C280 0.01uF
C274 0.01uF
0.85V_TSNS0
0.85V_TSNS1
C277 3.3nF
C275 680pF
C276 680pF
R229 3.01K
R240 4.99K
R238 10K VCCINT_SDA
R239 10K VCCINT_SCL
R237 10K
R230 10K
R220 30.1K
R232 3.57K
R219 DNI
R231 DNI
R233 16.2K
R234 17.4K
R247 10K
R248 23.2K
U13
VIN
VDD25
VDD33
INTVCC
RUN0
RUN1
TSNS0
TSNS1
ITH0
ITH1
SYNC
SDA
SCL
ALERT
SHARE_CLK
WP
VOUT0_CFG
VOUT1_CFG
VTRIM0_CFG
VTRIM1_CFG
FREQ_CFG
ASEL
TG0
BOOST0
SW0
BG0
ISENSE0+
ISENSE0-
VSENSE0+
VSENSE0-
GPIO0
GPIO1
TG1
BOOST1
SW1
BG1
ISENSE1+
ISENSE1-
VSENSE1
PGND
GND_PAD
LTC3880
CMDSH-3 D44
D45 CMDSH-3
C32 0.1uF
C33 0.1uF
Q9 RJK0305DPB
Q11 RJK0301DPB
Q1 RJK0301DPB
Q8 RJK0305DPB
Q2 RJK0301DPB
Q10 RJK0301DPB
drain-tab
C207 22uF 25V
C206 22uF 25V
LTC3880_IS0P
LTC3880_IS0N
LTC3880_IS1P
LTC3880_IS1N
S5_VCCINT
PG_VCCINT 10K R236
10K R235
C38 0.1uF
C31 0.1uF
R67 2.2K
R83 301K
R74 2.2K
R68 301K
L3 0.33uH
L4 0.33uH
R63 0.0015
R65 0.0015
V8 SNS RSNS SENSE_PAD
V10 SNS RSNS SENSE_PAD
V7 RSNS SNS SENSE_PAD
V9 RSNS SNS SENSE_PAD
0.9V
R64 0.001
C19 22uF 4V
C20 22uF 4V
C175 100uF 6.3V
C176 100uF 6.3V
C173 330uF 2.5V
C174 330uF 2.5V
C22 22uF 4V
C21 22uF 4V
C169 100uF 6.3V
C170 100uF 6.3V
C172 330uF 2.5V
C171 330uF 2.5V
R251 12.0K
R252 15.0K
3.3V
R250 0 MANUAL_RESETn
R222 DNI RT
VM_0P5V
U44
VCC
VM
TOL/MR
RT
SEL1
SEL2
RST
GND
EPAD
LTC2915
SV_VCCINT_PG R221 10K
C329 0.1uF

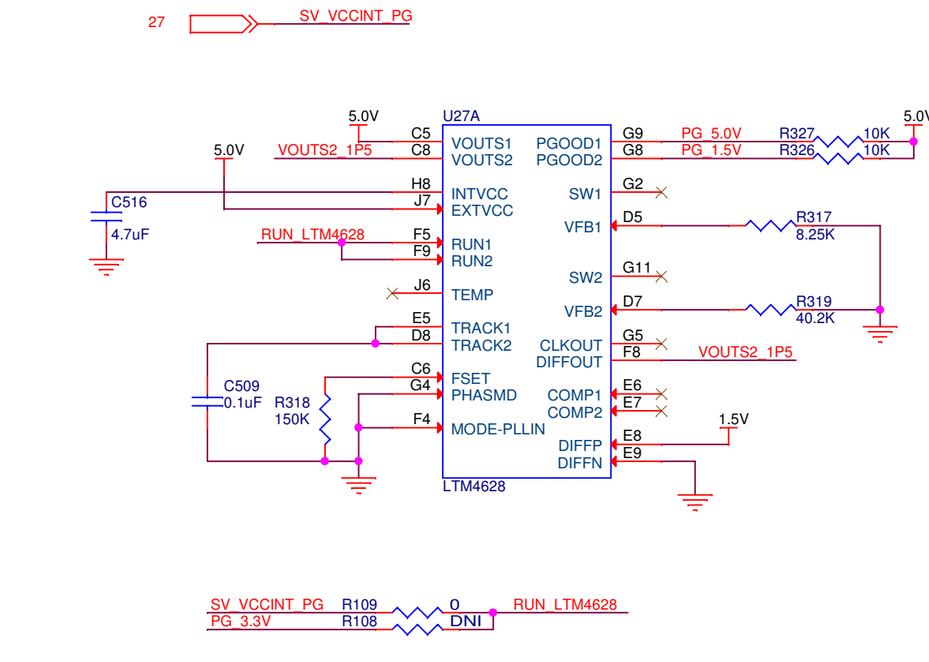
Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

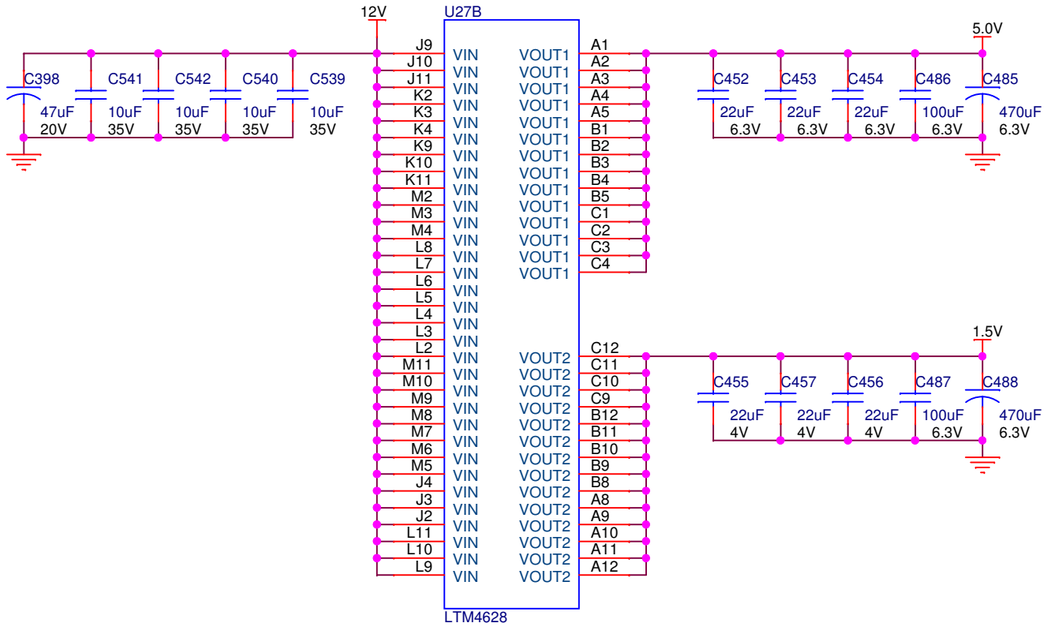
Title **Stratix V GX FPGA Development Kit Board**

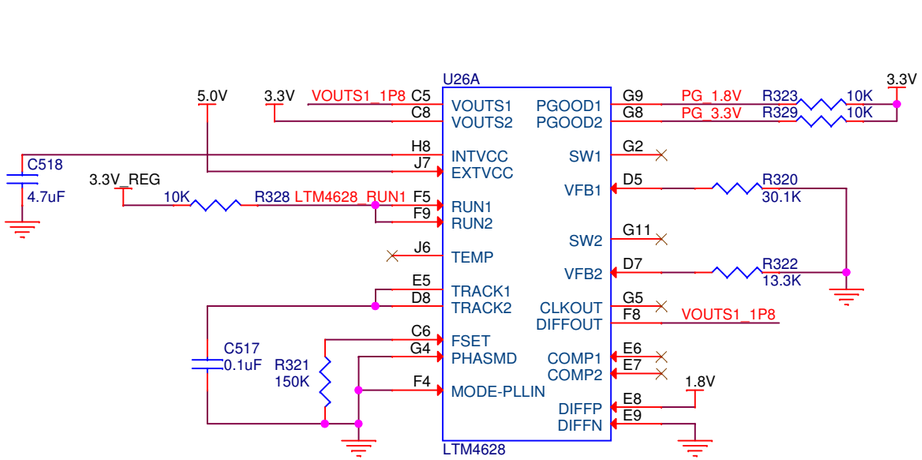
Size	Document Number		Rev
B	150-0320202-D1	(6XX-44143R)	D1.1

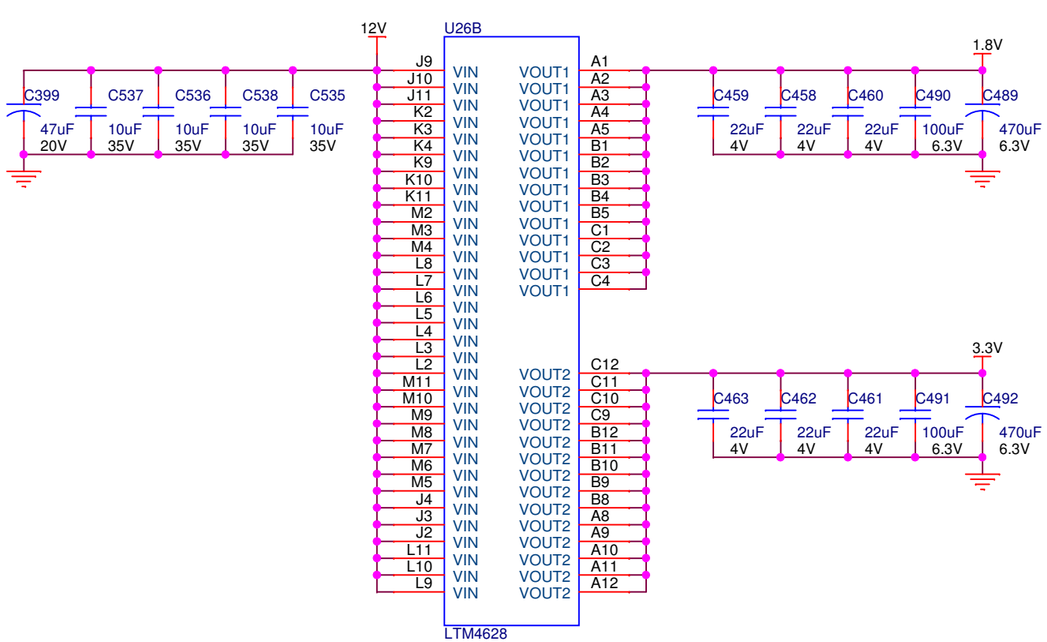
Date: Monday, June 03, 2013

Power 3 - 5.0V, 1.5V, 1.8V and 3.3V









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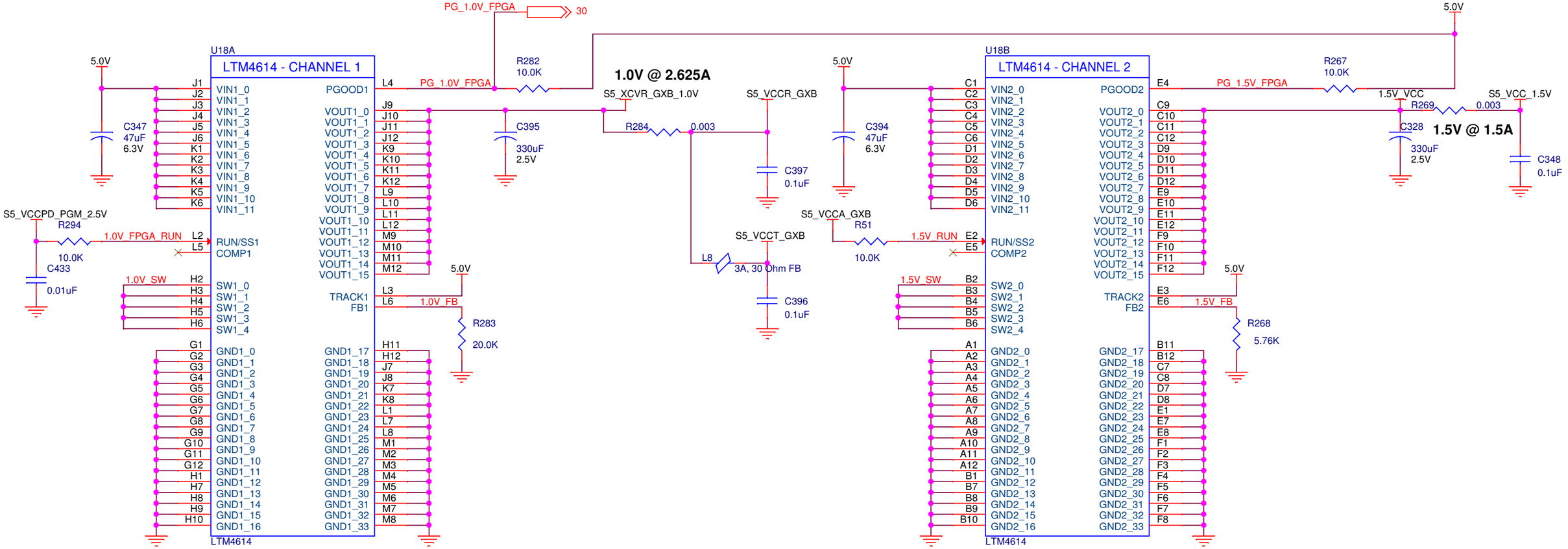
Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 28 of 34

Power 3 - 1.0V (GXB), 1.5V (VCCD_FPLL, VCCH_GXB, VCCPT)



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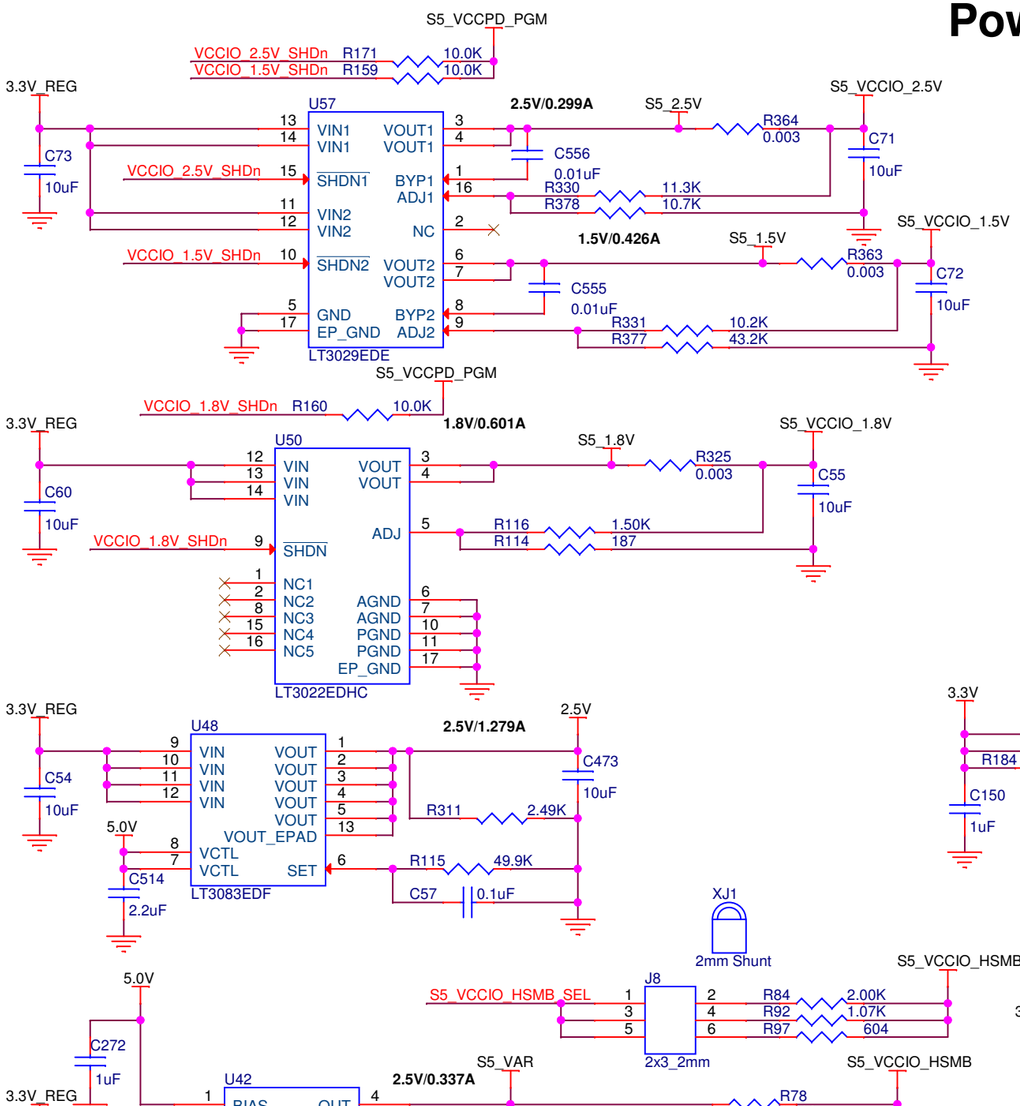
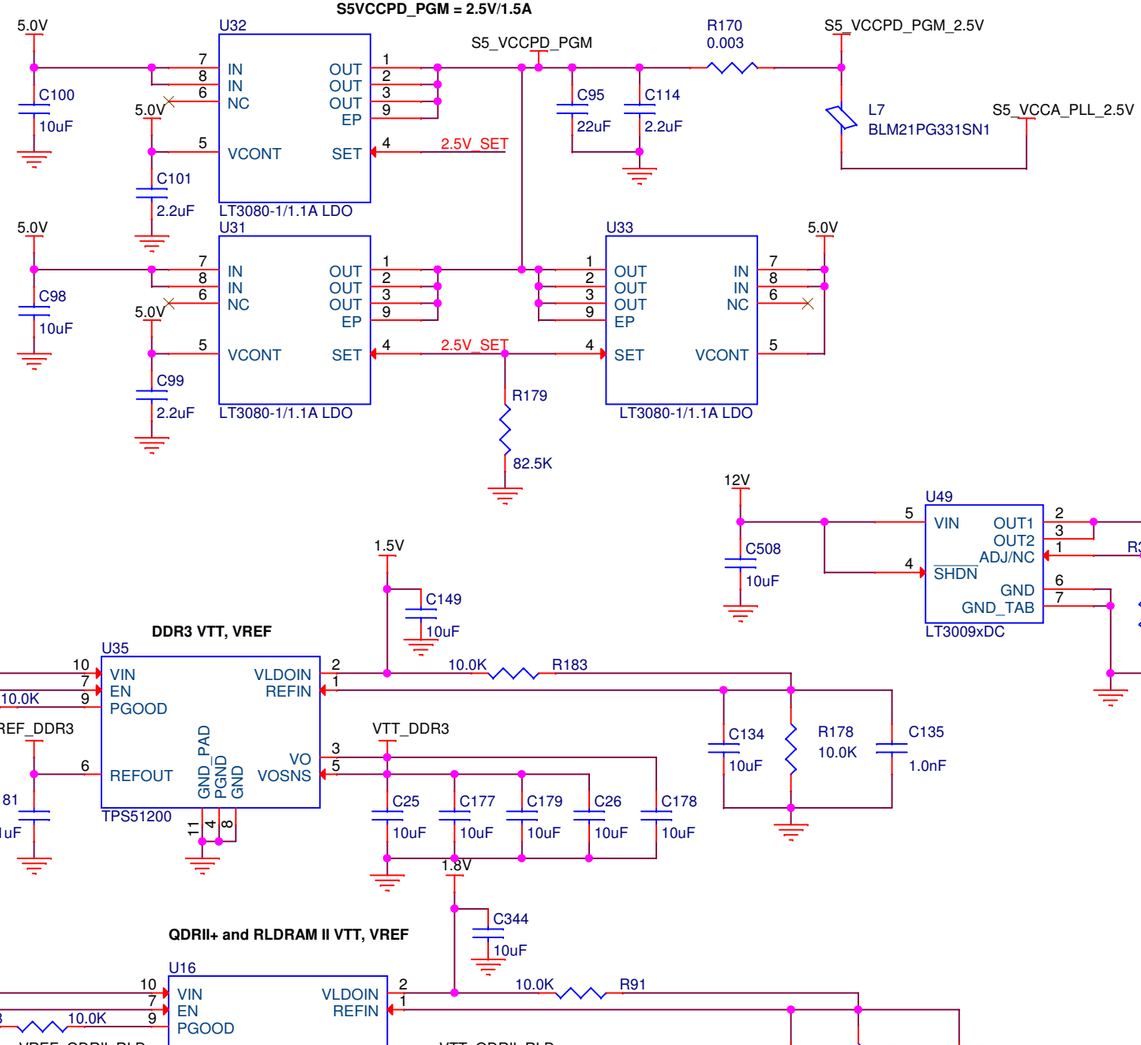
Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 29 of 34

Power 4 - Linear Regulators





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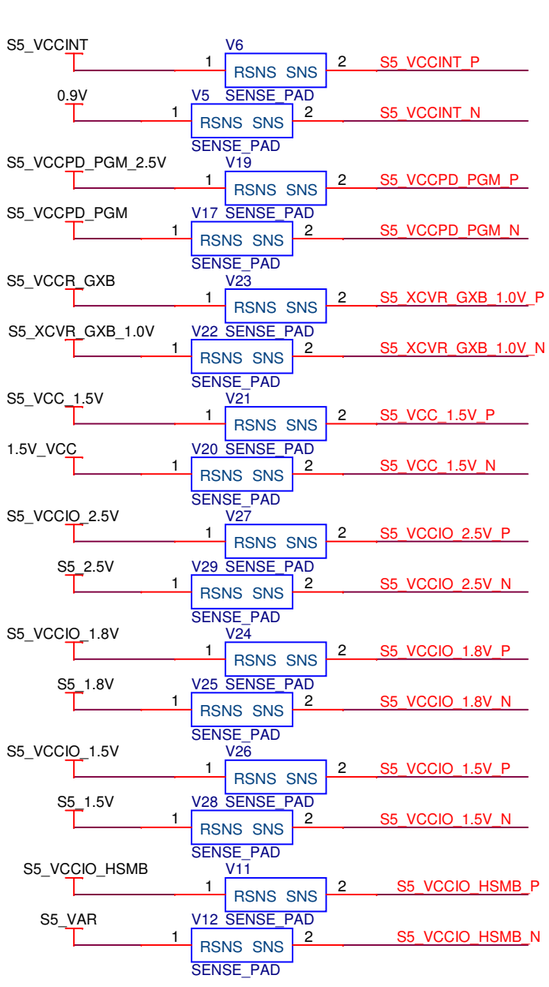
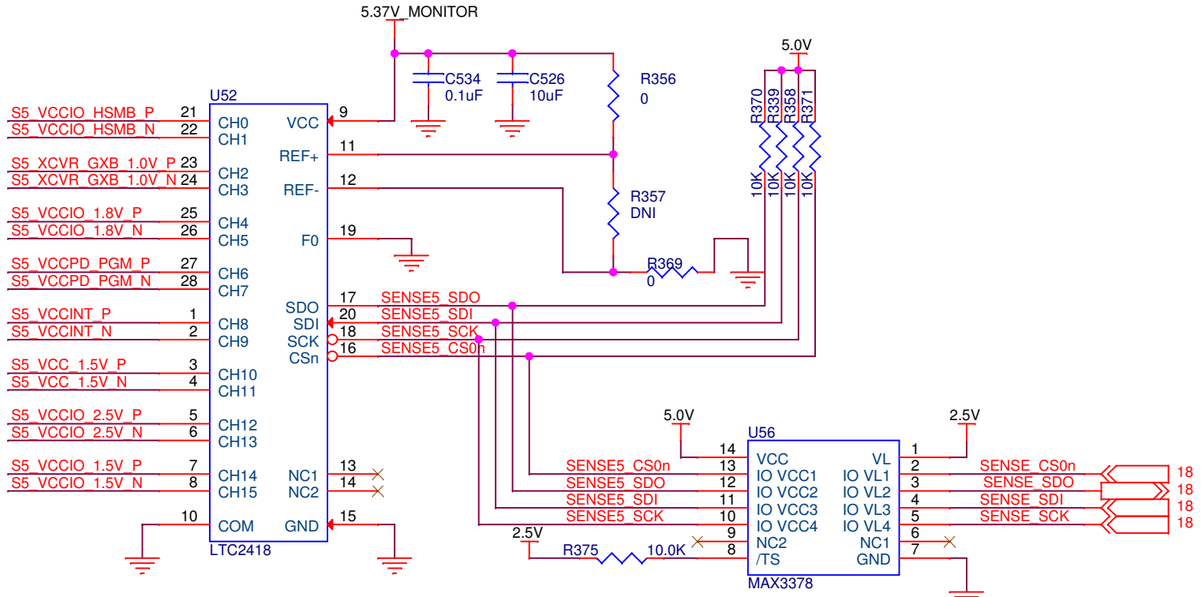
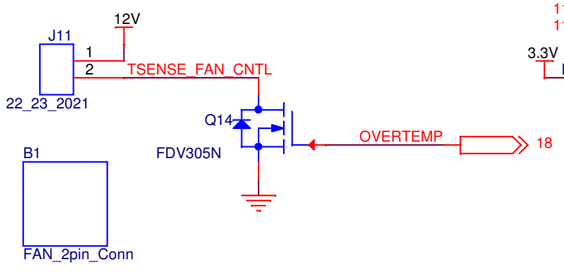
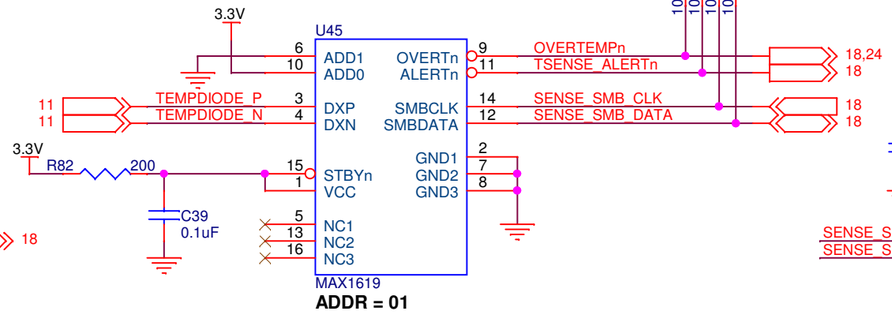
Title: **Stratix V GX FPGA Development Kit Board**			
Size: B	Document Number: 150-0320202-D1 (6XX-44143R)		Rev: D1.1
Date: Monday, June 03, 2013	Sheet 30 of 34		

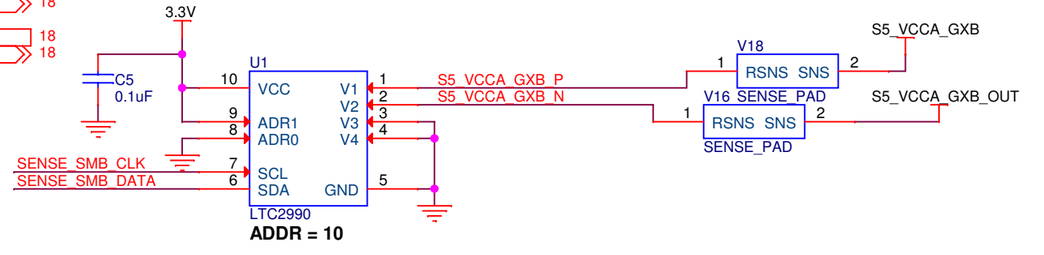
Power 6 - Power & Temperature Monitor











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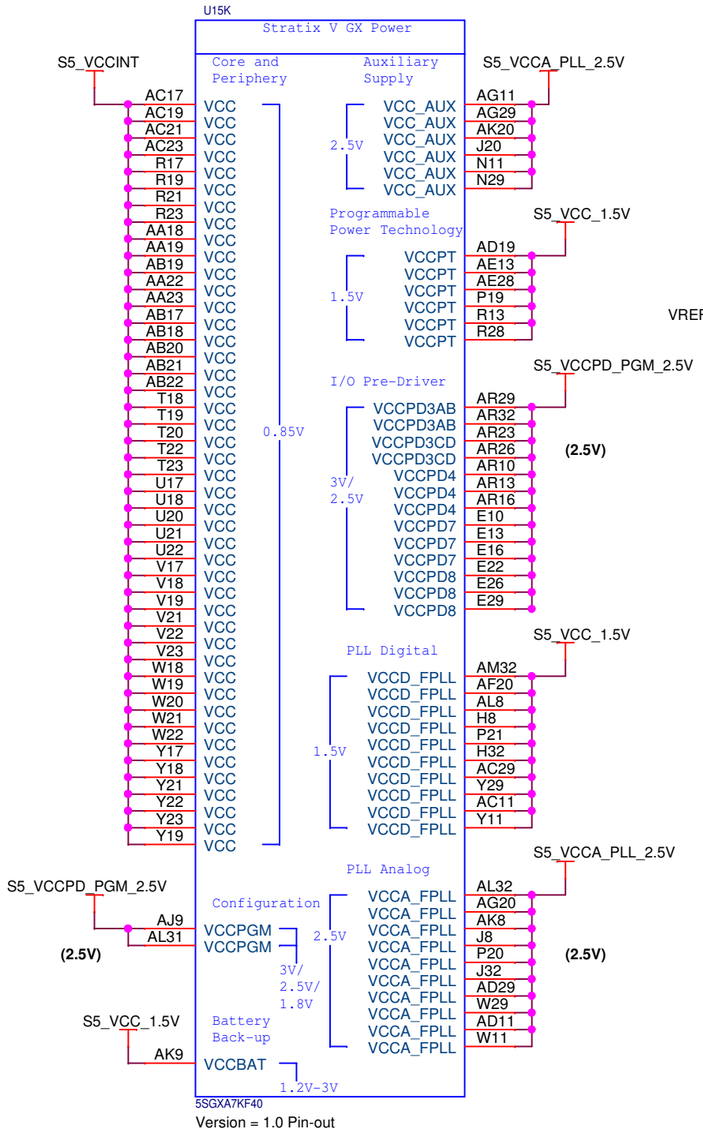
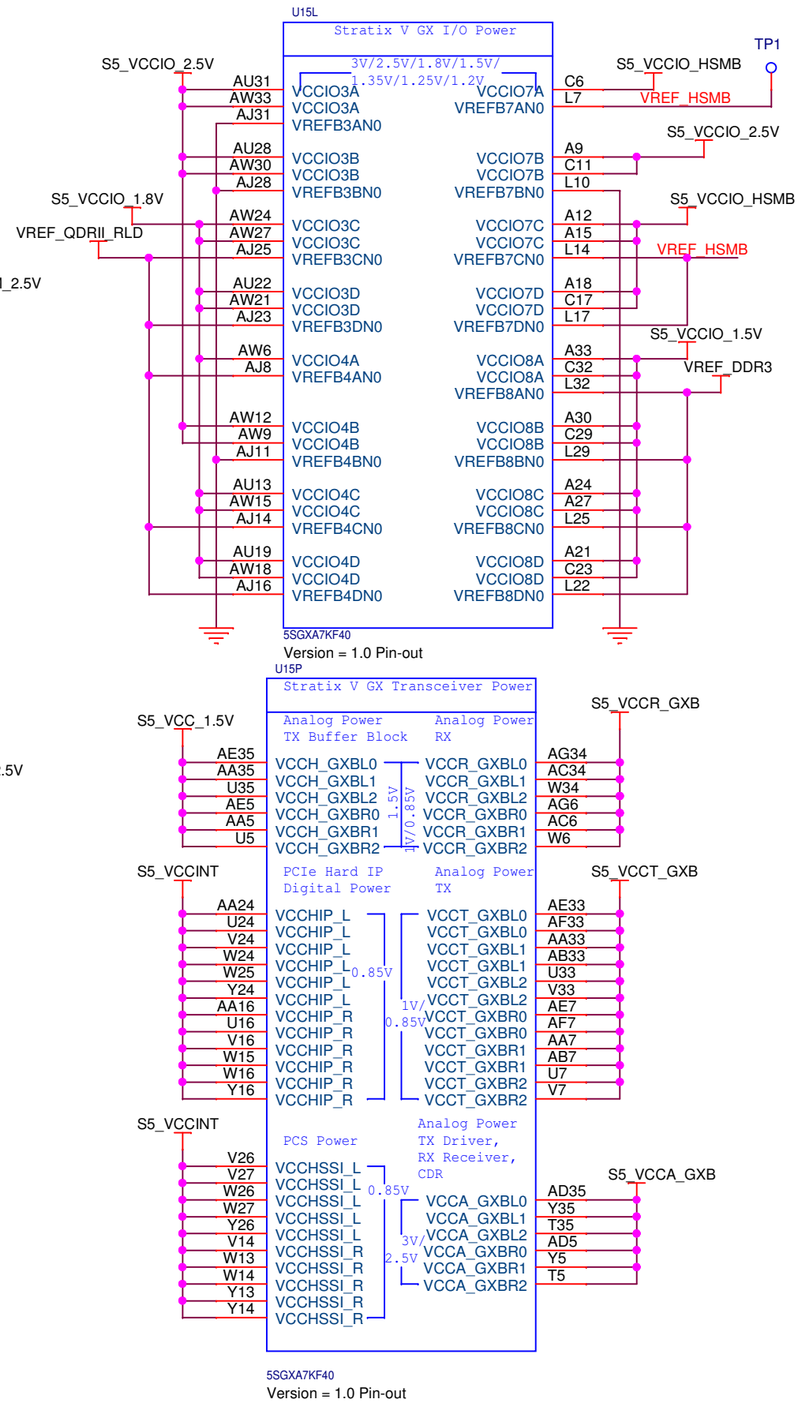
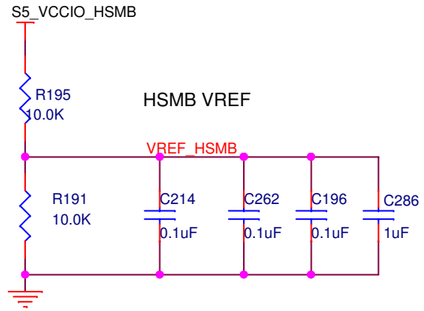
Title: Stratix V GX FPGA Development Kit Board		
Size: B	Document Number: 150-0320202-D1 (6XX-44143R)	Rev: D1.1
Date: Monday, June 03, 2013	Sheet 31 of 34	

Power 7 - Stratix V GX Power







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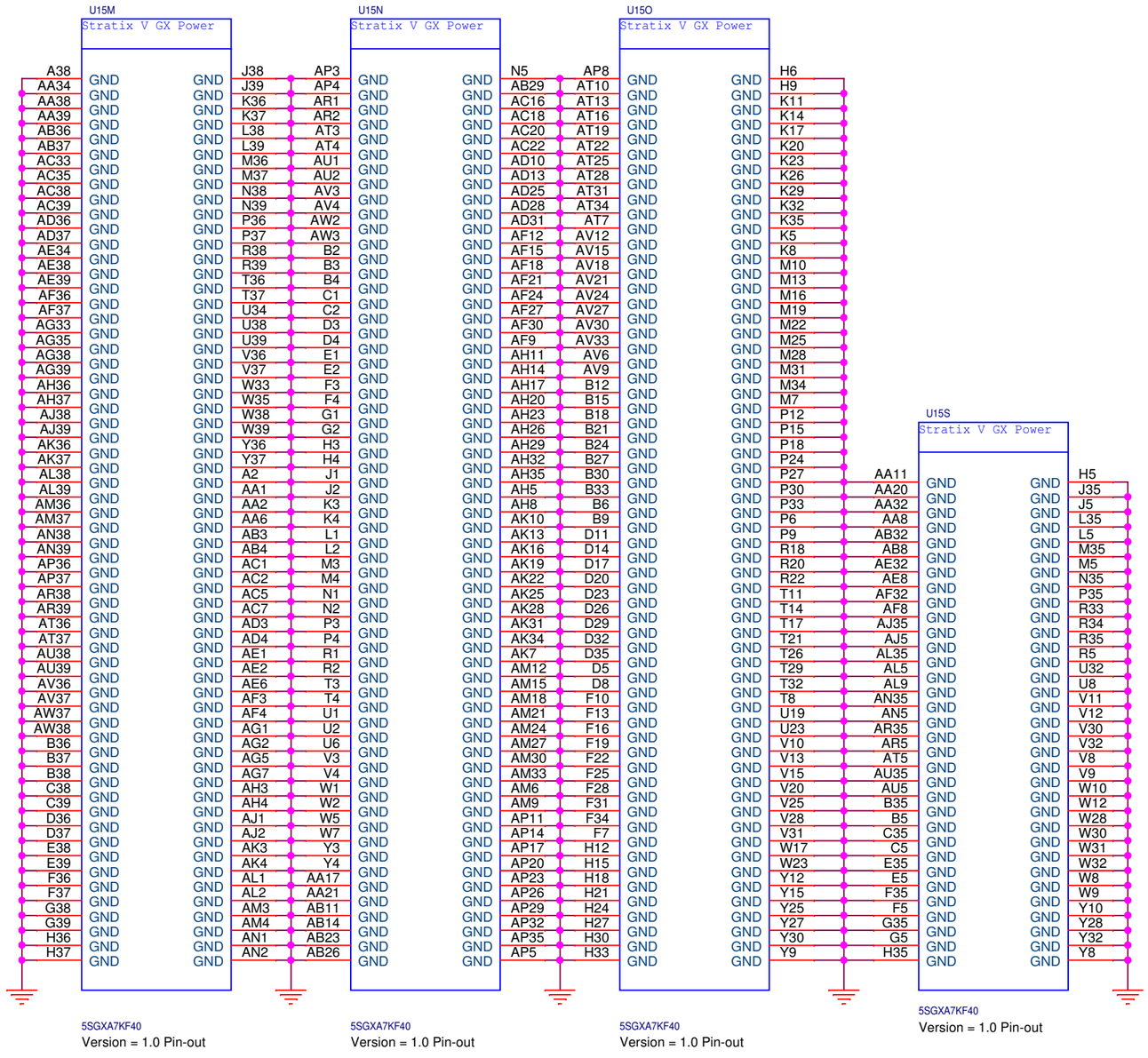
Size: B	Document Number: 150-0320202-D1 (6XX-44143R)		Rev: D1.1
Date: Monday, June 03, 2013	Sheet 32 of 34		

Power 8 - Stratix V GX Ground



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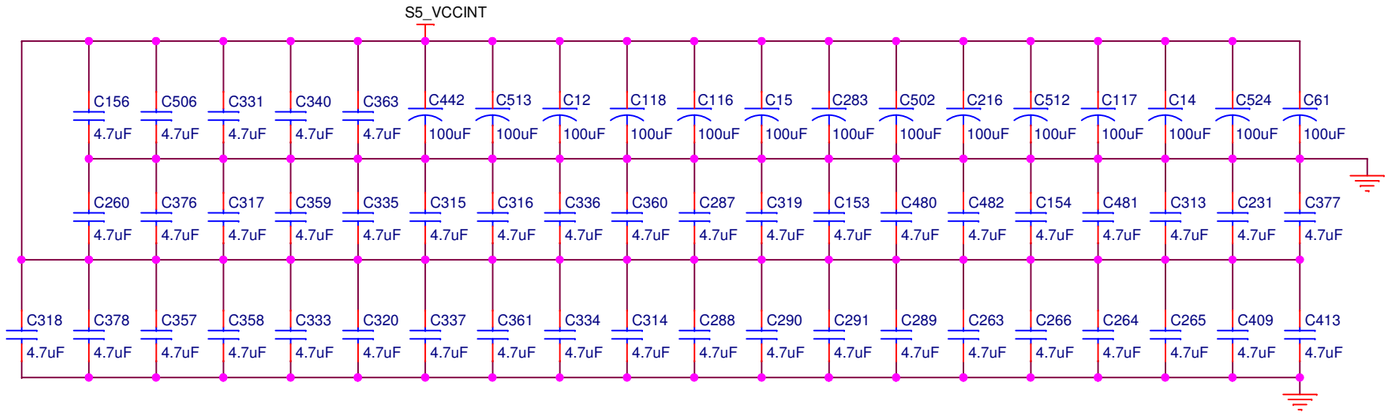
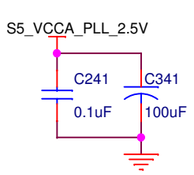
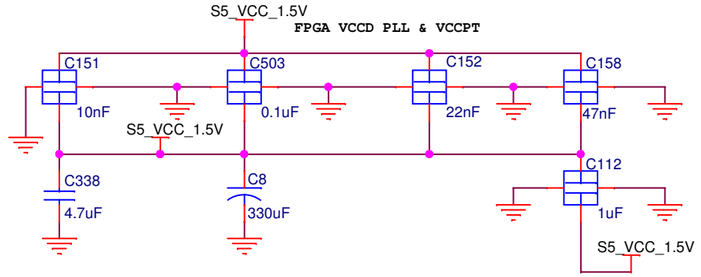
Title: Stratix V GX FPGA Development Kit Board		
Size: B	Document Number: 150-0320202-D1 (6XX-44143R)	Rev: D1.1
Date: Monday, June 03, 2013	Sheet 33 of 34	

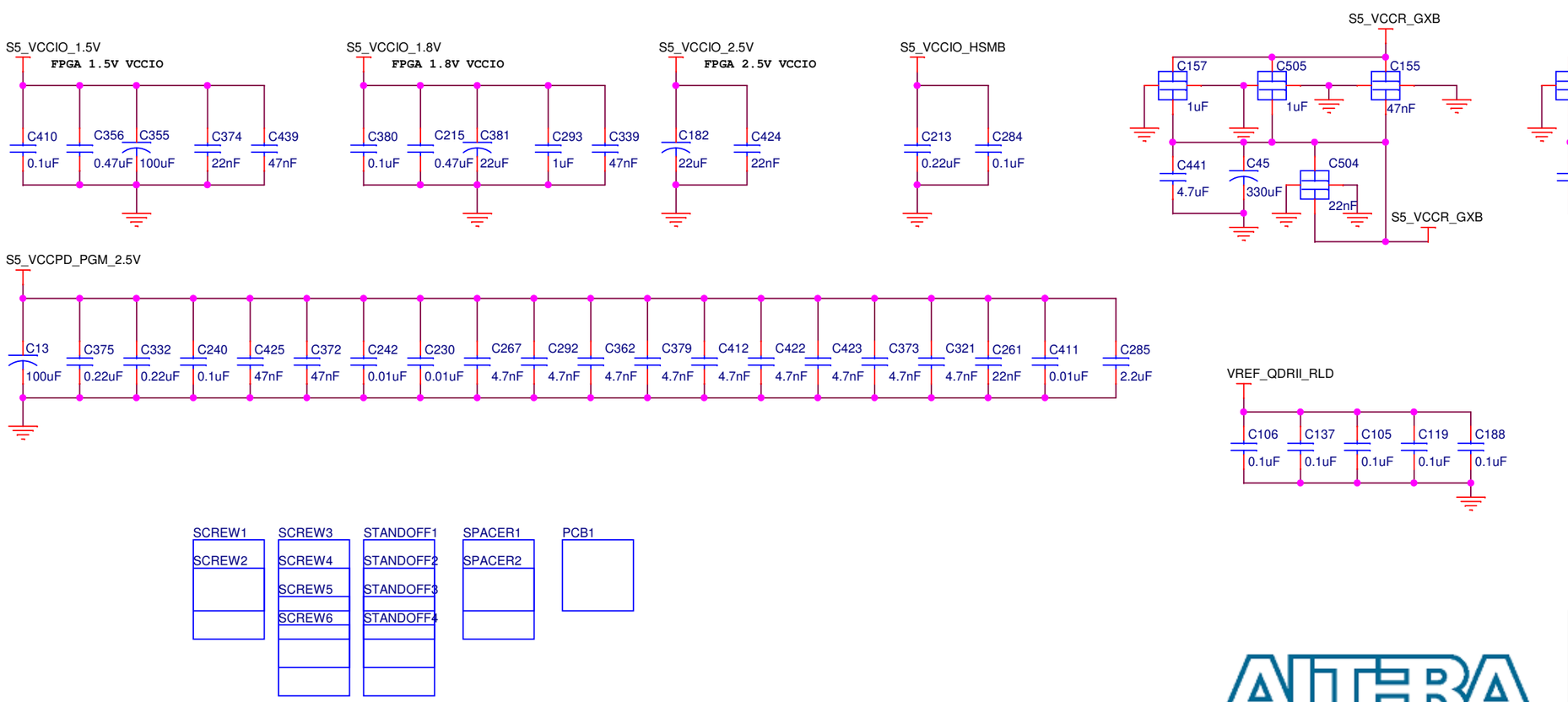
Decoupling

Place 6 vias minimum on each X2Y cap.









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Title: **Stratix V GX FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320202-D1 (6XX-44143R)	D1.1

Date: Monday, June 03, 2013 Sheet 34 of 34