AD9889B to ADV7513 Changeover Guide

SECTION 1: INTRODUCTION

The Analog Devices AD9889B HDMI Transmitter has been successfully employed for over 5 years now, but now we recommend to those considering this to upgrade to the ADV7513. The ADV7513 is the equal or better in every metric of the AD9889B. Listed below are a few of the improvements that the ADV7513 offers to the HDMI Tx designer:

- Internal HDCP keys (similar to AD9389B)
- Integrated CEC with 3 message buffer
- HDMI v1.4a features supported
    - 3D video
    - Advanced Colorimetry
        - xYCC601
        - Adobe RGB
        - Adobe YCC601
    - High bit-rate (HBR) audio
- Improved PLL for elimination of frequency 'gear' hopping in automatic mode.
- Expanded lower temperature range -25C to +85C

The following will need to be considered when converting from the AD9889B to the ADV7513:

- General board layout such as video data, audio data and TMDS lines are very similar
- Not pin-for-pin drop in mode compatibility
- ADV7513 offered in 64-lead LQFP package (12mm x 12mm outer pin dimension)
    - AD9889B offered in 3 packages: 80-lead LQFP (16mm x 16mm), 64-lead LFCSP (9mm x 9mm) and a 76-ball BGA (6mm x 6mm).
- Use of CEC requires a clock source – typically a 12MHz crystal oscillator
- 3.3V supply required for internal memory as well as for CEC support
- No EEPROM required for HDCP keys; no MDA/MCL lines
- Ground on EPAD below package
- Lower power consumption: @1080p60, AD9889B = 504mW (max); ADV7513 = 326mW (max)
- The software driver is different for the ADV7513. However most calls will be similar or the same

1.1 Similar board layout

The data-bus input orientation as well as the TMDS output of the ADV7513 are generally compatible with those of the AD9889B. To illustrate this, the pin-outs for all packages are shown below. The pin-out for the ADV7513 is in ► Figure 1; pin-out for the AD9889B (LQFP) is in ► Figure 2; pin-out for the AD9889B (LFCSP) is in ► Figure 3; pin-out for the AD9889B (BGA) is in ► Figure 4.

Figure 1 **ADV7513 package layout – LQFP 64**

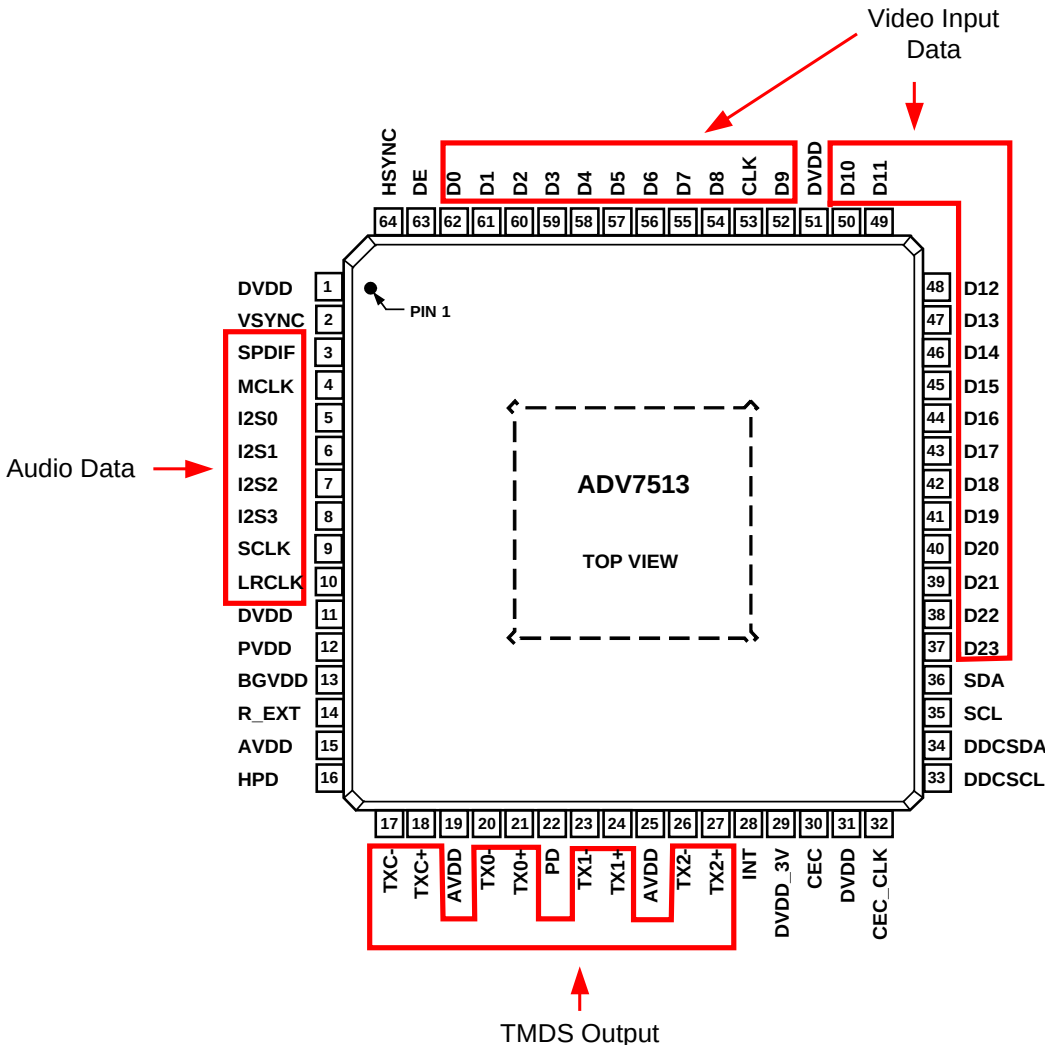


Figure 2 **AD9889B package layout LQFP**

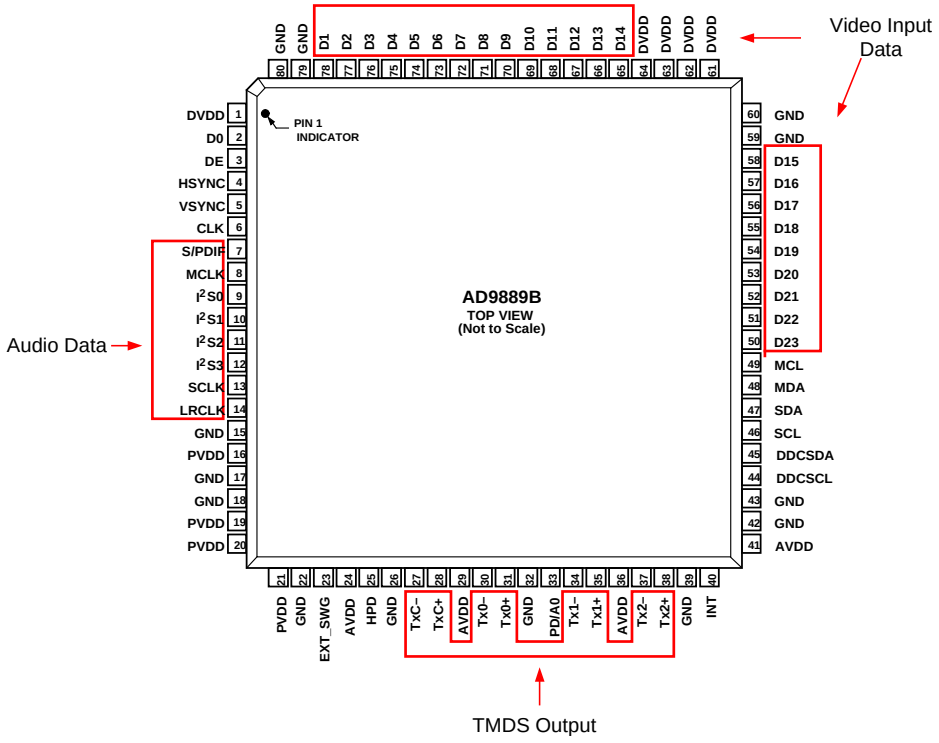


Figure 3 **AD9889B package layout LFCSP**

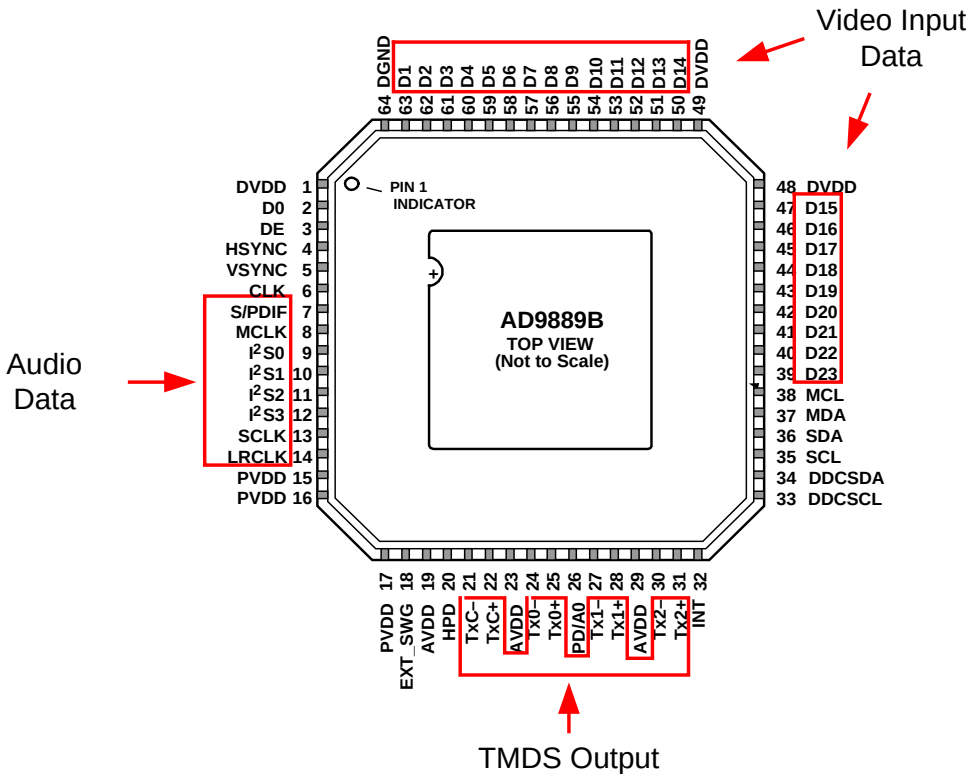
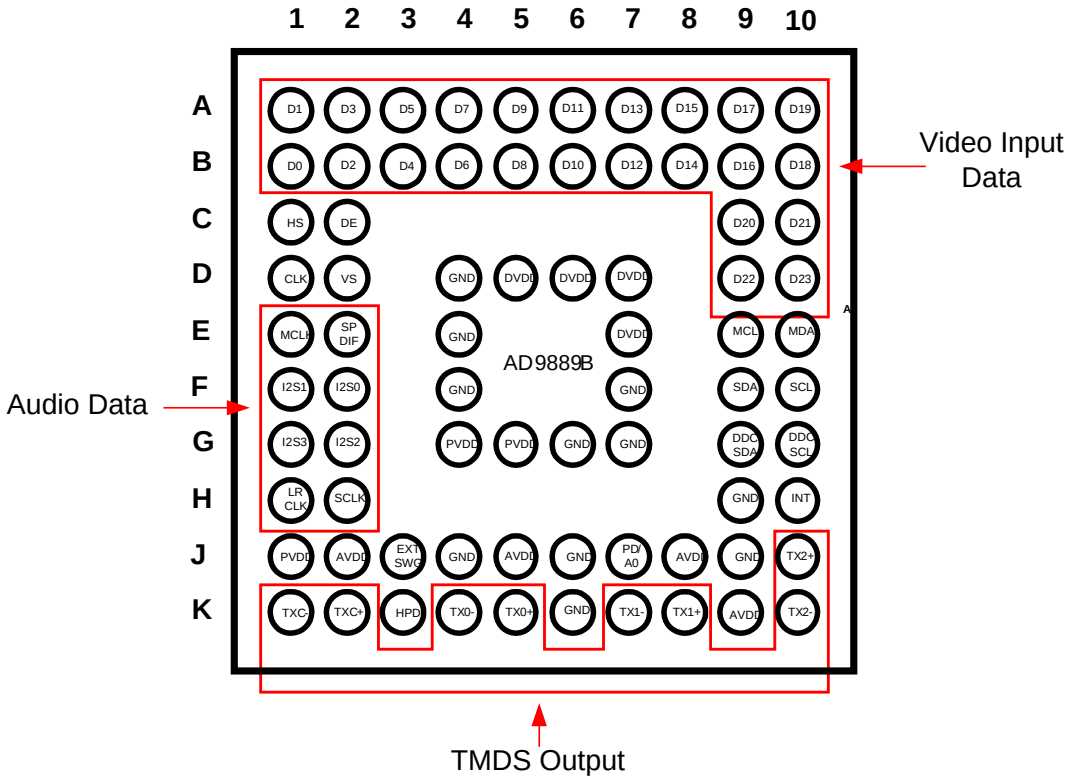


Figure 4 **AD9889B package layout BGA**



1.2 New Features:

ADV7513 has the following features that were not included in the AD9889B:

- CEC
- 3D
- Packet update - Pre-load
- HPD bypass

1.2.1 CEC – Consumer Electronics Control

The ADV7513 has a Consumer Electronic Control (CEC) receiver/transmitter function which captures and buffers three (3) command messages and passes them on to the host, reducing the real-time monitoring required by a host uP.

CEC is a single-wire, bidirectional interface intended to facilitate the control of any device on an HDMI network, as typified in ► Figure 5, with the remote control unit or on-device control buttons of any other device connected to the network. Defined as an optional feature in the HDMI specification, it is based on the AV Link function defined in the European SCART (Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs) specification. ► Table 1 describes some typical end-user CEC features.

Figure 5 Typical All-HDMI Home Theatre

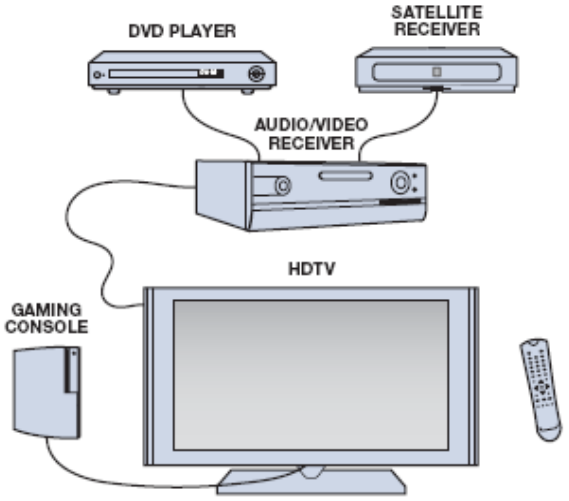


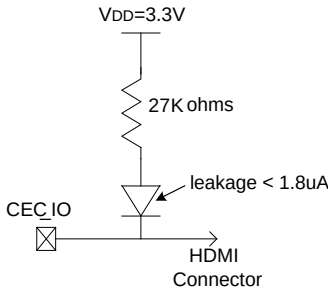
Table 1 Some useful "End-User" CEC Features:

Feature	Description
One-Touch Play	Pushing the "play" button commands a source to play and become the active video source for the TV.
Stand-By	Pushing the "power down" button of any active device commands all devices on the HDMI network to shut down.
One-Touch Record	Pushing the "record" button commands a recording device to power up and record the content currently displayed on the TV.

Many of these end-user features require sending multiple messages over the CEC bus such as "Active Source," and "Routing Change," which support the CEC feature "Routing Control." This feature allows a device to play and become the active source by switching the TV's source input. If the TV is displaying another source at the time this command is used, it may place the other source into "stand-by" mode, depending on the implementation.

Use of the CEC feature in the ADV7513 only requires 3 components: an external CMOS clock (from 3MHz – 100MHz – default is 12MHz), a low-leakage diode and a 27K ohm resistor pulled up to 3.3V.

Figure 6 CEC Connection to HDMI Connector



CEC programming registers and message storage are located in a separate map from the rest of the ADV7513. The address for this map is programmable (from the 'Main' map register 0xE1). Default map

address is 0x78. Registers 0x92 and 0x93 contain the interrupt enables and interrupt bits for the CEC wake-up opcodes. Registers 0x95 and 0x97 contain the interrupt enables and interrupt bits for CEC operation. The CEC Power Down bit is located in register 0xE2[0] of the 'Main' map.

1.2.2 3D Supported Formats

The ADV7513 has added 3D video support as defined in HDMI v 1.4a. If an HDMI source (TX) has 3D format capability, it must support at least one of the formats in Table 8-15 of the HDMI 1.4a specification. These primary 3D formats are shown in ► Table 2 as well as a number of secondary formats which are additionally supported. The ADV7513 does not detect the VIC for 3D formats, but the VIC in the AVI InfoFrame and the Vendor Specific InfoFrame must be setup. The VIC must be programmed using the manual pixel repeat mode by setting register 0x3B[6:5] to 0b10. The VIC should be programmed in register bits 0x3C[5:0]. A list of VICs can be found in the CEA861 document.

The Pixel repeat value should be set in register 0x3B[2:1] and register 0x3B[4:3]. This will be 0 for most formats; however, depending on the audio and video formats used, sometimes pixel repeat must be used to increase the bandwidth available for audio. Refer to the ADV7513 Programming Guide for further information.

Table 2 3D Format Support

HDMI 1.4a Primary 3D Mode Support			
Format (VIC)	**Frame Packing**	**Side-by-Side (Half)**	**Top-and-Bottom**
720p 60 (4)	No	Yes	Yes
720p 50 (19)	No	Yes	Yes
720p 24 (60)	No	Yes	Yes
720p 30 (62)	No	Yes	Yes
1080i 60 (5)	No	Yes	Yes
1080i 50 (20)	No	Yes	Yes
1080p 24 (32)	No	Yes	Yes
1080p 30 (34)	No	Yes	Yes
1080p 60 (16)	No	No	No
1080p 50 (31)	No	No	No

= Primary 3D Format

= Secondary 3D Format

1.2.3 Packet Update and Coefficient Pre-loading

1.2.3.1 *Packet Update*

The AD9889B supported packets for:

Packet	**Update bit**
AVI InfoFrame	Register 0x4A[6]
MPEG Infoframe	Register 0x3F[7]
GMP Packet	Register 0xBF[7]

Audio InfoFrame	Register 0x4A[5]
GC Packet	Register 0x4A[4]
SPD Packet	Register 0x1F[7]
ACP Packet	Register 0x5F[7]
ISRC1 Packet	Register 0x7F[7]
ISRC2 Packet	Register 0x9F[7]
Spare Packet 1	Register 0xDF[7]
Spare Packet 2	Register 0xFF[7]

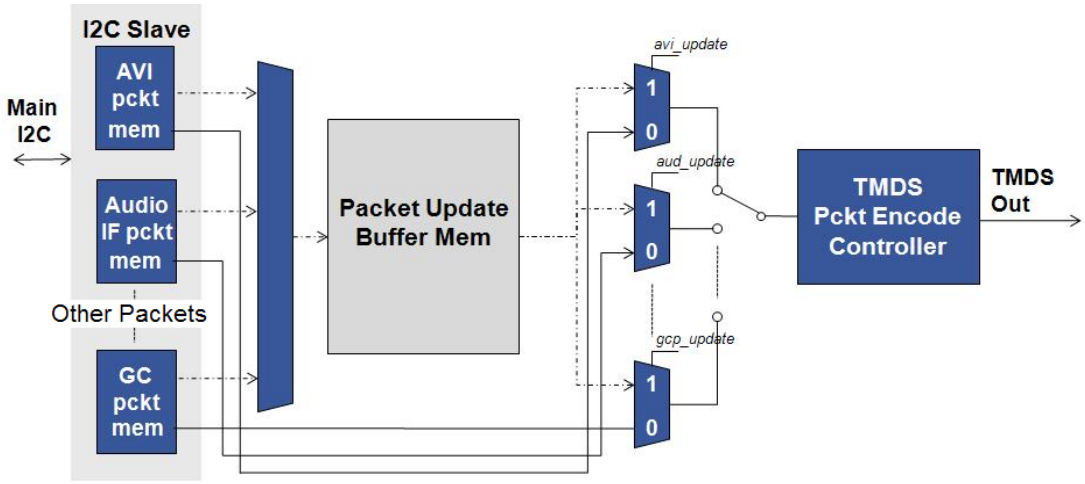
It was possible, however for these packets to be sent when only partially updated. This might have happened if insufficient time was available to update the packet before the blanking periods in which they are sent. To address this issue, the ADV7513 has incorporated a packet update feature which insures that the present contents of each packet continue to be sent until the update is complete. At that time, then the complete, updated contents are transmitted. Because there is only 1 packet update buffer (see ► Figure 7 below), only 1 packet may be updated at a time.

To avoid a partial update of the packets, the Packet Update feature should be used. By setting the Packet Update register bit (see column next to Packet list above) to '1', the current values will be stored and sent in the packets. The user should update the values then set the Packet Update register bit to '0' to begin sending the new packets.

When Packet Update is used, there are 3 steps for updating
a) Set Packet Update = 1 to buffer the packet contents
b) Set the new packet contents in I2C memory
c) Set Packet Update = 0 to enable the new packet contents at the next blanking period (Hsync or Vsync)

Updating then occurs during a blanking period which will guarantee complete frames to contain the same packet content.

Figure 7 Packet Update Block Diagram



1.2.3.2 *Coefficient Pre-loading*

The CSC (colorspace converter) can experience a similar issue to the packet update when changing the colorspace conversion coefficients. There are potentially 22 registers that may need to be changed from one colorspace definition to another. In order to prevent colorspace display errors due to incomplete update of the coefficients, an update feature (enabled with register 0x1A[5]) has been incorporated into this circuitry which allows the pre-loading of coefficients without enabling them to the matrix.

When Coefficient Update is used, there are 3 steps for updating
a) Set Coefficient Update = 1 to buffer the CSC Coefficients
b) Set the new CSC Coefficients
c) Set Coefficient Update = 0 to enable the new CSC Coefficients at the next Vsync rising edge

Updating then occurs during a Vsync blanking period which will guarantee complete frames to contain the same colorspace definition.

1.2.4 HPD Bypass

In the AD9889B, most registers were reset and the chip powered down upon loss of the HPD (Hot Plug Detect) signal. The loss of this signal indicates that no monitor is attached to the TX output. When this signal becomes active, the TX initiates a read of the monitor EDID and the driver configures the TX for the highest level of video supported. With the addition of a bypass for this signal, the initial debug and troubleshooting of a design is improved. HPD Bypass is enabled by setting register 0xD6[7:6] (Main map) to 0b11.

SECTION 2: ADV7513 REGISTER MAP

The ADV7513 contains four 256-byte register maps as described in the ADV7513 Programming Guide.
The four maps are:

Main Map	0x72 or 0x7A based upon whether the PD/AD pin (pin 22) is pulled low (0x72) or pulled high (0x7A)
EDID address	programmable and controlled in register 0x43, default address is 0x7E
Packet Memory	programmable and controlled in register 0x45, default address is 0x70.
CEC Memory	programmable and controlled in register 0xE1, default address is 0x78.

Highlighted sections indicate differences from the AD9889B Main Map

ADV7513 Main Register Map

Address (Main)	Type	Bits	Default Value	Register Name	Function
0x00	RO	[7:0]	00010000	Chip Revision	Revision of the chip
0x01	R/W	[19:0]	****0000	N	20 bit N used with CTS to regenerate the audio clock in the receiver.
0x02			00000000		
0x03			00000000		
0x04	RO	[7:4]	0000****	SPDIF Sampling Frequency	SPDIF Sampling Frequency from SPDIF Channel Status. 0000 = 44.1 kHz 0001 = N/A 0010 = 48.0 kHz 0011 = 32.0 kHz 0100 = N/A 0101 = N/A 0110 = N/A 0111 = N/A 1000 = 88.2 kHz 1001 = N/A 1010 = 96.0 kHz 1011 = N/A 1100 = 176.4 kHz 1101 = N/A 1110 = 192.0 kHz 1111 = N/A
0x04	RO	[19:0]	****0000	CTS Automatic	Cycle Time Stamp (CTS) Automatically Generated This 20 bit value is used in the receiver with the N value to regenerate an audio clock. For remaining bits see 0x05 and 0x06.
0x05			00000000		
0x06			00000000		
0x07	R/W	[19:0]	****0000	CTS Manual	Cycle Time Stamp (CTS) Manually Entered This 20 bit value is used in the receiver with the N value to regenerate an audio clock. For remaining bits see 0x08 and 0x09.
0x08			00000000		
0x09			00000000		
0x0A	R/W	[7]	0*******	CTS Select	CTS Source Select. 0 = CTS Automatic 1 = CTS Manual
		[6:4]	*000****	Audio Select	Audio Select

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					All others invalid 000 = I2S 001 = SPDIF 010 = N/A 011 = High Bit Rate (HBR Audio) 100 = N/A 101 = N/A 110 = N/A 111 = N/A
		[3:2]	****00**	Audio Mode	Mode Selection for Audio Select HBR (Audio Select register bits (0x0A[6:4] = 0b011)) 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding
		[1:0]	******01	MCLK Ratio	MCLK Ratio The ratio between the audio sampling frequency and the clock described using N and CTS 00 = 128xfs 01 = 256xfs 10 = 384xfs 11 = 512xfs
0x0B	R/W	[7]	0*******	SPDIF Enable	Enable or Disable SPDIF receiver – was 0x44[7] 0 = disable 1 = Enabled
		[6]	*0******	Audio Clock Polarity	SPDIF MCLK, I2S SCLK Polarity Indicates edge where input data is latched 0 = rising edge 1 = falling edge
		[5]	**0*****	MCLK Enable	MCLK Enable 0 = MCLK internally generated 1 = MCLK is available
		[4:1]	***0111*	Fixed	Must be set to Default Value
0x0C	R/W	[7]	1*******	Audio Sampling Frequency Select	Select source of audio sampling frequency for pixel repeat and I2S mode 4 0 = use sampling frequency from I2S stream 1 = use sampling frequency from I2C register
		[6]	*0******	Channel Status Override	Source of channel status bits when using I2S mode 4 0 = use channel status bits from I2S stream 1 = use channel status bits from I2C registers
		[5]	**1*****	I2S3 Enable	I2S3 enable for the 4 I2S pins. 0 = Disabled 1 = Enabled
		[4]	***1****	I2S2 Enable	I2S2 enable for the 4 I2S pins.

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					0 = Disabled 1 = Enabled
		[3]	****1***	I2S1 Enable	I2S1 enable for the 4 I2S pins. 0 = Disabled 1 = Enabled
		[2]	*****1**	I2S0 Enable	I2S0 enable for the 4 I2S pins. 0 = Disabled 1 = Enabled
		[1:0]	******00	I2S Format	I2S Format 00 = Standard I2S mode 01 = right justified mode 10 = left justified mode 11 = AES3 direct mode
0x0D	R/W	[4:0]	***11000	I2S Bit Width	I2S Bit Width For right justified audio only. Default is 24. Not valid for widths greater than 24.
0x0E	R/W	[5:3]	**000***	Subpacket 0 L Source	Source of sub packet 0, left channel
		[2:0]	*****001	Subpacket 0 R Source	Source of sub packet 0, right channel
0x0F	R/W	[5:3]	**010***	Subpacket 1 L Source	Source of sub packet 1, left channel
		[2:0]	*****011	Subpacket 1 R Source	Source of sub packet 1, right channel
0x10	R/W	[5:3]	**100***	Subpacket 2 L Source	Source of sub packet 2, left channel
		[2:0]	*****101	Subpacket 2 R Source	Source of sub packet 2, right channel
0x11	R/W	[5:3]	**110***	Subpacket 3 L Source	Source of sub packet 3, left channel
		[2:0]	*****111	Subpacket 3 R Source	Source of sub packet 3, right channel
0x12	R/W	[7]	0*******	Audio Sample Word (CS bit 1)	Audio Sample Word 0 = Audio sample word represents linear PCM samples 1 = Audio sample word used for other purposes Consumer Use Should be 0 for HDMI
		[6]	*0******	Consumer Use (CS bit 0)	Consumer Use Bit 0 = Audio sample word represents linear PCM samples 1 = Audio sample word used for other purposes
		[5]	**0*****	Copyright Bit (CS bit 2)	Copy Right Bit 0 = Copyright Protected

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					1 = Not Copyright Protected
		[4:2]	***000**	Additional Audio Info (CS bits 5-3)	Additional information for Channel Status Bits 000 = 2 audio channels w/o pre-emphasis 001 = 2 audio channels with 50/15uS pre-emphasis 010 = Fixed 011 = Fixed
		[1:0]	******00	Audio Clock Accuracy (CS bits 29-28)	Audio Clock Accuracy 00 = level II - normal accuracy +/-1000 X 10-6 10 = level III -variable pitch shifted clock 01 = level I - high accuracy +/-50 X 10-6 11 = Fixed
0x13	R/W	[7:0]	00000000	Category Code (CS bits 15-8)	Channel Status Category Code
0x14	R/W	[7:4]	0000****	Source Number (CS bits 19-16)	Channel Status Source Number
		[3:0]	****0000	Word Length (CS bits 35-32)	Audio Word Length 0000 = Not Specified 0001 = Not Specified 0010 = 16 Bits 0011 = 20 Bits 0100 = 18 Bits 0101 = 22 Bits 0110 = No description 0111 = No description 1000 = 19 Bits 1001 = 23 Bits 1010 = 20 Bits 1011 = 24 Bits 1100 = 17 Bits 1101 = 21 Bits 1110 = No description 1111 = No description
0x15	R/W	[7:4]	0000****	I2S Sampling Frequency (CS bits 27-24)	Sampling frequency for I2S audio. This information is used by both the audio Rx and the pixel repetition. 0000 = 44.1 kHz 0001 = Do not use 0010 = 48.0 kHz 0011 = 32.0 kHz 0100 = Do not use 0101 = Do not use 0110 = Do not use 0111 = Do not use 1000 = 88.2 kHz 1001 = HBR Audio 1010 = 96.0 kHz 1011 = Do not use 1100 = 176.4 kHz

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					1101 = Do not use 1110 = 192.0 kHz 1111 = Do not use
		[3:0]	****0000	Input ID	Input Video Format See ►**Error! Reference source not found.** to ►**Error! Reference source not found.** 0000 = 24 bit RGB 4:4:4 or YCbCr 4:4:4 (separate syncs) 0001 = 16, 20, 24 bit YCbCr 4:2:2 (separate syncs) 0010 = 16, 20, 24 bit YCbCr 4:2:2 (embedded syncs) 0011 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, separate syncs) 0100 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, embedded syncs) 0101 = 12, 15, 16 bit RGB 4:4:4 or YCbCr (DDR with separate syncs) (0xD0[3:2] must be set to 2'b11) 0110 = 8,10,12 bit YCbCr 4:2:2 (DDR with separate syncs) (0xD0[3:2] must be set to 2'b11) 0111 = 8, 10, 12 bit YCbCr 4:2:2 (DDR separate syncs) (0xD0[3:2] must be set to 2'b11) 1000 = 8, 10, 12 bit YCbCr 4:2:2 (DDR embedded syncs) (0xD0[3:2] must be set to 2'b11)
0x16	R/W	[7]	0*******	Output Format	Output Format 0 = 4:4:4 1 = 4:2:2
		[6]	*0******	Reserved	Must be set to Default Value
		[5:4]	**00****	Color Depth	Color Depth for Input Video Data. See ►**Error! Reference source not found.** to ►**Error! Reference source not found.** 00 = invalid 10 = 12 bit 01 = 10 bit 11 = 8 bit
		[3:2]	****00**	Input Style	Styles refer to the input pin assignments. See ►**Error! Reference source not found.** to ►**Error! Reference source not found.** 00 = Not Valid 01 = style 2 10 = style 1 11 = style 3
		[1]	******0*	DDR Input Edge	Video data input edge selection. Defines the first half of pixel data clocking edge. Used for DDR Input ID 5 and 6 only. 0 = falling edge 1 = rising edge
		[0]	*******0	Output Colorspace for Black Image	Input Color Space Selection Used for Black Image and Range Clipping 0 = RGB

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					1 = YCbCr
0x17	R/W	[7]	0*******	Fixed	Must be set to Default Value
		[6]	*0******	Vsync Polarity	Case 1: Sync Adjustment Register (0x41[1]) = 1 0 = high polarity 1 = low polarity Case 2: Sync Adjustment Register (0x41[1]) = 0 0 = sync polarity pass through 1 = sync polarity invert 0 = High polarity 1 = Low polarity
		[5]	**0*****	Hsync Polarity	Hsync polarity for Embedded Sync Decoder and Sync Adjustment Case 1: Sync Adjustment Register (0x41[1]) = 1 0 = high polarity 1 = low polarity Case 2: Sync Adjustment Register (0x41[1]) = 0 0 = sync polarity pass through 1 = sync polarity invert 0 = High polarity 1 = Low polarity
		[4:3]	***00***	Reserved @ 00b	Must be set to Default Value
		[2]	*****0**	4:2:2 to 4:4:4 Interpolation Style	4:2:2 to 4:4:4 Up Conversion Method 0 = use zero order interpolation 1 = use first order interpolation
		[1]	******0*	Aspect Ratio	Aspect ratio of input video. 0 = 4:3 Aspect Ratio 1 = 16:9 Aspect Ratio
		[0]	*******0	DE Generator Enable	Enable DE Generator See registers 0x35 - 0x3A 0 = Disabled 1 = Enabled
0x18	R/W	[7]	0*******	CSC Enable	Color Space Converter Enable was 0x3B[0] 0 = CSC Disabled 1 = CSC Enabled
		[6:5]	*10*****	CSC Scaling Factor	Color Space Converter Mode – was 0x17[4:3] Sets the fixed point position of the CSC coefficients. Including the a4, b4, c4, offsets. 00 = +/- 1.0, -4096 - 4095 01 = +/- 2.0, -8192 - 8190 10 = +/- 4.0, -16384 - 16380 11 = +/- 4.0, -16384 - 16380
0x18	R/W	[12:0]	***00110	A1 (CSC)	Color space Converter (CSC) coefficient for equations: **Equation 1: CSC Channel A**
0x19			01100010		

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					$Out\_A = \left[In\_A\frac{A1}{4096} + In\_B\frac{A2}{4096} + In\_C\frac{A3}{4096} + A4 \right] 2^{CSC\_Mode}$ **Equation 2: CSC Channel B** $Out\_B = \left[In\_A\frac{B1}{4096} + In\_B\frac{B2}{4096} + In\_C\frac{B3}{4096} + B4 \right] 2^{CSC\_Mode}$ **Equation 3: CSC Channel C** $Out\_C = \left[In\_A\frac{C1}{4096} + In\_B\frac{C2}{4096} + In\_C\frac{C3}{4096} + C4 \right] 2^{CSC\_Mode}$
0x1A	R/W	[5]	**0*****	Coefficient Update	There are 2 methods to update the coefficients. Method 1: When Coefficient Update is always 0, the coefficient will be updated directly. Method 2: When Coefficient Update is used, there are 3 steps for updating a) Set Coefficient Update = 1 to buffer the CSC Coefficients b) Set the new CSC Coefficients c) Set Coefficient Updated = 0 to enable the new CSC Coefficients at the next Vsync rising edge 0 = Update Complete 1 = Allow CSC Update
0x1A	R/W	[12:0]	***00100	A2 (CSC)	See description for registers 0x18 and 0x19
0x1B			10101000		
0x1C	R/W	[12:0]	***00000	A3 (CSC)	See description for registers 0x18 and 0x19
0x1D			00000000		
0x1E	R/W	[12:0]	***11100	A4 (CSC)	See description for registers 0x18 and 0x19
0x1F			10000100		
0x20	R/W	[12:0]	***11100	B1 (CSC)	See description for registers 0x18 and 0x19
0x21			10111111		
0x22	R/W	[12:0]	***00100	B2 (CSC)	See description for registers 0x18 and 0x19
0x23			10101000		
0x24	R/W	[12:0]	***11110	B3 (CSC)	See description for registers 0x18 and 0x19
0x25			01110000		
0x26	R/W	[12:0]	***00010	B4 (CSC)	See description for registers 0x18 and 0x19
0x27			00011110		
0x28	R/W	[12:0]	***00000	C1 (CSC)	See description for registers 0x18 and 0x19
0x29			00000000		

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
0x2A	R/W	[12:0]	***00100	C2 (CSC)	See description for registers 0x18 and 0x19
0x2B			10101000		
0x2C	R/W	[12:0]	***01000	C3 (CSC)	See description for registers 0x18 and 0x19
0x2D			00010010		
0x2E	R/W	[12:0]	***11011	C4 (CSC)	See description for registers 0x18 and 0x19
0x2F			10101100		
0x30	R/W	[9:0]	00000000	Hsync Placement (Embedded Sync Decoder)	Embedded Sync Decoder Hsync Placement (In Pixels)
0x31			00******		
0x31	R/W	[9:0]	**000000	Hsync Duration (Embedded Sync Decoder)	Embedded Sync Decoder Hsync Duration (In Pixels)
0x32			0000****		
0x32	R/W	[9:0]	****0000	Vsync Placement (Embedded Sync Decoder)	Embedded Sync Decoder Vsync Placement (In Hsyncs)
0x33			000000**		
0x33	R/W	[9:0]	******00	Vsync Duration (Embedded Sync Decoder)	Embedded Sync Decoder Vsync Duration (In Hsyncs)
0x34			00000000		
0x35	R/W	[9:0]	00000000	Hsync Delay (DE Generator)	DE Generation Hsync Delay (In Pixels)
0x36			00******		
0x36	R/W	[5:0]	**000000	Vsync Delay (DE Generator)	DE Generation. (In Hsyncs)
0x37	R/W	[7:5]	000*****	Interlace Offset (DE Generator)	Interlace Offset For DE Generation Sets the difference (in hsyncs) in field length between field 0 and field 1
0x37	R/W	[11:0]	***00000	Active Width (DE Generator)	DE Generation Active Width (In Pixels)
0x38			0000000*		
0x39	R/W	[11:0]	00000000	Active Height (DE Generator)	DE Generation Active Height (In Lines)
0x3A			0000****		
0x3B	R/W	[7]	1*******	Reserved @ 1b	Must be set to Default Value
		[6:5]	*00*****	PR Mode	Pixel Repetition Mode Selection. Set to b00 unless non-standard video is supported. 00 = auto mode 01 = max mode 10 = manual mode 11 = manual mode
		[4:3]	***00***	PR PLL Manual	The clock multiplication of the input clock used in

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					pixel repetition. 00 = x1 01 = x2 10 = x4 11 = x4
		[2:1]	*****00*	PR Value Manual	User programmed pixel repetition number to send to Rx. 00 = x1 01 = x2 10 = x4 11 = x4
		[0]	*******0	Reserved @ 0b	Must be set to Default Value
0x3C	R/W	[5:0]	**000000	VIC Manual	User programmed VIC to sent to Rx (value defined in CEA861D) 000000 = VIC#0: VIC Unavailable 000001 = VIC#1: VGA (640x480) 4:3 000010 = VIC#2: 480p-60, 4:3 000011 = VIC#3: 480p-60, 16:9 000100 = VIC#4: 720p-60, 16:9 000101 = VIC#5: 1080i-60, 16:9 000110 = VIC#6: 480i-60, 2x Clk, 4:3 000111 = VIC#7: 480i-60, 2x Clk, 16:9 001000 = VIC#8: 240p-60, 2x Clk, 4:3 001001 = VIC#9: 240p-60, 2x Clk, 16:9 001010 = VIC#10: 480i-60, 4x Clk, 4:3 001011 = VIC#11: 480i-60, 4x Clk, 16:9 001100 = VIC#12: 240p-60, 8x Clk, 4:3 001101 = VIC#13: 240p-60, 8x Clk, 16:9 001110 = VIC#14: 480p-60, 2x Clk, 4:3 001111 = VIC#15: 480p-60, 2x Clk, 16:9 010000 = VIC#16: 1080p-60, 16:9 010001 = VIC#17: 576p-50, 4:3 010010 = VIC#18: 576p-50, 16:9 010011 = VIC#19: 720p-50, 16:9 010100 = VIC#20: 1080i-50, 16:9 010101 = VIC#21: 576i-50, 2x Clk, 4:3 010110 = VIC#22: 576i-50, 2x Clk, 16:9 010111 = VIC#23: 288p-50, 2x Clk, 4:3 011000 = VIC#24: 288p-50, 2x Clk, 16:9 011001 = VIC#25: 576i-50, 4x Clk, 4:3 011010 = VIC#26: 576i-50, 4x Clk, 16:9 011011 = VIC#27: 288p-50, 8x Clk, 4:3 011100 = VIC#28: 288p-50, 8x Clk, 16:9 011101 = VIC#29: 576p-50, 2x Clk, 4:3 011110 = VIC#30: 576p-50, 2x Clk, 16:9 011111 = VIC#31: 1080p-50, 16:9 100000 = VIC#32: 1080p-24, 16:9 100001 = VIC#33: 1080p-25, 16:9 100010 = VIC#34: 1080p-30, 16:9

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					100011 = VIC#35: 480p-60, 4x Clk, 4:3 100100 = VIC#36: 480p-60, 4x Clk, 16:9 100101 = VIC#37: 576p-50, 4x Clk, 4:3 100110 = VIC#38: 576p-50, 4x Clk, 16:9 100111 = VIC#39: 1080i-50, Alt Blanking 101000 = VIC#40: 1080i-100, 16:9 101001 = VIC#41: 720p-100, 16:9 101010 = VIC#42: 576p-100, 4:3 101011 = VIC#43: 576p-100, 16:9 101100 = VIC#44: 576i-100, 4:3 101101 = VIC#45: 576i-100, 16:9 101110 = VIC#46: 1080i-120, 16:9 101111 = VIC#47: 720p-120, 16:9 110000 = VIC#48: 480p-120, 4:3 110001 = VIC#49: 480p-120, 16:9 110010 = VIC#50: 480i-120, 4:3 110011 = VIC#51: 480i-120, 16:9 110100 = VIC#52: 576p-200, 4:3 110101 = VIC#53: 576p-200, 16:9 110110 = VIC#54: 576i-200, 4:3 110111 = VIC#55: 576i-200, 16:9 111000 = VIC#56: 480p-240, 4:3 111001 = VIC#57: 480p-240, 16:9 111010 = VIC#58: 480i-240, 4:3 111011 = VIC#59: 480i-240, 16:9 111100 = VIC#60: 60+ For Future Use
0x3D	RO	[7:6]	00******	Pixel Repeat to Rx	The actual pixel repetition sent to Rx 00 = x1 01 = x2 10 = x4 11 = x4
		[5:0]	**000000	VIC to Rx	VIC sent to HDMI Rx and Used in the AVI InfoFrame Status (value defined in CEA861D) 000000 = VIC#0: VIC Unavailable 000001 = VIC#1: VGA (640x480) 4:3 000010 = VIC#2: 480p-60, 4:3 000011 = VIC#3: 480p-60, 16:9 000100 = VIC#4: 720p-60, 16:9 000101 = VIC#5: 1080i-60, 16:9 000110 = VIC#6: 480i-60, 2x Clk, 4:3 000111 = VIC#7: 480i-60, 2x Clk, 16:9 001000 = VIC#8: 240p-60, 2x Clk, 4:3 001001 = VIC#9: 240p-60, 2x Clk, 16:9 001010 = VIC#10: 480i-60, 4x Clk, 4:3 001011 = VIC#11: 480i-60, 4x Clk, 16:9 001100 = VIC#12: 240p-60, 8x Clk, 4:3 001101 = VIC#13: 240p-60, 8x Clk, 16:9 001110 = VIC#14: 480p-60, 2x Clk, 4:3 001111 = VIC#15: 480p-60, 2x Clk, 16:9 010000 = VIC#16: 1080p-60, 16:9

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					010001 = VIC#17: 576p-50, 4:3 010010 = VIC#18: 576p-50, 16:9 010011 = VIC#19: 720p-50, 16:9 010100 = VIC#20: 1080i-50, 16:9 010101 = VIC#21: 576i-50, 2x Clk, 4:3 010110 = VIC#22: 576i-50, 2x Clk, 16:9 010111 = VIC#23: 288p-50, 2x Clk, 4:3 011000 = VIC#24: 288p-50, 2x Clk, 16:9 011001 = VIC#25: 576i-50, 4x Clk, 4:3 011010 = VIC#26: 576i-50, 4x Clk, 16:9 011011 = VIC#27: 288p-50, 8x Clk, 4:3 011100 = VIC#28: 288p-50, 8x Clk, 16:9 011101 = VIC#29: 576p-50, 2x Clk, 4:3 011110 = VIC#30: 576p-50, 2x Clk, 16:9 011111 = VIC#31: 1080p-50, 16:9 100000 = VIC#32: 1080p-24, 16:9 100001 = VIC#33: 1080p-25, 16:9 100010 = VIC#34: 1080p-30, 16:9 100011 = VIC#35: 480p-60, 4x Clk, 4:3 100100 = VIC#36: 480p-60, 4x Clk, 16:9 100101 = VIC#37: 576p-50, 4x Clk, 4:3 100110 = VIC#38: 576p-50, 4x Clk, 16:9 100111 = VIC#39: 1080i-50, Alt Blanking 101000 = VIC#40: 1080i-100, 16:9 101001 = VIC#41: 720p-100, 16:9 101010 = VIC#42: 576p-100, 4:3 101011 = VIC#43: 576p-100, 16:9 101100 = VIC#44: 576i-100, 4:3 101101 = VIC#45: 576i-100, 16:9 101110 = VIC#46: 1080i-120, 16:9 101111 = VIC#47: 720p-120, 16:9 110000 = VIC#48: 480p-120, 4:3 110001 = VIC#49: 480p-120, 16:9 110010 = VIC#50: 480i-120, 4:3 110011 = VIC#51: 480i-120, 16:9 110100 = VIC#52: 576p-200, 4:3 110101 = VIC#53: 576p-200, 16:9 110110 = VIC#54: 576i-200, 4:3 110111 = VIC#55: 576i-200, 16:9 111000 = VIC#56: 480p-240, 4:3 111001 = VIC#57: 480p-240, 16:9 111010 = VIC#58: 480i-240, 4:3 111011 = VIC#59: 480i-240, 16:9 111100 = VIC#60: 60+ For Future Use
0x3E	RO	[7:2]	000000**	Actual VIC Detected	Input VIC Detected (value defined in CEA861D) 000000 = VIC#0: VIC Unavailable 000001 = VIC#1: VGA (640x480) 4:3 000010 = VIC#2: 480p-60, 4:3 000011 = VIC#3: 480p-60, 16:9 000100 = VIC#4: 720p-60, 16:9

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					000101 = VIC#5: 1080i-60, 16:9 000110 = VIC#6: 480i-60, 2x Clk, 4:3 000111 = VIC#7: 480i-60, 2x Clk, 16:9 001000 = VIC#8: 240p-60, 2x Clk, 4:3 001001 = VIC#9: 240p-60, 2x Clk, 16:9 001010 = VIC#10: 480i-60, 4x Clk, 4:3 001011 = VIC#11: 480i-60, 4x Clk, 16:9 001100 = VIC#12: 240p-60, 8x Clk, 4:3 001101 = VIC#13: 240p-60, 8x Clk, 16:9 001110 = VIC#14: 480p-60, 2x Clk, 4:3 001111 = VIC#15: 480p-60, 2x Clk, 16:9 010000 = VIC#16: 1080p-60, 16:9 010001 = VIC#17: 576p-50, 4:3 010010 = VIC#18: 576p-50, 16:9 010011 = VIC#19: 720p-50, 16:9 010100 = VIC#20: 1080i-50, 16:9 010101 = VIC#21: 576i-50, 2x Clk, 4:3 010110 = VIC#22: 576i-50, 2x Clk, 16:9 010111 = VIC#23: 288p-50, 2x Clk, 4:3 011000 = VIC#24: 288p-50, 2x Clk, 16:9 011001 = VIC#25: 576i-50, 4x Clk, 4:3 011010 = VIC#26: 576i-50, 4x Clk, 16:9 011011 = VIC#27: 288p-50, 8x Clk, 4:3 011100 = VIC#28: 288p-50, 8x Clk, 16:9 011101 = VIC#29: 576p-50, 2x Clk, 4:3 011110 = VIC#30: 576p-50, 2x Clk, 16:9 011111 = VIC#31: 1080p-50, 16:9 100000 = VIC#32: 1080p-24, 16:9 100001 = VIC#33: 1080p-25, 16:9 100010 = VIC#34: 1080p-30, 16:9 100011 = VIC#35: 480p-60, 4x Clk, 4:3 100100 = VIC#36: 480p-60, 4x Clk, 16:9 100101 = VIC#37: 576p-50, 4x Clk, 4:3 100110 = VIC#38: 576p-50, 4x Clk, 16:9 100111 = VIC#39: 1080i-50, Alt Blanking 101000 = VIC#40: 1080i-100, 16:9 101001 = VIC#41: 720p-100, 16:9 101010 = VIC#42: 576p-100, 4:3 101011 = VIC#43: 576p-100, 16:9 101100 = VIC#44: 576i-100, 4:3 101101 = VIC#45: 576i-100, 16:9 101110 = VIC#46: 1080i-120, 16:9 101111 = VIC#47: 720p-120, 16:9 110000 = VIC#48: 480p-120, 4:3 110001 = VIC#49: 480p-120, 16:9 110010 = VIC#50: 480i-120, 4:3 110011 = VIC#51: 480i-120, 16:9 110100 = VIC#52: 576p-200, 4:3 110101 = VIC#53: 576p-200, 16:9 110110 = VIC#54: 576i-200, 4:3 110111 = VIC#55: 576i-200, 16:9

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					111000 = VIC#56: 480p-240, 4:3 111001 = VIC#57: 480p-240, 16:9 111010 = VIC#58: 480i-240, 4:3 111011 = VIC#59: 480i-240, 16:9 111100 = VIC#60: 60+ For Future Use
0x3F	RO	[7:5]	000*****	Auxiliary VIC Detected	This register is for video input formats that are not inside the 861D table. 000 = Set by Register 0x3E 001 = 240p Not Active 010 = 576i not active 011 = 288p not active 100 = 480i active 101 = 240p active 110 = 576i active 111 = 288p active
		[4:3]	***00***	Progressive Mode Information	Information about 240p and 288p modes. Case 1: 240p 01 = 262 lines 10 = 263 lines Case 2: 288p 01 = 312 lines 10 = 313 lines 11 = 314 lines
0x40	R/W	[7]	0*******	GC Packet Enable	GC Packet Enable 0 = GC Packet Disabled 1 = GC Packet Enabled
		[6]	*0******	SPD Packet Enabled	SPD Packet Enable 0 = Disabled 1 = Enabled
		[5]	**0*****	MPEG Packet Enabled	MPEG Packet Enable 0 = Disabled 1 = enable
		[4]	***0****	ACP Packet Enable	ACP Packet Enable 0 = Disabled 1 = Enabled
		[3]	****0***	ISRC Packet Enable	ISRC Packet Enable 0 = Disabled 1 = Enabled
		[2]	*****0**	GM Packet Enable	GM Packet Enable 0 = Disabled 1 = Enabled
		[1]	******0*	Spare Packet 2 Enable	Spare Packet 2 Enable 0 = Disabled 1 = Enabled
		[0]	*******0	Spare Packet 1	Spare Packet 1 Enable

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
				Enable	0 = Disabled 1 = Enabled
0x41	R/W	[6]	*1******	POWER DOWN	Main Power Down 0 = all circuits powered up 1 = power down whole chip, except I2C, HPD interrupt, Monitor Sense interrupt, CEC 0 = Normal Operation 1 = ADV7513 Powered Down
		[5]	**0*****	Fixed	Must be set to Default Value
		[4]	***1****	Reserved @ 1b	Must be set to Default Value
		[3:2]	****00**	Fixed	Must be set to Default Value
		[1]	******0*	Sync Adjustment Enable	Enable Sync Adjustment 0 = Disabled 1 = Enabled
		[0]	*******0	Fixed	Must be set to Default Value
0x42	RO	[7]	1*******	Power Down Polarity	Polarity for chip pin 0 = active low 1 = active high
		[6]	*0******	HPD State	State of HDMI sink 0 = Hot Plug Detect state is low 1 = Hot Plug Detect state is high
		[5]	**0*****	Monitor Sense State	state of the monitor connection 0 = HDMI clock termination not detected 1 = HDMI clock termination detected
		[4]	***1****	Fixed	
		[3]	****0***	I2S 32 Bit Mode Detect	I2S Mode Detections Shows the number of SCLK periods per LRCLK period. 0 = 32 bit mode detected 1 = 64 bit mode detected
		[2]	*****0**	Fixed	
0x43	R/W	[7:0]	01111110	EDID Memory Address	The I2C address for EDID memory
0x44	R/W	[7]	0*******	Reserved @ 0b	Must be set to Default Value
		[6]	*1******	N CTS Packet Enable	N CTS Packet Enable 0 = Disabled 1 = Enabled
		[5]	**1*****	Audio Sample Packet Enable	Audio Sample Packet Enable 0 = Disabled 1 = Enabled
		[4]	***1****	AVI InfoFrame	AVI InfoFrame Enable

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
				Enable	0 = Disabled 1 = Enabled
		[3]	****1***	Audio InfoFrame Enable	Audio InfoFrame Enable 0 = Disabled 1 = Enabled
		[2:1]	*****00*	Fixed	Must be set to Default Value
		[0]	*******1	Packet Read Mode	Packet Memory Read Mode 0=Allow user to read from packet memory 1=Allow HDMI logic to read from packet memory
0x45	R/W	[7:0]	01110000	Packet Memory I2C Map Address	I2C address for the packet memory was 0xCF
0x46	R/W	[7:0]	00000000	Fixed	Must be set to Default Value
0x47	R/W	[7]	0*******	Fixed	Must be set to Default Value
		[6]	*0******	PaPb Sync	For HBR audio this syncs PaPb with sub packet 0.
		[5]	**0*****	Audio Sample 3 Valid	Indicates when sub packet 3 has invalid data.
		[4]	***0*****	Audio Sample 2 Valid	Indicates when sub packet 2 has invalid data.
		[3]	****0***	Audio Sample 1 Valid	Indicates when sub packet 1 has invalid data.
		[2]	*****0**	Audio Sample 0 Valid	Indicates when sub packet 0 has invalid data.
0x48	R/W	[7]	0*******	Reserved	Must be set to Default Value
		[6]	*0******	Video Input Bus Reverse	Bit order reverse for input signals. 0 = Normal Bus Order 1 = LSB .... MSB Reverse Bus Order
		[5]	**0*****	Fixed	Must be default for proper operation
		[4:3]	***00***	Video Input Justification	Bit Justification for YCbCr 4:2:2 modes. See ►**Error! Reference source not found.** to ►**Error! Reference source not found.** 00 = evenly distributed 01 = right justified 10 = left justified 11 = Invalid
0x49	R/W	[7:2]	101010**	Reserved	Must be default for proper operation
0x4A	R/W	[7]	1*******	Auto Checksum Enable	Auto Checksum Enable 0 = Use checksum from registers

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					1 = Use automatically generated checksum
		[6]	*0******	AVI Packet Update	AVI Packet Update: Before updating the AVI Packet using I2C set to '1' to continue sending the current values. 0 = AVI Packet I2C update inactive 1 = AVI Packet I2C update active
		[5]	**0*****	Audio InfoFrame Packet Update	Audio InfoFrame Packet Update: Before updating the Audio InfoFrame Packet using I2C set to '1' to continue sending the current values. 0 = Audio InfoFrame Packet I2C update inactive 1 = Audio InfoFrame Packet I2C update active
		[4]	***0****	GC Packet Update	GC Packet Update: Before updating the GC Packet using I2C set to '1' to continue sending the current values. 0 = GC Packet I2C update inactive 1 = GC Packet I2C update active
0x4B	R/W	[7]	0*******	Clear AV Mute	Clear Audio Video Mute was 0x45[7] 0 = Clear 1 = Set clear av mute
		[6]	*0******	Set AV Mute	Set Audio Video Mute was 0x45[6] 0 = Clear 1 = Set av mute.
0x4C	R/W	[7:0]	00000000	Fixed	Must be default for proper operation
0x4D	R/W	[7:0]	00000000	GC Byte 2	Reserved in CEA 861D
0x4E	R/W	[7:0]	00000000	GC Byte 3	Reserved in CEA 861D
0x4F	R/W	[7:0]	00000000	GC Byte 4	Reserved in CEA 861D
0x50	R/W	[7:0]	00000000	GC Byte 5	Reserved in CEA 861D
0x51	R/W	[7:0]	00000000	GC Byte 6	Reserved in CEA 861D
0x52	R/W	[2:0]	*****010	AVI InfoFrame Version	Version of AVI InfoFrame Should be left default
0x53	R/W	[4:0]	***01101	AVI InfoFrame Length	Length of packet body, excluding checksum
0x54	R/W	[7:0]	00000000	AVI InfoFrame Checksum	Checksum for AVI IF. Only used in manual checksum mode..
0x55	R/W	[7]	0*******	AVI Byte 1 bit 7	Reserved per HDMI spec. - set to 0
		[6:5]	*00*****	Y1Y0 (AVI InfoFrame)	Output format - this should be written when 0x16[7:6] is written. was 0x45[5:4] 00 = RGB 01 = YCbCr 4:2:2 10 = YCbCr 4:4:4 11 = reserved

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
		[4]	***0****	Active Format Information Status (AVI InfoFrame)	Active Format Information Present was 0x45[3] 0 = no data 1 = Active format Information valid
		[3:2]	****00**	Bar Information (AVI InfoFrame)	B[1:0] was 0x45[2:1] 00 = invalid bar 01 = vertical 10 = horizontal 11 = Both
		[1:0]	******00	Scan Information (AVI InfoFrame)	S[1:0] was 0x46[7:6] 00 = no data 01 = TV 10 = PC 11 = None
0x56	R/W	[7:6]	00******	Colorimetry (AVI InfoFrame)	C[1:0] was 0x46[5:4] 00 = no data 01 = ITU601 10 = ITU709 11 = Extended Colorimetry Information Valid (Indicated in register 0x57[6:4])
		[5:4]	**00****	Picture Aspect Ratio (AVI InfoFrame)	M[1:0] was 0x46[3:2] 00 = no data 01 = 4:3 10 = 16:9 11 = None
		[3:0]	****0000	Active Format Aspect Ratio (AVI InfoFrame)	R[3:0] was 0x47[7:4] 1000 = Same as Aspect Ratio 1001 = 4:3 (center) 1010 = 16:9 (center) 1011 = 14:9 (center)
0x57	R/W	[7]	0*******	ITC	IT Content was 0xCD[6] 0 = None 1 = IT content available in register bits 0x59[5:4]
		[6:4]	*000****	EC[2:0]	E[2:0] All other values reserved per HDMI 1.4A Specification 000 = xvYCC 601 001 =xvYCC 709 010 = sYCC601 011 = AdobeYCC601 100 = AdobeRGB
		[3:2]	****00**	Q[1:0]	RGB Quantization range 00 = default range 01 = limited range 10 = full range 11 = reserved
		[1:0]	******00	Non-Uniform	SC[1:0] was 0x46[1:0]

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
				Picture Scaling (AVI InfoFrame)	00 = unknown 01 = scaling in Horizontal direction 10 = scaling in Vertical direction 11 = scaling in Both H & V directions
0x58	R/W	[7]	0*******	Byte 4 Bit 7 (AVI InfoFrame)	Reserved per HDMI spec. Set to '0'. was 0xCD[7]
0x59	R/W	[7:4]	0000****	Byte 5 bit [7:4] (AVI InfoFrame)	YQ[1:0] 00 = Limited Range 01 = Full Range 10 = Reserved 11 = Reserved
0x5A	R/W	[7:0]	00000000	Active Line Start LSB (AVI InfoFrame)	Active Line Start was 0x48 This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar.
0x5B	R/W	[7:0]	00000000	Active Line Start MSB (AVI InfoFrame)	Active Line Start was 0x49 This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar.
0x5C	R/W	[7:0]	00000000	Active Line End LSB (AVI InfoFrame)	Active Line End was 0x4A This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar.
0x5D	R/W	[7:0]	00000000	Active Line End MSB (AVI InfoFrame)	Active Line End was 0x4B This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar.
0x5E	R/W	[7:0]	00000000	Active Pixel Start LSB (AVI InfoFrame)	Active Pixel Start This represents the last pixel in a vertical pillar-bar at the left side of the picture. If 0, there is no left bar.
0x5F	R/W	[7:0]	00000000	Active Pixel Start MSB (AVI InfoFrame)	Active Pixel Start This represents the last pixel in a vertical pillar-bar at the left side of the picture. If 0, there is no left bar.
0x60	R/W	[7:0]	00000000	Active Pixel End LSB (AVI InfoFrame)	Active Pixel End This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar.
0x61	R/W	[7:0]	00000000	Active Pixel End MSB (AVI InfoFrame)	Active Pixel End was 0x4F This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar.
0x62	R/W	[7:0]	00000000	Byte 14 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x63	R/W	[7:0]	00000000	Byte 15 (AVI	Reserved per HDMI spec. Set to 0x00.

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
				InfoFrame)	
0x64	R/W	[7:0]	00000000	Byte 16 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x65	R/W	[7:0]	00000000	Byte 17 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x66	R/W	[7:0]	00000000	Byte 18 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x67	R/W	[7:0]	00000000	Byte 19 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x68	R/W	[7:0]	00000000	Byte 20 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x69	R/W	[7:0]	00000000	Byte 21 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6A	R/W	[7:0]	00000000	Byte 22 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6B	R/W	[7:0]	00000000	Byte 23 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6C	R/W	[7:0]	00000000	Byte 24 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6D	R/W	[7:0]	00000000	Byte 25 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6E	R/W	[7:0]	00000000	Byte 26 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6F	R/W	[7:0]	00000000	Byte 27 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x70	R/W	[2:0]	*****001	Audio InfoFrame Version	Version of Audio InfoFrame Set to 001 as defined in CEA861
0x71	R/W	[4:0]	***01010	Audio InfoFrame Length	Length of packet body, excluding checksum
0x72	R/W	[7:0]	00000000	Audio InfoFrame Checksum	Checksum for AVI InfoFrame packet. Only used in manual checksum mode.
0x73	R/W	[7:4]	0000****	Coding Type (Audio InfoFrame)	Coding Type Set to 0 according to HDMI Specification 1.4a
		[3]	****0***	Byte 1 bit 3 (Audio InfoFrame)	Fixed per HDMI spec. Set to 0.
		[2:0]	*****000	CC (Audio	Channel Count was 0x50[7:5]

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
				InfoFrame)	000 = Refer to Stream Header 001 = 2 channels 010 = 3 channels 011 = 4 channels 100 = 5 channels 101 = 6 channels 110 = 7 channels 111 = 8 channels
0x74	R/W	[7:5]	000*****	Byte 2 bit [7:5] (Audio InfoFrame)	Fixed per HDMI spec. Set to 0.
		[4:2]	***000**	Sampling Frequency (Audio InfoFrame)	Audio sampling frequency. Should be 0, except for SACD.
		[1:0]	******00	Sample Size (Audio InfoFrame)	Set to 0
0x75	R/W	[7:0]	00000000	Byte 3 (Audio InfoFrame)	Set to 0
0x76	R/W	[7:0]	00000000	Speaker Mapping (Audio InfoFrame)	CA[7:0] Speaker mapping or placement for up to 2 channels. was 0x51
0x77	R/W	[7]	0*******	DM_INH (Audio InfoFrame)	Down-mix Inhibit was 0x50[4]
		[6:3]	*0000***	Level Shift (Audio InfoFrame)	LSV[3:0]-Audio Level Shift Values With Attenuation Information was 0x50[3:0] 0000 = 0dB attenuation 0001 = 1dB attenuation 0010 = 2dB attenuation 0011 = 3dB attenuation 0100 = 4dB attenuation 0101 = 5dB attenuation 0110 = 6dB attenuation 0111 = 7dB attenuation 1000 = 8dB attenuation 1001 = 9dB attenuation 1010 = 10dB attenuation 1011 = 11dB attenuation 1100 = 12dB attenuation 1101 = 13dB attenuation 1110 = 14dB attenuation 1111 = 15dB attenuation
		[2]	*****0**	Byte 5 bit [2]	Fixed per HDMI spec
		[1:0]	******00	LFEPBL[1:0]	Set to 0b0,ow Frequency Effect Playback Level

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					00 = No information 01 = 0 dB playback 10 = +10 dB playback 11 = Reserved
0x78	R/W	[7:0]	00000000	Byte 6 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'
0x79	R/W	[7:0]	00000000	Byte 7 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'
0x7A	R/W	[7:0]	00000000	Byte 8 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'
0x7B	R/W	[7:0]	00000000	Byte 9 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'
0x7C	R/W	[7:0]	00000000	Byte 10 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'
0x92	R/W	[7]	0*******	Wake Up Opcode 1 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 1 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[6]	*0******	Wake Up Opcode 2 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 2 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[5]	**0*****	Wake Up Opcode 3 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 3 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[4]	***0****	Wake Up Opcode 4 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 4 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[3]	****0***	Wake Up Opcode 5 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 5 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[2]	*****0**	Wake Up	CEC Wake Up Code Interrupt Enable

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
				Opcode 6 Interrupt Enable	Enable interrupt detecting Wake Up Opcode 6 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[1]	******0*	Wake Up Opcode 7 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 7 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[0]	*******0	Wake Up Opcode 8 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 8 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
0x93	R/W	[7]	0*******	Wake Up Opcode 1 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 8 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[6]	*0******	Wake Up Opcode 2 Interrupt	CEC Wake Up Code Interrupt Enable interrupt detecting Wake Up Opcode 7 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[5]	**0*****	Wake Up Opcode 3 Interrupt	CEC Wake Up Code Interrupt Enable Interrupt detecting Wake Up Opcode 6 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[4]	***0****	Wake Up Opcode 4 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 5 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[3]	****0***	Wake Up Opcode 5 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 4 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[2]	*****0**	Wake Up Opcode 6 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 3 in CEC message

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					0= No Interrupt Detected 1 = Interrupt Detected
		[1]	******0*	Wake Up Opcode 7 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 2 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[0]	*******0	Wake Up Opcode 8 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 1 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
0x94	R/W	[7]	1*******	HPD Interrupt Enable	HPD Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[6]	*1******	Monitor Sense Interrupt Enable	Monitor Sense Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[5]	**0*****	Vsync Interrupt Enable	Vsync Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[4]	***0****	Audio FIFO Full Interrupt Enable	Audio FIFO Full Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[3]	****0***	Fixed	Must be set to Default Value
		[2]	*****0**	EDID Ready Interrupt Enable	EDID Ready Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[1]	******0*	HDCP Authenticated Interrupt Enable	HDCP Authenticated Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[0]	*******0	Fixed	Must be set to Default Value
0x95	R/W	[7]	0*******	DDC Controller Error Interrupt Enable	DDC Controller Error Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[6]	*0******	BKSV Flag Interrupt Enable	BKSV Flag Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[5]	**0*****	Tx Ready Interrupt Enable	CEC Tx Ready Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[4]	***0****	Tx Arbitration Lost Interrupt	CEC Tx Arbitration Lost Interrupt Enable 0 = interrupt disabled

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
				Enable	1 = interrupt enabled
		[3]	****0***	Tx Retry Timeout Interrupt Enable	CEC Tx Retry Timeout Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[2]	*****0**	Rx Ready 3 Interrupt Enable	CEC Rx Ready 3 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[1]	******0*	Rx Ready 2 Interrupt Enable	CEC Rx Ready 2 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[0]	*******0	Rx Ready 1 Interrupt Enable	CEC Rx Ready 1 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x96	R/W	[7]	0*******	HPD Interrupt	HPD Interrupt 0 = no interrupt detected 1 = interrupt detected
		[6]	*0******	Monitor Sense Interrupt	Monitor Sense Interrupt 0 = no interrupt detected 1 = interrupt detected
		[5]	**0*****	Vsync Interrupt	Vsync Interrupt 0 = no interrupt detected 1 = interrupt detected
		[4]	***0****	Audio FIFO Full Interrupt	Audio FIFO Full Interrupt 0 = no interrupt detected 1 = interrupt detected
		[3]	****0***	Fixed	Must be set to Default Value
		[2]	*****0**	EDID Ready Interrupt	EDID Ready Interrupt 0 = no interrupt detected 1 = interrupt detected
		[1]	******0*	HDCP Authenticated	HDCP Authenticated 0 = no interrupt detected 1 = interrupt detected
		[0]	*******0	Fixed @ 0b	Reserved
0x97	R/W	[7]	0*******	DDC Controller Error Interrupt	DDC Controller Error Interrupt 0 = no interrupt detected 1 = interrupt detected
		[6]	*0******	BKSV Flag Interrupt	BKSV Flag Interrupt 0 = no interrupt detected 1 = interrupt detected
		[5]	**0*****	Tx Ready Interrupt	CEC Tx Ready Interrupt 0 = no interrupt detected 1 = interrupt detected

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
		[4]	***0****	Tx Arbitration Lost Interrupt	CEC Tx Arbitration Lost interrupt 0 = no interrupt detected 1 = interrupt detected
		[3]	****0***	Tx Retry Timeout Interrupt	CEC Tx Retry Timeout interrupt 0 = no interrupt detected 1 = interrupt detected
		[2]	*****0**	Rx Ready 3 Interrupt	CEC Rx Ready 3 Interrupt 1 = interrupt detected for rx buffer 3 0 = no interrupt detected for buffer 3 1 = interrupt detected for buffer 3 0 = no interrupt detected for buffer 3
		[1]	******0*	Rx Ready 2 Interrupt	CEC Rx Ready 2 Interrupt 1 = interrupt detected for buffer 2 0 = no interrupt detected for buffer 2 1 = interrupt detected for buffer 2 0 = no interrupt detected for buffer 2
		[0]	*******0	Rx Ready 1 Interrupt	CEC Rx Ready 1 Interrupt 1 = interrupt detected for rx buffer 1 0 = no interrupt detected for buffer 1 1 = interrupt detected for buffer 1 0 = no interrupt detected for buffer 1
0x98	R/W	[7:0]	00001011	Fixed	Must be set to 0x03 for proper operation
0x99	R/W	[7:0]	00000010	Fixed	Must be set to Default Value
0x9A	R/W	[7:1]	0000000*	Fixed	Must be set to 0b1110000
0x9B	R/W	[5:0]	**011000	Fixed	Must be set to Default Value
0x9C	R/W	[7:0]	01011010	Fixed	Must be set to 0x30 for proper operation
0x9D	R/W	[7:4]	0110****	Fixed	Must be set to Default Value
		[3:2]	****00**	Input Pixel Clock Divide	Input Video CLK Divide 00 = Input Clock not Divided 01 = Input Clock Divided by 2 10 = Input Clock Divided by 4 11 = Invalid Setting
		[1:0]	******00	Fixed	Must be set to 1 for proper operation
0x9E	RO	[4]	***0****	PLL Lock Status	PLL Lock Status 0 = PLL Not Locked 1 = PLL Locked
		[3:0]	****0000	Fixed	
0x9F	R/W	[7:0]	00000000	Fixed	Must be set to Default Value
0xA0	RO	[7:0]	00000000	Fixed	
0xA1	R/W	[7]	0*******	Fixed	Must be set to Default Value
		[6]	*0******	Monitor Sense	Monitor Sense Power Down

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
				Power Down	0 = Monitor Sense monitoring enabled 1 = Monitor Sense monitoring disabled
		[5]	**0*****	Channel 0 Power Down	Channel 0 Power Down 0 = power up 1 = power down
		[4]	***0****	Channel 1 Power Down	Channel 1 Power Down 0 = power up 1 = power down
		[3]	****0***	Channel 2 Power Down	Channel 2 Power Down 0 = power up 1 = power down
		[2]	*****0**	Clock Driver Power Down	Clock Driver Power Down 0 = power up 1 = power down
0xA2	R/W	[7:0]	10000000	Fixed	Must be set to 0xA4 for proper operation
0xA3	R/W	[7:0]	10000000	Fixed	Must be set to 0xA4 for proper operation
0xA4	R/W	[7:1]	0000100*	Fixed	Must be set to Default Value
0xA5	R/W	[7:1]	0000010*	Fixed	Must be set to Default Value
0xA6	R/W	[7:0]	00000000	Fixed	Must be set to Default Value
0xA7	R/W	[7:0]	00000000	Fixed	Must be set to Default Value
0xA8	R/W	[7:0]	00000000	Fixed	Must be set to Default Value
0xA9	R/W	[7:1]	0000000*	Fixed	Must be set to Default Value
0xAA	R/W	[7:0]	00000000	Fixed	Must be set to Default Value
0xAB	R/W	[7:3]	01000***	Fixed	Must be set to Default Value
0xAC	RO	[7:0]	00000000	Fixed	
0xAD	RO	[7:0]	00000000	Fixed	
0xAE	RO	[7:5]	010*****	Fixed	
0xAF	R/W	[7]	0*******	HDCP Enable	Enable HDCP 0 = HDCP Disabled 1 = HDCP Encryption Enabled
		[6:5]	*00*****	Fixed	Must be set to Default Value
		[4]	***1****	Frame Encryption	Enable HDCP Frame Encryption 0 = Current Frame NOT HDCP Encrypted 1 = Current Frame HDCP Encrypted
		[3:2]	****01**	Fixed	Must be set to Default Value
		[1]	******0*	HDMI/DVI Mode Select	HDMI Mode 0 = DVI Mode 1 = HDMI Mode

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
		[0]	*******0	Fixed	Must be set to Default Value
0xB0	RO	[7:0]	00000000	Byte 0 of An or AKSV Byte 0	Byte 0 of An or AKSV Byte 0
0xB1	RO	[7:0]	00000000	Byte 1 of An or AKSV Byte 1	Byte 1 of An or AKSV Byte 1
0xB2	RO	[7:0]	00000000	Byte 2 of An or AKSV Byte 2	Byte 2 of An or AKSV Byte 2
0xB3	RO	[7:0]	00000000	Byte 3 of An or AKSV Byte 3	Byte 3 of An or AKSV Byte 3
0xB4	RO	[7:0]	00000000	Byte 4 of An or AKSV Byte 4	Byte 4 of An or AKSV Byte 4
0xB5	RO	[7:0]	00000000	Byte 5 of An	byte 5 of An
0xB6	RO	[7:0]	00000000	Byte 6 of An	byte 6 of An
0xB7	RO	[7:0]	00000000	Byte 7 of An	byte 7 of An
0xB8	RO	[7]	0*******	Fixed	
		[6]	*0******	HDCP Encryption Status	A/V content is being encrypted at present. 0 = A/V Not Encrypted 1 = A/V Encrypted
		[5]	**0*****	Fixed	
		[4]	***0****	Key Read Error	HDCP key reading error. 0 = Read HDCP Keys Correctly 1 = Errors Encountered Reading HDCP Keys
0xB9	R/W	[7:0]	00000000	Fixed	Must be set to Default Value
0xBA	R/W	[7:5]	000*****	Clock Delay	Programmable delay for input video clock. Default is 0. Should be set to 0b011 for no delay. 000 = -1.2ns 001 = -0.8ns 010 = -0.4ns 011 = no delay 100 = 0.4ns 101 = 0.8ns 110 = 1.2ns 111 = 1.6ns
		[4]	***1****	Fixed	Must be set to Default Value.
		[3]	****0***	Fixed	Must be set to Default Value
		[2]	*****0**	Display AKSV	Show AKSV in registers 0xB0 to 0xB4, Check R_i' before and after update, Must be set to Default 0 = Don't Show AKSV 1 = Show AKSV in 0xB0 - 0xB4
		[1]	******0*	R_i Two Point Check	R_i Two Point Check. Check R_i' before and after update. 0 = HDCP R_i standard

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					1 = enable HDCP Ri two point check
0xBB	R/W	[7:0]	00000000	Fixed	Must be set to Default Value
0xBC	RO	[7:0]	00000000	Fixed	
0xBD	RO	[7:0]	00000000	Fixed	
0xBE	RO	[7:0]	00000000	BCAPS	HDCP related register [7] Reserved, [6] Repeater, [5] BKSV FIFO ready, [4] Fast DDC Bus, [3:2] Reserved, [1] HDCP 1.1 Features, [0] Fast Re-Authentication.
0xBF	RO	[7:0]	00000000	BKSV Byte 0	Bksv read from Rx by the DDC Controller
0xC0	RO	[7:0]	00000000	BKSV Byte 1	Bksv read from Rx by the DDC Controller
0xC1	RO	[7:0]	00000000	BKSV Byte 2	Bksv read from Rx by the DDC Controller
0xC2	RO	[7:0]	00000000	BKSV Byte 3	Bksv read from Rx by the DDC Controller
0xC3	RO	[7:0]	00000000	BKSV Byte 4	Bksv read from Rx by the DDC Controller
0xC4	R/W	[7:0]	00000000	EDID Segment	Sets the E-DDC segment used by the EDID Fetch routine.
0xC5	R/W	[7:0]	00000000	Fixed	
0xC6	RO	[7:0]	00000000	Fixed	
0xC7	R/W	[7]	0*******	Fixed	Must be set to Default Value
	RO	[6:0]	*0000000	BKSV Count	BKSVs Available in Sink's BKSV FIFO
0xC8	RO	[7:4]	0000****	DDC Controller Error	DDC Controller Error Error code report when the DDC Controller Error Interrupt register 0x97[7] = 1
		[3:0]	****0000	DDC Controller State	DDC Controller State State of the controller used for HDCP debug purposes
0xC9	R/W	[4]	***0****	EDID Reread	Rereads current segment if toggled from 0 to 1 0 = disable 1 = enable
		[3:0]	****0011	EDID Tries	Maximum number of times that the EDID read will be attempted if unsuccessful.
0xCA	RO	[7:0]	00000000	HDCP BSTATUS[15:8]	BSTATUS information for HDCP [15:8]
0xCB	RO	[7:0]	00000000	HDCP BSTATUS[7:0]	BSTATUS information for HDCP [7:0]
0xCC	RO	[2:0]	*****000	Fixed	
0xCD	R/W	[7:4]	0000****	Fixed	Must be set to Default Value
0xCE	R/W	[7:0]	00000001	Fixed	Must be set to Default Value
0xCF	R/W	[7:0]	00000100	Fixed	Must be set to Default Value
0xD0	R/W	[7]	0*******	Enable DDR	Enable DDR Negative Edge Clock Delay Adjust

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
				Negative Edge CLK Delay	0 = Disable DDR Negative Edge CLK Delay 1 = Enable DDR Negative Edge CLK Delay
		[6:4]	*011****	DDR Negative Edge CLK Delay	Delay Adjust for the Input Video CLK Negative Edge for DDR Capture Should be set to 0b011 for No Delay 000 = -1200 ps 001 = -800 ps 010 = -400 ps 011 = no delay 100 = 400 ps 101 = 800 ps 110 = 1200 ps 111 = Invert CLK
		[3:2]	****00**	Sync Pulse Select	Case 1: Input ID register bits (0x15[3:0] = 5,6,7,8 Must be 0b11 Case 2: For input ID 1, 2, 3, 4 with 1X clock (See the Input Data Clock section, number 0). Can be set to any value. Case 3: For 2X or 4X input clock (See Input Data Clock section) with ID 1, 2, 3, 4. 1X generated clock synchronizes with. 00 = DE 01 = Hsync 10 = Vsync 11 = no sync pulse
		[1]	******0*	Timing Generation Sequence	Timing Generation Sequence 0 = sync adjustment then DE generation 1 = DE generation then sync adjustment
		[0]	*******0	Fixed	Must be set to Default Value
0xD1	R/W	[7:0]	11111111	Fixed	Must be set to Default Value
0xD2	R/W	[7:0]	10000000	Fixed	Must be set to Default Value
0xD3	R/W	[7:0]	10000000	Fixed	Must be set to Default Value
0xD4	R/W	[7:0]	10000000	Fixed	Must be set to Default Value
0xD5	R/W	[7:4]	0000****	Fixed	Must be set to Default Value
		[3:2]	****00**	High Refresh Rate Video	High Refresh Rate Video for VIC Detection 00 = normal refresh rate 01 = 2x refresh rate 10 = 4x refresh rate 11 = not valid
		[1]	******0*	YCbCr Code Shift	YCbCr Code Shift 0 = Code Shift Disabled 1 = Code Shift Enabled
		[0]	*******0	Black Image	Black Image 0 = Black Image Disabled

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
					1 = Black Image Enabled
0xD6	R/W	[7:6]	00******	HPD Control	HPD Control 00 = HPD is from both HPD pin or CDC HPD 01 = HPD is from CDC HPD 10 = HPD is from HPD pin 11 = HPD is always high
		[5]	**0*****	Fixed	Must be default for proper operation,
		[4]	***0****	TMDS CLK Soft Turn On	Soft TMDS Clock Turn On 0 = Soft Turn On Disabled 1 = Soft Turn On Enabled
		[3:1]	****000*	Fixed	Must be set to Default Value
		[0]	*******0	Audio and Video Input Gating	Audio and Video Input Gating 0 = video input and clock not gated 1 = video input and clock gated
0xD7 0xD8	R/W	[9:0]	00000000 00******	Hsync Placement (Sync Adjustment)	Hsync Front Porch (In Pixels)
0xD8 0xD9	R/W	[9:0]	**000000 0000****	Hsync Duration (Sync Adjustment)	Hsync Duration (In Pixels)
0xD9 0xDA	R/W	[9:0]	****0000 000000**	Vsync Placement (Sync Adjustment)	Vsync Front Porch (In Hsyncs)
0xDA 0xDB	R/W	[9:0]	******00 00000000	Vsync Duration (Sync Adjustment)	Vsync Duration (In Hsyncs)
0xDC	R/W	[7:5]	000*****	Offset (Sync Adjustment)	Offset for Sync Adjustment Vsync Placement Used only with interlaced formats (In Hsyncs)
0xDC 0xDD	R/W	[8:0]	***00000 0000****	Fixed	Must be default for proper operation.
0xDE	R/W	[7:4]	0001****	Fixed	Must be set to Default for proper operation
		[3]	****0***	TMDS Clock Inversion	TMDS Clock Inversion 0 = Normal TMDS Clock 1 = Inverted TMDS Clock
		[2:1]	*****000	Fixed	Must be set to Default for proper operation
0xDF	R/W	[7:0]	00000000	Fixed	Must be set to Default Value
0xE0	R/W	[7:0]	10000000	Fixed	Must be set to 0xD0 for proper operation
0xE1	R/W	[7:0]	01111000	CEC Map Address	CEC ID I2C address for CEC I2C control map
0xE2	R/W	[3:1]	****000*	Fixed	Must be set to Default Value

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
		[0]	*******0	CEC Power Down	CEC Power Down Power down CEC logic and reset CEC I2C map 0 = disabled 1 = enabled
0xE3	R/W	[7:1]	0000000*	Fixed	Must be set to Default Value
0xE4	R/W	[7:2]	011000**	Fixed	Must be set to Default Value
0xF5	RO	[7:0]	01110101	Chip ID High Byte	Chip ID High Byte
0xF6	RO	[7:0]	00010001	Chip ID Low Byte	Chip ID Low Byte
0xF7	RO	[7:4]	00000000	Reserved	
0xF9	R/W	[7:0]	01111100	Fixed	Must be set to 0x00 for proper operation
0xFA	R/W	[7:5]	000*****	Hsync Placement MSB (Embedded Sync Decoding)	This is the MSB for Hsync Placement of Embedded Sync Decoding. See Register 0x35[7:0].
		[4:2]	***000**	Hsync Placement MSB (Sync Adjustment)	This is the MSB for Hsync Placement of Sync Adjustment. See register 0xD7[7:0].
		[1:0]	******00	Fixed	Must be default for proper operation.
0xFB	R/W	[7]	0*******	Hsync Delay MSB (DE Generation)	MSB for Hsync delay of DE generation. See Register 0x35[7:0]
		[6:5]	*00*****	Vsync Delay MSB(DE Generation)	MSB for Vsync delay of DE generation. See Register bits 0x36[5:0]
		[4]	***0****	Width MSB (DE Generation)	MSB for DE width of DE generation. See Register bits 0x37[4:0]
		[3]	****0***	Height MSB (DE Generation)	MSB for height of DE generation. See Register bits 0x39[7:0]
		[2:1]	*****00*	Low Refresh Rate (VIC Detection)	Low Refresh Rate indicates if input video VS refresh rate if it is less than 50Hz 00 = not low refresh rate 01 = 24Hz 10 = 25Hz 11 = 30Hz
0xFC	R/W	[7:6]	00******	R_i Checking Frequency	R_i Checking Frequency 00 = 128 frames 01 = 64 frames 10 = 32 frames 11 = 16 frames

ADV7513 Main Register Map					
Address (Main)	**Type**	**Bits**	**Default Value**	**Register Name**	**Function**
		[5:3]	**000***	R_i Checking Position Delay	R_i Checking Position Delay in Units of Hsync 0 = no delay 1 = 8 Hsyncs 2 = 16 Hsyncs 3 = 32 Hsyncs 4 = 64 Hsyncs 5 = 128 Hsyncs 6 = 256 Hsyncs 7 = 512 Hsyncs
		[2:0]	*****000	BCAPS Read Delay	Delay Between Reading of BKSV and BCAPs 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms
0xFD	R/W	[7:5]	000*****	An Write Delay	Delay Between Reading of BCAPS and Writing of An 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms
		[4:2]	***000**	AKSV Write Delay	Delay Between Writing of An and Writing of AKSV 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms
0xFE	R/W	[7:5]	000*****	HDCP Start Delay	Delay Between Setting Enable HDCP Register 0xAF[7] = 1 and Reading of BKSV 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms