

Evaluation Board for 16-Bit, 1.2 MSPS CMOS, Sigma-Delta ADC

EVAL-AD7723CB

FEATURES

Full-Featured Evaluation Board for the AD7723 EVAL-CONTROL BOARD Compatible Stand Alone Capability Versatile Analog Signal Conditioning Circuit On-Board 2.5V Reference Crystal or CMOS Clock Oscillator Sampling Clock Serial or Parallel Conversion Data Interface Various Linking Options PC Software for Control and Data Analysis when used with EVAL-CONTROL BOARD Patch-work Area for User Expansion

INTRODUCTION

This Technical Note describes the evaluation board for the AD7723 16-Bit, 1.2MSPS, CMOS, Sigma-Delta ADC. The AD7723 evaluation board is designed to demonstrate the AD7723's performance and to provide a flexible interface for a variety of applications. Full data on the AD7723 is available in the AD7723 data sheet available from Analog Devices and should be consulted in conjunction with this Technical Note when using the Evaluation Board.

The AD7723 can operate with it's internal reference or the on-board AD780 precision bandgap reference can be used as an external reference. The analog input is conditioned using two AD8047 op-amps and this circuit can be configured to drive the AD7723 with complimentary signals. The EVAL-AD7723CB offers the flexibility of using an external sampling clock, an on-board CMOS clock oscillator, or the AD7723's crystal oscillator circuit. The board can be configured for either parallel or serial mode operation. In parallel mode, a 16-bit register, 74FCT162374, latches the conversion results to a 40 pin IDC connector (P5). In serial mode, the AD7723's serial interface signals are buffered with a 74FCT162244 and are available from a 20pin header (P4).

The EVAL-AD7723CB is ideal for use as a stand-alone unit or with the EVAL-CONTROL BOARD which is available from Analog Devices under the order entry "EVAL-CONTROL BOARD". Software is provided with the evaluation board package to allow analysis of the ADC's performance when using the EVAL-CONTROL BOARD. A 96-pin DIN connector (P1) interfaces the control board directly to the EVAL-AD7723CB.

The evaluation board uses extensive power and ground planes to minimize high frequency noise interference from the on-board clocks or any other source. The A_{GND} plane is kept separate from the D_{GND} plane and is joined under the AD7723. It is not recommended to connect the A_{GND} and D_{GND} planes elsewhere to avoid ground loop problems.

Figure. 1: FUNCTIONAL BLOCK DIAGRAM



REV. B

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Link and Switch Options

There are 37 link options which must be set for the required operating setup before using the evaluation board. The functions of these options are outlined below.

Link No. Function.

- J1 J2 Both of these links must be used together. These links are in place when using an AIN signal that is biased around 0V. These links are removed when using an AIN signal that is biased around 2.5V. The noise floor of high quality signal sources will, in most cases, be higher than the actual noise floor of the AD7723. For this reason, it is important that the signal source should be filtered using a bandpass or, for low frequency signals, a lowpass filter before being applied to the signal input of the evaluation board. For low frequency signal sources, a simple RC lowpass filter is sufficient to demonstrate the very low noise floor of the AD7723.
- J3 This link selects the clock source for the AD7723. In position "B" the on-board CMOS clock oscillator is selected. In position "A" an external sampling clock connected to SK2 is selected. To use the AD7723's crystal oscillator circuit, J3 must be removed and a 19.6MHz quartz crystal must be inserted in position Y1, two 33pF ceramic (0603 case) capacitors must be inserted in positions C13 & C14 and a $1M\Omega$ resistor (0805 case) must be inserted in position R12.
- J4 This link is used to select the source of the AV_{DD} power plane. In position "A" the AV_{DD} power plane is supplied from the external power terminal P2. In position "B" the AV_{DD} power plane is supplied by the EVAL-CONTROL BOARD.
- J5 This link is used to choose the power source for the positive supply pin of the op-amps (V+). When connecting to the EVAL-CONTROL BOARD, this link must be removed if using the AD8047 op-amps supplied with the evaluation board. In this case, an external +7.5V must be supplied via the "+VS" pin of P2. If using AD8041 op-amps (not supplied), this link can remain in place and the EVAL-CONTROL BOARD can supply the required +5V. Please note that using AD8041 op-amps causes a 2dB degradation in the ADC's SNR.
- J6 This link is used to choose the power source for the negative supply pin of the op-amps (V-). When connecting to the EVAL-CONTROL BOARD, this link must be removed if using the AD8047 op-amps supplied with the evaluation board. In this case, an external -2.5V must be supplied via the "-VS" pin of P2. If using AD8041 op-amps (not supplied), this link can remain in place and the EVAL-CONTROL BOARD supplies -5V. Although the EVAL-CONTROL BOARD supplies a dual 5V power supply to the AD7723 evaluation board, the AD8041 only requires a single 5V power supply when being used with the AD7723. Please note that using AD8041 op-amps causes a 2dB degradation in the ADC's SNR.
- J7 J8 J9 J10 These jumpers allow operation with either the internal reference of the AD7723 or the AD780 external reference. To operate the board using the internal reference of the AD7723, both links, J9 & J10 must be removed and both links, J7 & J8 must be in position "A". To operate the board using the external reference (AD780), both links, J9 & J10 must be in place, link J7 must be in position "B" and remove link J8.
- J11 This link selects the reference voltage output from the AD780 voltage reference. When this link is "in place" the AD780 produces a +3V reference. When this link is "removed" the AD780 produces a +2.5V reference.
- J12 J13 These links are used to select serial mode or parallel mode operation. J12 corresponds to MODE1 while J13 corresponds to MODE2. With a link in position "A", the corresponding MODE pin is tied to AV_{DD} while the pin is tied to GND when its corresponding link is in position "B". With both of these links in position "B" the AD7723 is configured for serial operation. Any other combination of these links selects parallel mode operation, the polarity of the MODE pins determining whether decimate by 16 mode, decimate by 32 mode (lowpass) or bandpass mode is selected. See Table 1 and Table 2 on the AD7723 Data Sheet for further information. Note that the AD7723 can only be used in decimate by 32 mode when interfaced to the EVAL-CONTROL BOARD and running on a 19.2 MHz clock. To interface the AD7723 to the EVAL-CONTROL BOARD in decimate by 16 mode, the master clock must be reduced to less than 16 MHz.
- J14 J15 These two links are used together in parallel mode operation to select how the conversion data is latched into the 16-bit data register (U7). With the header shunt installed in J15, conversion results are latched on the falling edge of the DRDY output. With the header shunt installed in J14, conversion results are latched on the rising edge of the DRDY output.
- J16 J17 In serial mode operation, J16 must be removed and J17 must be in position "B". In parallel mode operation, J16 is inserted and J17 is removed.

- J18-J23 Data pins DB0 to DB3, DB14 and DB15 are connected to links J18-J23. These pins are not used in serial mode and should be tied to GND. Inserting the links ties these pins to GND. In parallel mode, remove these links.
- J24 When "in place" this link bypasses the 50Ω resistor on the V_{IN} socket, SK1. A 440 Ω resistor is used between the AD8047 op-amp and the signal source. This 440 Ω resistor is made up using a 50 Ω resistor and a 390 Ω resistor. When a signal source which has a source resistance of 50 Ω is used, the 50 Ω present on the evaluation board can be bypassed.
- J25-J28 These links are connected to pins TSI/DB10, SLP/DB11, SLDR/DB12 and SCR/DB13. When the AD7723 is configured for parallel mode operation, links J25-J28 are removed as the above pins are configured as digital outputs. When the AD7723 is configured for serial mode operation, the above pins are configured as inputs and, are used to select the decimate by 16 mode, decimate by 32 mode (lowpass) or bandpass mode. With a link in position "A", the corresponding pin is tied to AV_{DD}. With a link is position "B" the corresponding pin is tied to GND. Consult Table 1 in the datasheet for information on selecting the different modes.
- J29 Set to position "A" to disable the on-chip crystal oscillator amplifier to allow use of an external clock source. Set to position "B" when using an external crystal between the CLKIN and XTAL pins.
- J30 Set link to position "A" to select the half power mode. With HALF-PWR set to 1, the AD7723 can be operated with a CLKIN of 10MHz maximum. Otherwise set link to position "B".
- J31 This link must always be set to position "B".
- J32 Selects either bipolar or unipolar analog input range. Position "A" for unipolar operation and position "B" for bipolar operation.
- J33 Used to connect the A_{GND} and D_{GND} planes.
- J34 This link is tied to DV_{DD}/\overline{CS} . In serial mode, this pin is configured as DV_{DD} . The link must be set to position "A" so that DV_{DD}/\overline{CS} is tied high. In parallel mode, this pin operates as a Chip Select Digital input. In this mode, the link must be set to position "B" so that \overline{CS} is tied low.
- J35 This selects the power source for the digital circuitry on the eval board. When it is removed, power must be supplied via the 2-pin header P6. Power can be supplied from the EVAL-CONTROL BOARD when this header is in place.
- J36 J37 These links must be in place if using AD8041 op-amps. They connect the AD8041's DISABLE pin to logic high.

SET-UP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as per the required operating mode. Table I shows the position in which all the links are set when the evaluation board is packaged.

Table I. Initial Link and Switch Positions

Link No.	Position	Function.
J1 J2	IN	Set for AIN signal biased around 0V.
13	В	Selects the on-board CMOS 20MHz clock oscillator as the clock source for the evaluation board.
J4	В	The AV_{DD} power plane is supplied from the Eval-Control Board.
J5 J6	OUT	+7.5V/-2.5V to be supplied at P2 for AD8047 op-amps supply.
J7 J8 J9 J10	J7-B, J8-OUT, J9-IN, J10- IN	Board is set to use the external reference, AD780.
J11	OUT	AD780 set to supply +2.5V reference.
J12 J13	A B	Parallel mode (lowpass decimate by 32) operation selected.
J14 J15	J14-OUT,	In Parallel mode operation, data is latched on the falling edge of $\overline{\text{DRDY}}$.
	J15-IN	
J16 J17	J16-IN,	Set for parallel mode operation.
	J17-OUT	
J18-J23	OUT	Set for parallel mode operation.
J24	IN	Resistor R1 is bypassed.
J25-J28	OUT	Set for parallel mode operation.
J29	А	Board is set to use the on-board 20MHz CMOS clock oscillator (AD7723's on-chip crystal oscillator amplifier is disabled).
J30	В	Normal operation mode $(HALF_PWR = 0)$.
J31	В	Always set to position "B".
J32	В	Bipolar analog input range selected.
J33	IN	A _{GND} and D _{GND} planes connected at P1.
J34	В	AD7723's \overline{CS} active in parallel mode.
J35	IN	Digital power is supplied from the Eval-Control Board.
J36 J37	OUT	Must be out when using AD8047 op-amps.

CONNECTORS

There are six connectors on the AD7723 evaluation board as outlined in Table II.

Table I	I. C	onnector	Functions
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Connector	Function
P1	96-Way DIN Connector used to interface to the Eval-Control board.
P2	3-Way Terminal Block used to supply analog power and ground (+7.5V, -2.5V and 0V), when these are not supplied by the EVAL-CONTROL BOARD.
P3	10-Way Header.
P4	20-Way Header used to access the AD7723 serial interface signals when interfacing to systems other than the EVAL-CONTROL BOARD.
Ρ5	40-Way IDC Connector used in parallel mode to interface to systems other than the EVAL-CONTROL BOARD.
P6	2-Way Terminal Block used to supply digital power and ground (+5V and 0V), when these are not being supplied by the EVAL-CONTROL BOARD.

SOCKETS

There are two input sockets relevant to the operation of the AD7723 on this evaluation board. The function of these sockets is outlined in Table III.

Table III. Socket Functions

Socket	Function
SK1	$50\Omega~SMB$ socket for analog input signal.
SK2	50Ω SMB socket for external sampling clock input.

Suitable cables for these sockets are available from Pasternack Enterprises.

INTERFACING TO THE EVAL-AD7723CB

The EVAL-AD7723CB is designed to be interfaced to the EVAL-CONTROL BOARD or to operate as a stand-alone unit.

EVAL-CONTROL BOARD

The EVAL-CONTROL BOARD is available from Analog Devices under the order entry "EVAL-CONTROL BOARD". When operated with this control board, all supplies (except +7.2V/-2.5V for AD8047 op-amps) and control signals for operating the AD7723 are provided by the EVAL-CONTROL BOARD when it is run under control of the AD7723 software which is provided with the AD7723 evaluation board package. This EVAL-CON-TROL BOARD will also operate with all Analog Devices evaluation boards which end with the letters CB in their title.

The 96-way connector on the EVAL-AD7723CB plugs directly into the 96-way connector on the EVAL-CON-

TROL BOARD. No power supplies (except +7.2V/-2.5V for AD8047 op-amps) are required in the system. The EVAL-CONTROL BOARD generates all the required supplies for itself and the EVAL-AD7723CB. The EVAL-CONTROL BOARD is powered from a 12V ac transformer. This is a standard 12V ac transformer capable of supplying 1A current and is available as an accessory from Analog Devices under the following part numbers:

EVAL-110VAC-US:	For use in the U.S. or Japan
EVAL-220VAC-UK:	For use in the U.K.
EVAL-220VAC-EU:	For use in Europe

These transformers are also available from other suppliers including Digikey (U.S.) and Campbell Collins (U.K.).

Connection between the EVAL-CONTROL BOARD and the serial port of a PC is via a standard RS-232 cable which is provided as part of the EVAL-CONTROL BOARD package. Please refer to the manual which accompanies the EVAL-CONTROL BOARD for more details on the EVAL-CONTROL BOARD package.

EVAL-CONTROL BOARD INTERFACING

Interfacing to the EVAL-CONTROL BOARD is via a 96-way connector, P1. The pinout for the P1 connector is shown in Figure 2 and its pin designations are given in Table IV.



Figure 2: Pin Configuration for the 96-Way Connector, P1

96-Way Connector Pin Description

D0-D15	Data Bus.
D_{GND}	Digital Ground. These lines are connected to the D_{GND} plane on the evaluation board. It allows the user to provide the digital supply via the connector along with the other digital signals.
$\overline{IRQ2}$	Interrupt Request 2.
\overline{CS}	Chip Select.
+5VD	Digital +5V Supply. These lines are con nected to the VCC supply via link J35.
A _{GND}	Analog Ground. These lines are con nected to the $A_{\rm GND}$ plane on the evaluation board.
-5V	Analog -5V Supply. These lines are con nected to the V- supply for the op-amps via link J6 if using AD8041 op-amps.
+ 5 V	Analog +5V Supply. These lines are con nected to the V+ supply for the op-amps via link J5 if using AD8041 op-amps and to the AV_{DD} supply for the AD7723 via

link J4.

Table IV. 96-Way Connector Pin Functions.

	ROW A	ROWB	ROWC
1			
2		D0	
3		D1	
4	DGND	DGND	DGND
5		D2	
6		D3	
7		D4	
8	+5VD	+5VD	+5VD
9		D5	
10		D6	<u>CS</u>
11		D7	
12	DGND	DGND	DGND
13		D8	
14		D9	
15		D10	
16	DGND	DGND	DGND
17		D11	<u>IRQ2</u>
18	D12	D13	D14
19			D15
20	DGND	DGND	DGND
21	AGND	AGND	AGND
22	AGND	AGND	AGND
23	AGND	AGND	AGND
24	AGND	AGND	AGND
25	AGND	AGND	AGND
26	AGND	AGND	AGND
27		AGND	
28		AGND	
29	AGND	AGND	AGND
30		AGND	
31	-5V	-5V	-5V
32	+ 5 V	+ 5 V	+ 5 V

Note : The unused pins of the 96-way connector are not shown.

OPERATING AS A STAND-ALONE UNIT

It is possible to operate the board as a stand-alone unit. When using the evaluation board as a stand-alone unit, external supplies must be connected to the 3-way power connector (P2). If using AD8047 op-amps (supplied on the evaluation board), supplies of +7.5V/0V/-2.5V are required. If using the AD8041 op-amps (not supplied), supplies of +5V/0V are required. Please note that using AD8041 op-amps will cause a 2dB degradation in the AD7723's SNR. An external +5V and D_{GND} (0V) must also be connected to a 2-pin power connector (P6). All power supplies are decoupled to the relevant ground plane with a 22µF tantalum capacitor and a 0.1µF ceramic capacitor. Each device power pin is also decoupled with a 0.1µF capacitor to the relevant ground plane. The board can be configured for either parallel or serial mode operation. In parallel mode, a 16-bit register, 74FCT162374, latches the conversion results to a 40-pin IDC connector (P5). In serial mode, the AD7723's serial interface signals are buffered with a 74FCT162244 and are available from a 20pin header (P4). The user must use their own connectors to interface to either of the connectors to gain access to the AD7723 signals.



Figure 3: Main Screen - FFT Mode

SOFTWARE DESCRIPTION

The software which controls the Eval-Control Board and hence the AD7723 evaluation board has three main screens. The screen shown in Figure 3 is the screen which appears when the software is run. The main function of this screen is to allow the user to read a predetermined number of samples from the AD7723 evaluation board and display them in both the time and frequency domain. The screen can be divided into three sections.

The upper third of the screen contains the control buttons, the menu bar and various status windows. The control buttons allow the user to take samples, reset the part and quit the program. The menu bar allows the user to enter the setup menu, select which printer port is being used to control the Eval-Control Board, load and save samples, get information about the software etc. The status windows indicate the setup of the AD7723 evaluation board/device, number of samples taken, and any information/error messages that are generated.

The middle third of the screen is a Digital Storage Oscilloscope (DSO). When samples are uploaded from the Eval-Control Board, they are displayed here. The samples can be displayed as either integer values or as voltages. Once samples have been displayed, clicking at any point in the graph will display the sample number and the value of the point directly beneath the cursor. Along the axis of the graph are the **Zoom Handles**. These allow the user to zoom in and out to get a closer look at a particular sample if required. When another set of samples is taken, the graph will attempt to display all values collected unless the **Hold Zoom** check box is ticked. In this case, the graph will keep the same axis settings as for the previous set of data samples. Additional check boxes are provided to give the user control over the vertical and horizontal grids and data points.

The lower third of the screen will show either a Fast Fourier Transform (FFT) of the data or a Histogram which shows the number of occurrences of each particular code read back. The FFT (the default option) is typically used when the user is concerned with examining an ADC's performance in the frequency domain. When performing a Fourier Transform, the data can be windowed by a Blackman-Harris window before the transform by clicking the B-H box. When the B-H box is not clicked on, the data is not windowed. The Histogram will give an indication of the ADC's performance to DC signals. The option displayed can be toggled by clicking on the FFT Mode/ Histogram Mode button in the top right of the screen. Figure 4 shows how the main screen looks when the Histogram Mode option is selected.



Figure 4: Main Screen - Histogram Mode

SETUP SCREEN

The Setup Screen is responsible for allowing the user to load a configuration file for the evaluation board. The configuration file will give the software detailed information about the evaluation board and the part connected to the Eval-Control Board such as number of bits, maximum sampling rate, power supply requirements, etc. The configuration file also tells the software the name of the DSP program file which it should download to the Eval-Control Board. These files are supplied by Analog Devices with the evaluation board. Figure 5 shows the setup screen. For the AD7723 evaluation board, the configuration file is called ad7723.cfg.

SETTING UP THE EVAL-CONTROL BOARD

The Eval-Control Board and AD7723 evaluation board should be connected together via the 96-way connector. The power should be applied to the Eval-Control Board. At this stage, the red LED should be flashing which indicates that the Eval-Control Board is functional and ready to receive instructions. The software which should have been installed should be loaded before the printer port cable is connected between the Eval-Control Board and the PC. This will ensure that the printer port has been initialized properly. The printer port cable can then be connected between the PC and the Eval-Control Board.

RUNNING THE SOFTWARE

With the hardware setup, the user is ready to use the AD7723 evaluation board with the Eval-Control Board. In the software, the user should select the File menu and click on **Setup**. This will display the setup form. A window on the left of the setup form lists all the available configuration The configuration file is a text based file which files. contains information about the AD7723 evaluation board such as part name, number of samples to be taken, default and maximum sampling frequency power supply settings, etc. The configuration file also contains the name of the DSP program file which is to be downloaded to the Eval-Control Board. The user should select the configuration file and click Load. The Eval-Control Board will be reset and the DSP program will be downloaded. During the download, the power supply settings indicated in the configuration file are set and the user may hear some relays clicking. The pulldown menu items such as 'number of samples' and 'sampling frequency' will have been set to the default values specified by the configuration file. The user is free to change these at will. Once the settings have been decided, the user can click **Close** to return to the main form.

🖝 Setup Menu		×
Select a Configuration File	Select No. Of Samples	Input Max (V)
ad7723.cfg	2048 💌	2.00
	Select Clock Frequency 20000000 Hz	Input Min (V) -2.00
Supply Settings	Output Word Rate 625000 Hz	Load
±12V AVDD DVDD	AVDD DVDD BUS	Close
ON ON ON	5V 5V ON	Cancel

Figure 5: Setup Screen

TAKING SAMPLES

When the user clicks **Sample**, the software will instruct the Eval-Control Board to take the required number of samples at the required frequency from the AD7723 evaluation board. These samples are then uploaded and displayed. An FFT and Histogram are also calculated and displayed. If the user clicks **Cont Samp**, the software will repeat the process indefinitely until the user clicks **Stop Samp**. While the software is continuously sampling data, the other control buttons are disabled.

OTHER BUTTONS

The **Reset** button will cause the Eval-Control Board to perform a reset function. When this occurs, the power supplies are turned off and the program in DSP memory is lost. The user should repeat the setup instructions to download another configuration file, if required.

The **Quit** button will exit the software. The program running on the Eval-Control Board is not terminated.

MENU BAR ITEMS

The main screen of the program contains a number of options available as pulldown menu items. The functions of these are listed below.

File Menu

Setup Menu: Selecting this option displays the Setup Screen as shown in Figure 5.

Load Raw Data: Selecting this option allows the user to load data which has been saved by the software during a previous session.

Save Raw Data: Selecting this option allows the user to save the current set of sample data points. The data can be

reloaded to the Eval-Control Board software at a later date or can be used by other programs for further analysis.

Save Binary Data: Selecting this option allows the user to save the current set of sample data points. The data is saved in binary format as a text file. This method can be useful for examining code flicker, looking for stuck bits, etc.

Save FFT Data: Selecting this option allows the user to save the current set of FFT data points. FFT data cannot be reloaded into the Eval-Control Board software but can be loaded into other software packages for further analysis.

Exit: Quits the program.

Printer Port

This menu item allows the user to select which printer port should be used for communication with the Eval-Control Board.

LPT1: This option selects 0x378 as the printer port address. This is the default option.

LPT2: This option selects 0x278 as the printer port address.

 $\ensuremath{\textbf{PRN}}\xspace$: This option selects 0x3BC as the printer port address.

Help

This menu item gives information about the current revision of software for the AD7723 evaluation board being used.

SOFTWARE CONFIGURATION FILE

The software configuration file gives the Eval-Control Board software information on how the software and hardware should perform. It contains information such as the name of the DSP program to be downloaded, the default and maximum sample frequencies, the number of samples to take and the power supply settings to use. A typical Software Configuration file (*.cfg) is shown in Listing 1.

[EVAL-CONTROL BOARD] partname:AD7723 programname:ad7723.PRG

clockfrequency:20000000
samples:2048

+/-15V:on dvdd:5:on avdd:5:on bus:on ;options 2scomp, binary dataformat:2scomp numberofbits:16 inputVmax:2.0 inputVmin:-2.0 [endofconfig]

Listing 1. Software Configuration File.



Figure 6. AD7723 Evaluation Board Circuit Diagram (Sheet 1 of 3)



Figure 7. AD7723 Evaluation Board Circuit Diagram (Sheet 2 of 3)



Figure 8. AD7723 Evaluation Board Circuit Diagram (Sheet 3 of 3)



Eval-AD7723CB (Rev. B01) Comp. Side view) Component Side Silkscreen

Figure 9: AD7723 Evaluation Board Component Side Silkscreen Artwork



Eval-AD7723CB (Rev. B01) Comp. Side view)

Solder Side Silkscreen

Figure 10: AD7723 Evaluation Board Solder Side Silkscreen Artwork



Eval-AD7723CB (Rev. B01) Comp. Side view) Layer 1. - Component Side

Figure 11: AD7723 Evaluation Board Component Side Artwork (Layer 1)



Eval-AD7723CB (Rev. B01) Comp. Side view)

Layer 4. – Solder Side.



Eval-AD7723CB (Rev. B01) Comp. Side view) Layer 2 - Ground Planes

Figure 13: AD7723 Evaluation Board Layer 2 (Ground Planes) Artwork



Figure 14: AD7723 Evaluation Board Layer 3 (Power Planes) Artwork

Table V. AD7723 Evaluation Board Bill of Materials

<u>Qty</u>	Reference Designator	Description/Value	<u>Manuf. No.</u>	Supplier No.
2	U1-2	AD8047AN	ADI AD8047AN	ADI
1	U3	AD780	ADI AD780AN	ADI
1	U4	20MHz Crystal Oscillator	IQD 20MHz IQXO-35BE	FEC 221-480
1	U5	74AC00	Harris CD74AC00M	FEC 485-755
1	U6	74AC04	Harris CD74AC04M	FEC 485-779
1	U7	74FCT162374TPV 16 bit register	Integrated Device Tech.	Hamilton Hallmark
1	U8	74FCT162244TPV 16 bit buffer	Integrated Device Tech.	Hamilton Hallmark
1	U9	AD7723	ADI	ADI
1	Y1	19.6MHz Crystal	IQD 19.6MHz HC49	IQD
2	L1 L2	RFI SUPPRES. BEAD		FEC 108-267
1	C1	Unused capacitor spacing		
1	C2	220pF Ceramic 0805 Case	AVX 08051A220JAT00J	FEC 498-609
8	C3 C5 C7 C9 C11 C21 C38 C43	10uF 16V Tant. TAJ-B Case	AVX TAJB106K016R	FEC 498-737
31	C4 C6 C8 C10 C12 C16 C18 C20 C22 C28-37 C39 C40 C44 C49-57	0.1uF Ceramic 0805 Case	AVX CM21X7R104K25VAT	FEC 499-687
2	C13 C14	33pF Ceramic 0603 Case (unused)	AVX 06035A330JAT00J	FEC 498-555
5	C15 C17 C19 C24 C48	22uF 16V Tant. TAJ-D Case	AVX TAJD226K016R	FEC 498-749
1	C23	22nF Ceramic 0805 Case	AVX 08055C223KAT00J	FEC 578-198
1	C25	220nF Ceramic 0805 Case	AVX CM21X7R224K16VAT	FEC 499-699
6	C26 C41 C42 C45 C46 C47	10nF Ceramic 0805 Case	AVX 08055C103KAT00J	FEC 499-225
1	C27	1uF Ceramic 1206 Case	AVX CM316X7R106K16VAT	FEC 499-71
1	R1	51w 5% 0.1W 0805 Case	Multicomp	FEC 771-181
1	R2	390w 5% 0.1W 0805 Case	Multicomp	FEC 613-046
4	R3 R5-R7	220w 5% 0.1W 0805 Case	Multicomp	FEC 613-010
2	R4 R8	27w 5% 0.1W 0805 Case	Multicomp	FEC 612-900
1	R9	20kw 5% 0.1W 0805 Case	Multicomp	FEC 771-791
1	RIO	10kW 5% 0.1W 0805 Case	Multicomp	FEC 613-216
1	KII DI2	1kw 5% 0.1w 0805 Case	Multicomp	FEC 613-095
1	R12	1MW 5% 0.1W 0805 Case (unused)	Multicomp	FEC 613-459
1	R15 B14 10	20W 5% 0.1W 0805 Case	Multicomp	FEC //1-152
2	R20-21	4.7kw 5% 0.1W 0805 Case 10W 5% 0.1W 0805 Case	Multicomp	FEC 612-856
1	P1	DIN41612 C96 90 ⁰ plug	Harting 0903-196-7921	FEC 104-986
1	P2	3 Pin Power Connector	Lumberg KRM3	FEC 151-786
1	Р3	10 Way DIL Header	Preci-Dip 892-90-010-10-802	Futura Elect.
1	P4	20 Way DIL Header	Preci-Dip 892-90-020-10-802	Futura Elect.
1	P5	40 Way Shrouded Header	3M 2540-6002UB	Digikey mhb40k-nb
1	P6	2 Pin Power Connector	Lumberg KRM2	FEC 151-785
2	SK1 SK2	50W Gold Plated PCB SMB Jack	Pasternack Enter. PE4174	FEC 310-682
21	J1 J2 J5 J6 J9-J11 J14-16 118-24 J33 J35-37	2 Way Jumper	Preci-Dip 890-90-002-10-802	Futura Elect.
16	J3 J4 J7 J8 J12 J13 J17 J25-32 J34	3 way jumper	Preci-Dip 890-90-003-10-802	Eutura Elect
37	J1-J37	Shorting links	Preci-Dip 999-19-310-00	Futura Elect
13	TP1 TP2 TP9-TP19	White Testpoint	Keystone Cat. No. 5002	Futura Elect
4	TP4 TP6 TP7 TP20	Red Testpoint	Keystone Cat. No. 5000	Futura Elect.
5	TP3 TP5 TP8 TP21 TP22	Black Testpoint	Keystone Cat. No. 5001	Futura Elect.
3	U1 U2 U3	Ultra low profile socket strip	Preci-Dip 714-91-108-31-012	Futura Elect.