8	7	6	5	4	3	2	1

JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	16FEB15	LIANG XU
B	AS PER ECR-057768	26FEB16	LIANG XU

RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

D

C

B

A

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

	DATE
TEMPLATE ENGINEER -	
HARDWARE SERVICES -	
HARDWARE SYSTEMS -	
TEST ENGINEER -	
COMPONENT ENGINEER -	
TEST PROCESS -	
HARDWARE RELEASE -	
DESIGNER V. JAYME II	16FEB15
PTD ENGINEER LIANG XU	16FEB15
CHECKER -	

SCHEMATIC

ANALOG DEVICES

```
HW TYPE    : Customer Evaluation
Product(s): AD9576
           : N/A
PACKAGE    : 64-lead 9X9X0.75 CSP-family
           : 0.5MM-pitch StyleVendor Style
```

MASTER PROJECT TEMPLATE: TBD
TESTER TEMPLATE: no_template

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS X.XX +-0.010 X.XXX +-0.005 | FRACTIONS +-1/32 | ANGLES +-2

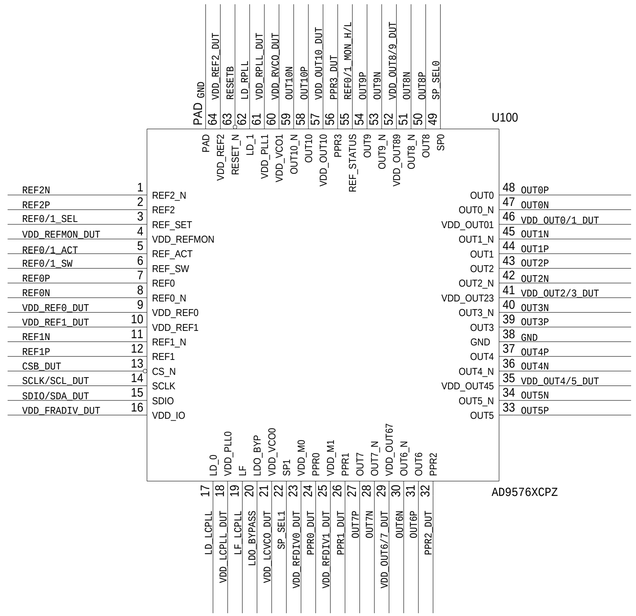
DRAWING NO. 02_040335
REV. B

SIZE D | SCALE 1:1 | CODE ID NO. CodeID | SHEET 1 OF 7

8	7	6	5	4	3	2	1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

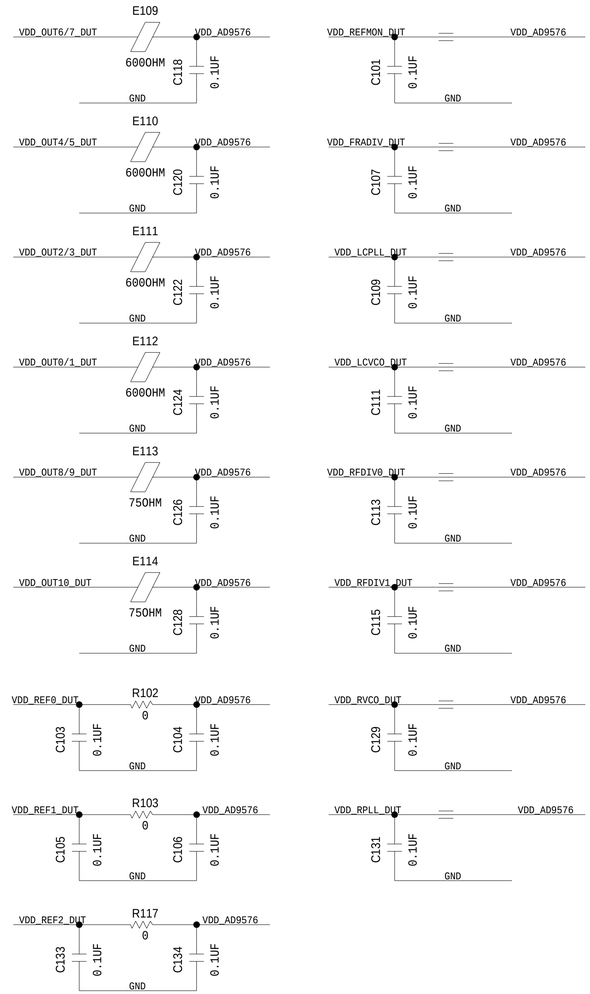
AD9576 SECTION



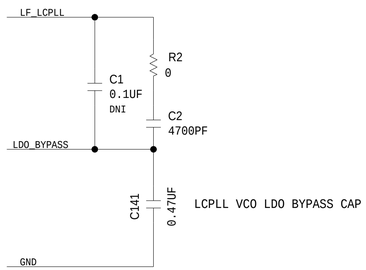
CURRENT ESTIMATION(TYP):400 MA
CURRENT ESTIMATION(MAX):550 MA

BYPASS CAPS

(DNI CAPS GO ON BOTTOM-SIDE OF PCB)

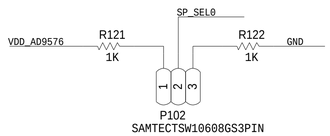


LCPLL EXTERNAL LPF CIRCUITS



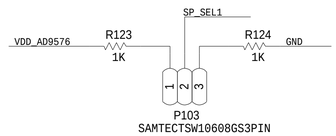
NOTE:C1 DO NOT INSTALL, ONLY FOR 8KHZ REFIN

SP SELECT0



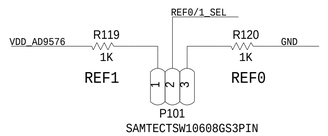
DEFAULT: FLOAT

SP SELECT1



DEFAULT: FLOAT

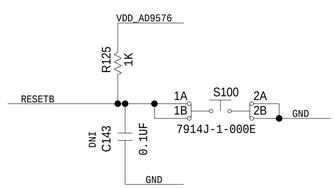
REF0/1 SELECT



DEFAULT: REF0

SP_sel0	SP_sel1	spi_i2c_select[3:0]	function
Floating	Floating	0000	SPI with PPR
Floating	Low	0001	I2C with address 0x39
Floating	High	0010	I2C with address 0x3a
Low	floating	0011	I2C with address 0x3b
Low	Low	0100	I2C with address 0x3c
Low	High	0101	I2C with address 0x3d
High	Floating	0110	I2C with address 0x3e
High	Low	0111	I2C with address 0x3f
High	High	1000	SPI without PPR

RESETB



ANALOG DEVICES

SCHEMATIC

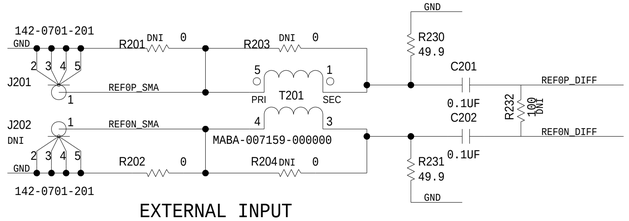
HW TYPE : Customer Evaluation
Product(s): AD9576
: N/A

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_040335	B
PTD ENGINEER: LIANG XU	SIZE: D / SCALE: 1:1	SHEET 2 OF 7

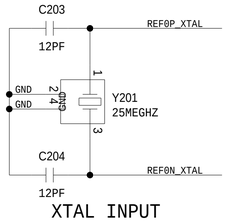
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

REF INPUTS SECTION

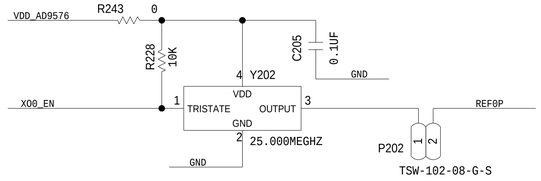
REF0 INPUT



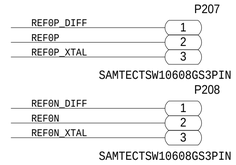
EXTERNAL INPUT
REF0 FORMAT: DIFF
EXTERNAL SE INPUT, RECOMMEND SQUARE WAVE



XTAL INPUT
REF0 FORMAT: XTAL

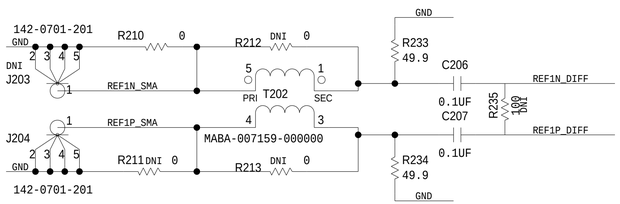


STANDARD XO INPUT
REF0 FORMAT: CMOS

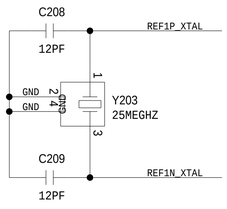


CONNECT PIN1 AND PIN2 OF P207/P208 FOR DIFF INPUT
CONNECT PIN3 AND PIN2 OF P207/P208 FOR XTAL INPUT
CONNECT P202 AND ENABLE XO0_EN FOR XO INPUT

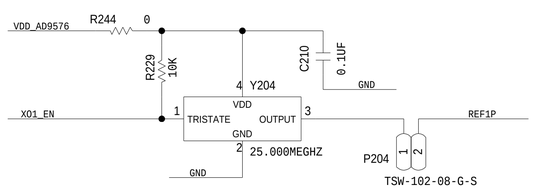
REF1 INPUT



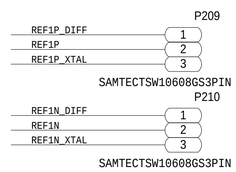
EXTERNAL INPUT
REF1 FORMAT: DIFF
EXTERNAL SE INPUT, RECOMMEND SQUARE WAVE



XTAL INPUT
REF1 FORMAT: XTAL

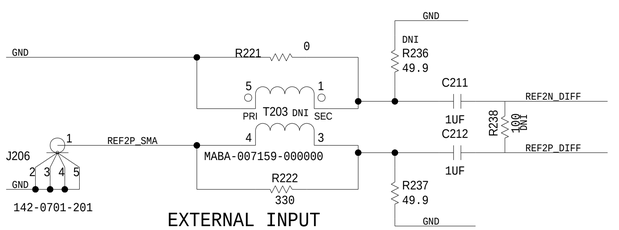


STANDARD XO INPUT
REF1 FORMAT: CMOS

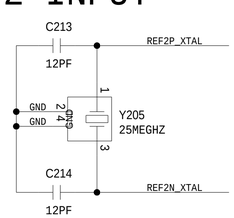


CONNECT PIN1 AND PIN2 OF P209/P210 FOR DIFF INPUT
CONNECT PIN3 AND PIN2 OF P209/P210 FOR XTAL INPUT
CONNECT P204 AND ENABLE XO1_EN FOR XO INPUT

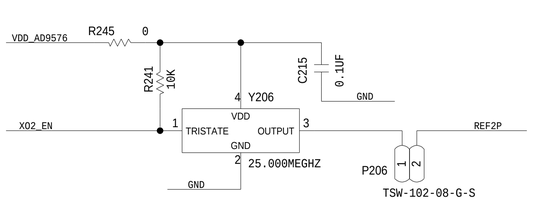
REF2 INPUT



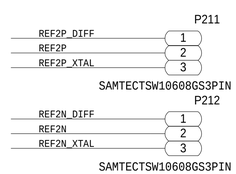
EXTERNAL INPUT
REF2 FORMAT: DIFF
NOTE:DEFAULT FOR EXTERNAL 3.3V CMOS MONITOR CLOCK INPUT



XTAL INPUT
REF2 FORMAT: XTAL



STANDARD XO INPUT
REF2 FORMAT: CMOS



CONNECT PIN1 AND PIN2 OF P211/P212 FOR DIFF INPUT
CONNECT PIN3 AND PIN2 OF P211/P212 FOR XTAL INPUT
CONNECT P206 AND ENABLE XO2_EN FOR XO INPUT

ANALOG DEVICES

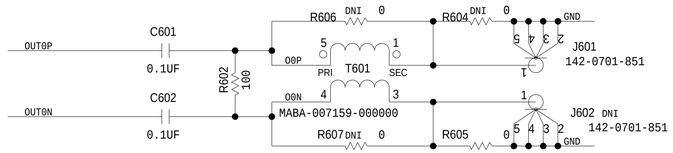
SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): AD9576
: N/A

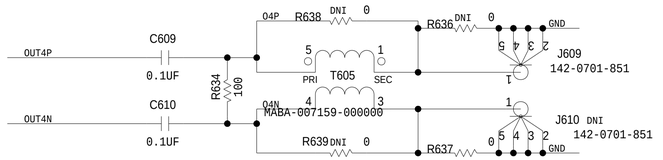
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_040335	B
PTD ENGINEER: LIANG XU	SIZE: D / SCALE: 1:1	SHEET 3 OF 7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

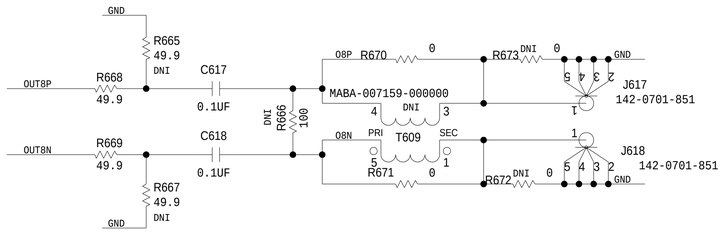
CLOCK OUTPUTS SECTION



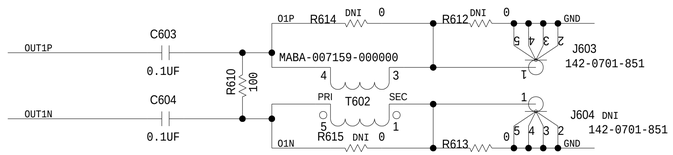
OUT0:HSTL/LVDS/1.8VCMOS



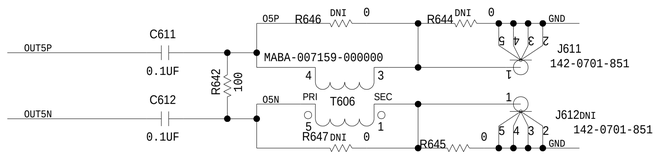
OUT4:HSTL/LVDS/1.8VCMOS



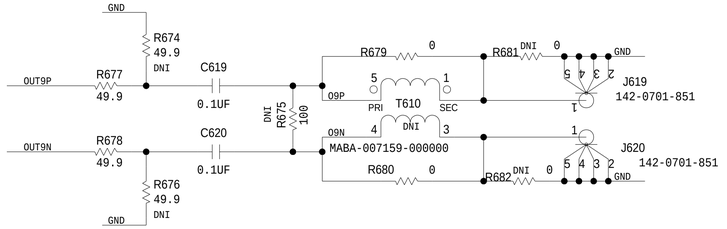
OUT8:HSTL/LVDS/HCSL/LVCMOS(1.8V/2.5V/3.3V)



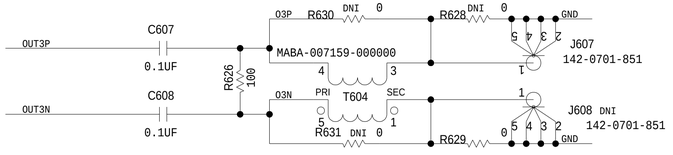
OUT1:HSTL/LVDS/1.8VCMOS



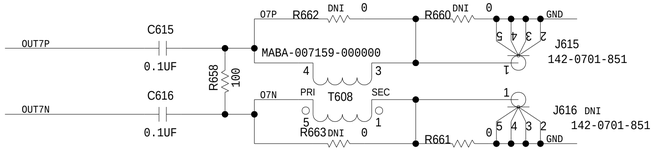
OUT5:HSTL/LVDS/1.8VCMOS



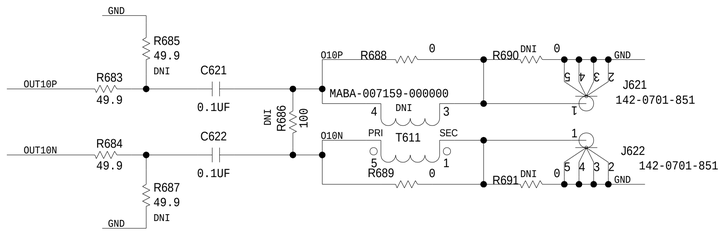
OUT9:HSTL/LVDS/HCSL/LVCMOS(1.8V/2.5V/3.3V)



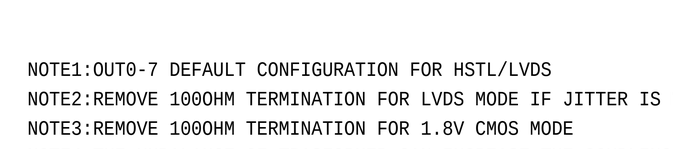
OUT2:HSTL/LVDS/1.8VCMOS



OUT6:HSTL/LVDS/1.8VCMOS



OUT10:HSTL/LVDS/HCSL/LVCMOS(1.8V/2.5V/3.3V)



OUT3:HSTL/LVDS/1.8VCMOS

OUT7:HSTL/LVDS/1.8VCMOS

NOTE1:OUT0-7 DEFAULT CONFIGURATION FOR HSTL/LVDS
NOTE2:REMOVE 100OHM TERMINATION FOR LVDS MODE IF JITTER IS NOT GOOD FROM E5052
NOTE3:REMOVE 100OHM TERMINATION FOR 1.8V CMOS MODE
NOTE4:THE UNBALANCE OF TRASFORMER CAN INCREASE THE COUPLING

NOTE1:OUT8-10 DEFAULT CONFIGURATION FOR 3.3V CMOS
NOTE2:SOLDER 50OHM TO GND FOR HCSL MODE
NOTE3:SOLDER 100OHM AND CHANGE 50OHM SERIES RESISTOR
TO 0OHM FOR LVDS/HSTL MODE

ANALOG DEVICES

SCHEMATIC

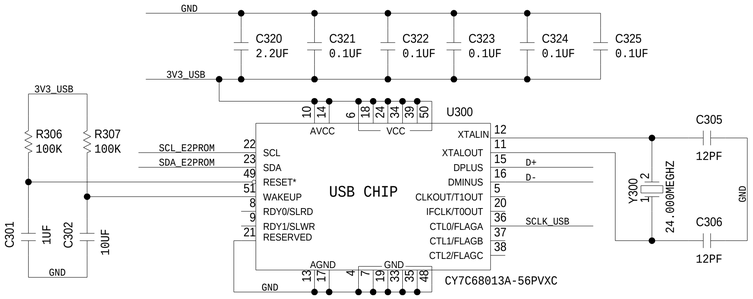
HW TYPE : Customer Evaluation
Product(s): AD9576
: N/A

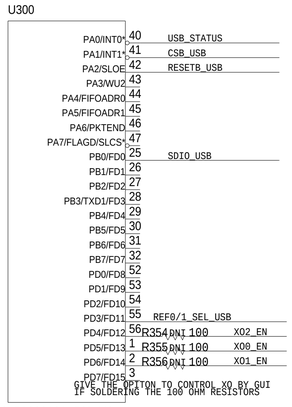
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_040335	B

PTD ENGINEER	SIZE	SCALE	SHEET	OF
LIANG XU	D	1:1	4	7

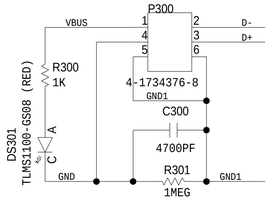
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

USB SECTION

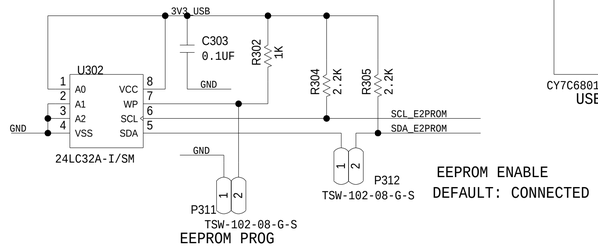




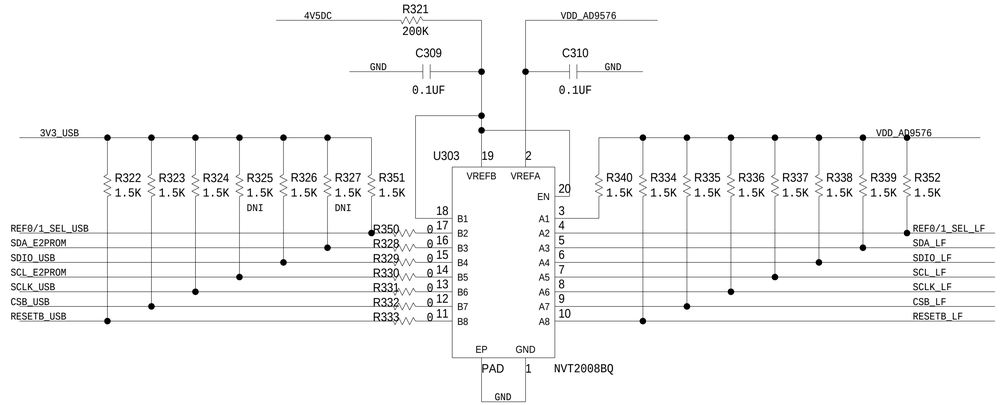
USB CONNECTOR



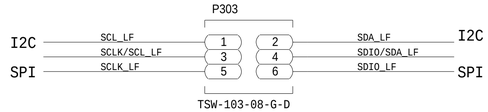
EEPROM



LEVEL TRANSLATOR

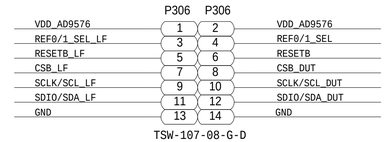


SPI/I2C SWITCH JUMPERS



DEFAULT:SPI

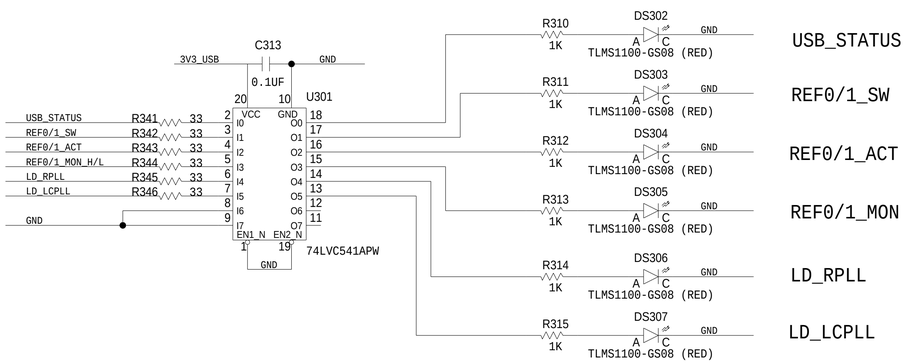
CONTROL JUMPERS



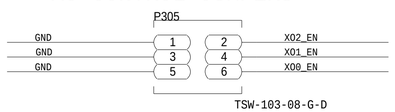
DEFAULT:ONLY CONNECT CSB/SCLK/SDIO

NOTE:DON'T PRESS THE RESETB BUTTON OR SWITCH THE REF_SEL JUMPER
WHEN RESETB AND REF_SEL ARE CONNECTED WITH USB CONTROLLER

LEDS

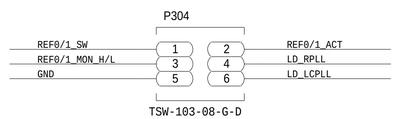


XO CONTROL JUMPERS



DEFAULT:CONNECT WITH GND TO DISABLE XO
ENABLE XO:DISCONNECT WITH GND

MONITOR SIGNAL HEADERS



ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): AD9576
: N/A

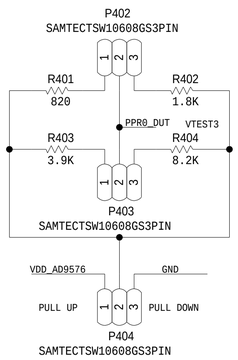
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_040335	B
PTD ENGINEER: LIANG XU	SIZE: D / SCALE: 1:1	SHEET 5 OF 7

PPR CONTROL SECTION

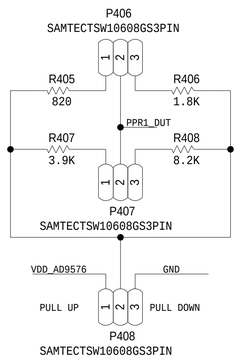
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

PPR2/PPR3 Profile #	PPR2 State	PPR3 State	REF0/REF1 Freq (MHz)	OUT0-3 Freq (MHz)	OUT0-3 Format	OUT4-5 Freq (MHz)	OUT4-5 Format	OUT6-7 Freq (MHz)	OUT6-7 Format	OUT8-9 Freq (MHz)	OUT8-9 Format	OUT8-9 From	PPR0 State
0	0	0	25	PD	HSTL	PD	HSTL	PD	HSTL	PD	HSTL	Receiver	
1	0	1	25	156.25	HSTL	156.25	HSTL	156.25	HSTL	156.25	HSTL	LC-PLL	
2	0	2	25	156.25	LVDS	156.25	LVDS	156.25	LVDS	156.25	LVDS	LC-PLL	
3	0	3	25	156.25	HSTL	156.25	HSTL	100	HSTL	25	3.3V CMOS	Receiver	
4	0	4	25	156.25	LVDS	156.25	LVDS	100	HSTL	25	3.3V CMOS	Receiver	
5	0	5	25	156.25	HSTL	125	HSTL	100	HSTL	50	3.3V CMOS	Ring-PLL	
6	0	6	25	156.25	HSTL	125	HSTL	100	HSTL	25	3.3V CMOS	Receiver	
7	0	7	25	156.25	LVDS	125	LVDS	100	HSTL	25	3.3V CMOS	Receiver	
8	1	0	25	156.25	LVDS	125	LVDS	25	HSTL	25	3.3V CMOS	Receiver	
9	1	1	25	156.25	HSTL	125	HSTL	25	HSTL	25	3.3V CMOS	Receiver	
10	1	2	25	156.25	HSTL	100	HSTL	50	HSTL	125	HSTL	LC-PLL	
11	1	3	25	156.25	LVDS	100	LVDS	50	HSTL	125	HSTL	LC-PLL	
12	1	4	25	156.25	LVDS	100	LVDS	100	LVDS	25	3.3V CMOS	Receiver	
13	1	5	25	156.25	HSTL	100	HSTL	25	HSTL	25	3.3V CMOS	Receiver	
14	1	6	25	156.25	LVDS	100	LVDS	25	HSTL	25	3.3V CMOS	Receiver	
15	1	7	25	156.25	HSTL	100	HSTL	125	HSTL	312.5	HSTL	LC-PLL	
16	2	0	25	156.25	LVDS	100	LVDS	125	LVDS	312.5	LVDS	LC-PLL	
17	2	1	25	156.25	HSTL	312.5	HSTL	125	HSTL	25	HSTL	Receiver	
18	2	2	25	156.25	LVDS	312.5	LVDS	125	LVDS	25	LVDS	Receiver	
19	2	3	25	312.5	HSTL	100	HSTL	100	HSTL	156.25	HSTL	LC-PLL	
20	2	4	25	312.5	LVDS	100	LVDS	100	LVDS	156.25	LVDS	LC-PLL	
21	2	5	25	312.5	HSTL	100	HSTL	125	HSTL	156.25	HSTL	LC-PLL	
22	2	6	25	312.5	LVDS	100	LVDS	125	LVDS	156.25	LVDS	LC-PLL	
23	2	7	25	312.5	HSTL	100	HSTL	156.25	HSTL	156.25	HSTL	LC-PLL	
24	3	0	25	312.5	LVDS	100	LVDS	156.25	LVDS	156.25	LVDS	LC-PLL	0~7
25	3	1	25	625	HSTL	100	LVDS	100	LVDS	156.25	HSTL	LC-PLL	
26	3	2	25	100	HSTL	312.5	HSTL	156.25	HSTL	125	HSTL	LC-PLL	
27	3	3	25	100	LVDS	312.5	LVDS	156.25	LVDS	125	LVDS	LC-PLL	
28	3	4	25	100	HSTL	312.5	HSTL	156.25	HSTL	25	HSTL	Receiver	
29	3	5	25	100	LVDS	312.5	LVDS	156.25	LVDS	25	LVDS	Receiver	
30	3	6	25	100	HSTL	100	HSTL	100	HSTL	100	HCSL	LC-PLL	
31	3	7	25	100	LVDS	100	LVDS	100	LVDS	100	HCSL	LC-PLL	
32	4	0	25	125	HSTL	125	HSTL	125	HSTL	125	HSTL	LC-PLL	
33	4	1	25	125	LVDS	125	LVDS	125	LVDS	125	LVDS	LC-PLL	
34	4	2	25	125	HSTL	100	HSTL	100	HSTL	33.33	HSTL	Ring-PLL	
35	4	3	25	125	LVDS	100	LVDS	100	LVDS	33.33	LVDS	Ring-PLL	
36	4	4	25	125	HSTL	100	HSTL	25	HSTL	25	HSTL	Receiver	
37	4	5	25	125	LVDS	100	LVDS	25	LVDS	25	LVDS	Receiver	
38	4	6	25	25	LVDS	25	LVDS	125	LVDS	100	HCSL	LC-PLL	
39	4	7	25	100	LVDS	100	LVDS	125	HSTL	25	3.3V CMOS	Receiver	
40	5	0	25	100.000	HSTL	100.000	HSTL	125.000	HSTL	25	3.3V CMOS	Receiver	
41	5	1	25	156.250	HSTL	50.000	HSTL	125.000	HSTL	25	3.3V CMOS	Receiver	
42	5	2	25	156.250	LVDS	50.000	LVDS	125.000	LVDS	25	3.3V CMOS	Receiver	
43	5	3	25	100.000	HSTL	100.000	HSTL	100.000	HSTL	100	HCSL	Ring-PLL	
44	5	4	25	100.000	LVDS	100.000	LVDS	100.000	LVDS	100	HCSL	Ring-PLL	
45	5	5	25	25.000	HSTL	25.000	HSTL	25.000	HSTL	400	LVDS	Ring-PLL	
46	5	6	25	156.25	HSTL	50	HSTL	125	HSTL	400	HCSL	Ring-PLL	
47	5	7	25	156.25	LVDS	50	LVDS	125	LVDS	400	HCSL	Ring-PLL	
48	6	0	25	70.656	HSTL	70.656	HSTL	70.656	HSTL	25	HSTL	Receiver	
49	6	1	25	24.576	HSTL	24.576	HSTL	24.576	HSTL	100	HCSL	Ring-PLL	
50	6	2	25	24.576	LVDS	24.576	LVDS	24.576	LVDS	100	HCSL	Ring-PLL	
51	6	3	25	322.26563	HSTL	161.13281	HSTL	161.13281	HSTL	100	HCSL	Ring-PLL	0,1,4~7
52	6	4	25	322.266	LVDS	161.133	LVDS	161.133	LVDS	100	HCSL	Ring-PLL	
53	6	5	25	148.500	HSTL	148.500	HSTL	148.500	HSTL	100	HCSL	Ring-PLL	
54	6	6	25	148.5	LVDS	148.5	LVDS	148.5	LVDS	100	HCSL	Ring-PLL	
55	6	7	19.44	644.53125	HSTL	161.13281	HSTL	161.13281	HSTL	100	HCSL	Ring-PLL	
56	7	0	19.44	644.53125	LVDS	161.13281	LVDS	161.13281	LVDS	100	HCSL	Ring-PLL	
57	7	1	19.44	156.25	HSTL	125	HSTL	50	HSTL	100	LVDS	Ring-PLL	
58	7	2	19.44	156.25	LVDS	125	LVDS	50	LVDS	100	LVDS	Ring-PLL	
59	7	3	30.72	156.25	HSTL	50	HSTL	125	HSTL	25	3.3V CMOS	LC-PLL	4~7
60	7	4	30.72	156.25	LVDS	50	LVDS	125	LVDS	25	3.3V CMOS	LC-PLL	
61	7	5	30.72	156.25	HSTL	125	HSTL	50	HSTL	100	HCSL	Ring-PLL	
62	7	6	30.72	156.25	LVDS	125	LVDS	50	LVDS	100	HCSL	Ring-PLL	
63	7	7	122.88	122.88	HSTL	122.88	HSTL	122.88	HSTL	400	LVDS	Ring-PLL	

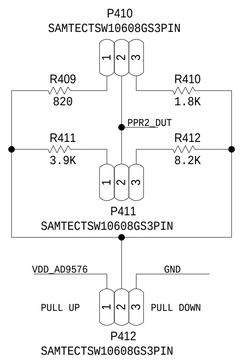
Note: If PPR0 is 0~3, REF0/REF1 is for LCPLL and Ring PLL , REF2 for monitor clock.
If PPR0 is 4~7, REF0/REF1 is for LCPLL , REF2 must be 25MHz for Ring PLL



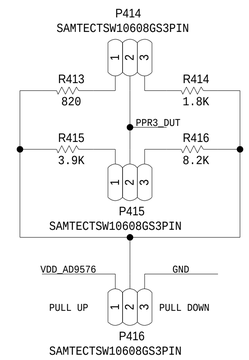
PPR0



PPR1



PPR2



PPR3

PPR0 State	REF0/REF1 Input Format	REF2 Input Format	REFIN Selected For LC PLL	REFIN Selected For Ring PLL	REF Doubler For LC PLL	REF Doubler For Ring PLL
0	XTAL	2.5V/3.3V CMOS	REF0 or REF1	REF0 or REF1	ON	OFF
1	2.5V/3.3V CMOS	2.5V/3.3V CMOS	REF0 or REF1	REF0 or REF1	ON	OFF
2	2.5V/3.3V CMOS	2.5V/3.3V CMOS	REF0 or REF1	REF0 or REF1	OFF	OFF
3	DIFF	2.5V/3.3V CMOS	REF0 or REF1	REF0 or REF1	OFF	OFF
4	XTAL	XTAL	REF0 or REF1	REF2	ON	OFF
5	2.5V/3.3V CMOS	2.5V/3.3V CMOS	REF0 or REF1	REF2	ON	OFF
6	DIFF	XTAL	REF0 or REF1	REF2	ON	OFF
7	DIFF	2.5V/3.3V CMOS	REF0 or REF1	REF2	ON	OFF

Note1: DIFF mode can accept 1.8V CMOS with REF_P ac-coupled to signal and REF_N ac-coupled to ground
Note2: LC PLL and Ring PLL are the same REF input when PPR0 State is 0~3, REF0 or REF1 selected by REF_SEL pin.
Note3: REF Doubler on can get better phase noise but worse ref spurs if input dutycycle is not good, REF doubler off can get better ref spur but worse phase noise

PPR1 State	OUT10 FREQ (MHz)	OUT10 Format
0	25	2.5V/3.3V CMOS
1	33.33	2.5V/3.3V CMOS
2	50	2.5V/3.3V CMOS
3	66.67	2.5V/3.3V CMOS
4	100	LVDS
5	133	LVDS
6	200	LVDS
7	400	LVDS

Note: 2.5V/3.3V CMOS depends on the power supply voltage.

ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): AD9576
: N/A

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02_040335	B

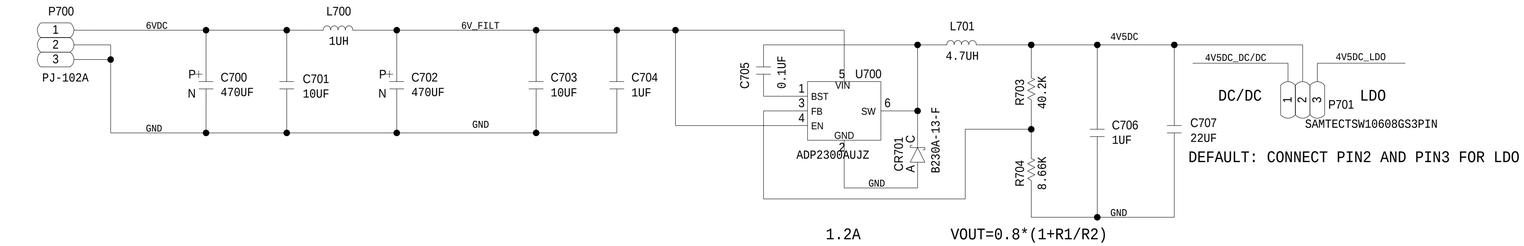
PTD ENGINEER	SIZE	SCALE	SHEET
LIANG XU	D	1:1	SHEET 6 OF 7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

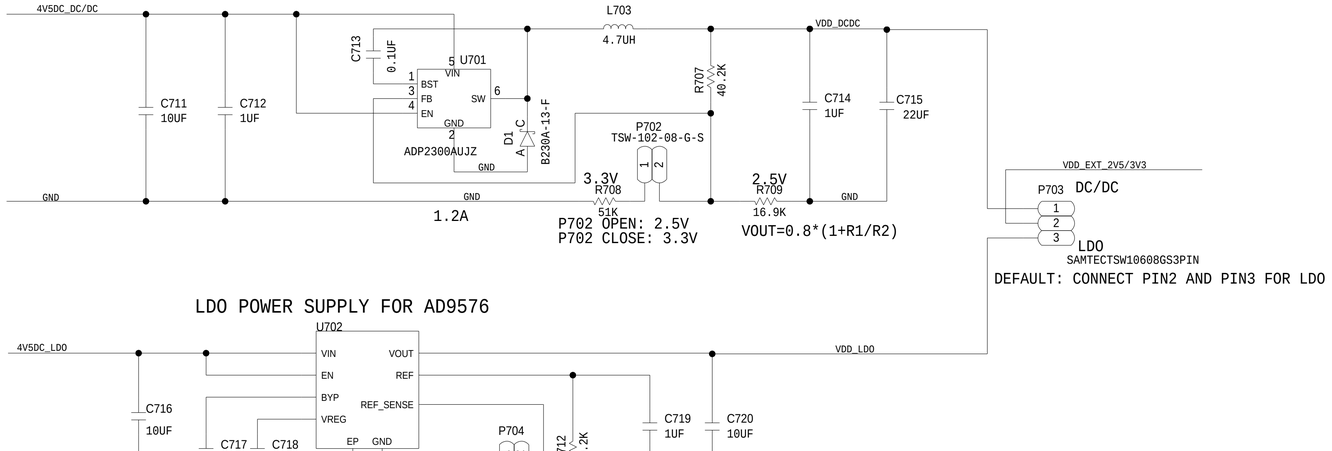
DC/DC CONVERTOR AND USB/XO LDO SECTION

6V IN

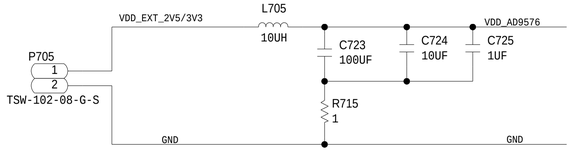
DC TO DC STEP DOWN 6V TO 4.5V



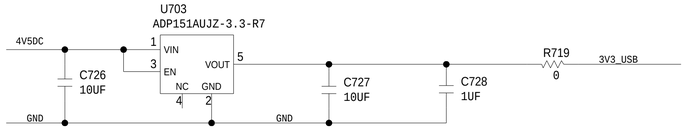
DC/DC POWER SUPPLY FOR AD9576



LDO POWER SUPPLY FOR AD9576



EXT POWER SUPPLY INPUT FOR AD9576
FLOATING P703 AND P701 IF USING P705



3.3V FOR USB SECTION

	SCHEMATIC		
ANALOG DEVICES	HW TYPE : Customer Evaluation Product(s): AD9576 : N/A		
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	PTD ENGINEER LIANG XU	SIZE D / SCALE 1:1	SHEET 7 OF 7