AD7705/AD7706/AD7707 Instrumentation Converter FAQs: Calibration

How is self-calibration implemented?

For calibration to occur regardless of which calibration mode is used on the selected channel, the ADC's on-chip microcontroller must record the modulator output for two different analog input conditions. These are the "zero-scale" and "full-scale" points. With these conversions, the microcontroller can calculate the gain slope for the input to output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of 16 bits.

In self-calibration mode, the ADC determines the calibration points internal to the ADC. The zero-scale point used to determine the calibration coefficients is with both inputs shorted (i.e. AIN(+) = AIN(–) = Vref) internally within the ADC. Signals connected to the analog input pins of the device will not affect the calibration procedure as long as they are within the common range of the input. The full-scale coefficient is determined by applying a voltage of VREF to the modulator inputs.

Self-calibration mode is invoked by writing to bits MD1 and MD0 in the Setup register.

In this calibration mode, the shorted inputs node is switched in to the modulator first and a conversion is performed. The VREF node is then switched in and another conversion is performed. DRDY can be used to determine when the calibration is complete and new data pertaining to the analog input is available at the output. DRDY goes high on the initiation of the calibration and will not return low until a conversion result on the external analog input is available. The self-calibration procedure takes into account the selected gain on the PGA.

What is system calibration and how is it implemented?

System calibration allows the converter to compensate for external system gain and offset errors as well as its own internal errors. Calibration is basically a conversion process on two specific input voltages (zero scale and full-scale) from which the offset error coefficient and full-scale error coefficient are determined. With system calibration, the zero scale voltage and full-scale voltage must be applied to the ADC by the user.

System calibration is a two-step process. The zero-scale point must be presented to the converter first. This voltage is applied to the analog input of the converter before the zero-scale system calibration step is initiated and must remain stable until the step is complete. System calibration is initiated by writing the appropriate values to the MD1 and MD0 bits in the setup register. The DRDY output indicates when the step is complete by going low or the mode bits can be monitored via software - these return to normal mode when calibration is complete. After the zero-scale point is calibrated, the full-scale point is applied and the full-scale system calibration process is initiated by again writing the appropriate code to the MD bits. The full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the duration of the calibration. DRDY goes low at the end of this second step to indicate that the system calibration is complete.

The calibration procedure is dependent on whether unipolar mode or bipolar mode is used. In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function while in the bipolar mode, it is performed between mid-scale and positive full-scale.

When performing a system calibration, the zero-scale voltage and full-scale voltage must be switched into the analog input channel of the ADC. This can be performed by using a SPDT (Single Pole Double Throw) CMOS switch that has low on-resistance. One of the switch inputs can be connected to the analogue input which represents the full-scale value while the other input can be connected to the zero-scale voltage. Using this switch ensures that the signal chain on both analog inputs for the zero-scale calibration and full-scale calibration is identical. By so doing, the system zero-scale calibration will compensate for the insertion loss of the switch. The ADG736 is a dual SPDT switch with a Ron of < 4Ohms and matching of better than 0.4Ohms.

When should a calibration be performed on the AD7705/AD7706 family of sigma delta ADCs?

A calibration must be performed when there is a change in

- gain
- Update Rate
- Temperature or when Switching between channels that share coefficients registers but have different operating conditions.

With any gain change, there will be a matching error between gain ranges and this error needs to be calibrated out. In switching between gains 1,2,4 and 8, it may be possible to switch without the need for a calibration as this gain is implemented by multiple sampling of the input capacitor. This is accurately controlled and minimal error is introduced. In

switching between any other of the gain ranges, a calibration is required as the gain is implemented by scaling of capacitors. Capacitor errors exist due to processing errors etc.

If the update rate is changed for any reason, a calibration is required to alter the calibration coefficients in order to get accurate data results. The ADC architecture uses gross scaling factors internally when determining the calibration coefficients. Thus, the coefficients used by the part vary substantially across the range of update rates available.

Drift errors are due to changes in temperature. Calibration can be used effectively to remove any errors associated with temperature drift. Self-calibration will remove the effects of temperature drift within the ADC itself. System calibration can be used to remove the drift errors in the ADC itself and also the drift errors associated with the front-end signal conditioning circuitry.

How often should a calibration be implemented in a system?
To determine the frequency of calibrations within a system, consider:.

- What accuracy is required from the converter?
- How does drift performance of the ADC limit performance?
- Over what temperature range does the system operate?

Taking these three questions into account will give some indication as to how often a calibration is required. Other system parameters should also be considered when determining how often to calibrate. These are all related to circuit sensitivities to temperature change as follows:

- Parasitic thermocouple effects.
- Gain drift due to the reference temperature coefficient.
- Drift sources external to the converter.

In general, the higher the accuracy requirement, the more often a calibration will be required in order to maintain system accuracy. After a calibration has been performed, high-resolution converters will have some offset and gain drift associated with them, for example, the AD7705's offset drift due to temperature is typically 0.5uV/°C and the gain drift is typically 0.5ppm of full-scale range/°C. In accessing the complete effects on accuracy due to temperature, the temperature effects due to parasitic thermocouples and drift sources external to the converter also need to be factored into the equation.

If factory system calibration is performed, can temperature drift errors associated with the ADC be removed in the field without performing additional system calibrations?
System calibration can be easily implemented as part of a factory calibration but it is much harder to implement in the field since the system zero-scale and system full-scale voltages must be applied to the analog inputs during the calibration. These input voltages are not always easily available when operating in the field. Following the factory system calibration, the user still has the issue of removing ADC drift errors in the field due to temperature changes. The following outlines a method of overcoming this problem. This is outlined in two sections below: firstly the system factory calibration and secondly the field calibration.

Factory-Calibration:

- Perform a Self-Calibration at the required operating gain and update rate.
- Read and store the calibration register contents. Offset=Z0 and Gain=G0.
- Perform a System Calibration at the required operating gain and update rate as before.
- Read and store the calibration register contents. Offset =ZS and Gain=GS.The system can be shipped to the field with the system calibration coefficients loaded to the ADC. If the ambient temperature changes, the offset and gain drift errors need to be calibrated out of the system as follows:

Field-Calibration:

- Perform a Self-Calibration at the required operating gain and update rate. The Gain and update rate must remain the same as in the original self and system calibrations.
- Read the calibration register contents. Offset=Z1 and Gain=G1.

- Calculate the new calibration coefficients.

ZN=ZS+(Z1-Z0)

GN=GS*(G1/G0)

- Write ZN and GN to the calibration registers.

This procedure retains the original system calibration but adjusts the coefficients to remove errors due to temperature drift in the ADC. This procedure removes drift errors due to the ADC only. Drift errors due to the analog front end signal chain are not removed.

Can the calibration coefficients be altered manually to cater for input ranges other than the nominal ranges?

This situation arises when the user has a specific input range other than the nominal range but cannot implement a system calibration as the zero and full-scale voltages are not available during calibration. The following description shows how to alter the coefficients to accommodate input ranges other than 0 to Vref and +/-Vref. The part must first be calibrated using the self-calibration procedure with the appropriate gain, input range, update rate and bipolar/unipolar input range selected. The coefficients generated from the self-calibration procedure are used to generate new coefficients.

For example, if the required input voltage Vin is represented by:

Vin = A * VREF + B

Where B is an offset voltage and A * Vref is the input span.

The self-calibration procedure operates on shorted inputs for zero scale calibration and VREF for full-scale calibration which results in A = 1 and B = 0. The following procedure can be implemented so as to accommodate input ranges other than the nominal 0 to Vref or +/-Vref. The offset B is subtracted so that an output code of zero will be obtained when the analog input voltage is B. The span is adjusted to A * VREF so that this full-scale voltage will output a full-scale code.

- Perform a self-calibration and read back the calibration coefficients and let:
- Z0=Zero-scale coefficient and
- F0=Full-scale coefficient.

These coefficients can then be modified to cater for the new input range using the following formulae to generate the new coefficients ZN and FN.

ZN= Z0 + (B * 2^20 / (SPAN * F0 / 2^24))

FN= F0 / A

Where SPAN is the full-scale voltage span under nominal conditions which equals VREF/Gain in unipolar mode and 2VREF/gain in bipolar mode.

B is the offset voltage in volts and A is the scaling factor applied to the nominal span. A must have a value between 0.8 and 1.05 for guaranteed operation.

- Write ZN and FN to the ADC calibration registers to accommodate the new input range.

For example, suppose the ADC has a zero-scale coefficient of 2,165,373 and a full-scale coefficient of 5,416,211 following a self-calibration in unipolar mode. Since unipolar mode is used, the range used for the calibration is 0 to VREF where VREF is equal to 2.5V when a 5 V power supply is used. If the user requires an analog input range of 0.2 V to 2.6 V then, B is equal to 0.2 while A equals (2.6 – 0.2) / 2.5 = 0.96. The new zero-scale coefficient ZN is

ZN = 2,165,373 + (0.2 * 2^20 / (2.5 * 5,416,211 / 2^24)) = 2,425,218 and

FN = 5,416,211 / 0.96 = 5,641,886.

This scheme is useful only if the user knows the exact upper and lower limits of the desired input range and the ratio of the actual input span to the nominal input span.

With this method, the ADC will continue to meet the noise specifications given in the datasheet if the user ensures that the variable A is between 0.8 and 1.05. For example, the AD7705 has an rms noise spec of 4.1 uV when operated with a 5V power supply, a 50 Hz update rate and a gain of 1 which results in a signal range of 0 to 2.5 V in unipolar mode. If the input range is altered so that it varies from 0.2V to 2.5V as in the above example, the noise will continue to be 4.1 uV if the operating conditions (update rate, gain, etc) are not changed. With the original range, the peak to peak resolution equals log (2.5V / 6.6 * 4.1uV) / log 2 = 16 bits when rounded to the nearest 0.5 bit. With the altered range, the peak to peak resolution equals log (2.4V / 6.6 * 1.5uV) / log 2 = 16 also when rounded to the nearest 0.5 bit.