AD779x Instrumentation Converters
Frequently Asked Questions

General FAQs

What are the advantages and disadvantages of Σ-Δ ADCs?

The penalty paid for the high resolution achievable with Σ-Δ technology has always been speed. The hardware has to operate at the oversampled rate, which is much larger than the maximum signal bandwidth, thus demanding great complexity of the digital circuitry. Because of this limitation, Σ-Δ converters have traditionally been relegated to high resolution, very low frequency applications and more recently speech, audio, and medium speeds (100 kHz to 1 MHz).

The digital filtering stage results in long latency between the start of the sampling cycle and the first valid digital output; similarly, there is a significant lag thereafter between digital outputs and their corresponding sampling instants. These characteristics reduce the throughput time in multiplexed systems, as it takes many clock cycles for the digital filter to settle after switching from one channel to the next.

Most of the circuitry in Σ-Δ converters is digital, allowing these converters to be fabricated on a wide range of IC processes. This implies that performance will not drift significantly with time and temperature. They are inherently monotonic (that is, a change in the digital output always has the same slope as the analog input). This is of particular importance in closed-loop control systems where misinterpretation of the direction of change of a measured variable may cause the system to become unstable. They are inherently linear and present little differential nonlinearity. External sample-and-hold circuits are not required due to the high input sampling rate and low precision of the analog-to-digital conversion in the modulator (the devices are inherently self-sampling and tracking). Requirements for analog antialiasing filters are minimum—in most cases, a simple single-pole RC filter suffices, as the bandwidth of interest is considerably lower than the first image that occurs about the modulator frequency. In contrast, the filters required for medium to high resolution applications using other (nonoversampling) technologies are very sophisticated, difficult to design, large, and expensive.

What are the main applications?

These devices provide a complete analog front end for low frequency measurement applications. These applications include portable instrumentation, process control, smart transmitters, weigh scale, and transducer-based applications, as well as temperature and pressure measurement systems. In pressure and temperature measurement systems, for example, the system designer is faced with the task of measuring small signals that are generated from pressure sensors, RTDs (resistance temperature detectors), or thermocouples and resolving these to resolutions of 16 bits or higher. The major design tasks include signal conditioning of the output signal from the transducer, processing the signal to achieve the required resolution and accuracy, and ensuring that power consumption is low enough for portable applications. This family of Σ-Δ converters consists of fully integrated solutions that incorporate the required signal conditioning, filtering, and an analog-to-digital converter onto a single chip, allowing direct transducer interface without the need for front-end signal conditioning. The AD779x family consists of 16-bit and 24-bit resolution ADCs, which have a power consumption of typically 2 mW, making them ideal choices for portable data acquisition applications.

What is the traditional approach to analog front-end solutions, and how do Σ-Δ solutions overcome their shortcomings?

Traditional approaches to the problem of measuring signals from transducers have used a high resolution analog-to-digital converter (ADC) as the core element in the process. These were generally integrating ADCs or voltage-to-frequency converters (VFC) that provided high resolution for low input bandwidth signals. This type of ADC had to be surrounded by a considerable amount of analog signal conditioning circuitry to boost the transducer output signal so that the full dynamic range of these converters could be used to achieve the required performance. The performance of this signal conditioning circuitry, rather than the high resolution converter, often determined the system success in measuring low level signals. In designing gain stages, a number of factors have to be taken into account; the first and most critical is noise, both in the measurement environment and in the components that constitute the high gain stage. Common sources of noise in the circuit design environment are mains frequency noise and power supply noise. Other causes for concern include common-mode rejection of the gain stage, as the transducer output may sit on a large dc signal, therefore necessitating conversion from a differential input signal to a single-ended output. Offset in the amplifiers along with drift performance play havoc with circuit performance, leading to the use of expensive chopper stabilized amplifiers. Programmability was difficult to design into these systems, and calibration was performed mainly with the use of the system microcontroller. This leads to the requirement for external memory to store calibration coefficients.

Advances in design have enabled low cost, low power, highly accurate, integrated solutions to be developed. These architectures address the real-world problems of low power design required for data acquisition applications. The advantages that an integrated solution offers the system designer includes signal conditioning necessary for direct transducer interface integrated on chip to greatly reduce analog circuit design and layout complexity. Integrated solutions also offer better control of specifications and error budgets than those of discrete solutions. Σ-Δ converters provide enough dynamic range to allow direct transducer interface, thus removing the need for a high gain signal conditioning stage in front of the ADC.

The data sheet mentions that large external capacitors between the input and ground can affect measurement accuracy in unbuffered mode. Can you explain why this is the case? Does it only affect ac input signals, or are dc input signals affected, too?

If you use the ADC in unbuffered mode, large RC constants on the input can interact with the internal sampling capacitor and effectively starve

the sampling capacitor of charging current. This will cause gain errors in the ADC. The solution is either to use buffered mode or ensure that you respect the maximum RC values given in the data sheet.

The reference inputs are also unbuffered so, as with using the analog inputs in unbuffered mode, the RC loading on the reference inputs must be sufficiently low to avoid introducing errors into the conversion process.

The AD7792/AD7793/AD7794 can use an external clock. What is the frequency range of the external clock?

Although the on-chip 64 kHz clock is used by most customers, the AD7792/AD7793/AD7794 have the capability of being driven from an external clock. The parts can use an external clock from 60 kHz to 70 kHz and still meet the data sheet specifications. While the part continues to function with clock frequencies outside this range, performance is not guaranteed.

What is the output data update rate when the AD7792/AD7793/AD7794 are used with a master clock other than 64 kHz?

The devices have 16 selectable output rates from 4.17 Hz to 470 Hz. These values are determined by the internal clock. When the master clock frequency is changed, the output data rate will scale with the applied clock. For example, the default output data rate equals 16.7 Hz when the master clock is 64 kHz. If the master clock is reduced to 60 kHz, then the output data rate is reduced to (60/64) × 16.7 = 15.66 Hz.

Changing the output data rate will also affect the filter notches. When the output data rate equals 16.7 Hz, there are notches placed at 50 Hz and 60 Hz. If the master clock frequency is reduced to 60 kHz, the 50 Hz notch is moved to 46.87 Hz and the 60 Hz notch is moved to 56.25 Hz.

The ADC is seeing overvoltages in my application. How can I protect the ADC against these overvoltages?

The analog input pins can tolerate a voltage between GND − 0.3 V and AVDD + 0.3 V. There are ESD diodes connected from each analog input to AVDD and from each analog input to GND. If an overvoltage is seen on the analog input (a voltage that is in excess of 500 mV outside the power supply rails), these diodes will turn. These ESD diodes provide a low resistance path so the overvoltage is directed away from the ADC's modulator. However, the ESD diodes can only tolerate a continuous current less than 10 mA. So, to prevent damage of the ADC, some external resistance is required so that the current is limited to less than 10 mA.

Using external limiting resistors prevents the ADC from getting damaged. However, the external overvoltage may cause the on-chip registers to be corrupted.

To prevent the internal registers from being corrupted, the overvoltage needs to be directed away from the ADC. Connecting Schottky diodes from each analog input to AVDD and GND is one method that can be used. The Schottky diode must have a turn-on voltage of 300 mV. This ensures that the external diode turns on before the ADC's internal diodes so that the overvoltage is directed away from the ADC. Since the ADC does not experience any overvoltage, the on-chip registers will remain intact.

Are there any suggested protection schemes against ESD that should be considered with these products?

These converters are manufactured on a standard CMOS process; therefore, all standard practices and protection schemes apply to these devices as with all other CMOS devices. There are ESD protection diodes on all the inputs that protect the device from possible ESD hits due to handling and production. These ESD protection diodes will act to clamp the voltage at any pin to within 0.5 V of the supplies. They can carry quite high currents but only for a short period of time; thus, they can protect the IC from large pulses of short duration (the total energy is still quite low). The latchup current is typically 100 mA on all pins.

The maximum dc current that these protection diodes can withstand is 10 mA. Therefore, the maximum current that can be applied to any input is 10 mA. If it is possible for a current in excess of 10 mA to be applied to a pin due to an overvoltage, external protection is required. Protection schemes that can be applied include transzorbs on the power supply lines, series resistors on digital input lines, and resistors and diodes on analog inputs. For example, the external protection could be a resistor in series with the input pin to limit the current into the pin to less than 10 mA. For example, if the maximum overvoltage applied to a pin will be 5 V, a 1 kΩ series resistor in each line will limit the current to 5 mA.

There are a number of application notes and seminar material available on this topic. These are available on *www.analog.com:*

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What about susceptibility to conducted and radiated electromagnetic emissions?

Any Σ-Δ ADC will be susceptible to conducted RF into the inputs, the power supply pins, or the reference. The reason is that spurious RF signals and their harmonics can be averaged by the Σ-Δ modulator and show up as a dc offset or an increase in the noise floor. Radiated RF is a little more difficult to discuss, but similar problems can occur and there are situations where it is necessary to shield the Σ-Δ ADC in a system from large RF fields generated locally within the system.

The amount of protection required will depend on the strength of the local field. There are no hard and fast rules when designing for EMC compatibility as every system will be different. However, there are general guidelines that can be followed:

- Consider the inputs, reference, and power supply pins and ensure that each of these lines is properly filtered up to the required maximum frequency.
- Decoupling capacitors on the power supply, mounted locally to the IC, possibly a small inductor between the analog and digital supplies.
- Filtering on the reference and the inputs is also critical.
- A solid low impedance ground plane and separation of the analog and digital grounds.

These are all the usual good practices with the ground plane running under the whole of the IC. The evaluation board provides a good starting point.

Occasionally, it is necessary to provide a Faraday shield for an ADC if the part is operating in the presence of high EM fields such as next to a power supply or relay or RF transmitter. However, this is an exceptional case.

As a component manufacturer, Analog Devices does not perform EMC testing as a general rule since EMC is a system level specification rather than a component specification. It is the responsibility of the PCB designer to ensure that sensitive parts of the circuitry are protected from spurious signals. We don't have guaranteed bulletproof EMC design that we can give to customers, but if you use the evaluation board and follow standard practices for layout, grounding, and decoupling, it is possible to design a system that meets the CE mark and beyond without expending too much design effort. The final chapter in all our seminar books is dedicated to hardware design techniques and deals with such issues as

grounding, decoupling, parasitic thermocouples, and good PCB design. *www.analog.com/hardware_designtech_sec10.*

Analog Performance FAQs

How is the programmable gain function implemented?

The AD779x uses an instrumentation amplifier to implement the gain stage when the gain is set between 4 and 128. For a gain of 2, the gain is implemented capacitively (the reference capacitor in the modulator is halved). An instrumentation amplifier was used for the higher gains, as it consumes less power than a capacitive PGA.

The data sheet mentions that the analog input of the ADC can accept bipolar inputs of ±30 mV centered around 0 V when the buffer is not used. Can a 3 V/5 V single supply part really do this?

Yes! Each analog input has ESD diodes from the pin to AVDD and to GND. The input stage is truly differential; in theory, it can tolerate negative input voltages. However, leakage through the ESD protection diodes limits the ability to handle negative voltages. The diodes will turn on when the voltage across them is 300 mV approximately. This turn-on voltage is temperature dependent. The effect of leakage through these diodes is to increase the noise at the input and, hence, reduce the overall resolution. Analog Devices guarantees full data sheet performance for analog inputs of ±30 mV over the full specified temperature range (gain = 1 or 2, and buffer disabled).

What voltage is within specifications on the analog input pins?

The analog input pins can tolerate a voltage from GND – 30 mV to AVDD + 30 mV when the gain is equal to 1 or 2 and the buffer is disabled. When the buffer is enabled, the buffer itself will require some headroom. The absolute voltage on the analog input pins must be between GND + 100 mV and AVDD – 100 mV. The buffer will be nonlinear outside this range, so the device will be unable to meet the data sheet specifications. When the in-amp is enabled (gains of 4 or higher), the in-amp itself requires some headroom. Hence, the absolute voltage on an analog input pin is now limited to GND + 300 mV and AVDD – 1.1 V. If the analog input is outside this range, the ADC will function; but the part will not meet the data sheet specifications, as the in-amp is nonlinear near the power supply rails.

The ADC is seeing overvoltages in my application. How can I protect the ADC against these overvoltages?

The analog input pins can tolerate a voltage between GND – 0.3 V and AVDD + 0.3 V. There are ESD diodes connected from each analog input to AVDD, and from each analog input to GND. If an overvoltage is seen on the analog input (a voltage that is in excess of 500 mV outside the power supply rails), these diodes will turn. These ESD diodes provide a low resistance path so the overvoltage is directed away from the ADC's modulator. However, the ESD diodes can only tolerate a continuous current less than 10 mA. To prevent damage of the ADC, some external resistance is required so the current is limited to less than 10 mA.

Using external limiting resistors prevents the ADC from getting damaged. However, the external overvoltage may cause the on-chip registers to be corrupted.

To prevent the internal registers from being corrupted, the overvoltage needs to be directed away from the ADC. Connecting Schottky diodes from each analog input to AVDD and GND is one method that can be used. The Schottky diode must have a turn-on voltage of 300 mV. This ensures that the external diode turns on before the ADC's internal diodes so the overvoltage is directed away from the ADC. Since the ADC does not experience any overvoltage, the on-chip registers will remain intact.

When the ADC is operated with the inputs shorted, different output codes are obtained depending on whether the part is operated in buffered or unbuffered mode. Is this normal?

If an internal offset and gain calibration is performed when the buffer is selected or deselected, the same code should be obtained from the ADC in both buffered and unbuffered mode within the noise limit of the part. If a calibration is not performed, it is quite possible to see a different output code in buffered and unbuffered mode for the same input voltage. The buffer is similar to an operational amplifier; therefore, it will have an offset voltage. When the user switches between buffered and unbuffered mode, a calibration is essential to remove this offset.

It is important to remember that a calibration must be performed whenever the filter word, input range, or the mode of the buffer is changed. The data sheet includes noise tables that list the expected noise and code spread for the various operating conditions.

I'm measuring the input leakage current in unbuffered mode. It is significantly higher than the value specified in the data sheet. Why is this?

Static leakage current is specified in the data sheet. The dynamic leakage current (the leakage current when the ADC is converting) is not specified. If you put the ADC into unbuffered mode and measure the input current, you will observe a combination of leakage current and the dynamic current charging and discharging the sampling capacitor. If the dynamic charging current is likely to be a problem in your application (for example, if you have a high source impedance) you can use the on-chip buffer to isolate the input from these dynamic charging currents. However, this will result in reduced input common-mode voltage. The buffer input common-mode range is 1.1 V below VDD and 300 mV above AGND compared to a common-mode range of 30 mV above VDD and 30 mV below AGND for unbuffered mode.

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If you use the ADC in unbuffered mode, large RC constants on the input can interact with the internal sampling capacitor and effectively starve the sampling capacitor of charging current. This will cause gain errors in the ADC. The solution is either to use buffered mode or ensure that you respect the maximum RC values given in the data sheet.

The reference inputs are also unbuffered; as with using the analog inputs in unbuffered mode, the RC loading on the reference inputs must be sufficiently low to avoid introducing errors into the conversion process.

How does switching between channels affect throughput?

The output data rate, which is listed in the data sheet, is the rate at which valid conversions are available when continuous conversions are being performed on a single channel. When the user switches to another channel, additional time is required for the Σ-Δ modulator and digital filter to settle. The settling time associated with these converters is the time it takes the output data to reflect the input voltage following a channel change. To accurately reflect the analog input following a channel change, the digital filter must be flushed of all data pertaining to the previous analog input. With the AD779x parts, it takes two times the programmed output data rate (conversion time) to clear the filter due to chopping. Therefore, if the output data rate is 16.6 Hz, for example, the time required to generate a valid conversion after switching channels equals [$1/(2 \times 16.6$ Hz)].

When a channel change occurs, the digital filter and modulator are automatically reset; DRDY goes high and will remain high until a valid conversion is available from the new analog input channel. Therefore,

following a channel change, DRDY will remain high until the digital filter has calculated a valid conversion (that is, it will remain high for two conversion cycles).

When a step change occurs (on the analog input channel being converted), the ADC is not reset. The ADC continues to output conversions, and DRDY continues to pulse when a conversion is valid. However, the conversions will not be valid, as the digital filter will require two conversion periods to generate a digital word relevant to the altered analog input. If the step change occurs at the beginning of a conversion cycle, the ADC will output a valid word two conversion cycles later. However, if the step change occurs asynchronously so that it occurs in the middle of a conversion, the ADC needs to complete the present conversion and then perform two more conversions to generate an output valid to the new analog input. Therefore, it may take three conversion cycles from the instant at which the step change occurs to the instant at which a valid conversion is available.

In summary, the channel switching speed is one half the data output rate. Therefore, in switching applications, such as data acquisition systems, it is important to realize that the rate at which conversions are available is two times less than the output data rate achieved when continuously sampling a single channel.

With the AD7794 and AD7795, chopping can be disabled. With chopping disabled, the settling time is equal to the conversion time. So, the ADC operates as a zero-latency ADC when chopping is disabled. Therefore, when switching between channels, a conversion will be available at 1/output data rate after the channel change.

What is the ESD rating for the AD779x?

The AD779x pass 1.5 kV (human body model) and pass 250 V (FICDM model).

Are there any suggested protection schemes against ESD that should be considered with these products?

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Explain the converter noise with respect to the noise tables in the data sheet and the sources of this noise.

The noise tables in the data sheet show the output rms noise for the selectable output data rate for the part. The numbers given are for the bipolar input ranges with a specified reference and VDD supply used. These noise numbers are typical and are generated at an analog input voltage of 0 V, based on 1000 conversion results at the specified output data rate. The rms noise numbers are also converted to effective resolution in bits. These numbers can be represented as effective resolution in bits rms or bits

peak-to-peak. Effective resolution in bits rms is defined as the magnitude of the output rms noise with respect to the input full scale ($2 \times V_{REF}$/gain). It is important to note that the peak-to-peak numbers represent the resolution for which there will be no code flicker. They are not calculated based on rms noise but on peak-to-peak noise.

Peak-to-peak noise = $6.6 \times$ rms noise
Bits (peak-to-peak) = effective bits (rms) − 2.5

The numbers given are for bipolar input ranges. For the unipolar ranges, the rms noise numbers will be the same as the bipolar range, but the peak-to-peak resolution is based on half the signal range, which effectively means losing 1 bit of resolution.

The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second is that when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

For example, consider the AD7794 operating with a 4.17 Hz output data rate, a 5 V power supply, and a 2.5 V reference. With a gain of 128, the rms noise equals 41 nV as given in the data sheet.

When operated in bipolar mode, the full-scale analog input is 5 V/128 = 39 mV. The peak-to-peak noise is 6.6×41 nV = 270.6 nV peak-to-peak. Therefore, the ratio of full-scale input to peak-to-peak noise is 39 mV/270.6 nV = 144124, which is the resolution in counts. Converting this to bits peak-to-peak: log(144124)/log(2) = 17.5 bits peak-to-peak, rounded to the nearest 0.5 bit.

What is the peak-to-peak resolution if the ADC is interfaced to a transducer that generates an analog output of 0 mV to 15 mV?

If the AD7794 is operated with a 5 V power supply, a 2.5 V reference, and an output data rate of 4.17 Hz, the rms noise is 41 nV when the gain equals 128 (full-scale range = 0 mV to 20 mV in unipolar mode). Since the transducer has an analog output range of 0 mV to 15 mV, the peak-to-peak resolution in the application is 15 mV/6.6 $\times$ 41 nV = 55432 counts, which equates to 15.76 bits peak-to-peak. Therefore, there will be no code flicker at the ADC's digital output to the 15-bit level.

What is the bandwidth of the AD779x?

The −3 dB bandwidth is equal to $0.24 \times f_{ADC}$, where f_{ADC} is the selected output data rate.

Are there benefits to postfiltering the data from a converter?

Improvements in noise performance can be obtained using postfiltering. The on-chip modulator of these converters provides samples at 64 kHz to the digital filter when f_{CLKIN} is 64 kHz. The on-chip digital filter decimates these samples to provide data at an output rate that corresponds to the programmed output rate of the filter. Since the output data rate is higher than the Nyquist criterion (which states that the output data rate must be at least twice the bandwidth), the output rate for a given bandwidth will satisfy most application requirements. However, there may be some applications that require a higher data rate for a given bandwidth and noise performance. Applications that need this higher data rate will require some postfiltering following the digital filter.

For example, if the required bandwidth is 7.86 Hz but the required output data rate is 50 Hz, the data can be taken from the converter at the 50 Hz rate, giving a −3 dB bandwidth of 12 Hz. Postfiltering can then be applied to reduce the bandwidth and output noise to the 7.86 Hz bandwidth level, while maintaining an output rate of 50 Hz.

Postfiltering can also be used to reduce the output noise from the device for bandwidths below 1 Hz. At a gain of 128 and a bandwidth of 1 Hz, the output rms noise is 41 nV. This is essentially device noise or white noise that has primarily a flat frequency response. By reducing the bandwidth below 1 Hz, the noise in the resultant pass band can be reduced. A reduction in bandwidth by a factor of 2 results in a reduction of approximately $\sqrt{2}$ in the output rms noise. This additional filtering will reduce the system throughput.

What output coding is used in unipolar and bipolar mode?

The output coding is straight binary in unipolar mode and offset binary in bipolar mode.

Unipolar mode (binary coding): With an analog input voltage of 0 V, the output code is 0x000000 for the 24-bit parts and 0x0000 for the 16-bit devices. With analog input voltage of V_{REF}/gain, the output code is 0xFFFFFF for the 24-bit parts and 0xFFFF for the 16-bit devices. The output code for any analog input voltage can be represented as follows:

Code = $(A_{IN} \times$ gain $\times$ 2n$)/V_{REF}$ where A_{IN} is the analog input voltage, and n = 16 for the 16-bit parts and 24 for the 24-bit ADCs.

Bipolar mode (offset binary coding): With an analog input voltage of ($-V_{REF}$/gain), the output code is 0x000000 for the 24-bit parts and 0x0000 for the 16-bit parts. With an analog input voltage of 0 V, the output code is 0x800000 for the 24-bit parts and 0x8000 for the 16-bit parts. With an analog input voltage of ($+V_{REF}$/gain), the output code is 0xFFFFFF for the 24-bit parts and 0xFFFF for the 16-bit parts. Note that the analog inputs are pseudo bipolar inputs and the absolute analog input voltage must remain within the common-mode input range at all times. The output code for any analog input voltage can be represented as follows:

Code = 2n − 1 $\times$ [($A_{IN} \times$ I.C./V_{REF}) + 1] where A_{IN} is the analog input voltage and n = 16 for the 16-bit parts and n = 24 for the 24-bit parts.

What is the recommended common-mode input range for the reference inputs?

The common-mode range for the reference input is from GND to AVDD. The reference input is unbuffered; therefore, the common-mode input range includes the supplies.

How is the input range set?

The input range is dependent on the reference voltage, unipolar/bipolar mode selection, and gain setting chosen. In unipolar mode, the input range is given as [V_{REF}(+) − V_{REF}(−)]/gain. In bipolar mode, the input range is given as $\pm$[V_{REF}(+) − V_{REF}(−)]/gain. The gain setting for the PGA is set using bits G2, G1, and G0 in the configuration register. The reference is nominally 2.5 V, but the AD779x can be operated with a reference from 0.1 V to AVDD. When the device is used in fully differential mode, the common-mode voltage can be varied; but the user must ensure that the absolute voltages on the positive and negative analog input terminals be within the specified ranges.

Can an analog input range other than those specified in the data sheet be used?

Yes, the analog input range can be altered. There are two methods to do this:

- A system calibration can be performed during which the user applies the user-specified zero-scale and full-scale voltages to the ADC during the calibration process. The user must ensure that the full-scale value used is within 0.8 V_{REF}/gain and 1.05 V_{REF}/gain for specified operation. The ADC will then continue to meet the noise values listed in the data sheet for the original voltage range. For example, the AD7794 has an rms noise spec of 1.55 μV when operated with an output data rate of 16.7 Hz, an external 2.5 V reference, and a gain of 1, which results in a signal range of 0 V to 2.5 V in unipolar mode. If the new full-scale

value is within 0.8×2.5 V and 1.05×2.5 V, the rms noise will continue to be 1.55 μV.

- The reference voltage can be altered. For example, if an analog input range of 0 V to 1.5 V is required, using a reference voltage of 1.5 V will result in an analog input of 0 V giving an output code of 0x000000 and an analog input of 1.5 V giving a code of 0xFFFFFF. Following a self-calibration with the 1.5 V reference supplying the ADC, the rms noise will be the same as that for a 2.5 V reference that is given in the data sheet. Using the example above, the AD7794 has an rms noise of 1.55 μV when operated with a 16.7 Hz output data rate, a 2.5 V reference, and a gain of 1. If the reference voltage is changed to 1.5 V and a self-calibration is performed, the rms noise will continue to be 1.55 μV assuming the output data rate, gain, etc. remain unchanged. The peak-to-peak resolution equals 19 bits when operated with a 2.5 V reference. With a 1.5 V reference, the peak-to-peak resolution equals $\log(2$ V$/6 \times 1.55$ μV$)/\log(2) = 18.5$. The reduction in peak-to-peak resolution is due to the reduced input signal span.

What crystals does ADI recommend using with the Σ-Δ ADCs, and which parameters are important?

A low drift, high accuracy crystal should be used with the AD779x. With any Σ-Δ ADC, the output data rate and −3 dB point are directly related to the master clock frequency. The initial accuracy determines the output data rate and, hence, the notch locations as the filter notches are dependent on the output data rate. Low drift ensures that the output data rate and, hence, the filter notch locations do not move considerably from the desired locations. For example, with a 16.7 Hz output data rate, the AD779x has notches at 50 Hz and 60 Hz that allow the device to reject mains-injected noise. If the crystal frequency changes, these notches will move, and the rejection at 50 Hz and 60 Hz may degrade. Companies such as CMAC manufacture low drift crystals with high initial accuracy.

I am using the AD779x in my system. When I look at the output of the ADC, I don't get the full resolution; a few of the LSBs are flickering. Why is this happening?

While the AD779x has a resolution of 24 bits or 16 bits, the accuracy of the part varies with output data rate and gain. The data sheet lists the rms noise and achievable accuracy for different output data rates and gains. For example, the AD7794 has a peak-to-peak resolution of 19 bits when the gain is 1 (analog input range of ± 2.5 V when a 2.5 V reference is used), an output data rate of 16.7 Hz is used, and bipolar mode is selected. If the output data rate is changed to 470 Hz, the peak-to-peak resolution is reduced to 16 bits. If the gain is then changed to 128 (± 20 mV input range), the peak-to-peak resolution is reduced to 13.5 bits.

The accuracy of an ADC is specified as effective resolution, or peak-to-peak resolution. The effective resolution is calculated using the rms noise that is given in the data sheet. The effective resolution equals $\log($input span$/$rms noise$)/\log(2)$. The peak-to-peak resolution is the number of bits that do not flicker and is calculated using the peak-to-peak noise, which equals $6.6 \times$ rms noise. Therefore, the peak-to-peak noise also equals $\log($input span$/(6.6 \times$ rms noise$))/\log(2)$.

The data sheet rms noise values are measured with the chosen analog input channel shorted to some voltage such as AVDD/2 (both terminals of the analog input channel are connected to AVDD/2). Therefore, the user should short the analog input on their system board using a similar method to ensure that the best performance is being obtained from the part. After performing a calibration, commence conversions. Using several thousand samples, the rms noise can be calculated, and from these, the peak-to-peak resolution can be determined. The obtained value should be compared with the values given in the data sheet. If the accuracy specified in the data sheet is not obtained, this is due to noise on the circuit board. For example, ensure that ground loops do not exist, and ensure that the power supply is adequately decoupled using a 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor from each power supply to its respective ground. The capacitors should be placed as close as possible to the ADC's pins.

With a constant dc input, the output of the ADC drifts with temperature. Why?

The performance of any ADC varies with temperature. When a calibration is performed at a temperature, the offset error and gain error are minimized at the temperature at which the calibration is performed. However, the offset error and gain error vary with temperature. For example, if you short the analog inputs to some voltage, such as the references voltage, and perform a calibration, the peak-to-peak resolution given in the data sheet for the specific output data rate and gain should be met. If the temperature varies, the ADC output will vary as the offset error and gain error have drifted with temperature. These drifts are specified in the data sheet.

There will also be drift in the remainder of the signal chain. For example, the reference voltage will vary with temperature also. This variation is specified in the voltage reference data sheet. Resistance values also will vary with temperature. Therefore, it is important to use an accurate reference that has low drift along with resistors with tight tolerances. Solder joints on a circuit board will also have thermal qualities. Each solder joint connects two dissimilar metals, which generates a small thermocouple. Therefore, signal paths for analog signals such as the analog inputs should be kept identical. This will ensure that effects outside the ADC on the analog input lines due to temperature variation are matched and will be removed as a common-mode effect.

The integral nonlinearity is expressed as % of full scale. For what gain setting is this valid?

The INL spec is valid for all gain settings.

What is the link between random conversion noise, peak-to-peak, and rms noise given in the data sheet?

Assume that the noise is truly random and is described by a normal distribution (white noise):

$$V_{NOISE} \text{ (peak-to-peak)} = V_{NOISE} \text{ (rms)} \times 6.6 \text{ (for 99.9\% of the time)}$$

Refer to the AN-615 Application Note, *Peak-to-Peak Resolution vs. Effective Resolution* at *www.analog.com/AN-615* for more detailed information.

Do I need an antialias filter for my Σ-Δ converter?

Yes, an antialias filter is required. However, because a Σ-Δ converter oversamples the analog input, the design of the antialias filter is greatly simplified compared to an ADC that samples at the Nyquist rate (maximum signal bandwidth $\times$ 2).

The AD779x uses a digital filter. As the filter is digital, the frequency response is reflected around the sampling frequency (64 kHz). This means that the filter will provide 0 dB of attenuation at frequencies that are integer multiples of the sampling frequency. Therefore, an antialias filter in the analog domain is required to adequately attenuate these frequencies; usually a single-pole (possibly a 2-pole) RC filter is all that is required. A 1 kΩ resistor in series with each analog input, a 0.1 μF capacitor from $A_{IN}(+)$ to $A_{IN}(-)$, and a 0.01 μF capacitor from each analog input pin to GND is recommended when the analog input channel is buffered.

When the Σ-Δ converter is operated in unbuffered mode, the inputs look directly into the sampling capacitor of the modulator. The modulator is continually charging and discharging the sampling capacitor. If the time constant of the antialiasing filter is too large, the modulator may be unable to fully charge the sampling capacitor—and gain errors will result. To prevent the R-C combination from introducing errors, the data sheet for each ADC specifies the maximum allowable R and C values that can be used for the different gain settings in unbuffered mode.

Which reference should be used with the AD779x?

A low noise reference source is required to achieve the best performance from the ADC. Some of the AD779x devices include an internal, 1.17 V reference that has a drift of 15 ppm/°C. Suitable external references include the ADR391 and ADR381. It is recommended to decouple the output of these references to further reduce the noise level.

In applications such as pressure measurement systems or weigh scales, the excitation voltage for the bridge can be used to derive the reference voltage for the ADC also. If the excitation voltage is equal to or less than AVDD, it can be connected directly to the reference pins of the AD779x device, as the AD779x can accept reference voltages up to AVDD. In these applications, the effect of the noise in the excitation voltage will be removed as the application is ratiometric.

How does the internal temperature sensor work?

When the temperature sensor is selected and bipolar mode is selected, the device should return a code of 0x800000 when the temperature is 0 K. A one-point calibration is needed to get the optimum performance from the sensor. Therefore, a conversion at 25°C should be recorded and the sensitivity calculated. The sensitivity is approximately 0.81 mV/°C. The equation for the temperature sensor will be

$$\text{Temp (K)} = ((\text{Conversion} - 0x800000) \times V_{REF}/2^{23} \text{ K})/0.81 \text{ mV}$$

$$\text{Temp (°C)} = \text{Temp (K)} - 273$$

$$\text{where } V_{REF} = 1.17 \text{ V}$$

So, for example, the device returns a code of 0x9A1F77 at room temperature. This equates to 0.238 V. The temperature is therefore 0.238 V/0.81 mV = 295 K. So, the temperature is 295 − 273 = 22°C.

I am using the internal bias voltage generator to bias a signal. However, the generator is introducing noise into the conversions. Why?

The bias voltage, which is equal to AVDD/2, is generated by attenuating the power supply voltage AVDD. It is a buffered version of the attenuated signal. Any noise in the power supply will be present on the bias voltage also. The bias voltage is made available on $A_{IN}(-)$. If there is no external filtering on $A_{IN}(+)$ and $A_{IN}(-)$, then the voltage on $A_{IN}(+)$ and $A_{IN}(-)$ is the same so the conversions are not affected by the bias voltage noise (it appears as a common-mode signal). In applications such as thermocouple, a lot of external filtering may be used. The bias voltage is not affected by these filters at $A_{IN}(-)$. However, a filtered version of the bias signal appears at the $A_{IN}(+)$ pin. Since the signal at $A_{IN}(+)$ no longer matches the signal at $A_{IN}(-)$, the ADC will see the difference between the signals. This difference will affect the conversions within the ADC. To prevent this, the bias voltage needs to be applied differently. The bias voltage needs to be applied at the same point to both $A_{IN}(+)$ and $A_{IN}(-)$, that is, the bias voltage needs to be applied at the external filter so both $A_{IN}(+)$ and $A_{IN}(-)$ see a filtered version of the bias voltage. So, an external bias can be applied to $A_{IN}(+)$ and $A_{IN}(-)$. Alternatively, if the ADC has an unused channel, the bias voltage can be made available on this unused channel, then applied to both $A_{IN}(+)$ and $A_{IN}(-)$.

Serial Interface FAQs

How does the serial interface operate?

The serial interface on this family of converters is implemented as a state machine. The interface works by counting clocks on each data transfer. Therefore, if you are performing a write operation to one of the ADC's 16-bit registers, 16 SCLK cycles must be applied to the ADC, and the converter will transfer in the 16 bits of data on the DIN line on each of the eight SCLK cycles. When this operation is complete, the part returns to a state in which it expects the next operation to be a write operation to the communications register. This happens regardless of which register has been accessed and whether a read or write operation has taken place. The ADC knows how many clock cycles should be in a transfer to/from a particular register and in this way knows when the transfer is complete.

The first bit of the communications register is a gating bit that must be set to 0 to access the communications register. If there is a 1 on the DIN line when the part is expecting a write to this bit, the part effectively wraps itself around to monitoring that bit. If there is a 0 on the DIN line when the part is expecting a write to this bit, the part continues to load the next seven bits of the communications register on the next seven SCLK cycles.

The serial interface on these converters consists of four signals: $\overline{CS}$, SCLK, DIN, DOUT/$\overline{RDY}$. The DIN line is used for transferring data into the on-chip registers while the DOUT/$\overline{RDY}$ line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT/$\overline{RDY}$) occur with respect to this SCLK signal. The DOUT/$\overline{RDY}$ pin operates as a data ready signal also, the line going low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when not to read from the device. This is to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select the device. It can be used to decode the individual converters in systems where a number of parts are connected to the serial bus.

The serial interface can operate in 3-wire mode by tying the $\overline{CS}$ input low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the converter. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port bit. For microcontroller interfaces, it is recommended that the SCLK idle high between data transfers.

These converters can also be operated with $\overline{CS}$ used as a frame synchronization signal. This scheme is suitable for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$ since $\overline{CS}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers provided the timing numbers are obeyed.

What is the recommended initialization sequence for the AD779x?

On power-up, it is advisable to perform a reset by writing 32 ones to the AD779x. This will reset the serial interface, and it will also reset the on-chip registers to their default conditions. The device does have a power-on reset function. However, any glitches during power-up can cause corruption of the registers, so a reset in the initialization routine is advisable.

After the reset, the device can be configured for the application. Each channel to be used in the application should be selected in turn, the operating conditions for that channel selected, and the channel calibrated.

A write to the mode register is required to set the output data rate and the clock source, configure the power switch, and set the operating mode. A write to the configuration register is required to select the channel and the reference source and set the gain. Calibrations can then be initiated.

Are there any precautions that should be taken to make the interface more robust?

The interface implementation on these converters is basically a state machine that counts clock pulses and defaults to waiting for a write to the communications register when an operation is complete. When the communications register is written to, specifying a write to the mode register, for example, the ADC knows that 16 clocks are required to clock in the data. Spurious clocks on the interface cause the interface to lose synchronization, leading to wrong registers being addressed and thereby corrupting the interface. Tying DIN high between write operations prevents invalid data being written to the ADC.

The first bit in the write operation to the communications register is a gating bit that must be 0 to allow the remaining seven bits to be clocked into the register to specify the next operation. To avoid the possibility of interface issues due to spurious clocks, it is advised to take the DIN line of the converter to a logic high as soon as each write to the converter is complete. Since these converters default to waiting for a write to the communications register, taking DIN high when it has completed a sequence prevents invalid data being written to the communications register if spurious clocks occur. At this time, the ADC is waiting for a 0 on DIN before it enables further data into the register. If the part is set up for a write to the communications register with the DIN high, it is effectively immune to spurious serial clocks. This will not prevent spurious clocks received during a write operation from corrupting the interface.

If the interface does get corrupt, what are the options to regain control of the ADC?

Writing 32 ones to the interface will reset the serial interface into a known state where the ADC is waiting for a write to the communications register. This resets the interface and all of its internal registers to their power-on reset values.

How do I interface to multiple ADCs over the same serial interface?

A single microcontroller/DSP can be used to communicate with several AD779x devices. The $\overline{CS}$ input of the ADC can be used to enable or disable the serial interface of the ADC. By controlling the $\overline{CS}$ inputs to the ADCs using a decoder, the microcontroller/DSP can communicate with each ADC individually or simultaneously. The following figure shows the interface between a microprocessor and several ADCs. The $\overline{CS}$ input of each ADC is connected to the decoder. Using the decoder, the microprocessor can select the ADC with which it wants to transfer data/instructions. When $\overline{CS}$ is high, the serial interface of the ADC is disabled and it ignores any activity on the data bus. To communicate with the ADC, its $\overline{CS}$ line can be taken low. The ADC will then have access to the data bus between itself and the microprocessor. The data sheet should be consulted for timing specifications.
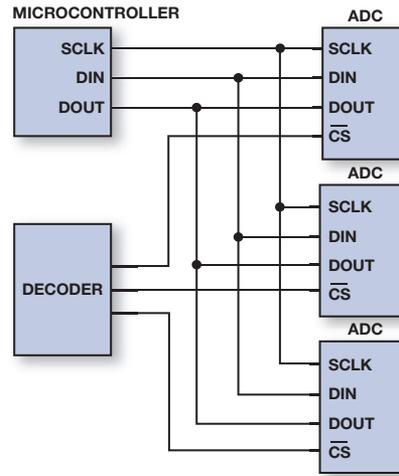
Interfacing several ADCs to a single microcontroller.

When reading from the AD779x, only the first read after power-up is successful. All subsequent read operations give invalid results. What could be happening?

It is probable that the digital interface is entering an unexpected state following the read operation. When using the digital interface of the AD779x, it is critical that the correct number of clock cycles is provided when reading from or writing to the control registers. If one extra clock cycle is provided and a write operation is then attempted, the part will enter an unexpected state. Similarly, if less than 16 clocks are provided when reading from a 16-bit register, the interface will lose synchronization.

Another probable cause is spurious clocks on the SCLK line. The first bit of any write to the communications register is a 0. The ADC will ignore bus activity until it receives a 0. If DIN is left low after performing a read, any spurious clocks on the SCLK line will clock a bit into the communications register. The next time that eight bits are written to the communications register, only the first seven bits will be loaded, and the eighth bit will be interpreted as the first bit of a subsequent write. This problem can be avoided by pulling DIN high after each write.

If the $\overline{CS}$ line is being used as a frame synchronization signal, ensure that this line is brought high at the correct time. Also ensure that the correct number of clock pulses have occurred before $\overline{CS}$ is brought high.

If the interface does lose synchronization, writing 32 ones into the device will reset the interface and the on-chip registers to their power-on values.

What is the sequence of events when switching between channels for the AD779x?

Every sequence of events with this converter commences with a write to the communications register to specify the next operation. The sequence of events for a channel switching operation using the AD779x is as follows (channels $A_{IN}1(+) - A_{IN}1(-)$ and $A_{IN}2(+) - A_{IN}2(-)$ being used). The operating conditions for both channels are gain = 1, buffer on, bipolar mode; external reference applied between $REF_{IN}1(+)$ and $REF_{IN}1(-)$ is reference source for the ADC. The AD779x is a 24-bit part. Every sequence of events with this converter commences with a write to the communications register to specify the next operation to be performed. When the specified operation is complete, the interface defaults to waiting for the next instruction.

Write 0x10 to communications register: This specifies that the next operation is a write to the configuration register.

Write 0x0010 to configuration register: This configures the AD779x for the above gain, polarity, and reference source and selects Channels $A_{IN}1(+) - A_{IN}1(-)$.

Write 0x58 to the communications register: This specifies that the next operation is a write of the data register.

Poll DOUT/$\overline{RDY}$: Poll the DOUT/$\overline{RDY}$ pin to determine if valid data is available in the data register. When DOUT/$\overline{RDY}$ goes low, apply 24 serial clocks to clock the data from the ADC. A read should not be initiated when DOUT/$\overline{RDY}$ is high.

Write 0x10 to communications register: This specifies that the next operation is a write to the configuration register.

Write 0x0011 to configuration register: This configures the AD779x for the Above gain, polarity, and reference source and selects Channels $A_{IN}2(+) - A_{IN}2(-)$.

Write 0x58 to the communications register: This specifies that the next operation is a write of the data register.

Poll DOUT/$\overline{RDY}$: Poll the DOUT/$\overline{RDY}$ pin to determine if valid data is available in the data register. When DOUT/$\overline{RDY}$ goes low, apply 24 serial clocks to clock the data from the ADC. A read should not be initiated when DOUT/$\overline{RDY}$ is high.

Continually running through this loop will allow data to be read from each of the channels continuously.

What is the throughput when switching channels?

For the AD7794/AD7795, the throughput time will be ½ of the programmed output data rate when chopping is enabled and equal to the output data rate when chopping is disabled.

For the remainder of the AD779x family, the throughput time will be ½ of the programmed update.

If a conversion is not read and the next conversion is completed, how long does DOUT/RDY go high?

The DOUT/$\overline{RDY}$ pin goes high for approximately 0.8 ms. During this time, the data register is updated with the new conversion data so the user should not attempt to read the data register.

When single conversion mode is used, can $\overline{CS}$ be taken high after the single conversion is initiated?

The serial interface is independent of the sampling process. So, once the single conversion is initiated, the AD779x will power up and perform the single conversion irrespective of the $\overline{CS}$ polarity. So, the user could take $\overline{CS}$ low, initiate the single conversion, and then take $\overline{CS}$ high again. When the conversion is complete, $\overline{CS}$ can be taken low to read the conversion and another single conversion can be started if required.

When $\overline{CS}$ is taken high, the DOUT/$\overline{RDY}$ pin is tristated. Therefore, the DOUT/$\overline{RDY}$ pin will not indicate the end of the conversion. The user can determine the end of the conversion by reading the status register. Alternatively, the conversion time could be timed out by the microprocessor clock.

When information (conversion data or information from the on-chip registers) is read from the ADC, the LSB readback is always 1. Why?

The DOUT and $\overline{RDY}$ functions share a pin on the AD779x. Every time a conversion is completed, the pin goes low, indicating to the microprocessor that a valid conversion is available. When the user requests a read of the data register, the DOUT/$\overline{RDY}$ pin functions as a DOUT pin. When pulses are applied to the SCLK pin, the data is placed on the DOUT pin. The data is output from the AD779x following the SCLK falling edge and is valid on the SCLK rising edge. When the LSB of the data is output, the DOUT/$\overline{RDY}$ pin functions as a $\overline{RDY}$ pin again. The change from the DOUT to the $\overline{RDY}$ function occurs on the last SCLK rising edge. The microprocessor is latching the bits on the SCLK rising edge. So, if the microprocessor is slow, then the DOUT/$\overline{RDY}$ pin is functioning as a $\overline{RDY}$ pin when the LSB is latched into the microprocessor. So, the microprocessor reads the value of the $\overline{RDY}$

pin rather than the LSB, causing the LSB to be a 1. To prevent this, a faster microprocessor must be used. Alternatively, general-purpose input/output pins of the microprocessor can be used to represent a serial interface. By bit-banging, the user has more control over the read instant. By reading the values on the DOUT pin when SCLK is low rather than latching in the data on the SCLK rising edge, all bits of the data read will be valid.

Calibration FAQs

How is self-calibration implemented on the AD779x?

For calibration to occur, regardless of which calibration mode is used on the selected channel, the ADC's on-chip microcontroller must record the modulator output for two different analog input conditions. These are the *zero-scale* and *full-scale* points. With these conversions, the microcontroller can calculate the gain slope for the input-to-output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of either 16 bits or 24 bits.

In self-calibration mode, the ADC determines the calibration points internal to the ADC. The zero-scale point used to determine the calibration coefficients is with both inputs shorted, (that is, $A_{IN}(+) = A_{IN}(-) = AVDD/gain$, internally within the ADC. Signals connected to the analog input pins of the device will not affect the calibration procedure as long as they are within the common range of the input. The full-scale coefficient is determined by applying a voltage of AVDD/gain to the modulator inputs.

Self-calibration mode is invoked in the AD779x by writing to the mode bits (MD2, MD1, and MD0 bits) in the mode register.

In this calibration mode, the shorted inputs' node is switched into the modulator first, and a conversion is performed. The AVDD/gain node is then switched in, and another conversion is performed. DRDY can be used to determine when the calibration is complete and new data pertaining to the analog input is available at the output. DRDY goes high on the initiation of the calibration and will not return low until a conversion result on the external analog input is available.

What is system calibration and how is it implemented?

System calibration allows the converter to compensate for external system gain and offset errors, as well as its own internal errors. Calibration is basically a conversion process on two specific input voltages (zero-scale or offset calibration, and full-scale calibration) from which the offset error coefficient and full-scale error coefficient are determined. With system calibration, the zero-scale voltage and full-scale voltage must be applied to the ADC by the user.

System calibration is a two-step process. The zero-scale point must be presented to the converter first. This voltage is applied to the analog input of the converter before the zero-scale system calibration step is initiated and must remain stable until the step is complete. System calibration is initiated by writing the appropriate values to the MD2, MD1, and MD0 bits of the mode register. The DRDY output from each device indicates when the step is complete by going low, or the mode bits can be monitored via software—these return to idle mode when calibration is complete. After the zero-scale point is calibrated, the full-scale point is applied; and the full-scale system calibration process is initiated by again writing the appropriate code to the MD bits. The full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the duration of the calibration. DRDY goes low at the end of this second step to indicate that the system calibration is complete.

The calibration procedure is dependent on whether unipolar mode or bipolar mode is used. In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function; while in the bipolar mode, it is performed between midscale and positive full-scale.

When performing a system calibration, the zero-scale voltage and full-scale voltage must be switched into the analog input channel of the ADC. This can be performed by using a low R_{ON} SPDT (single-pole double-throw) CMOS switch. One of the switch inputs can be connected to the analog input, which represents the full-scale value, while the other input can be connected to the zero-scale voltage. Using this switch ensures that the signal chains on both analog inputs for the zero-scale calibration and full-scale calibration are identical. By so doing, the system zero-scale calibration will compensate for the insertion loss of the switch. The ADG736 is a dual SPDT switch with a R_{ON} < 4 Ω and matching of better than 0.4 Ω.

When should a calibration be performed on the AD779x family of Σ-Δ ADCs?

A calibration must be performed when there is a change in

- Gain
- Polarity
- Temperature (when switching between channels that share coefficients registers but have different operating conditions)

With any gain change, there will be a matching error between gain ranges, and this error needs to be calibrated out.

Drift errors are due to changes in temperature. Calibration can be used effectively to remove any errors associated with temperature drift. Self-calibration will remove the effects of temperature drift within the ADC itself. System calibration can be used to remove the drift errors in the ADC itself and also the drift errors associated with the front-end signal conditioning circuitry. Chopping continuously removes offset and offset drift; thus, with chopping enabled, internal zero-scale calibrations are not required. If chopping is disabled, then zero-scale calibrations are required.

Therefore, it is important that a calibration be performed when switching between these channels if the operating conditions (gain and polarity) between the two differ. If the two channels are configured identically and self-calibration is used, there is no need to perform a calibration when switching channels. However, if system calibration is being used, a calibration should be performed when switching between channels, as the applied analog input levels may be different.

How often should a calibration be implemented in a system?

To determine the frequency of calibrations within a system, consider

- What accuracy is required from the converter?
- How does drift performance of the ADC limit performance?
- Over what temperature range does the system operate?

Taking these three questions into account will give some indication as to how often a calibration is required. Other system parameters should also be considered when determining how often to calibrate. These are all related to circuit sensitivities to temperature change as follows:

- Parasitic thermocouple effects
- Gain drift due to the reference temperature coefficient
- Drift sources external to the converter

In general, the higher the accuracy requirement, the more often a calibration will be required in order to maintain system accuracy. After a calibration has been performed, high resolution converters like the AD779x

will have some offset and gain drift associated with them. The AD779x's offset drift due to temperature is typically 10 nV/°C, and the gain drift is typically 1 ppm of full-scale range/°C.

In accessing the complete effects on accuracy due to temperature, the temperature effects due to parasitic thermocouples and drift sources external to the converter also need to be factored into the equation.

What is the relationship between analog input and the calibration coefficients?

The equations for the output digital word s. the applied analog input voltage follow:

In unipolar mode, the relationship is

$$\text{Data} = [(0.75 \times V_{IN} \times \text{Gain}/V_{REF}) \times (2^{23}) - (\text{Offset\_Reg} - \text{0x800000})] \times \text{Full\_Scale\_Reg}/\text{0x400000} \times 2$$

In bipolar mode, the relationship is

$$\text{Data} = [(0.75 \times V_{IN} \times \text{PGA\_Gain}/V_{REF}) \times (2^{23}) - (\text{Offset\_Reg} - \text{0x800000})] \times \text{Full\_Scale\_Reg}/\text{0x400000} + \text{0x800000}$$

Where

Data = digital conversion

V_{IN} = applied analog input voltage

Gain = PGA gain setting

V_{REF} = reference voltage

Offset_Reg = value contained in the offset register

Full_Scale_Reg = value contained in the full-scale register

The nominal values of Offset_Reg is 0x800000 and of Full_Scale_Reg is 0x555555.

The 0.75 number will vary slightly from part to part because of manufacturing tolerances.

What is the value or *weight* of an LSB in the offset and gain register?

1 LSB of the offset register is equivalent to approximately 1.3 LSB of the data register, assuming the nominal full-scale coefficients are present. The exact value varies slightly from part to part, and the ratio changes if the full-scale register coefficients are modified.

The exact ratio can be derived by dividing the value in the full-scale register by 0x400000. This gives a value close to 1.33 with the nominal full-scale coefficient of 0x555555. But if the full-scale register is modified by the user, the ratio changes. This occurs since the offset removal is performed before the gain scaling when the ADC is adjusting the converter output.

The full-scale register can be interpreted as a multiplication factor, whose value equals (full-scale coefficient/0x400000.) Since the scaling is done after the offset register is removed, the relative weight of an offset register LSB is different to a data register LSB.

The nominal value of 1.3 for the gain scaling is because the input signal is attenuated by ¾ as part of the ADC conversion. A $^4/_3$ scaling is then required to digitally compensate for this. (This is normally transparent to the user; it's only when manipulating calibration values that this can become apparent.)

The signal flow can be viewed as

[Input Signal] → [PGA] → [Attenuation by 0.75] → [ADC Conversion] →
[Subtract Offset] → [Scale by FS/0x400000] → [Data Register]

If the system offset calibration is done using the ADC's system zero-scale calibration mode with the systems zero-scale point applied as input voltage, then this scaling factor does not need to be accounted for, since the ADC calibration routine will write the correct value into the offset register. It's only if calibrations are done using regular conversions (that is, a result is written into the data register) that a scaling factor is required before writing into the offset register.

For the full-scale coefficient or full-scale calibrations, it is a simple scaling coefficient, so to increase the gain of the ADC by 10%, the full-scale coefficient needs to be increased by 10%.

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