LINEAR TECHNOLOGY

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IN THIS ISSUE

µModule Isolation Solution for High Resolution 1Msps ADCs Reads Data at 100MHz, Serves Multiple ADCs

Brian Jadus

The ideal isolator for an analog-to-digital converter (ADC) is one that is invisible. It manages all the control and data signals, maximizes the sampling rate and minimizes the effects of jitter on SNR performance. The LTM2893 µModule isolator achieves these goals for ADCs with SPI interfaces, in the 1Msps range, and supports a 6000V_{RMS} isolation rating.

The LTC2063 zero-drift, 20kHz amplifier enables high resolution measurement at extremely low power levels. See page page 30.

Reading data from high resolution successive approximation register (SAR) analog-to-digital converters through a digital isolator is limited with more traditional options. When reading from a serial peripheral interface (SPI) most high speed digital isolators max out at 25MHz, with a few specialty devices operating up to 40MHz. The LTM®2893 reads data at up to 100MHz, is flexible, and handles multiple ADCs solving the timing issues and limitations of standard digital isolators interfacing to SAR ADCs.

REASONS TO ISOLATE ADCs

The isolation barrier allows the ADC to float to the common mode of the input signal and absorbs harsh conditions and transients. Even applications that don't require isolation can benefit from it. The LTM2893 makes it particularly easy to add a layer of isolation, improving system safety. For instance, whereas process and test equipment require isolation to protect inputs

(continued on page 4)

LINEAR TECHNOLOGY | NOW PART OF ANALOG DEVICES

In the News

In this issue...

TALE OF THREE BOOKS

Seven years ago, several individuals at Linear Technology met to discuss a major industry challenge: how to teach analog circuit design, and how to get designers excited about the technology. We're all so busy, heads down, doing the hard work of analog design that we sometimes don't take the time to teach what we know in this challenging craft/science of analog design. One of the individuals in this room was well known for walking his talk. His name was Jim Williams.

Jim was well known—and well respected—throughout the analog world, both for the excellence of his circuit design techniques and for his writing. For over thirty years, Jim took the time to write extensive application notes, detailing the fine art and science of analog circuit design. Each of his dozens of app notes was published by Linear Technology, and also handed off to *EDN* magazine, which published each one as a feature article.

Another individual in the room was Bob Dobkin, Linear Technology cofounder and CTO. Bob Dobkin is widely recognized as an analog industry guru, holder of over 100 patents related to linear integrated circuits and mentor of many analog designers.

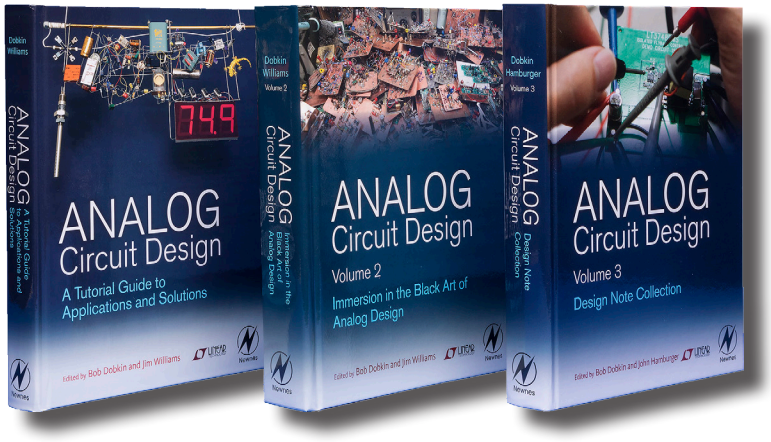
Jim Williams and Bob Dobkin agreed that it would be a useful exercise to compile the deep technical analog application articles by Jim, Bob and other authors into book form as a way of passing on this vast technical expertise to other designers. The result of this effort is a three volume book set published by Elsevier:

- *Analog Circuit Design, A Tutorial Guide to Applications and Solutions*, edited by Bob Dobkin and Jim Williams
- *Analog Circuit Design, Volume 2, Immersion in the Black Art of Analog Design*, edited by Bob Dobkin and Jim Williams
- *Analog Circuit Design, Volume 3, Design Note Collection*, edited by Bob Dobkin and John Hamburger

These books are available from Elsevier and Amazon or via links at www.linear.com/designtools/acd_book.php.

NOW AVAILABLE IN FOUR LANGUAGES

The much anticipated Chinese language version of *Analog Circuit Design, Volume 2, Immersion in the Black Art of Analog Design* is now available from Taobao, Amazon, Xinhua Bookstore and other bookstores, as well as item.jd.com/12097166.html or product.dangdang.com/24167976.html.



The three volume *Analog Circuit Design* book series brings the nuances of analog circuit techniques to a wide audience in both e-book and hardcover formats.

At 1038 pages, the book includes application notes on power management, data conversion and signal conditioning circuit solutions, and an extensive circuit collection of reference designs. The content is based on the research and writings of analog design experts Bob Dobkin and the late Jim Williams, as well as industry experts Carl Nelson and Bob Widlar.

Regarding the new Chinese version of the book, People's Posts & Telecom Press stated, "The *Analog Circuit Design* book has very high credibility, based on the extensive applications. The circuit design techniques can be used to solve almost all circuit problems. In addition, the book includes application examples for engineers, showing design details, design theory, high level solutions, and is an important reference in the field."

People's Posts & Telecom Press is currently working on a Chinese translation of *Analog Circuit Design, A Tutorial Guide to Applications and Solutions*, planned for publication next year.

Japanese language versions of the *Analog Circuit Design* books have also been published by CQ Publishing of Japan. CQ has published the following Japanese editions:

- *Analog Circuit Design, A Tutorial Guide to Applications and Solutions*, which is published in a 2-volume set.
- *Analog Circuit Design, Volume 2, Immersion in the Black Art of Analog Design, Part 1 Power Management*

The next Japanese volume is planned for later this year, and will cover Part 2 of *Analog Circuit Design, Volume 2, Immersion in the Black Art of Analog Design*, including signal conditioning, data conversion, and high frequency/RF. The Japanese language versions can be ordered at shop.cqpub.co.jp

A Korean language version of *Analog Circuit Design, A Tutorial Guide to Applications and Solutions* was published by Acorn Publishing Company in Korea. At 1025 pages, this is a Korean translation of the first *Analog Circuit Design* volume, with extensive analog and power management application writings by Jim Williams, Bob Dobkin, Carl Nelson and other analog experts: www.acornpub.co.kr/book/analog-circuit-design.

Over a year in development, the recently published Chinese version of *Analog Circuit Design, Volume 2, Immersion in the Black Art of Analog Design*, is now available to the China audience.

CONFERENCES & EVENTS

Tech Taipei—IoT Seminar, Fubon International Conference Center, July 6—Showcasing SmartMesh® wireless sensor networks for industrial IoT applications. site.eettaiwan.com/events/iot_2017

IEEE Nuclear and Space Radiation Effects Conference, New Orleans Marriott, New Orleans, Louisiana, July 17–21, Booth 302—Showcasing products for space and harsh environments. www.nsrec.com

Industrial Seminars in China, July 18 in Xian, July 20 in Wuhan—Featuring the latest products and technology for industrial applications. www.01ea.com/invitation/linear/201707

The Battery Show/Electric & Hybrid Vehicle Technology Expo, Suburban Collection Showplace, Novi, Michigan, September 12–14, Booth 904—Presenting battery management system products. www.thebatteryshow.com

General purpose digital isolators and dedicated SPI isolators can be used to isolate ADCs, but such solutions use multiple digital isolators to support signals such as conversion start or busy status signals, in addition to the 3- or 4-wire SPI port.

(LTM2893, continued from page 1)

from damage due to accidental misconnections or overvoltage events, an isolator can also be used as a high voltage level shifter to extend the common mode range or to reduce ground noise. The LTM2893 ignores common mode transient events up to 50kV/µs with a low capacitance isolation barrier and fully differential data communication.

PRIOR GENERAL PURPOSE DIGITAL ISOLATORS FALL SHORT

General purpose digital isolators and dedicated SPI isolators can be used to isolate ADCs, but such solutions use multiple digital isolators to support signals such as conversion start or busy status signals, in addition to the 3- or 4-wire SPI port. Standard digital isolators are limited by the signal propagation delay in sending an SCK signal to the isolated SPI port and waiting for the return of the MISO (SDO) data before the next latching edge of the SCK signal can occur, as shown in Figure 2. This adds propagation delays in addition to the response delay from the ADC SPI port. Adding up all the delays, a read may take up to 38ns from what initially appeared an attractive 150Mbps digital isolator. This reduces the effective SCK frequency to 25MHz or less.

STREAMING ISOLATOR

The LTM2893 is tailored to communicate with ADCs with a dedicated master SPI function on the isolated side and a dedicated slave function with a buffer on the logic side as shown in Figure 3.

The isolated side master SPI engine monitors status signals from the ADC and fetches the data after the BUSY signal goes low. This function initiates without logic side interaction after the start of a conversion.

The logic side slave SPI engine contains a buffer register to receive data from the isolated side through the isolation barrier. During an ADC conversion operation, when the buffer register receives data from the isolated side SPI master, the logic side BUSY signal goes low indicating the SPI slave port is ready to be read.

The LTM2893 has the logic functions to fetch and buffer the data to minimize the data interaction across the isolation barrier. Data is streamed internally at 200Mbps when two ADCs are read at 100MHz.

SAR ADC SPECIFIC SIGNAL ISOLATION

Typical SAR ADCs have a conversion start (CNV) signal to initiate resolving the input signal into a digital result, and a BUSY signal to indicate when the conversion is in progress. The LTM2893 is tailored for SAR ADCs by including a conversion start (CNV) and busy (BUSY) signals to manage communication to the ADC. The conversion start signal is transported through the LTM2893 from the CNV input to the CNV2 output on a rising edge.

The transport of the conversion start signal through the isolator has low jitter to minimize degradation to the aperture jitter of the ADC sample. The BUSY signal remains high after a rising edge of the CNV input and will go low when data

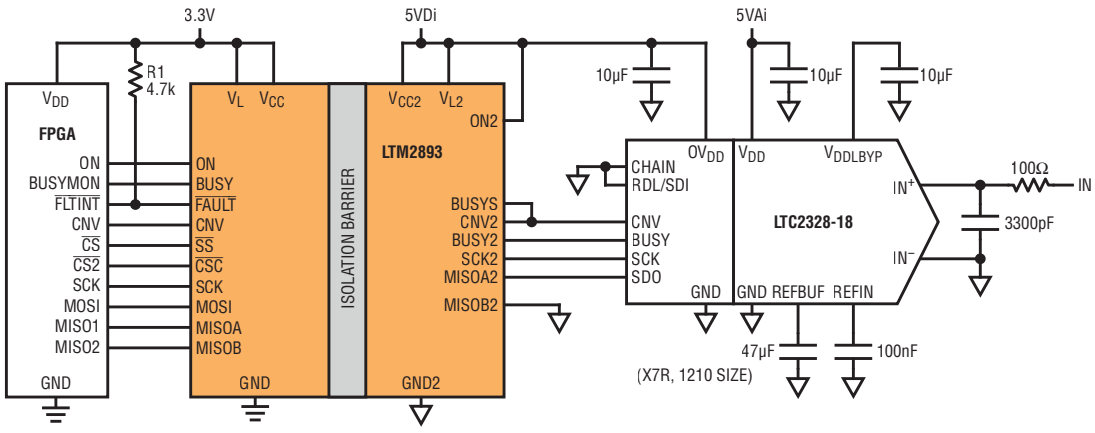


Figure 1. Typical application

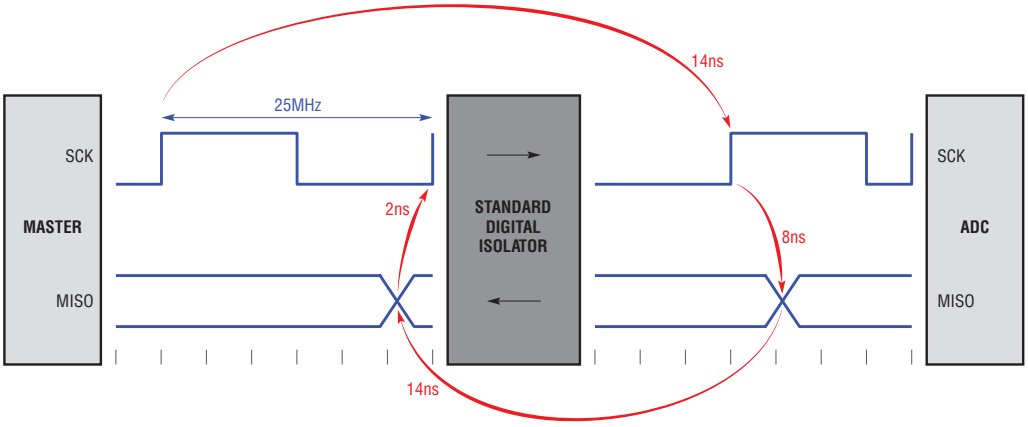


Figure 2. Standard digital isolator SPI read delays can add up to 38ns, reducing effective SCK frequency to approximately 25MHz.

has been received in a local SPI buffer from the isolated side. Once the BUSY signal goes low the local SPI port is ready to be read. ADCs without conversion start and busy signals are also compatible with the LTM2893, by connecting the CNV2 and BUSY2 pins together.

AUXILIARY CHANNELS FOR MULTIPLEXER CONTROL SIGNALS

The LTM2893 provides three signals for controlling functions across the isolation barrier in either direction. The signals are ideal for controlling devices such as an analog multiplexer (Figure 4), a programmable gain amplifier, or control signals on an ADC such as power down or resets. The select signals cannot be used at the beginning or during a conversion, but are ideal for changing settings or making selections prior to starting a conversion. A configuration register allows individual adjustment in the direction of the three select signals.

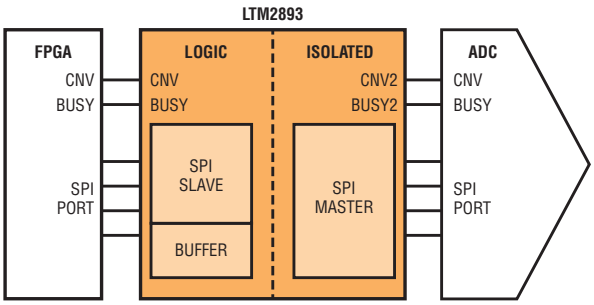


Figure 3. ADC streaming isolator can effectively read ADCs at 100MHz

FLEXIBILITY

The factory sets the LTM2893 SPI port to an SCK2 frequency of 100MHz, with a 24-bit data word length, and a single word count, which is selected to operate directly with the LTC2338, LTC2328, and LTC2378 ADCs. The SCK2 frequency setting is the serial clock frequency used to read data from the ADC. The logic side SPI port can be operated down to 1/128 of the SCK2 frequency setting. The second chip select (CSC) enables writing to two configuration

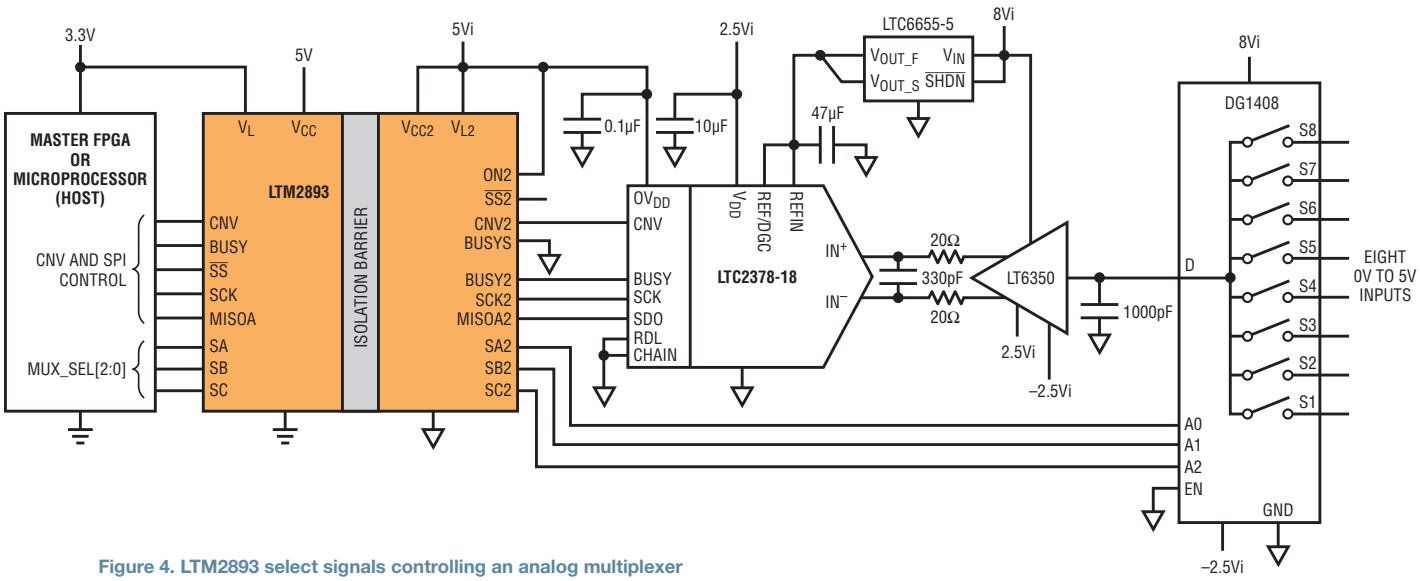


Figure 4. LTM2893 select signals controlling an analog multiplexer

The LTM2893 has a dual read port (MISOA, MISOB) that allows two ADC results to be read simultaneously. Two ADCs can be connected to the isolated side of the LTM2893 and share the CNV2 and SCK2 signals; the BUSYS and BUSY2 signals independently connect to each ADC, while the SDO outputs of the ADCs connect MISOA and MISOB, respectively.

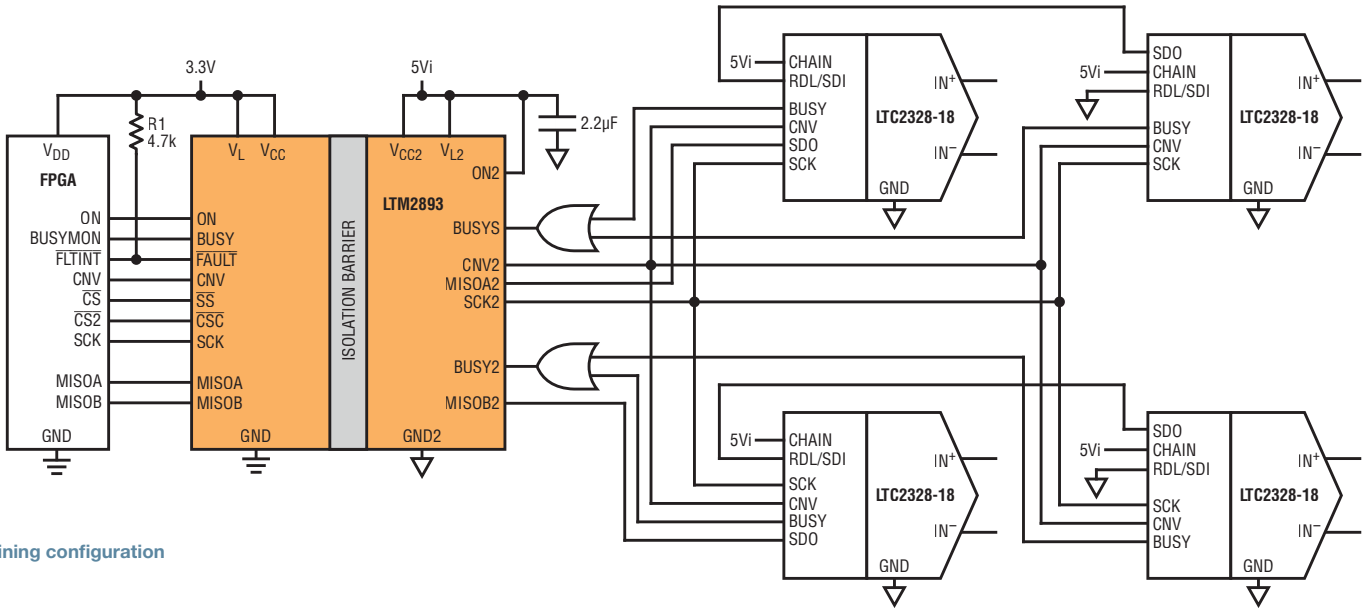


Figure 5. Chaining configuration

registers in the LTM2893 selecting SPI clock speeds, word lengths, and word counts.

The SCK2 frequency has eight selections in the configuration register supporting ADC SPI ports from 100MHz to 6.25MHz.

The 24-bit data word length setting works for a number of our general purpose SAR ADCs with 16-bit to 24-bit results and 1Msps performance. This word length setting defines the number of bits the isolated side SPI master retrieves from the ADC and stores in the logic side buffer. Reading the data from the logic side SPI port does not require reading the full word length. The word length can be optimized in the configuration register for the parameters of the ADC to reduce sampling time or reduce power with eight settings from 32 bits to 8 bits. The word count setting selects how many multiple words are read in a single conversion cycle.

ISOLATING MULTIPLE ADCs

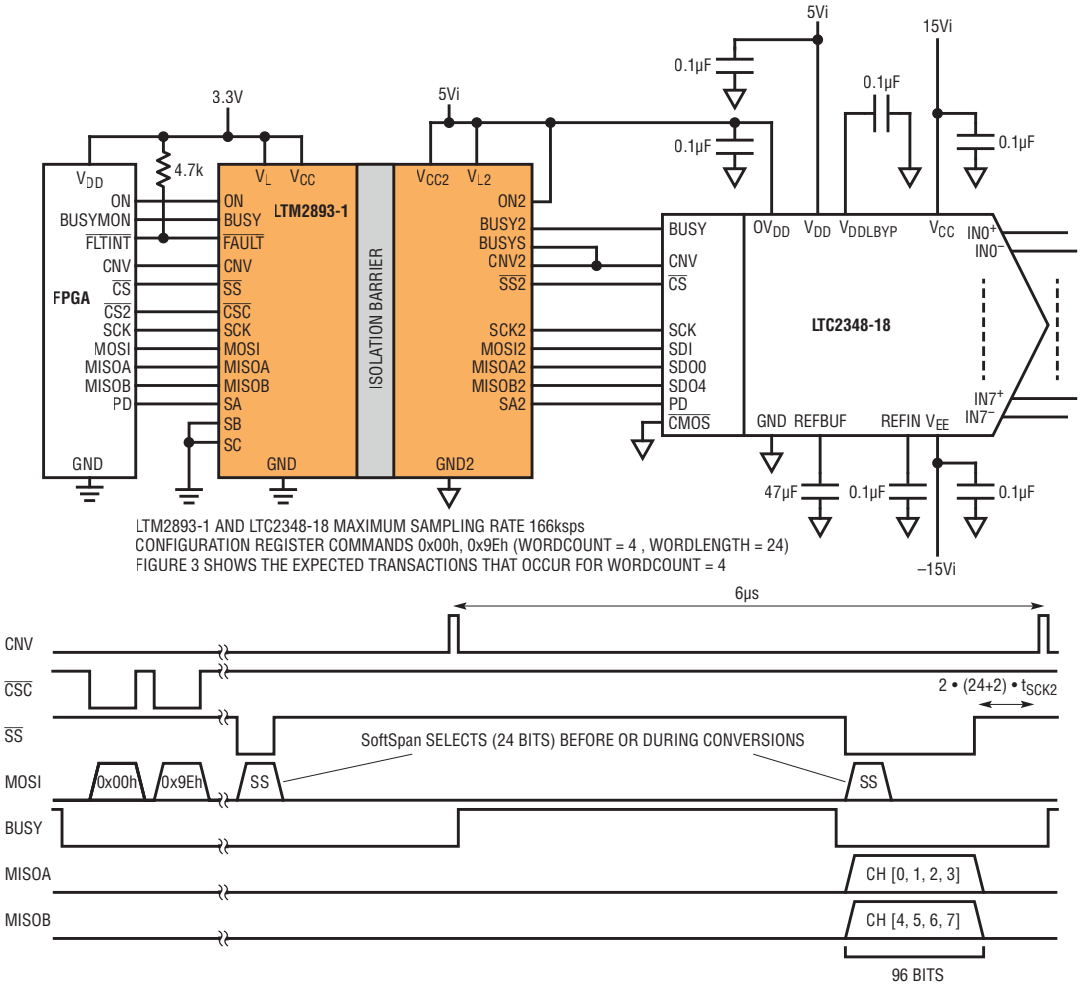
The LTM2893 has a dual read port (MISOA, MISOB) enabling two ADC results to be read simultaneously. Two ADCs can be connected to the isolated side of the LTM2893 and share the CNV2 and SCK2 signals; the BUSYS and BUSY2 signals independently connect to each ADC, while the SDO outputs of the ADCs connect MISOA and MISOB, respectively.

Digital isolators for ADCs and DACs

	LTM2893	LTM2893-1	LTM2895
Function	SAR ADC interface	SAR ADC interface with configuration	DAC or general purpose SPI interface
SPI communication	read only	read/write for LTC2348/LTC2358 ADC family	write with readback
Maximum SCK frequency	100MHz	100MHz	100MHz
Effective number of communicated signals	9 (4 SPI, 5 control)	10 (5 SPI, 5 control)	9 (5 SPI, 4 control)

The LTM2893-1 read and write SPI ADC isolator enables configuring the SoftSpan register and reading all the multiplexed data results from an LTC2348. The LTC2348 ADC family has eight analog inputs that are simultaneously sampled, sequentially converted, and accessed through an 8-output SPI port.

Figure 6. LTM2893-1 and the LTC2348-18



Additionally, with ADCs that support chaining (Figure 5), up to eight ADCs can be connected to a single LTM2893. Reading more than two parallel ADCs requires a write to the configuration register in the LTM2893 to select the number of devices. The configuration register allows the selection of two, four, six or eight devices to be accessed through the two MISOA and MISOB SPI outputs.

ISOLATE THE LTC2348 MULTIPLEXED ADC WITH THE LTM2893-1

Most ADCs require only a read-capable SPI port. The LTM2893 is dedicated to reading ADCs with a read-only SPI port. The LTM2893-1 is dedicated to ADCs with configuration registers such as the LTC2348 simultaneous sampling ADC family, shown in Figure 6.

The LTM2893-1 read and write SPI ADC isolator enables configuring the SoftSpan™ register and reading all the multiplexed data results from an LTC2348. The LTC2348 ADC family has eight analog inputs that are simultaneously sampled, sequentially converted, and accessed through an 8-output SPI port. Connecting ports 0 and 4 to the MISOA2 and MISOB2 inputs of the LTM2893-1 and setting the LTM2893-1 configuration register to a word length of 24 and a device count of 8 shifts two channels of four results per conversion. Adding an isolator to the LTC2348 has a

The addition of any digital isolator can introduce timing jitter resulting in performance degradation. The LTM2893 is designed with a low jitter path for the conversion start signal to minimize degradation in signal-to-noise performance. The system performance of the LTM2893 with a LTC2328-18 is similar to the standalone performance of the LTC2328-18.

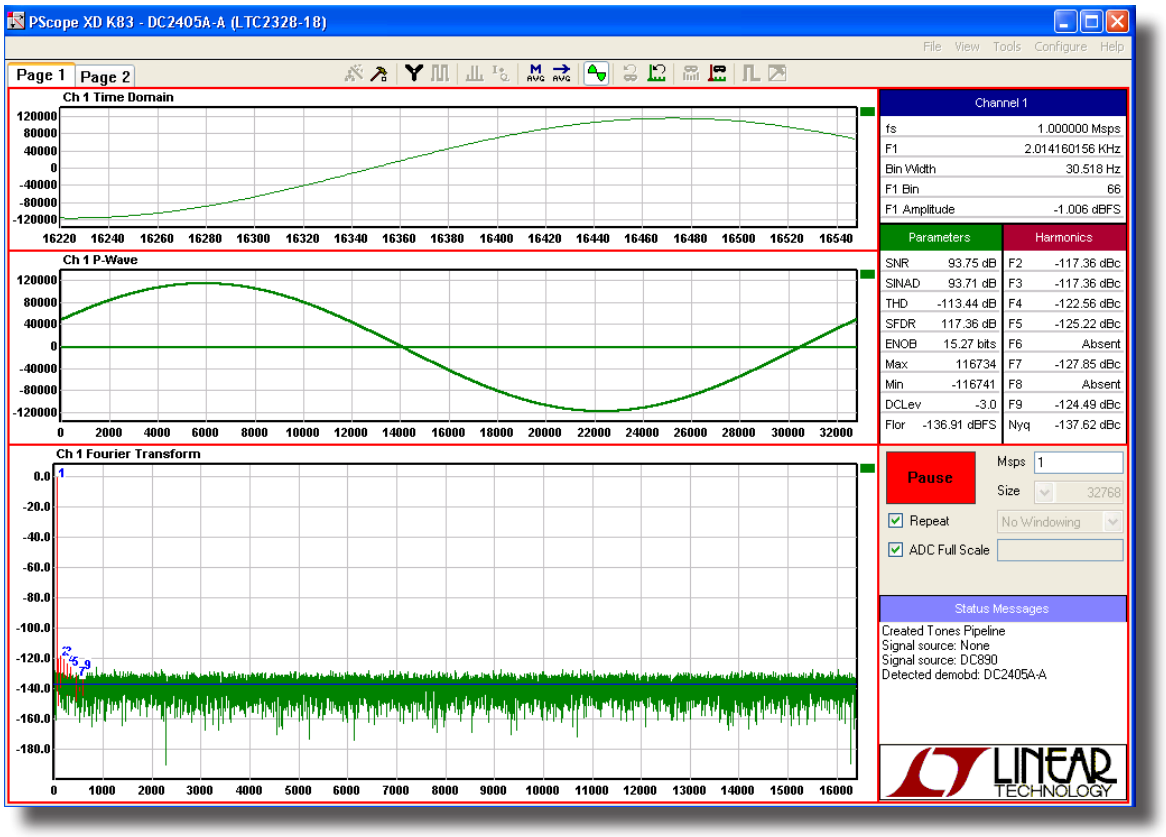


Figure 7. PScope plot of the DC2405A demonstration circuit

small penalty on sampling rate, reducing the ideal speed of 200ksps to 166ksps.

SYSTEM PERFORMANCE

The addition of any digital isolator can introduce timing jitter resulting in performance degradation. The LTM2893 is designed with a low jitter path for the conversion start signal to minimize degradation in signal-to-noise performance. The system performance of the LTM2893 with a LTC2328-18 is similar to the standalone performance of the LTC2328-18. To illustrate this performance, Figure 7 shows a plot of the DC2405A demo board capturing a 2kHz input at –1dBFS with our PScope™ application.

CONCLUSION

The LTM2893 is a fully integrated isolation solution specifically designed for ADC applications. The LTM2893 handles all the necessary signals for accessing ADCs through an isolation barrier with minimal performance degradation. The LTM2893 meets 100MHz SPI operation when interfaced with ADCs. In contrast, other, piecemeal isolated solutions must reduce the clock frequency to overcome propagation delays. The LTM2893's flexible interface allows it to isolate multiple ADCs, reducing overall component count and system complexity, compared to other SPI isolation solutions. Because it is optimized for ADCs, designers can easily add it to any solution requiring a robust interface. ■

High Efficiency, High Density, Switched Capacitor Converter for High Power Applications

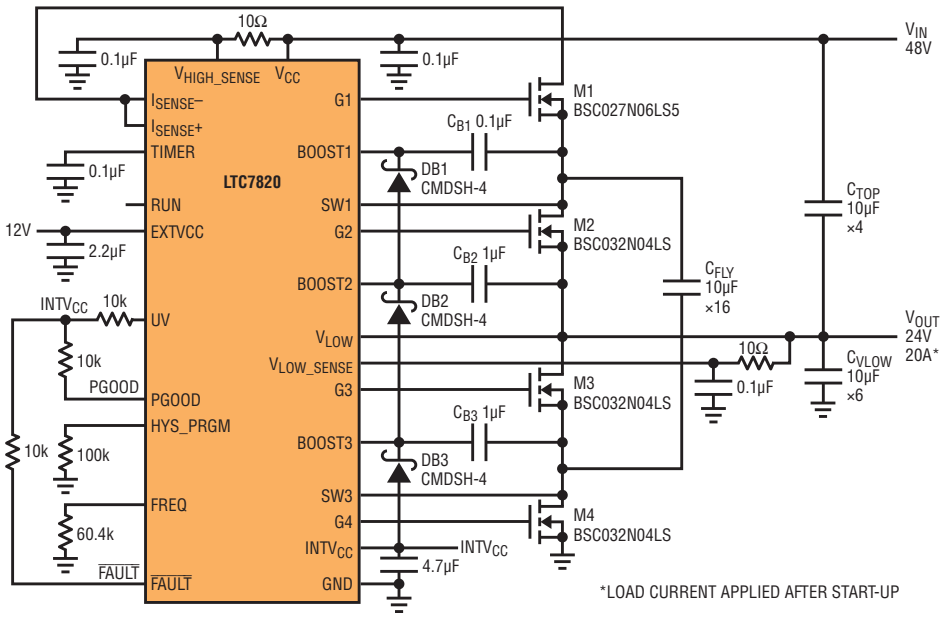
Jian Li, Jeff Zhang, Ya Liu, and Marvin Macairan

The power density of a DC/DC converter is generally limited by bulky magnetic components, especially in applications where the input and output voltages are relatively high. Inductor/transformer size can be reduced by increasing the switching frequency, but this reduces converter efficiency because of switching-related losses. Better, eliminate the magnetics altogether with an inductorless switched capacitor converter (charge pump) topology. Charge pumps can increase power density as much as 10× over a conventional converter without sacrificing efficiency. Instead of an inductor, a "flying capacitor" stores and transfers the energy from input to output. Despite the advantages of charge pump designs, switched capacitor converters are traditionally limited to low power applications, due to the challenges presented in start-up, protection, gate drive and regulation.

The LTC®7820 is a fixed ratio, high voltage, high power switched capacitor controller that yields small and cost-effective solutions for high power, nonisolated intermediate bus applications with fault protection. The LTC7820's features include:

- Low profile, high power density, capable of 500W+
- V_{IN} max for voltage divider (2:1): 72V
- V_{IN} max for voltage doubler (1:2)/inverter (1:1): 36V
- Wide bias V_{CC} range: 6V to 72V
- Soft switching: 99% peak efficiency and low EMI
- Soft start-up into steady state operation
- Input current sensing and overcurrent protection
- Integrated gate drivers
- Output short-circuit/OV/UV protection with programmable timer and retry
- Thermally enhanced 28-pin 4mm × 5mm QFN package

Figure 1. A 48V to 24V/20A voltage divider with a power density of 4000W/in^3

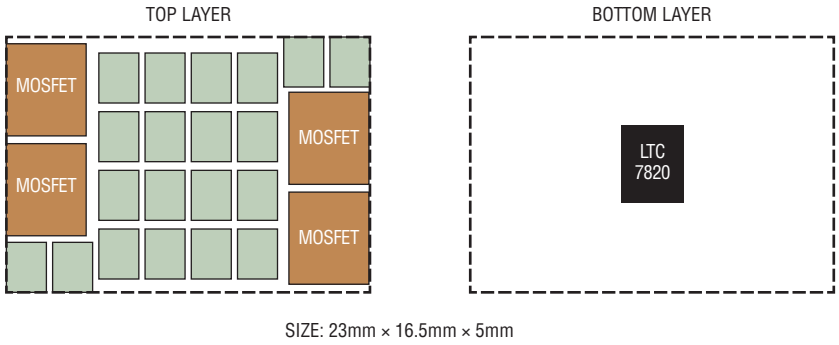


48V TO 24V/20A VOLTAGE DIVIDER WITH POWER DENSITY OF 4000W/IN^3

Figure 1 shows a 480W output voltage divider circuit featuring the LTC7820. The input voltage is 48V and the output is 24V at up to 20A load. Sixteen 10µF ceramic capacitors (1210 size) act as a flying capacitor to deliver the power. The approximate solution size is 23mm × 16.5mm × 5mm as shown in Figure 2, and the power density is as high as 4000W/in^3.

Since no inductor is used in the circuit, all four MOSFETs are soft switched, greatly reducing switching-related losses. The converter can achieve high efficiency, where the peak efficiency is 99.3% and the full load efficiency is 98.4%.

Figure 2. Estimated solution size features 5mm maximum height



HIGH EFFICIENCY

Since there is no inductor used in the circuit, all four MOSFETs are soft switched, greatly reducing switching-related losses. The converter can achieve high efficiency as shown in Figure 3, where the peak efficiency is 99.3% and the full load efficiency is 98.4%. The thermograph in Figure 4 shows a balanced thermal design with a hot spot temperature about 82.3°C in an ambient environment of 23°C and no forced airflow.

PRE-BALANCE PREVENTS INRUSH CURRENTS

In addition to impressive efficiency and thermal performance, the LTC7820 includes a proprietary pre-balance method to minimize inrush current in voltage divider applications. The LTC7820 controller detects the V_{LOW_SENSE} pin voltage before switching and compares it with the $V_{HIGH\_SENSE}/2$ internally. If the voltage at the V_{LOW_SENSE} pin is much lower than $V_{HIGH\_SENSE}/2$, a current source injects 93mA of current at the V_{LOW} pin to pull V_{LOW} up. If the voltage at V_{LOW_SENSE} is much higher than $V_{HIGH\_SENSE}/2$, another current source sinks 50mA from V_{LOW} to pull it down. If the voltage at V_{LOW_SENSE} is near $V_{HIGH\_SENSE}/2$, that is, within the preprogrammed window, both current sources are disabled and the LTC7820 starts switching.

Figure 5 shows the enormous input inrush current that occurs at start-up without pre-charging—more than enough to damage the MOSFETs and capacitors. In

Figure 3. Efficiency at 48V input, 24V output and a 200kHz switching frequency

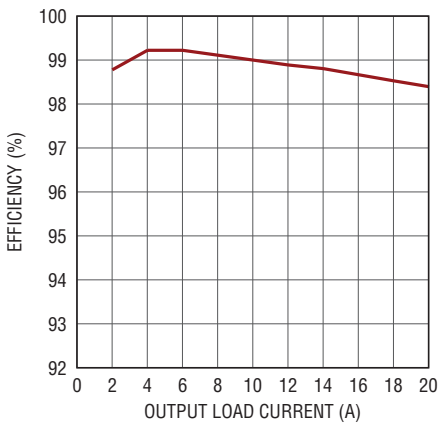
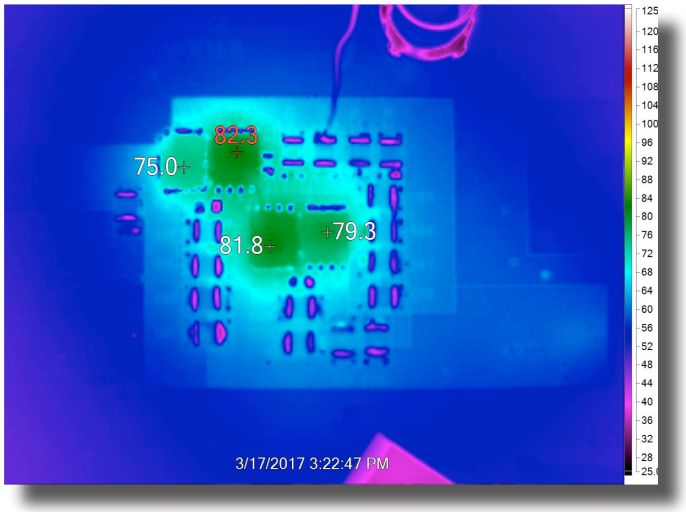


Figure 4. Thermal test at 48V input, 24V output at 20A and 200kHz switching frequency



Even though the LTC7820-based voltage divider is an open-loop controlled converter, load regulation is tight due to its high efficiency, with the output voltage dropping only 1.7% at full load.

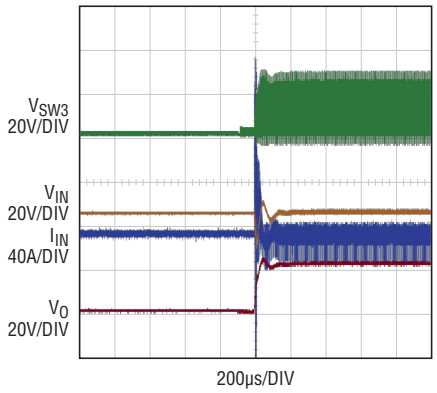


Figure 5. Start-up waveform without pre-balance shows large inrush current

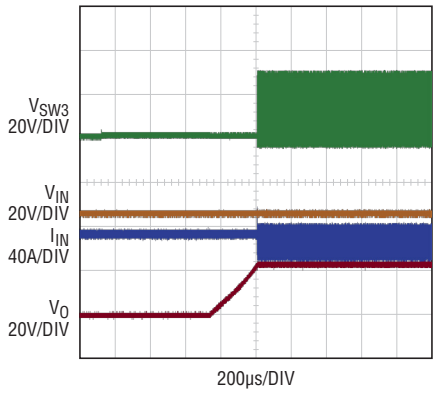


Figure 6. Start-up waveform with LTC7820 pre-balance shows elimination of inrush current

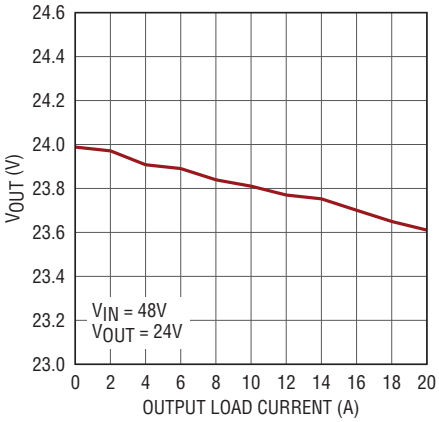


Figure 7. Load regulation

contrast, no excessive inrush current is observed after the pre-balance method is applied, as shown in Figure 6.

TIGHT LOAD REGULATION

Even though the LTC7820-based voltage divider is an open-loop controlled converter, load regulation is tight due to its high efficiency. As shown in Figure 7, the output voltage drops only 1.7% at full load.

PROTECTION FEATURES

The LTC7820 includes protection features to ensure high converter reliability. Overcurrent protection is enabled through a sensing resistor on the high voltage side. A precision rail-to-rail comparator monitors the differential voltage between the I_{SENSE}+ pin and the I_{SENSE}– pin, which are Kelvin connected to a sensing resistor. When the voltage at I_{SENSE}+ is 50mV higher than the I_{SENSE}–, an overcurrent fault is triggered, the FAULT pin is pulled down to ground, and the LTC7820 stops switching and starts retry mode based on the timer pin setup.

Further protection is available through the OV/UV window comparator. In normal operation, the voltage at V_{LOW_SENSE} should approach half of V_{HIGH_SENSE}. A window comparator monitors V_{LOW_SENSE} and compares it to $V_{HIGH\_SENSE}/2$. The hysteresis window voltage can be programmed and is equal to the voltage at the HYS_PRGM pin. With a 100k resistor on the HYS_PRGM pin, the $V_{HIGH\_SENSE}/2$ voltage must be within a (V_{LOW_SENSE} ±1V) window during start-up and normal operation. Otherwise a fault is triggered and the LTC7820 stops switching.

CONCLUSION

The LTC7820 is a fixed ratio high voltage, high power switched capacitor controller that meets the power density demands of bus converters, high power distributed power systems, communications systems and industrial applications. No inductors are needed. ■

Low Power Op Amps: Only 20µA for 1.3MHz, 240µA for 30MHz

Aaron Schultz, Catherine Chang and Philip Karantzalis

Our op amp family has expanded with industry-leading speed versus supply current. For super low 20µA supply current, the LTC6258/LTC6259/LTC6260 (single, dual, quad) provide 1.3MHz at a with 400µV maximum offset voltage and rail-to-rail input and output. The still-low 240µA of the LTC6261/LTC6262/ LTC6263 (single, dual, quad) provide 30MHz with 400µV maximum offset voltage and rail-to-rail input and output. In combination with 1.8V to 5.25V supply, these op amps enable applications requiring good performance with low power and low voltage.

LOW NOISE REFERENCE

One such application is a low noise reference based on the LT6656 precision series voltage reference with a low 1µA supply current. In combination with a simple filter, the LTC6258 can lower the LT6656's effective noise and enhance its output current drive capability while maintaining low total power consumption.

Figure 1 shows the configuration. First, a very low cutoff frequency follows the LT6656 output (R_{IN1} and C_{IN1}, lower than 5Hz cutoff). Large values of R_{IN1} can develop significant offset voltage due to the LTC6258's input bias current. Setting R_{IN1} to 2.7kΩ produces an offset that is lower than the nominal input offset voltage of the op amp. C_{IN1} can be larger or smaller, with more or less filtering accordingly. The voltage withstanding requirement of C_{IN1} is low, resulting in relatively large capacitance in a small volume.

This circuit takes advantage of the ability of the LTC6258 to drive large capacitive loads. Use of a large output capacitor bank attached to the LTC6258 enables significant bypassing of follow-on circuits that use the reference voltage. In total, the combination of LT6656 and LTC6258, in this configuration, develops a reference voltage with low noise, at low power, and with appreciably large bypass capacitance.

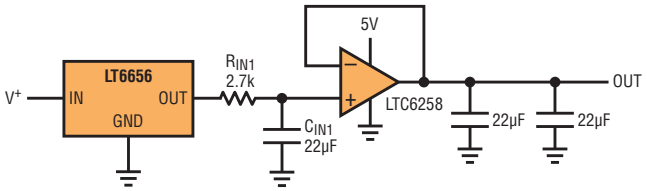


Figure 1. Low noise reference

Voltage spectral noise densities are shown in Figure 2. Greater noise from the reference below 10kHz drops down once a filter (R_{IN1} and C_{IN1}) follows the reference. The op amp, configured in unity gain, with or without a large 44µF load, remains stable and contributes only a small amount of low frequency noise. Figure 3 shows the transient response of the combination of R_{IN1} – C_{IN1} filter and op amp circuit, with and without the 44µF output capacitor.

Importantly, there is no appreciable degradation in the output voltage accuracy with the introduction of the LTC6258 into the reference circuit. The LT6656 A-grade accuracy is 0.05%. At 1.25V, the

Figure 2. Buffer noise density

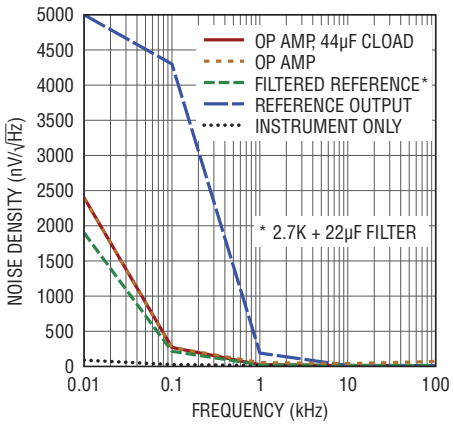
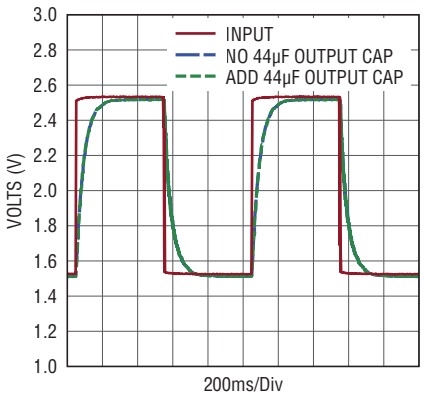


Figure 3. Reference buffer transient response



One such application is a low noise reference based on the LT6656 precision series voltage reference with a low 1µA supply current. In combination with a simple filter, the LTC6258 can lower the LT6656's effective noise and enhance its output current drive capability while maintaining low total power consumption.

error is ±625µV; the B-grade with 0.1% the error is ±1.25mV. Use of the LTC6258 with 400µV offset max will add some nominal output voltage uncertainty, but well within the order of magnitude of the LT6656's initial error. Measured supply current consumption is 21µA.

UTILITY SINE WAVE

One does not expect to generate a sine wave with –100dBc distortion using a 5V low power op amp. All the same, a bandpass filter using the LTC6258 can combine with an easy-to-use low power oscillator to create a sine wave at low cost, low voltage and extremely low dissipation.

Active Filter Component

The bandpass filter of Figure 4 is AC coupled to an input. As a result, the LTC6258 input does not place a burden on the previous stage to develop a particular absolute common mode voltage. A simple resistor divider with RA1 and RA2 provides biasing for the LTC6258 bandpass filter. Pegging the op amp inputs to a fixed voltage helps to reduce distortion that might arise with moving common mode.

This filter is centered at 10kHz. The exact resistance and capacitance values can be tweaked upward or downward, depending on whether lowest resistor noise or lowest total supply current is most important. This implementation is optimized for low dissipation by reducing current in the feedback loop. The capacitors C2 and C3 were initially 4.7nF or higher, with lower resistor values, but replaced with 1nF and higher resistor values, optimizing for lower dissipation.

Besides power dissipation, a secondary but no less important aspect of feedback impedance is loading of the op amp rail-to-rail output stage. Heavier loading, such as between 1K and 10K impedance, significantly lowers open loop gain, in turn affecting the accuracy of the bandpass filter. The data sheet suggests A_{VOL}

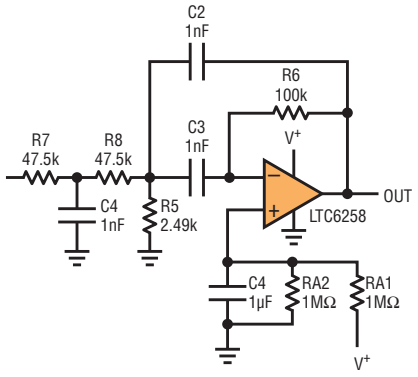


Figure 4. 10kHz bandpass filter

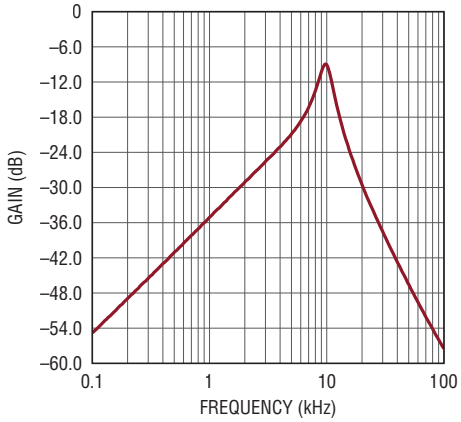


Figure 5. Bandpass filter gain/phase vs frequency

Figure 6. 10kHz oscillator circuit using LTC6906 TimerBlox® input

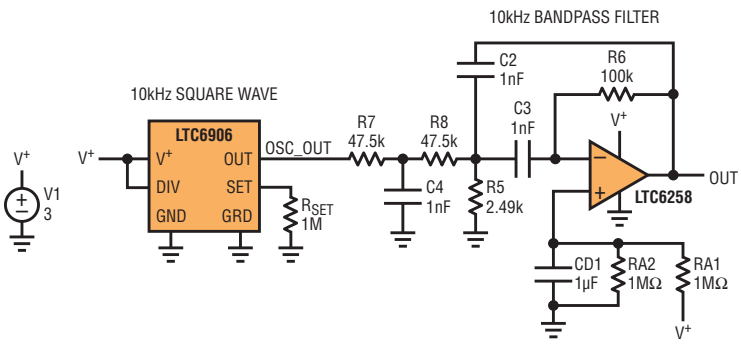
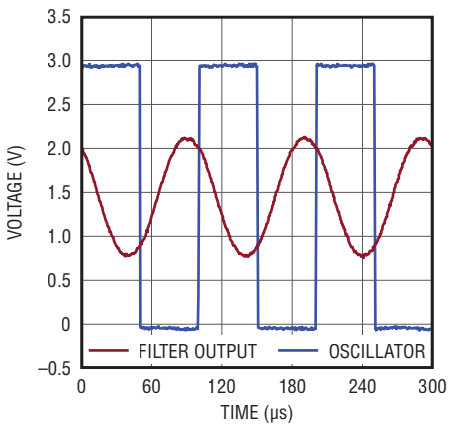


Figure 7. Voltage waveforms oscillator and filter output



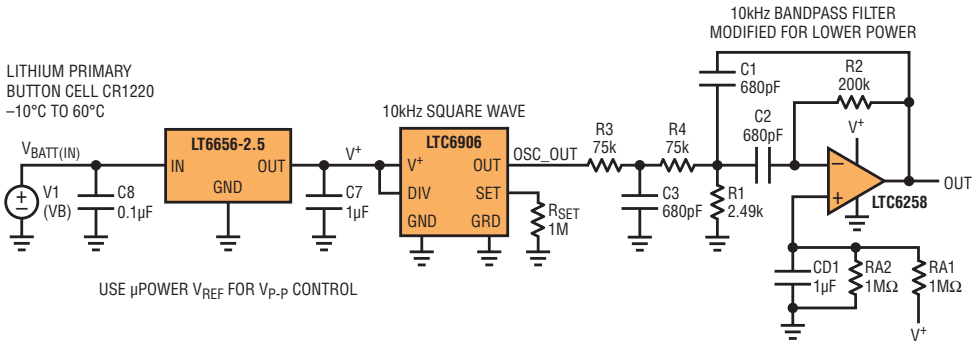


Figure 8. Oscillator and filter with a regulated supply

reduces by a factor of 5 from 100kΩ to 10kΩ. Lower C2 and C3 might be feasible, but then R6 becomes even larger, introducing more noise at the output.

The target Q of this bandpass filter is moderate, approximately 3. A moderate Q, rather than a high Q, allows use of 5% capacitors. Higher Q demands more accurate capacitors, and very likely higher open loop gain at 10kHz than is available with the feedback impedance load. Naturally, moderate Q results in less attenuation of harmonics than a higher Q.

Adding the Oscillator

A low power sine wave generator can be derived by driving a square wave into the bandpass filter. A complete schematic is shown in Figure 6. The LTC6906 micropower resistor set oscillator easily configures as a 10kHz square wave, and can drive the relatively benign loading seen in the bandpass filter input resistors. Supply current of the LTC6906 at 10kHz is 32.4µA.

Figure 7 shows the LTC6906 output and bandpass filter output. HD2 of the sine wave is –46.1dBc, and HD3 –32.6dBc. The output is 1.34V_{P-P} to 1.44V_{P-P} with the exact level varying slightly due to finite op amp open loop gain at 10kHz. Total current consumption is below 55µA on a 3V rail.

Other Enhancements

Figure 8 shows optional enhancements. A low power reference takes advantage of the ability of the LTC6906 and LTC6258 to operate on a very low supply. The reference provides 2.5V from a battery input. The fixed 2.5V supply stabilizes the output voltage swing in the presence of varying input voltage. In addition, even lower filter capacitor values with higher resistances reduce LTC6258 loading further, lowering dissipation and improving filter accuracy.

SELF-OSCILLATING LED DRIVER

LED blinking is an application where one would consider a microprocessor to provide simple control of a clock and duty cycle. Indeed, a microprocessor with a current limited output directly driving an LED offers the most direct implementation; the addition of a MOSFET with the LED and a current limiting resistor in the drain allows more current. These examples, however, do not provide means to control the LED current (LED brightness) without some additional circuitry. And, of course, a microprocessor adds the burden of code version control and maintenance, development platform, and programming steps in production.

Figure 9 shows an LED blinker with control of the ON LED current, without the use of a digitally synthesized frequency. R2 and R3 bring in a divided down copy of the supply voltage as a reference into the positive terminal. The op amp forces this voltage on the sense resistor R_{SENSE} in LED ON operation.

The circuit of Figure 9 combines edge detection with use of the $\overline{SHDN}$ pin of the LTC6258. C2 can AC couple any fast V_G gate drive action into the signal V_C. Hence, when the gate voltage of M1 increases when LED ON begins, V_C suddenly rises. V_C connects to the $\overline{SHDN}$ pin; a rising edge on the $\overline{SHDN}$ pin enables the LTC6258, which is already driving LED current through its feedback circuit, to stay on. However, M3 is also on while M1 is on, and as a result works with R9 to charge C2 slowly until V_C falls below the $\overline{SHDN}$ threshold. At that moment, the active low shutdown kicks in, and the LTC6258 turns off. A negative falling V_G voltage again feeds through C2, and a falling V_C and hence a falling $\overline{SHDN}$ pin voltage keeps the circuit in an "LED OFF" state for some time. M3 turns off, and C2 discharges until V_C is high enough to reactivate the LTC6258.

It may seem a bit odd to develop such a circuit when a microprocessor or a LTC6992 can provide on-off capability in combination with a single MOSFET and resistor. The problem with those circuits, however, is the lack of control over the LED current. In the circuit of Figure 9, a voltage is controlled across a sense resistor. The LED voltage is independent of LED drive current. The generation of the on-off,

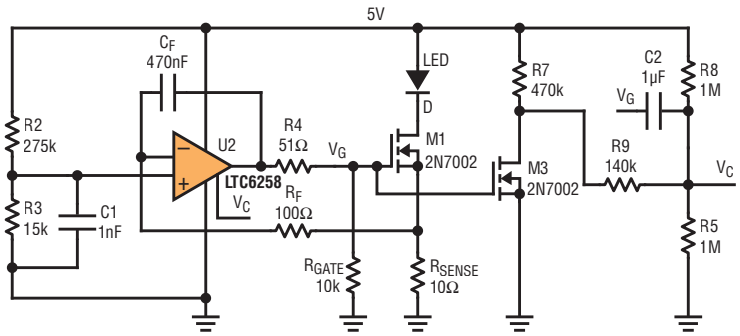


Figure 9. LED driver with self-oscillation

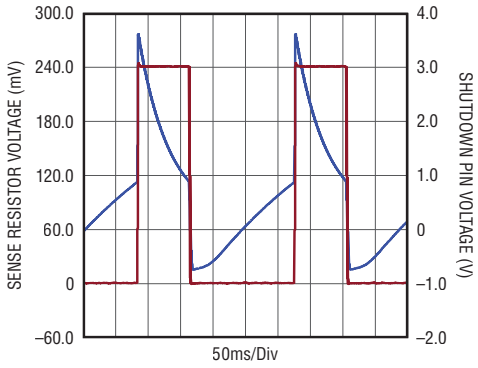


Figure 10. LED blinker current

or blinking, comes with the addition of a handful of low cost components.

It is interesting to note that the LED current depends on the supply in this implementation inasmuch as the supply feeds the reference through R2 and R3. The supply figures into the time of the on and off cycle since the supply powers the edge detection and relaxation part of the circuitry. When the supply falls, the LED current drops and the cycle time increases. This change of behavior can help in battery powered LED blinking applications to predict end of life. Alternatively, with a reference such as the LT6656 powering the entire circuit except for the LED and M1 branch, operation with unchanging LED brightness and frequency is possible.

Figure 10 shows the sense resistor voltage and the $\overline{SHDN}$ pin voltage. The $\overline{SHDN}$ voltage is tied to V_C; the gate drive couples through C2 as previously described.

Components R_F and C_F can significantly slow edges down. Adding this much delay is not essential, but it can help to smooth out any hiccups that occur when the part goes through a power up sequence after the $\overline{SHDN}$ pin goes inactive high. The 47µs time constant ($R_F \bullet C_F$) is insignificant in the time scale of the blinking (tens or hundreds of ms)—47µs is much smaller than any time constant associated with C2 and its resistors.

ACTIVE FILTERS

The LTC6261/62/63 op amps' high MHz-to-mA ratios can freshen up traditional filter circuits. The two filter examples discussed here display performance previously unachievable with such low power.

Second Order Bessel Filter

Ample bandwidth and low supply current enable deployment of active filters in portable and other low power applications. For instance, a second order Bessel filter, shown in Figure 11, provides a clean transient response at the expense of a less steep roll-off in the frequency domain.

Measured supply current consumption is about 230µA, although data sheet supply maximum values suggest that the consumption across production and temperature may be slightly higher. The values of resistors chosen minimize consumption at the expense of in-band noise.

If V_{REF} is derived from a high impedance resistor divider, then a large capacitor is required to ensure that the reference voltage is solid down to very low

Figure 11. Second order Bessel filter

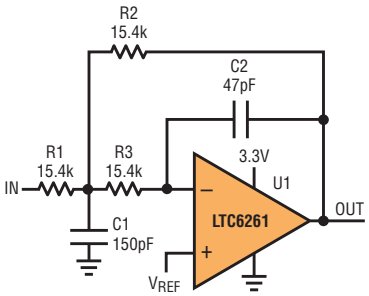


Figure 12. Second order Bessel frequency response

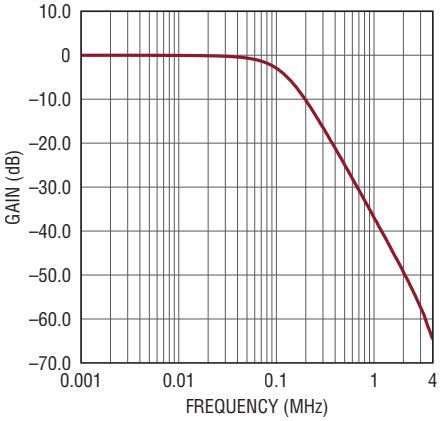


Figure 13. Bessel filter transient response

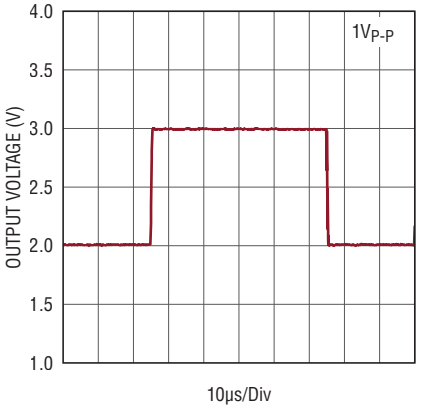


Table 1. Power efficient rail-to-rail input/output op amps

	GBW	I_S per AMP	GBW EFFICIENCY, MHz/mA	SR EFFICIENCY, V/µs/mA	e_n EFFICIENCY, (nV/√Hz)•√mA
LTC6258/9/60	1.3MHz	20µA	65	12	38
LTC6255/6/7	6.5MHz	65µA	100	24	5.5
LTC6261/2/3	30MHz	240µA	125	29	13
LTC6246/7/8	180MHz	1mA	180	90	4.2
LTC6252/3/4	720MHz	3.5mA	206	80	5.1

frequencies. The reference at the positive op amp input must be a good "AC ground" at all frequencies when using this inverting amplifier configuration.

The frequency response (Figure 12) shows an expected roll-off of two poles along with a gentle droop near the 3dB point; the transient response is very clean, as shown in Figure 13.

Third Order Butterworth Filter

Maximally flat magnitude response in the passband arises from use of a Butterworth filter. An extra RC stage is added in front of the filter in order to maximize the roll-off for a single amplifier circuit. Use of an extra stage complicates the math, but not intractably so.

Measured supply current consumption is about 235µA. The chosen values of resistors minimize consumption at the expense of in-band noise.

The frequency response (Figure 15) shows an expected roll-off of three poles, an extended plateau and a sharp roll-off; the transient response includes a small amount of ringing as shown in Figure 16.

BRIDGE-TIED DIFFERENTIAL OUTPUT AMPLIFIER

The low supply current of these op amps at the bandwidth and noise performance allows for excellent fidelity at a fraction of the usual dissipation in portable audio equipment. As with active filters, revisiting portable audio equipment headphone drivers is a rational enterprise, given the unique capabilities of the LTC6261.

One significant concern in a portable device is battery drain. Music played loudly, or listeners' musical choices affect the rate of battery drain—for the most part, the end-use of a device is out of the designer's control. Quiescent current, though, is not. Because much of a device's time may be spent idle, quiescent current is significant, as it drains batteries continuously. The LTC6261's low quiescent current increases battery discharge time.

Headphone speaker impedances range from 32Ω to 300Ω; their responsivity, from 80dB to 100dBSPL per 1mW and beyond. As an example, considering a headphone speaker with 90dBSPL per 1mW, it takes 100mW delivered to reach 110dBSPL. With 32Ω, the RMS current is 56mA and voltage 1.8V; with 120Ω, 29mA and 3.5V.

Given a 3.3V supply and the output of one LTC6261 amplifier, there may not be sufficient drive capability to yield 100mW. However, the combination of two 180° phased amplifiers is enough to provide the necessary drive to reach upwards of 100mW delivered power. Duplication of this bridge drive circuit enables power to both left and right sides. Figure 17 shows the driver schematic.

Figure 14. Third order Butterworth filter

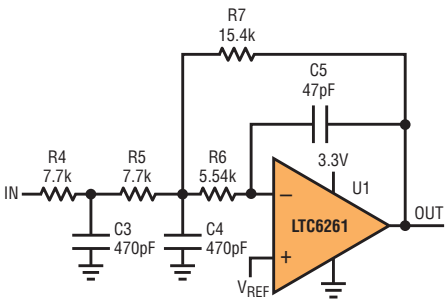


Figure 15. Third order Butterworth frequency response

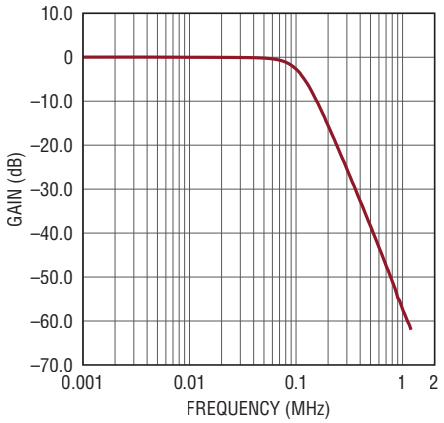
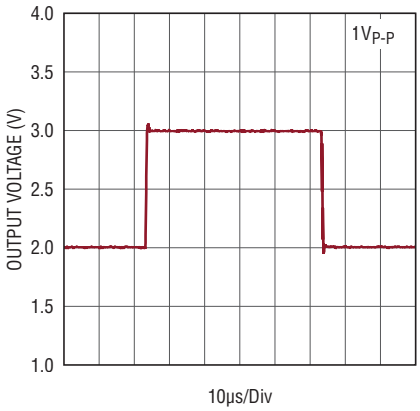


Figure 16. Butterworth filter transient response



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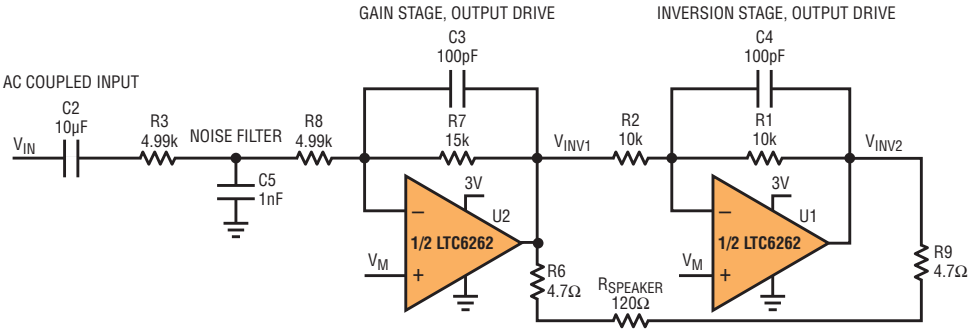


Figure 17. Audio headphones bridge driver

The LTC6263 provides four amplifiers in one small package. Data from a 2-amplifier LTC6262 driving what could be left or right is shown in Figures 18 and 19. Basic current consumption of the two amplifiers, with as much as $1V_{P-P}$ input but no load, is 500µA.

The solution shown in Figure 17 consists of first, an inverting gain stage with closed loop gain = 1.5, and a subsequent inverting stage. The combination of inverting stages produces a single-ended input to differential output gain of 3. With $500mV_{P-P}$ input, the output is $1.5V_{P-P}$, or 0.75V max, or $0.53V_{RMS}$. With 50Ω, 500mV input leads to approximately 5.6mW delivered power. At $1V_{P-P}$ input, the circuit delivers 22.5mW. Note that it helps that the LTC6261 output can swing close to rail-to-rail with load.

The first build of this circuit in the lab produced a significant tone at a few hundred Hz. It turned out that the positive input was not well grounded as an "AC ground" over all frequencies because the voltage was not strongly pegged. The need to peg the voltage arises when using a single supply rather than a dual supply. With a single supply, V_M is not ground, but rather a mid-rail voltage created to enable inverting topologies to work properly. The resistor divider that creates V_M has large resistance values (for example, two 470k in series) to minimize additional supply current. A large capacitor ensures a strong ground at low frequencies. Indeed, the addition of a large capacitor (1µF, which forms a pole with the 470k resistors in parallel) eliminates the mysterious distortion tone.

Despite the low quiescent current, this driver delivers low distortion to a headphone load. At high enough amplitude, distortion increases dramatically as the op amp output clips. Clipping occurs sooner with more loading as the output transistors start to run out of current gain.

CONCLUSION

The applications shown here take advantage of a unique combination of features available in the LTC6258/LTC6259/LTC6260 and LTC6261/62/63 op amp families. The low quiescent current of these devices does not diminish their ability to perform at levels usually reserved for more power hungry parts. Rail-to-rail input and output, shutdown, and choice of package are features that add to their versatility. ■

Figure 18. LTC6262 bridge driver THD and noise with different loads vs frequency

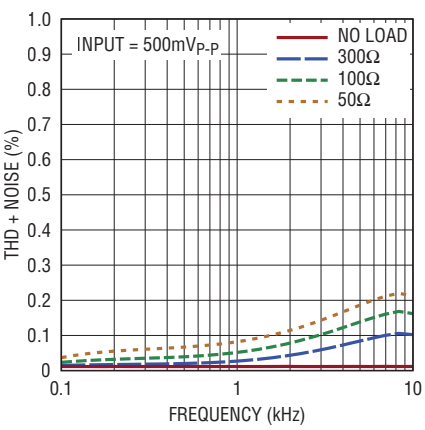
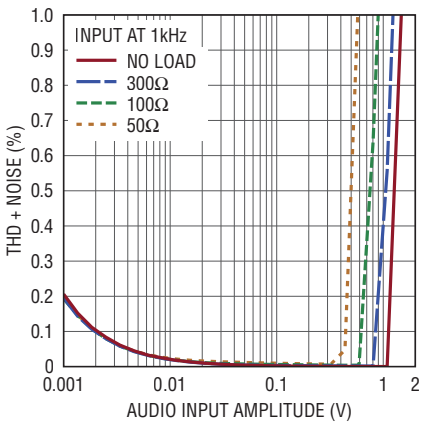


Figure 19. LTC6262 bridge driver THD and noise with different loads vs amplitude at 1kHz



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The LTspice® XVII simulator represents the 2017 release of this simulator and has many new features. One of the most significant usability enhancements is an updated graphics library that supports multi-monitor support (or floating windows). This allows users to display a schematic capture window in one monitor and display the simulation results in the waveform viewer window on another monitor. There are also several new interfaces for composing and editing various types of SPICE syntax. New simulator features include improved simulation speeds, support for Unicode, improved VDMOS model, native IGBT device, diode soft recovery, and an arbitrary state machine (.mach).

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Simulating ISO 7637-2 and ISO 16750-2 transients early in the design phase of an automotive product can pinpoint issues that would otherwise come to light during electromagnetic compatibility (EMC) testing. Spending a few minutes simulating the protection circuitry in LTspice helps to avoid expensive hardware respins due to EMC failures. The ISO16750-2 and ISO7637-2 symbols and models in LTspice simplify this task by providing a nearly complete set of ISO transients.

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- **LTC6362**: Baseband design example for a low power IQ modulator www.linear.com/solutions/7116

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- **LT8640S:** 42V, 6A synchronous step-down Silent Switcher®2 with 2.5µA quiescent current www.linear.com/LT8640S
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- **LTC6262**: Dual 30MHz, 240µA power efficient rail-to-rail I/O op amps www.linear.com/LTC6262

Voltage Reference

- **LT6658:** Precision dual output, high current, low noise, voltage reference www.linear.com/LT6658 ■

Power User Tip

SIMULATING SAR ADC ANALOG INPUTS

As resolution and sample rates continue to rise for ADCs, the driver circuitry for the analog inputs, not the ADC itself, has increasingly become the limiting factor in determining overall circuit accuracy. Beyond a simple 1-pole RC lowpass filter (LPF1) for noisy input signals (Figure 1), a coupling RC filter network (LPF2) is often used between the buffer and ADC input to minimize disturbances reflected into the buffer from ADC sampling transients. Long RC time constants at the analog inputs slow the settling of these disturbances. Therefore, LPF2 typically requires a wider bandwidth than LPF1. This filter also helps minimize the noise contribution from the buffer.

Simulating the interface between the amplifier and ADC presents some interesting trade-offs between settling time and noise performance. Experimenting with such simulations helps one develop an intuitive understanding of how the filter design affects these performance aspects.

The analog input of a fully differential SAR ADC can be modeled as a switched capacitor load on the drive circuit shown in equivalent form in Figure 2. The values shown are from the LTC2378-20 20-bit, 1Msps, low power SAR ADC but can easily be modified to represent other ADCs. During the acquisition phase, each input sees approximately 45pF (C_{IN}) from the sampling CDAC in series with 40Ω (R_{ON}) from the ON-resistance of the sampling switch. The inputs draw a current spike while charging the C_{IN} capacitors in this phase. During the subsequent conversion phase, the analog inputs draw only a small leakage current and the capacitors are fully discharged. This modeling of the ADC analog input highlights one of the biggest challenges in coupling an amplifier to a SAR ADC such as the LTC2378-20; dealing with current spikes drawn by the ADC inputs at the start of each acquisition phase.

A simulation schematic of this equivalent circuit is shown in Figure 3. The low power LTC6362 differential op amp is configured to convert a single-ended input signal to a fully differential output to drive the LTC2378-20. To simplify the simulation, the input ESD protection diodes are not included. The two 45pF input capacitors (C1 and C2) are charged via voltage controlled switches (S1 and S2) that are defined by a SW model statement with an ON resistance of 40Ω. These switches are driven by a pulsed voltage source with a duration of 312ns and period of 1µs to simulate the acquisition time of the LTC2378-20 SAR ADC at 1Msps. To ready the sampling capacitors for the next acquisition phase, an idealized behavior inverter (A1) is used to turn on the second set of switches (S3 and S4) that discharge the capacitors.

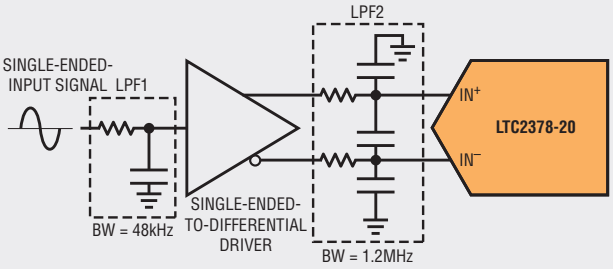


Figure 1. Simulating the interface between an amplifier and ADC can help determine trade-offs between noise and settling time.

The RC filter network between the amplifier and the ADC serves several purposes. First, the filter network reduces the amount of wideband noise entering the ADC. Second, the capacitors serve as a charge reservoir to absorb charge kickback from the ADC's internal sampling capacitors. After each conversion cycle, the discharged sample capacitors (45pF) are reconnected to the amplifier circuit. By placing a much larger reservoir capacitor at the ADC input, the voltage excursion caused by these sample capacitors is reduced. There is, however, a trade-off between wideband noise and settling time performance. While the sample capacitors are connected to the amplifier circuit (acquisition time), the RC network should fully settle to within the resolution of the ADC. Using too much reservoir capacitance in the filter network increases this settling time beyond acceptable limits. For further discussion of this trade-off, watch Kris Lokere's "SAR ADC Driver Interface" video at www.linear.com/solutions/4679.

Happy simulations!

Figure 2. Equivalent circuit for the analog input of the SAR ADC

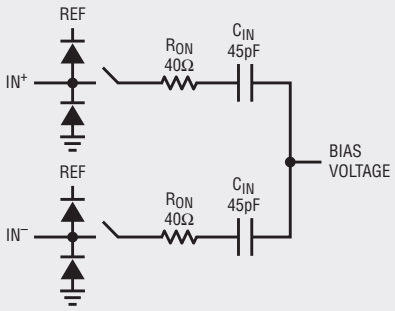
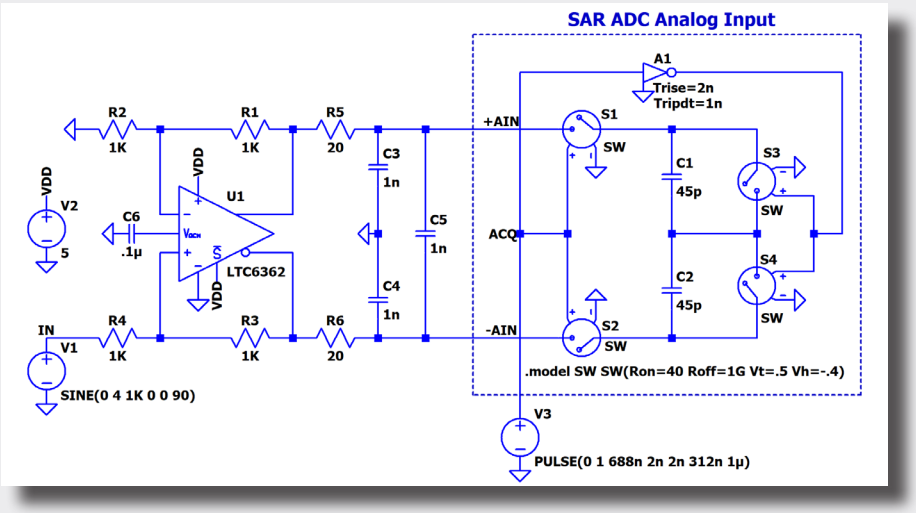


Figure 3. Simulation schematic of SAR ADC analog input equivalent circuit



Low Noise, Precision Op Amp Drives High Resolution SAR ADCs

Erjon Qirko and Kris Lokere

The LT6018 is an ultralow noise (1.2nV/√Hz at 1kHz) operational amplifier with ultralow distortion (–115dB at 1kHz). It has a gain bandwidth product of 15MHz, maximum offset voltage of 50µV and a maximum offset voltage drift of 0.5µV/°C. This combination of features makes it suitable for driving a variety of high resolution analog-to-digital converters (ADCs). This article presents circuits and optimization strategies to achieve the best signal-to-noise ratio (SNR) and total harmonic distortion (THD) when using the LT6018 to drive high speed 18-bit and 20-bit successive approximation register (SAR) ADCs.

ULTRALINEAR 20-BIT ADC

Figure 1 shows a modification of the DC2135A demonstration circuit, with the LT6018 (replacing the LT1468) driving the LTC2378-20 20-bit SAR ADC. The LTC2378-20 stands out for its unrivaled 2ppm linearity performance. The best way to create a differential signal while maintaining linearity is with the precision matched resistors in the LT®5400 used on this demo board. A detailed theory of operation for the circuit shown in Figure 1 appears in Design Note 1032 (where the LT1468 drives the LTC2377-20).

To measure the circuit's linearity, an ultrapure sine wave is fed into the input, and the FFT is calculated at the output. The resulting THD measurement serves as proxy for the circuit's INL (integral non-linearity) performance. At an ADC sample rate of 800kHz, we use an input frequency of about 100Hz (slightly adjusted to ensure coherent sampling, alleviating FFT numerical limitations).

The original demonstration circuit includes an RC lowpass filter directly after the op amp to filter out excess high frequency noise. The LT6018's noise density remains relatively low even at high frequencies, so removing this filter negligibly affects total noise. Without the filter, linearity (as measured by THD) improves markedly, since the single-ended-to-differential conversion is now entirely governed by the precisely matched resistors in the LT5400, uncorrupted by any poorly matched discrete components.

The LT6018's low noise density makes it suitable for circuits that require gain. Configured in a gain of 10, the signal strength increases by 20dB while the SNR

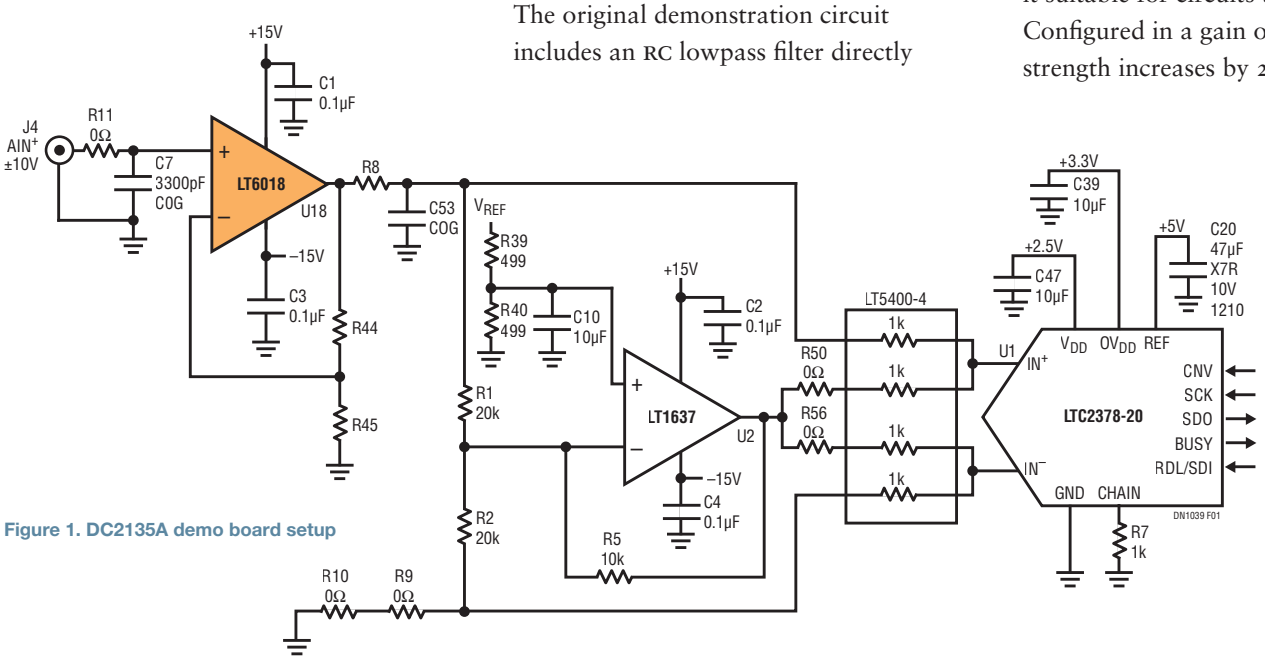


Figure 1. DC2135A demo board setup

Table 1. LT6018 driving LTC2378-20 SNR and THD results

LT6018 GAIN	R8 (Ω)	C53 (µF)	R44 (Ω)	R45 (Ω)	SNR (dB)	THD (dB)
1	10	0.01	0	Open	103.1	–110.7
1	0	0	0	Open	102.5	–121.7
10	14.7	0.0068	900	100	99.6	–98.5
10	10	0.01	900	100	100.5	–99.8

Table 2. LT6018 driving LTC2387-18 SNR and THD results

AMPLIFIER	R49 = R50 (Ω)	C73 = C75	C74	SNR (dB)	THD (dB)
LT6200	10	82pF	Open	94.2	–120
LT6018	10	82pF	Open	90.3	–72.9
LT6018	25	1nF	Open	94.5	–93.7
LT6018	25	1nF	1nF	96.0	–96.1
LT6018	13.7	1.8nF	1.8nF	95.9	–101.1

degrades by 2dB relative to full scale. If the input signals are small, this arrangement improves effective signal-to-noise ratio by 18dB. As expected, linearity is reduced by the same amount as the amplifier loop gain, or about 20dB. The results are summarized in Table 1.

DRIVING A HIGH SPEED 18-BIT ADC

The LTC2387-18 is an 18-bit SAR ADC that can sample up to 15Msps. At this sample rate, the ADC's internal sampling capacitor is connected to the amplifier output for less than 30ns ("acquisition time"). During that time, the amplifier (and filter) circuit must recover from charge kickback and replenish the charge of the sample capacitor, so the ADC can measure the correct input voltage at the next conversion cycle. Careful optimization of the amplifier and filter network is in order.

In Figure 2, two LT6018s are configured as unity gain followers, and connected to the LTC2387-18 demo board, which has provisions for filter resistors and capacitors at the ADC input.

Table 2 shows the SNR and THD results, measured for a 1.008kHz pure sine wave at the input, and the ADC sampling at a coherent 14.680Msps. The first table entry shows results with the LT6200 amplifier, a very high speed, low noise op amp. The filter configuration is the demo board default bandwidth of about 200MHz. This allows full settling of the ADC charge kickback, which results in excellent THD of –120dB. However, SNR is 2dB below the 96dB capability of the ADC.

The LT6018 has lower bandwidth than the LT6200, but much better DC accuracy (offset and drift). However, plugging the LT6018 into the same configuration as the LT6200 significantly degrades SNR and THD. SNR is degraded because amplifier noise density can be higher above its bandwidth than below, and this noise, if not filtered, will alias into the ADC. THD is degraded because the slower amplifier—when hit with the full ADC charge kickback—does not properly settle and leaves non-linear residues for the ADC to digitize.

We can filter the wideband amplifier noise by increasing the value of the resistors and capacitors, and by including a differential capacitor between the two ADC inputs. Doing so improves the SNR all the way to the theoretical maximum of 96dB for this ADC, which means that integrated amplifier noise has become negligible. Furthermore, by skewing the filter configuration toward smaller series resistors and larger capacitors, the initial effect of the charge kickback is attenuated, resulting in improved THD performance, well below –100dB.

CONCLUSION

Modern SAR ADCs combine low noise with high linearity and precise DC offset accuracy. Realizing these specs requires an amplifier with similarly good DC specs, low noise and sufficient bandwidth, such as the LT6018. With moderate speed ADCs (such as the 1Msps 20-bit LTC2378-20), the LT6018, in combination with precisely matched LT5400 resistors, can create a differential input signal with no additional filtering required. With ultrafast SAR ADCs (such as the 18-bit 15Msps LTC2387-18), careful optimization of an RC filter network between the op amp and ADC results in excellent noise and linearity performance. ■

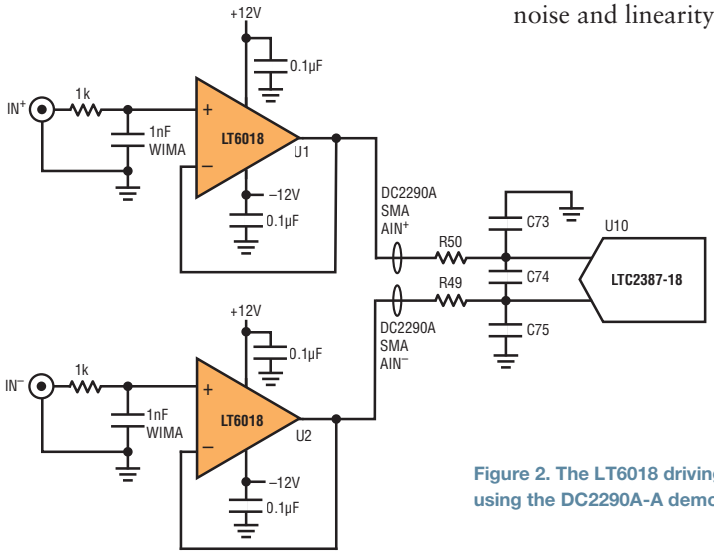


Figure 2. The LT6018 driving the LTC2387-18 using the DC2290A-A demo board

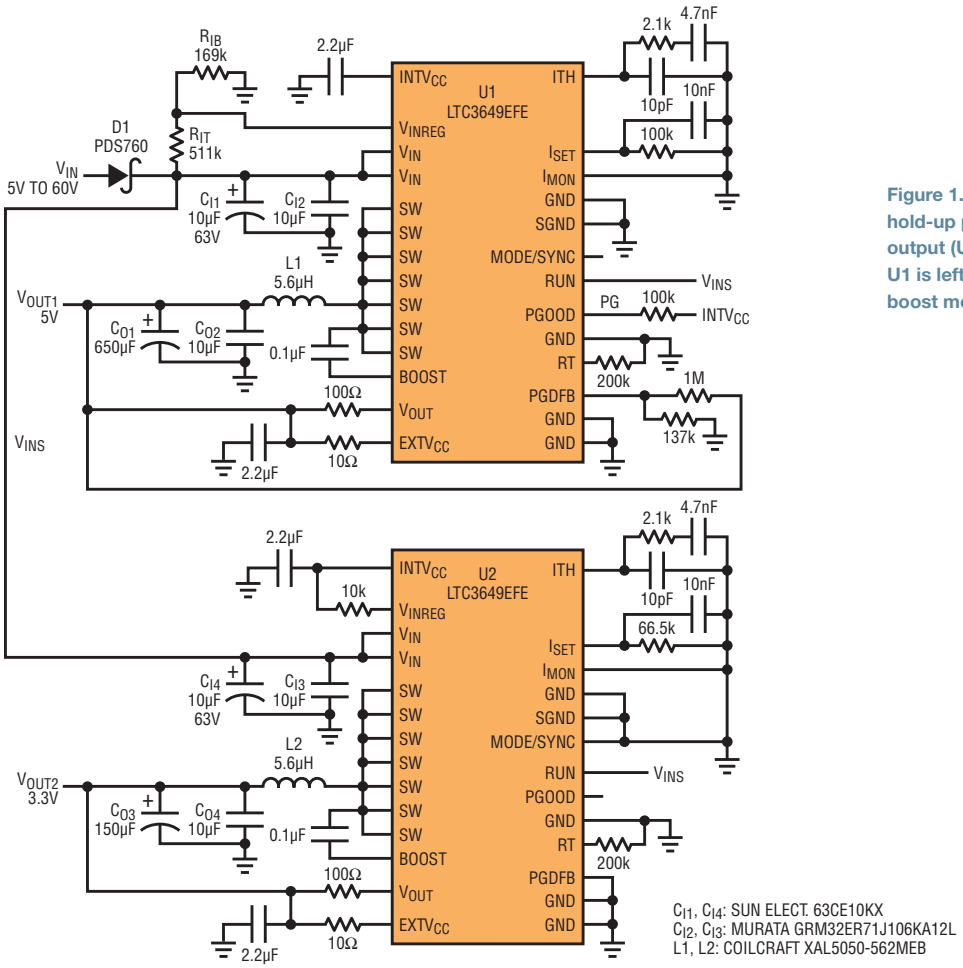
60V Input Monolithic Converter Powers Critical Circuits without Supercaps or Other Additional Components

Victor Khasiev

The LTC3649 is a monolithic step-down regulator capable of operating from an input voltage range of 3.1V to 60V, and efficiently producing a single resistor-programmable output voltage at up to 4A of output current. These features make it a compelling industrial or automotive supply for output voltages from (V_{IN} – 0.5V) to ground. The LTC3649 is capable of providing power to critical systems when there is a power outage, without any extra components.

Hold-up circuits supply power to critical systems when the main power rail fails, allowing them to perform important housekeeping tasks, such as data retention, for a short period before all available energy is lost. Typical hold-up solutions employ dedicated controllers and large storage capacitors,[1,2] where the additional cost and complexity is warranted if the critical circuits require significant power and hold-up time. But if the required hold-up energy is relatively low, the LTC3649 can easily perform this task with no additional circuitry.

The dual output converter described here works as a conventional step-down power supply under normal operating



C_{I1}, C_{I4}: SUN ELECT. 63CE10KX
C_{I2}, C_{I3}: MURATA GRM32ER71J106KA12L
L1, L2: COILCRAFT XAL5050-562MEB

Figure 1. The 5V output converter (U1) provides hold-up power for protected load on the 3.3V output (U2). Note that the pin MODE/SYNC of U1 is left floating, allowing the LTC3649 to enter boost mode.

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conditions. But during a power interruption, the converter becomes the energy source, maintaining the programmed output voltage to critical circuits. To perform this task, U1 becomes a step-up converter when input voltage is disconnected, discharging its output capacitor to provide hold-up energy.

DUAL OUTPUT CONVERTER AND HOLD-UP CIRCUIT

Figure 1 shows a hold-up design using the LTC3649. Under normal conditions, the unregulated rail, V_{IN} (V_{INS} via a blocking diode) supplies a converter based on U1 (converter A). This converter works in buck mode, generating a stable 5V on V_{OUT1}. V_{INS} is connected to a U2-based second converter (converter B), which supplies 3.3V on V_{OUT2} to a critical load. When V_{IN} fails, converter A enters boost mode and maintains its programmed output voltage (V_{INS}) by discharging its output filter capacitors C_{O1} and C_{O2}. Resistors R_{IT} and R_{IB} program this voltage level. The PGOOD (PG) signal produced by U1 can be used to communicate the power failure to systems that can disconnect noncritical circuitry to preserve energy. The MODE/SYNC pin is left floating to allow the LTC3649 to enter boost mode.

Figure 2 shows what happens to the LTC3649 in a boost mode. For the first 7ms of the capture, all voltages are stable. At 7ms, the power is turned off; both V_{IN} and V_{INS} begin to decline. When V_{INS} reaches 8V, it stabilizes and the PG signal changes state, signaling the beginning of the V_{OUT1} collapsing. V_{INS} remains at

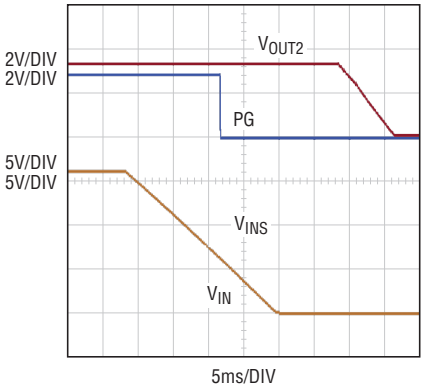

Figure 2. When the input voltage V_{IN} drops, the converter U1 boosts V_{OUT1} to maintain V_{INS} at 8V. V_{INS} provides power to keep V_{OUT2} in regulation for over 20ms after V_{IN} drops out.

8V as long as CO1 and CO2 have charge. V_{OUT2} holds constant during the entire process, supplying steady power to the critical load long after the power is interrupted. The LTspice model of this circuit is available at www.linear.com.[3]

CONCLUSION

LTC3649 is a monolithic step-down regulator with integrated power MOSFETs. It is highly efficient, with low quiescent current, important in many battery-operated systems. It is also highly versatile, with programmable frequency, a wide V_{IN} range up to 60V and an output voltage range down to ground. It simplifies the design of automotive and industrial supplies, especially when its inherent ability as a hold-up circuit is taken into account. ■

REFERENCES

[1] LTC3110 - 2A Bidirectional Buck-Boost DC/DC Regulator and Charger/Balancer www.linear.com/product/LTC3110

[2] LTC3643 - 2A Bidirectional Power Backup Supply www.linear.com/product/LTC3643

[3] LTC3649 Hold-Up Circuit Using a Buck Regulator with V_{IN} Boost Capabilities www.linear.com/solutions/7412

560V Input, No-Opto Isolated Flyback Converter

George Qian

In traditional isolated high voltage flyback converters, tight regulation is achieved using opto-couplers to transfer regulation information from the secondary-side reference circuitry to the primary side. The problem is that opto-couplers add significant complexity to isolated designs: there is propagation delay, aging, and gain variation, all of which complicate power supply loop compensation and can reduce reliability. Moreover, during start-up, either a bleeder resistor or high voltage start-up circuit is required to initially power up the IC. Unless an additional high voltage MOSFET is added to the start-up components, the bleeder resistor is a source of unwelcome power loss.

The LT8315 is a high voltage flyback converter with an integrated 630V/300mA switch. The LT8315 eliminates the need for an opto-coupler, complicated secondary-side reference circuitry, additional start-up components, and an external high voltage MOSFET.

PERFORMANCE AND SIMPLICITY

The LT8315 integrates a 630V MOSFET and control circuitry inside a thermally enhanced 20-pin TSSOP package with four pins removed for high voltage spacing. By sampling the isolated output voltage from the third winding, no opto-coupler is required for regulation. The output voltage is programmed with two external resistors and a third optional temperature compensation resistor. Boundary mode operation helps to achieve excellent load regulation. Because the output voltage is sensed when the secondary current is almost zero, no external load compensating resistors and capacitors are needed. As a result, the LT8315 solution has a low component count, greatly simplifying the design of an isolated flyback converter.

Figure 1 shows the complete schematic of a flyback converter with a wide input range from 20V to 450V. It has a 12V output and maintains tight regulation with a load current from 5mA to over 440mA. The output current capability increases with input voltage; the output current could reach 440mA when the input voltage exceeds 250V. This flyback converter has 85% peak efficiency. Even with no opto-coupler, load and line regulation remain tight, as shown in Figure 2.

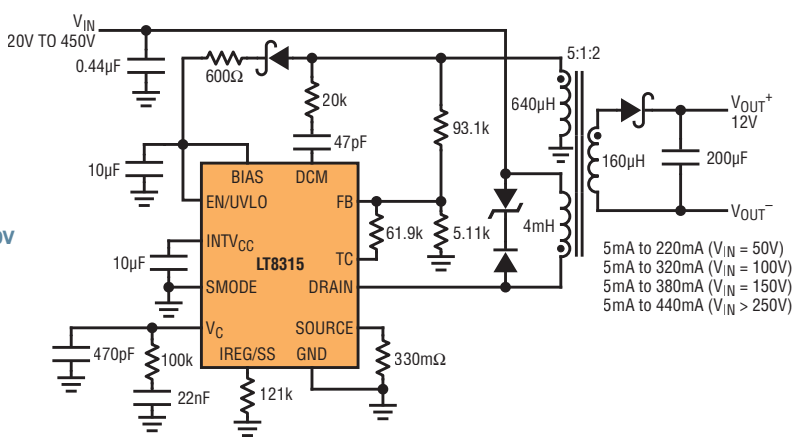

Figure 1. A complete 12V isolated flyback converter for a wide input from 20V to 450V

INTERNAL DEPLETION MOSFET FOR START-UP

The LT8315 features an internal depletion mode MOSFET, which has a negative threshold voltage and is normally on. At start-up, this MOSFET charges the $INTV_{CC}$ capacitor to 12V so that the LT8315 has power to begin switching. As a result, there is no need for an external bleeder resistor or other start-up components. Once $INTV_{CC}$ is charged, the depletion mode MOSFET turns off to reduce power loss.

LOW QUIESCENT CURRENT

The LT8315 typically requires a small preload at the output, which reflects back to the input as quiescent current. As the load becomes light, the LT8315 reduces the switching frequency while keeping the minimum current limit in order to reduce current while properly sampling the output voltage. The typical minimum switching frequency is

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about 3.5kHz. When the standby mode is enabled, the minimum frequency is further reduced to 220Hz, which is a 16× reduction for ultralow quiescent current.

In standby mode, the LT8315's preload is usually less than 0.1% of full output power, the quiescent current is lower than 100µA—important for applications requiring high efficiency in always-on systems.

NONISOLATED BUCK CONVERTER

The LT8315's high voltage input capability is easily applied in nonisolated solutions. Nonisolated converters do not require the transformer of an isolated converter, instead adopting a relatively inexpensive off-the-shelf inductor as the magnetizing component.

For a nonisolated buck application, the LT8315's ground pin is connected to the switch node of the buck topology, which is a varying voltage. The unique sensing scheme of LT8315 sees the output voltage only when the switch node is connected to ground, which leads to

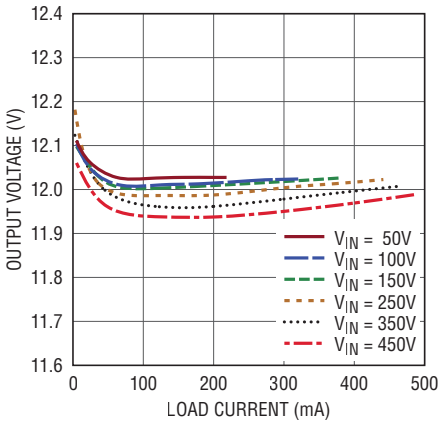


Figure 2. Load and line regulation of the flyback converter in Figure 1

a simple buck schematic, as shown in Figure 3. The diode, D2 and two resistors at the FB pin form the feedback path.

Figure 3 shows the schematic of a nonisolated buck converter, which converts an extremely wide-ranging input of 20V to 560V, to a regulated 12V output. This circuit can achieve efficiency as high as 85%.

CONCLUSION

The LT8315 operates at a wide input voltage range of 18V to 560V, delivering up to 15W of isolated output power. It requires no opto-coupler, and includes rich features such as low ripple Burst Mode® operation, soft-start, programmable current limit, undervoltage lockout, temperature compensation, and low quiescent current.

The high level of integration simplifies the design of low component count, high efficiency solutions in a wide variety of applications: from battery powered systems to automotive, industrial, medical, telecommunications power supplies and isolated auxiliary/housekeeping power supplies. ■

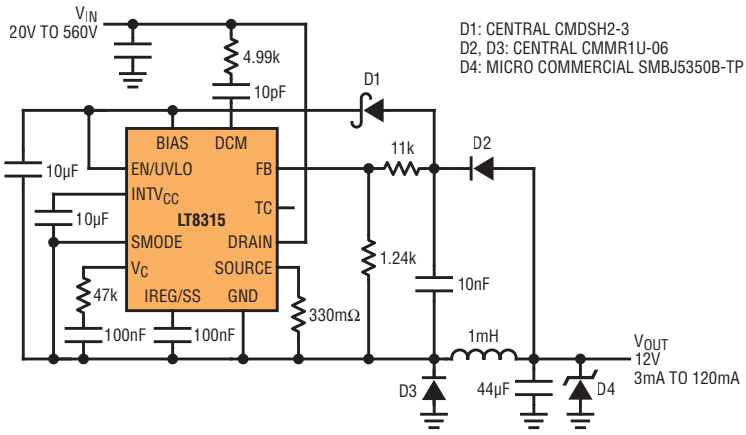


Figure 3. Schematic of a nonisolated buck converter: 20V to 560V input to 12V at 120mA

Electrolytic Capacitor-Based Data Backup Power Solution for a 12V System Regulated from 5V to 36V Input

Victor Khasiev

Data loss is a concern in telecom, industrial and automotive applications where embedded systems depend on a consistent supply of power. Sudden power interruptions can corrupt data during read and write operations for hard drives and flash memory. Often, embedded systems need just 10ms to 50ms to back up volatile data to prevent loss.

Data backup is used in embedded systems for maintenance, troubleshooting and repair work. In complex industrial metal machining equipment, it's important to store the position and state of multiple tools after power disconnect to prevent equipment failure when power is later restored. These applications require a stable power supply and data retention, but unreliable power sources make it difficult to accomplish. Long supply lines, discharged batteries, unregulated AC adapters, load dumps and switching high power electrical motors result in widely fallible input supplies. As a result, developers of embedded systems prefer to design with the widest possible input voltage range, enabling use in a variety of applications and environments.

CIRCUIT DESCRIPTION

Figure 1 shows a system that delivers reliable primary power plus hold-up power for data backup. This solution is centered on the LTC3643 bidirectional power backup supply. When the input voltage is present, the LTC3643 charges the storage capacitor, $C_{STORAGE}$, up to 40V in boost mode. When the input voltage is interrupted, the LTC3643 discharges the storage capacitor into the load in buck mode, keeping the nominal voltage at the load (V_{SYS}) in the range of 3V to 17V.

The relatively high voltage of the backup storage rail increases stored energy of this solution ($E = CV^2/2$) and enables the use of electrolytic capacitors as a backup storage component. Electrolytic capacitors are inexpensive and widely available, significantly reducing the cost of the backup solution. Another advantage of the LTC3643 is its ability to support 12V systems, the default standard voltage rail in many automotive and industrial applications.

In Figure 1, the LTM4607 µModule buck-boost converter acts as the front end regulator, producing 12V at up to 5A from a 5V to 36V input, such as a vehicle battery. The buck-boost regulator maintains a steady 12V output so long as the input voltage stays within the specified range, allowing V_{SYS} to ride through brownout and overvoltage conditions such as automotive cold crank and load dump. When the input voltage is interrupted or moves out of this range, the LTC3643-based backup power solution maintains the V_{SYS} system voltage to allow for short-term data backup.

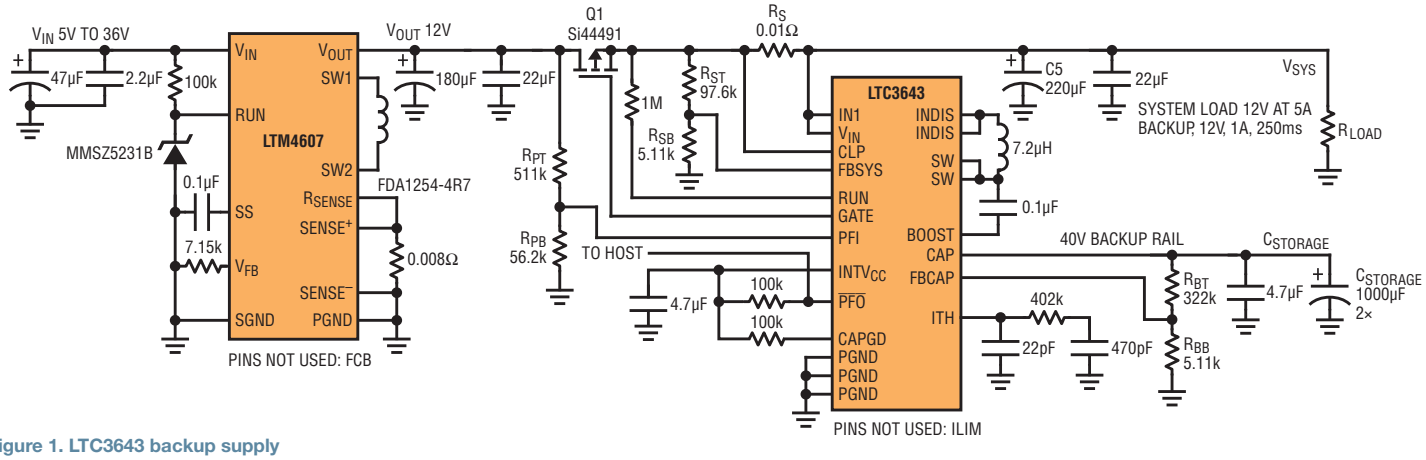


Figure 1. LTC3643 backup supply

The relatively high voltage of the backup storage rail increases stored energy of this solution ($E = CV^2/2$) and enables the use of electrolytic capacitors as a backup storage component. Electrolytic capacitors are inexpensive and widely available, significantly reducing the cost of the backup solution. Another advantage of the LTC3643 is its ability to support 12V systems, the default standard voltage rail in many automotive and industrial applications.

CIRCUIT FUNCTIONALITY

In normal operation, when the P-channel MOSFET Q1 is on, the flag PFO is low and the electrolytic capacitor array $C_{STORAGE}$ is charged to 40V. When the input voltage is interrupted, the LTC3643 turns Q1 off, sets the flag PFO high and starts to discharge the $C_{STORAGE}$ capacitor array, maintaining 12V to the load. When Q1 is in the off state, the body diode of this transistor effectively isolates the load from the input lines. The PFO flag identifies the fault and signals the host computer to disconnect the noncritical loads and supply circuitry. Here it is assumed that the critical circuitry related to data retention consumes 1A for up to 100ms.

Figure 2 illustrates the entire switchover process. At the start, the system load is supplied by the LTM4607, as the input voltage is present. When the input voltage is interrupted, the LTC3643 supports the system load by discharging the storage capacitor. Figure 3 shows the timing of the switchover in more detail. The load voltage falls to 10V, a value set by the resistor divider R_{PT}/R_{PB} and then recovers to the nominal 12V, set by the resistor divider R_{ST}/R_{SB}.

The formulas for an estimation of the required storage capacitance and holdup time are below. If a more detailed analysis is needed, the necessary information can be found in vendor's documentation.

Energy stored:

$$E_{CAP} = \frac{C_{STORAGE}}{2} \bullet (V_{CAP}^2 - V_{SYS}^2)$$

Energy needed to supply load for time, T_H:

$$E_{LOAD} = I_{SYS} \bullet V_{SYS} \bullet T_H$$

Holdup time:

$$T_H = \frac{C_{STORAGE} \bullet \left(V_{CAP}^2 - V_{SYS}^2\right) \bullet \eta}{2 \bullet I_{SYS} \bullet V_{SYS}}$$

η = EFFICIENCY

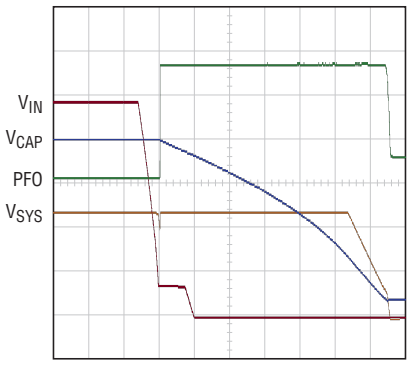
Storage capacitance:

$$C_{STORAGE} = \frac{2 \bullet V_{SYS} \bullet I_{SYS} \bullet T_H}{V_{CAP}^2 - V_{SYS}^2}$$

CONCLUSION

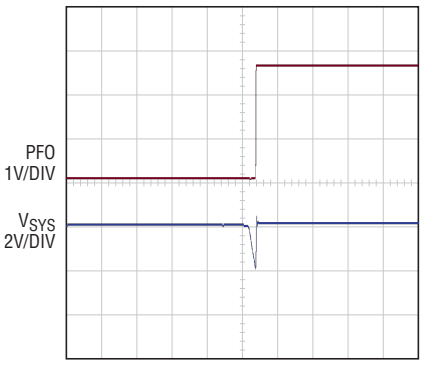
The LTC3643 is a highly integrated, high performance backup regulator. The design shown here combines the advantages of this IC with a high efficiency buck-boost LTM4607 µModule regulator. Together, these devices enable a small footprint, efficient and cost-effective solution for data retention and backup in automotive and industrial applications. ■

Figure 2. Switchover waveforms



V_{SYS}= LOAD VOLTAGE = 5V/DIV
V_{IN} = INPUT VOLTAGE = 5V/DIV
PFO = FLAG STATUS = 1V/DIV
V_{CAP} = $C_{STORAGE}$ VOLTAGE = 10V/DIV

Figure 3. Detailed view of switching waveforms



High Efficiency, 15V Rail-to-Rail Output Synchronous Step-Down Regulator Can Source or Sink 5A

Timothy Kozono

The LTC3623 is a high efficiency, monolithic synchronous step-down regulator capable of sourcing or sinking up to 5A of continuous output current from an input voltage range of 4V to 15V. Its compact 3mm × 5mm QFN package incorporates an abundance of features including a low EMI Silent Switcher architecture, output voltage cable drop compensation and single resistor output voltage programming. The constant frequency/controlled on-time architecture responds quickly to line and load transients even in low duty cycle, high frequency applications. The device offers a 400kHz to 4MHz operating frequency range with multiple optional protection and monitoring features, enabling compact, robust solutions. V_{IN} regulation, discontinuous/continuous mode and a supply current less than 1µA during shutdown make this regulator suitable for a wide range of power applications.

A single resistor is used to set the internal reference voltage for the device. The adjustable internal reference voltage sets the output voltage and allows the output voltage to operate rail-to-rail, from 0V to V_{IN}. The reference voltage can be driven directly as an audio driver or configured to operate as a TEC driver. Capable of sourcing or sinking 5A of output current, the regulator moves the output voltage quickly in either direction. The output current monitor signal can be used to increase the reference voltage to compensate for output voltage drop caused by cable resistance.

3.3V Output, 1MHz Buck Regulator

Figure 1 shows the complete schematic for a high efficiency 12V input to 3.3V output application. The compact package contains a low 30mΩ $R_{DS(ON)}$ synchronous bottom MOSFET switch and a 60mΩ $R_{DS(ON)}$ synchronous top MOSFET switch for high efficiency and minimal thermal issues.

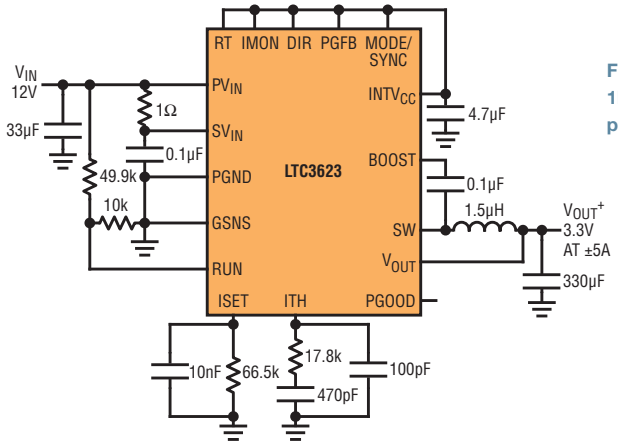


Figure 1. High efficiency 12V to 3.3V 1MHz step-down regulator with programmable reference

Figure 2. Efficiency and power loss for the solution in Figure 1 in CCM and DCM mode

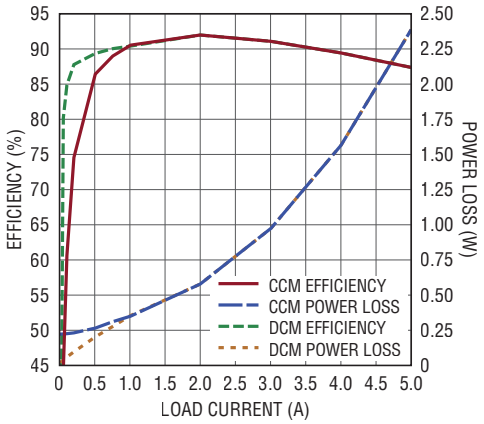
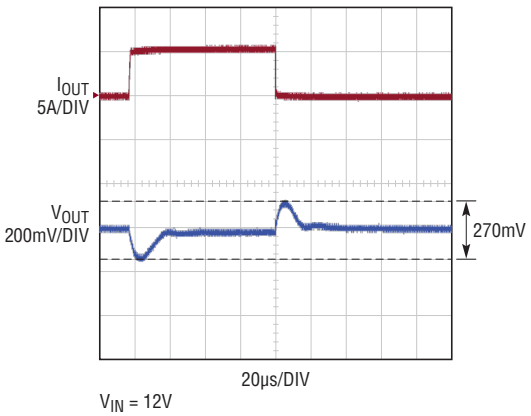


Figure 3. 0A to 5A load step response of the converter in Figure 1



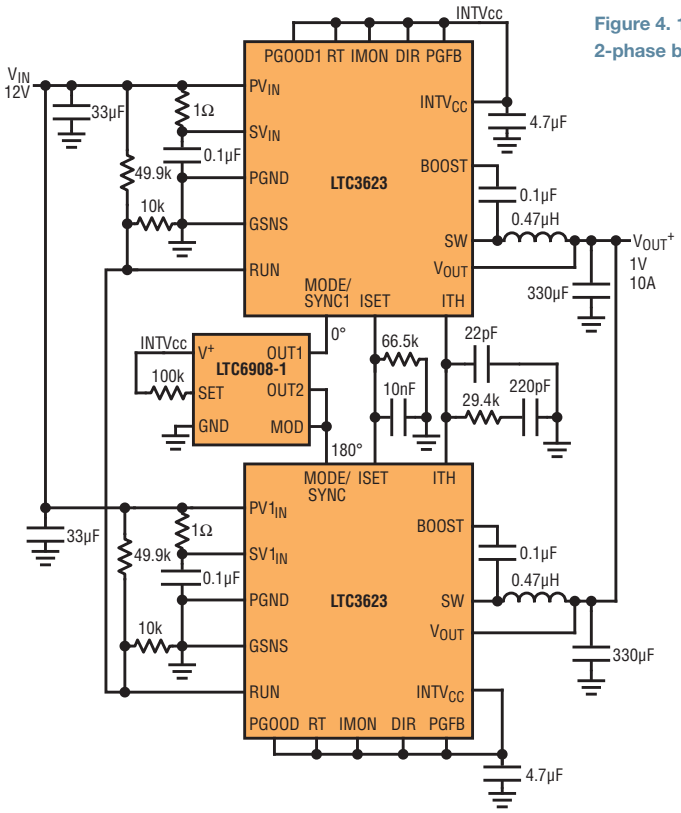


Figure 4. 12V to 1V at ±10A 2-phase buck converter

Figure 5. Efficiency and power loss for the 2-phase buck converter

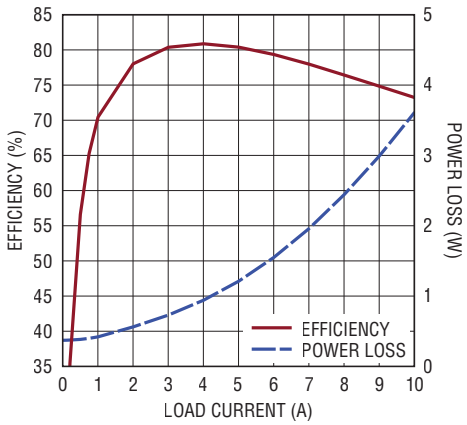


Figure 2 shows the continuous and discontinuous conduction mode efficiency and power loss. Discontinuous conduction mode significantly improves light load efficiency while adding a slight increase in output voltage ripple. Figure 3 shows the load-step response with only 330µF of output capacitance.

DUAL-PHASE DESIGN INCREASES OUTPUT CURRENT CAPABILITY

Figure 4 shows a complete 1MHz 12V input to 1V output dual-phase schematic capable of sourcing or sinking up to 10A. The phases are synchronized by the LTC6908-1 oscillator with 180° interleaving to lower output voltage ripple. Figure 5 shows the efficiency and power loss for the overall system. The low thermal resistance of the LTC3623 package uses the PCB to dissipate heat. The thermal image is shown in Figure 6. From Figure 5, we can see that each phase dissipates 1.8W at 10A output current, which raises the chip temperature to 63°C from an ambient temperature of 25°C with no airflow.

CONCLUSION

The LTC3623 step-down regulator enables compact POL solutions that can source or sink 5A without significant thermal mitigation. Power capability is easily expanded by paralleling devices, which has other benefits such as spreading the heat and reducing output ripple. Heat dissipation problems are minimized by the LTC3623's low thermal impedance and high efficiency capability. The LTC3623's extensive set of programmable features satisfies the requirements of a wide range of applications. ■

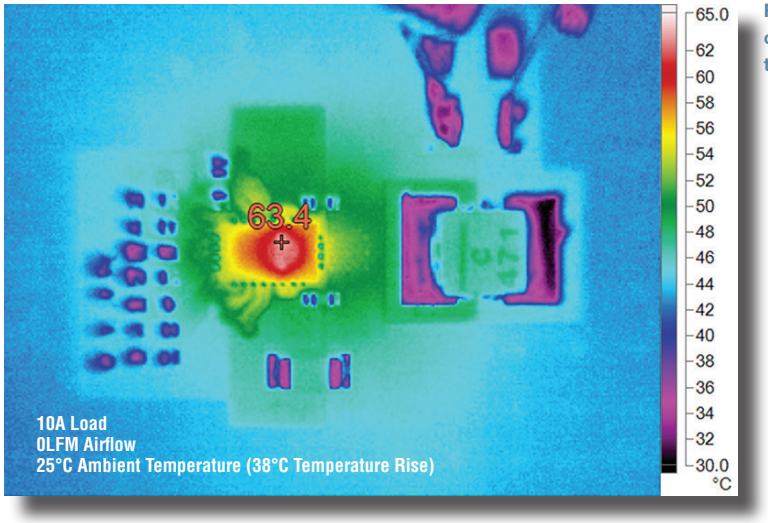


Figure 6. Thermal image of the master phase of the Figure 4 circuit

New Product Briefs

2µA SUPPLY CURRENT, LOW I_B, ZERO-DRIFT OPERATIONAL AMPLIFIER

The LTC2063 is a single low power, zero-drift, 20kHz amplifier. The LTC2063 enables high resolution measurement at extremely low power levels.

Typical supply current is 1.4µA with a maximum of 2µA. The available shutdown mode has been optimized to minimize power consumption in duty-cycled applications and features low charge loss during power-up, reducing total system power.

The LTC2063's self-calibrating circuitry results in very low input offset (5µV max) and offset drift (0.02µV/°C). The maximum input bias current is only 20pA and does not exceed 100pA over the full specified temperature range. The extremely low input bias current of the LTC2063 allows the use of high value power-saving resistors in the feedback network.

With its ultralow quiescent current and outstanding precision, the LTC2063 can serve as a signal chain building block in portable, energy harvesting and wireless sensor applications.

The LTC2063 is available in 6-lead SC70 and 5-lead TSOT- 23 packages and is fully specified over the –40°C to 85°C and –40°C to 125°C temperature ranges.

60V I²C BATTERY MONITOR MEASURES STATE OF CHARGE PARAMETERS WITH 1% ACCURACY

The LTC2944 multicell battery monitor, makes direct measurements of 3.6V to 60V battery stacks. No level shifting circuitry on the supply and measurement pins is required to interface with multicell voltages, so total current consumption is minimized and measurement accuracy is preserved. The LTC2944 is a true high voltage battery monitor that measures charge, voltage, current and temperature to 1% accuracy, the essential parameters required to accurately assess battery state of charge (SoC).

The LTC2944 is ideal for multicell applications, including electric vehicles, ebikes/motorcycles/scooters, wheelchairs, golf carts and battery backup systems. Battery current is measured by monitoring the voltage across an external, high side sense resistor and integrating this information to infer charge. A bidirectional analog integrator accommodates either current polarity (battery charge or discharge), and a programmable prescaler supports a wide range of battery capacities. Charge, voltage, current and temperature information are communicated to the host system over an I²C/SMBus-compatible 2-wire interface that is also used to configure the battery monitor. The host can program high and low thresholds for all measured parameters, which if tripped, signal an alert using either the SMBus alert protocol or by setting a register flag.

The LTC2944 is offered in commercial and industrial versions, supporting operating temperature ranges from 0°C to 70°C and –40°C to 85°C, respectively. The LTC2944 is available today in a small RoHS-compliant, 8-pin 3mm × 3mm DFN package.

ULTRATHIN 1.8mm, 3A µMODULE REGULATOR IN 6.25mm × 6.25mm LGA PACKAGE FOR PCIe, ATCA, MicroTCA CARDS & BACKSIDE PCB ASSEMBLY

The LTM4623 3A µModule (micromodule) step-down regulator features an ultrathin 1.8mm profile LGA package with only a 6.25mm × 6.25mm footprint. With solder paste, the package height is less than 2mm, meeting the height restrictions of many PCIe (peripheral component interconnect express), advanced mezzanine cards (AMC) for AdvancedTCA carrier cards in embedded computing systems. The small size and low height allow the LTM4623 to be mounted on the backside of the PCB, freeing space on the topside for components such as memory and FPGAs. The LTM4623 operates from 4V to 20V input supplies and precisely regulates an output voltage from 0.6V to 5.5V with 1.5% maximum total DC output voltage error. Application examples include ultra-dense data storage, gateway controllers and 40Gbps to 100Gbps network equipment.

The LTM4623 solution fits in a 0.5cm² dual-sided PCB or <1cm² on a single-sided PCB. The circuit requires only one input capacitor and one output capacitor, a resistor to set V_{OUT}, and a small capacitor for V_{OUT} tracking and soft-start. With an auxiliary 5V bias, the LTM4623 operates from input

supplies as low as 2.375V. The operating efficiency for converting 12V input to 1.5V and 3.3V out at 3A is 80% and 88%, respectively. Power loss for 12V in to 1.5V out is 1.1W, resulting in only a 24°C rise in junction temperature. The LTM4623 is rated for operation from –40°C to 125°C.

50A TO 300A, SCALABLE µMODULE REGULATOR NEEDS 60% LESS CAPACITANCE TO POWER SUB-28nm GPUs, FPGAs, ASICs & PROCESSORS

The LTM4650-1A and LTM4650-1B, dual 25A or single 50A µModule (power module) regulators are able to deliver 300A to high power, low voltage sub-28nm GPUs, FPGAs, ASICs and microprocessors. The low core voltage of these digital devices requires very accurate voltage regulation at both steady state (DC) and fast load current transients. The LTM4650-1A guarantees ±0.8% total DC voltage accuracy over reference, line, load and temperature (–40°C to 125°C), whereas the LTM4650-1B guarantees ±1.5%. Both devices can be optimized for ±3% or better total error band, including load step transients with a minimum number of ceramic capacitors to meet the core voltage window requirement of sub-28nm digital ICs.

Compared to competing power POL module regulators, the LTM4650-1A requires 60% less capacitance because of three main features (12V input, 1V output, 0A to 25A load step, 25A/µs):

1. Guaranteed ±0.8% total DC voltage accuracy allows more margin (less capacitance) for the AC variation due to a load transient response to satisfy a given processor core voltage tolerance window.
2. The device can be externally adjusted (compensated) for optimum loop response to deliver load transients with fewer output capacitors.
3. The device operates with phase interleaving, which reduces input and output current ripple, reducing the requirement for load capacitance.

The LTM4650-1 includes a dual output DC/DC regulator, inductors and MOSFETs in a 16mm × 16mm × 5.01mm BGA package. The LTM4650-1 regulates an output voltage ranging from 0.6V to 1.8V from an input voltage within 4.5V to 15V. Delivering 50A, 92% efficiency is recorded at 5V input, 1.8V output and 86% at 12V input, 1.0V output. The LTM4650-1 delivers the full 50A current up to 70°C ambient, from 12V input to 1.0V output with 200LFM airflow. The LTM4650-1 can be operated in parallel to increase output current, up to six in parallel for 300A of output current.

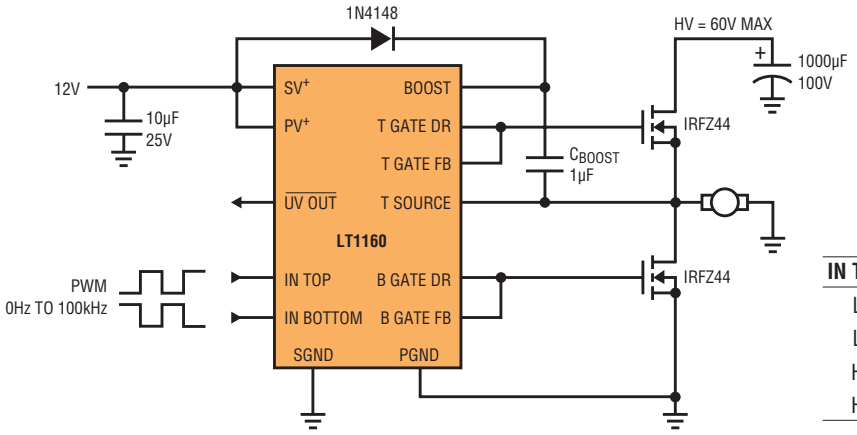
The LTM4650-1 is pin-compatible with the lower current LTM4630-1 (dual 18A or single 36A); so users can choose the correct device depending on load current without changing PCB layout.

2A, 2MHz, 28V BOOST/SEPIC/INVERTING DC/DC CONVERTER WITH I_Q = 6µA

The LT8335 is a current mode, 2MHz step-up DC/DC converter with an internal 2A, 28V switch. It operates from an input voltage range of 3V to 25V, suitable for applications with input sources ranging from a single-cell Li-ion to automotive inputs. The LT8335 can be configured as either a boost, SEPIC or an inverting converter. It utilizes a fixed 2MHz switching frequency, enabling designers to minimize external component sizes and avoid critical frequency bands, such as AM radio. Burst Mode operation reduces quiescent current to only 6µA while keeping output ripple below $15mV_{P-P}$. The combination of a 3mm × 2mm DFN package and tiny externals ensures a very compact footprint while minimizing solution cost.

The LT8335's 170mΩ switch delivers efficiencies of over 90%, while programmable undervoltage lockout (UVLO) optimizes system performance. A single feedback resistor sets the output voltage whether the output is positive or negative, minimizing external components. Other features include internal compensation, soft-start, frequency foldback and thermal shutdown protection.

The LT8335EDDB is available in a 3mm × 2mm DFN-8 package. An industrial temperature (–40°C to 125°C) version, the LT8335IDDB, is also available. ■



LT1160/LT1162: 60V MAX SUPPLY REFERENCED DC MOTOR HALF-BRIDGE DRIVER

The LT1160/LT1162 are cost effective half-/full-bridge N-channel power MOSFET drivers. The floating driver can drive the topside N-channel power MOSFETs operating off a high voltage (HV) rail of up to 60V.

www.linear.com/solutions/7900

IN TOP	IN BOTTOM	T GATE DR	B GATE DR
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

LT6018 LOW NOISE, HIGH CMRR INSTRUMENTATION AMPLIFIER

The LT6018 is a 33V precision operational amplifier with excellent noise performance. With 0.1Hz to 10Hz noise of only $30nV_{P-P}$, the LT6018 is an outstanding choice for applications where 1/f noise impacts system performance. The LT6018 has excellent DC performance with a maximum offset voltage of 50µV and a maximum offset voltage drift of 0.5µV/°C. The input offset voltage remains low over the entire common mode input range, providing a minimum CMRR of 124dB. Open loop gain is typically 142dB, enabling the device to achieve linearity better than 1ppm. The proprietary circuit topology of the LT6018 provides excellent slew rate and settling time without compromising noise or DC precision.

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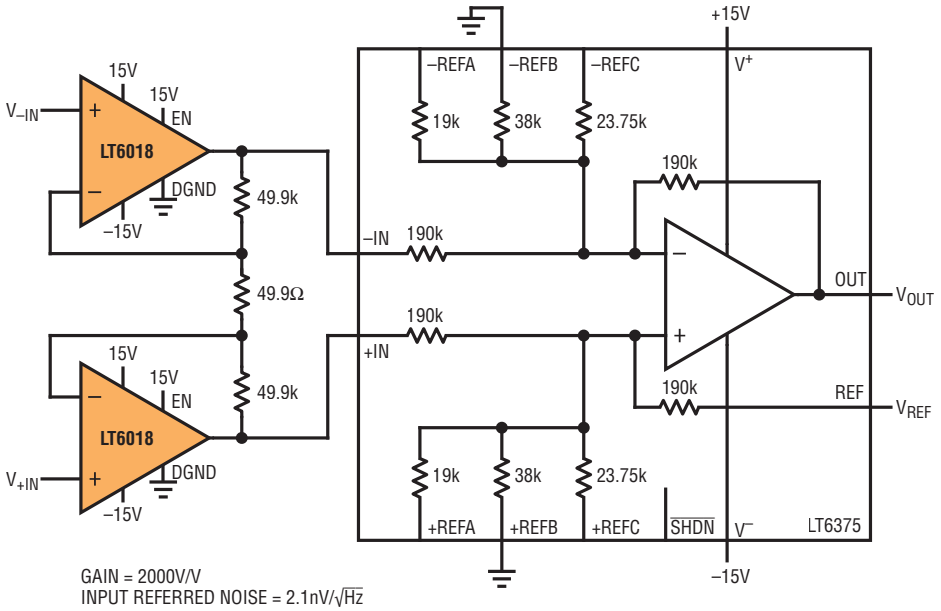

GAIN = 2000V/V
INPUT REFERRED NOISE = 2.1nV/√Hz
CMRR = 150dB
–3dB BANDWIDTH = 7.5kHz

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