LINEAR TECHNOLOGY

The LTC1605: New 16-Bit, 100ksps ADC

by Sammy Lum

Introduction

Linear Technology continues its push into the high resolution, high performance analog-to-digital converter market with the introduction of the LTC1605. Linear Technology's first 16-bit ADC has outstanding DC accuracy and a wide analog input range of ±10V. The LTC1605 provides an effective solution for a wide range of industrial control applications. Its simple I/O, low power and high performance make it easy to design into applications requiring wide dynamic range and high resolution.

Product Features

❏ 16-bits with no missing codes and ± 2LSB INL
❏ Single 5V supply with typical power dissipation of 55mW
❏ Complete ADC contains sample-and-hold and reference
❏ ±10V analog input with ±20V overvoltage protection on a 5V supply
❏ 28-pin PDIP, SO and SSOP packages

The device will not be damaged if the analog input is taken outside its nominal operating range of ±10V; it can withstand an overvoltage of ±20V, which makes it easier to protect from the harsh environments often found in industrial applications. The large least-significant-bit size (305μV) makes the input signal conditioning circuitry easier to design. The DC accuracy is guaranteed to be 16 bits with no missing codes, with an integral nonlinearity specification of ±2LSB over the industrial temperature range (–40°C to 85°C). The space-saving SSOP package occupies only 0.12 square inch.

Circuit Description

We will begin by briefly describing how the analog input signal progresses through the various elements of the LTC1605 to become a digital word. First, how does the LTC1605 handle a ±10V analog input signal while operating off a 5V supply? It uses a resistor network, as shown in the LTC1605 block diagram in Figure 1. The input signal is attenuated by a factor of eight and then one-half of the reference voltage is added to the attenuated signal. This reduced internal signal now has a least-significant-bit size of 38μV. Next, this attenuated signal is sampled and held. The output of the sample-and-hold is digitized with a switched-capacitor differential 16-bit successive approximation register ADC. This differential architecture provides greater immunity to power supply noise and to other external noise sources that can corrupt the result. Finally the digitized data is output to the user at a rate of up to 100ksps. The digital output word can be read as a parallel 16-bit word or it can be read as two 8-bit bytes. The 2-byte output requires using the BYTE pin. With the BYTE pin low the first eight MSBs are output on the D15–D8 pins. When the BYTE pin is taken high the eight LSBs replace the eight MSBs.

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Issue Highlights

Our cover article this month introduces Linear Technology's first 16-bit ADC, the LTC1605. This product has outstanding DC accuracy and a wide analog input range of ±10V. The LTC1605 provides an effective solution for a wide range of industrial control applications. Its simple I/O, low power and high performance makes it easy to design into applications requiring wide dynamic range and high resolution.

Also in the data conversion area, we debut a new 14-bit 800ksps ADC, the LTC1419. The LTC1419 satisfies the needs of new communications, spectral-analysis, instrumentation and data acquisition applications by providing an upgrade path to users of 12-bit converters. It provides outstanding 81.5dB SINAD (signal-to-noise and distortion ratio) and 95dB SFDR (spurious free dynamic range) for frequency-domain applications, and excellent ±1LSB DNL and no missing codes performance for time-domain applications.

On the power control front, this issue introduces two new products: the LTC1624 SO-8 N-channel switching regulator controller and the LTC1514/LTC1515 switched capacitor step-down converters. The newest member of Linear Technology's next generation of DC/DC controllers, the LTC1624 uses the same constant frequency, current mode architecture and Burst Mode™ operation as the LTC1435–LTC1439 controllers, but without the synchronous switch. The LTC1624 can operate in all standard switching configurations, including boost, step-down, inverting and SEPIC, without a limitation on the output voltage. A wide input voltage range of 3.5V to 36V allows operation from a variety of power sources, from as few as four NiCd cells up though high voltage wall adapters.

A unique architecture allows the LTC1514/LTC1515 to accommodate a wide input voltage range (2.0V to 10V) and adjust the operating mode as needed to maintain regulation. As a result, the parts can be used with a wide variety of battery configurations and/or adapter voltages. Low power consumption and low external parts count make the parts well suited for space-conscious low power applications, such as cellular phones, PDAs and portable instruments.

In the interface area, we present the LTC1685–87 family of RS485 transceivers. These transceivers can operate at data rates of >40Mbps over one hundred feet of category 5 unshielded twisted pair. They employ a unique architecture that guarantees excellent performance over process and temperature variations, with combined propagation delays for both the receiver and driver of 18.5ns ±3.5ns. A novel short-circuit protection technique permits indefinite shorts (to either driver or receiver output) to power or ground while sourcing/sinking a maximum of 50mA.

Also in this issue, we have a new application for the LTC1421 Hot Swap™ controller: hot swapping the PCI bus. The PCI bus is widely used in high volume personal computers and single-board computer designs. With the migration of the PCI bus into servers, industrial computers and computer-telephony systems, the ability to plug a peripheral into a live PCI slot becomes mandatory. Using the LTC1421 to control the power supplies, a peripheral can be inserted into a PCI slot without turning off the system power.

The Design Ideas section of this issue includes a –48V to 5V DC/DC converter that operates from a telephone line, a water tank pressure sensor interface, a chopped amplifier that requires only 5µA of supply current and a pair of circuits for generating a low noise –5V supply for use in data acquisition applications. The remainder of this section is occupied by part one of an epic disquisition on IC voltage references, to be concluded in the August issue.

The issue concludes with a quintet of new device cameos. *LT*

Figure 1. The block diagram shows that the LTC1605 has an onboard reference, sample-and-hold amplifier, clock and a 16-bit differential switched-capacitor ADC. The analog input accepts a ±10V signal and can withstand an overvoltage of ±20V on a 5V supply.

LTC1605, continued from page 1

The LTC1605 is easily connected to FIFOs, DSPs and microprocessors via the convert-start input (R/$\overline{C}$) and data ready signal ($\overline{BUSY}$). With $\overline{CS}$ low, the falling edge of the R/$\overline{C}$ signal will put the LTC1605 into the hold mode and start a conversion. $\overline{BUSY}$ goes low during the conversion and the output data can be latched after the conversion when $\overline{BUSY}$ goes back high.

The LTC1605 has a bandgap reference trimmed to a nominal voltage of 2.500V. As shown in Figure 2, it can be overdriven with an external reference if greater accuracy is needed. The REF pin is buffered by a unity-gain amplifier that drives the internal DAC, along with the level shifting input resistor. The output of the buffer is the CAP pin.

Figure 3 shows the fast Fourier transform (FFT) of a sine wave signal that has been digitized by the LTC1605. We see a very good AC response from the device. The measurement was made with the sampling frequency set at 100kHz and with a 1kHz sine wave applied to the analog input. The key results obtained were a signal-to-noise and
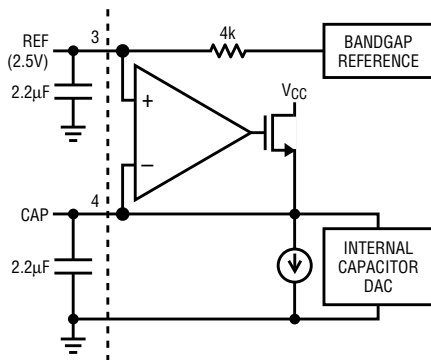
Figure 2. The LTC1605 has a 2.500V bandgap reference. The internal reference can be easily overdriven if greater accuracy is needed. The output of the internal or external reference is buffered by a unity-gain amplifier. The buffer drives the internal DAC and the input level-shift resistor.

Figure 3. The FFT plots shows that the THD of the LTC1605 is better than 100dB with a signal-to-noise and distortion of 87.5dB.

Figure 4. The INL error plot shows that the LTC1605 is very accurate. This is achieved without autocalibration and its associated overhead. The accuracy relies on capacitor matching, which is very stable over temperature and time.

Figure 5. Power supply feedthrough is extremely low over a wide frequency range.
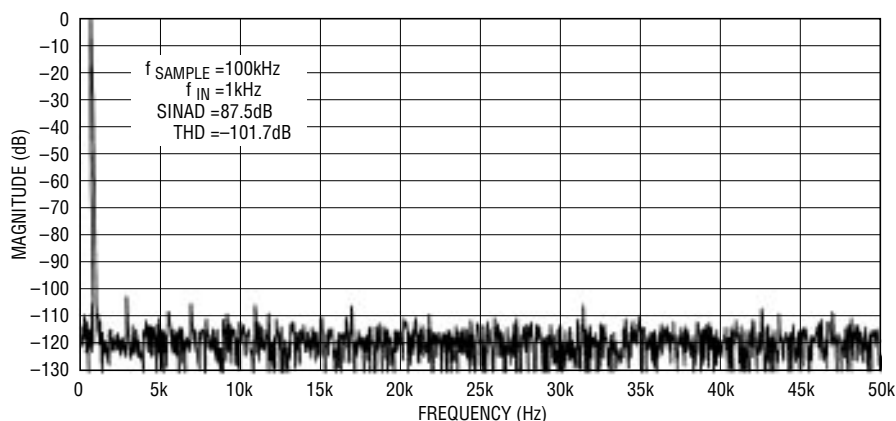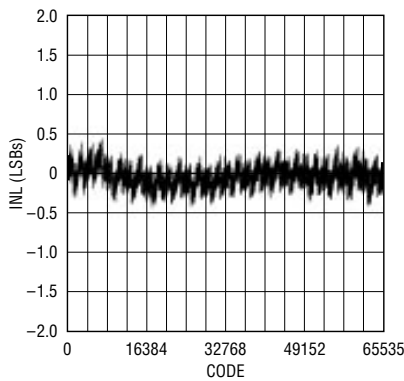

Figure 6. The histogram shows the LTC1605 has a RMS code transition noise of 1LSB.

distortion (SINAD) of 87.5dB and total harmonic distortion (THD) of –101.7dB. The ±10V input signal was generated with an Audio Precision System One audio analyzer.

One of the benefits of using a differential architecture for an ADC is good power supply rejection. Figure 5 shows the power supply rejection of the LTC1605 as a function of frequency.

DC and AC Performance

Figure 4 shows an INL error plot for the LTC1605. Guaranteed specifications include ±2.0LSB INL (max) and no missing codes at 16 bits over the industrial temperature range. The accuracy of the ADC is trimmed at the factory and does not carry the overhead for the user associated with autocalibration-type ADCs.

Histogram Noise Measurement

One way of measuring the transition noise associated with a high resolution ADC is to use a technique where a fixed DC signal is applied to the input of the ADC and the resulting output codes are collected over a large number of conversions. The shape of the distribution of codes will give an indication of the magnitude of the transition noise. For example, in Figure 6 the distribution of output codes is shown for a DC input that has been digitized 10,000 times. The distribution is Gaussian and the RMS code transition noise is about 1LSB.

Printed Circuit Board Layout

The suggested layout for an LTC1605 evaluation circuit included herein is an example of a properly designed printed circuit board that will help

obtain the best performance from this 16-bit ADC. The details of the layout along with the circuit schematic are shown in Figures 7a–7d. Pay particular attention to the design of the analog and digital ground planes. The DGND pin of the LTC1605 can be tied to the analog ground plane. Placing the bypass capacitors as close as possible to the power supply pin and the reference and reference buffer output pins is very important. A simple RC filter can be added to the external input resistor network, as shown in Figure 8. This will prevent high frequency noise from coupling into the analog input. An NPO-type capacitor gives the lowest distortion. The digital output latches and the onboard oscillator have been placed on the digital ground plane. The two ground planes
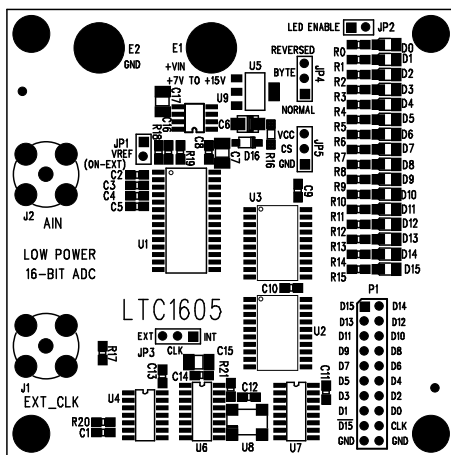
Figure 7a. Component side silkscreen for the suggested LTC1605 evaluation circuit
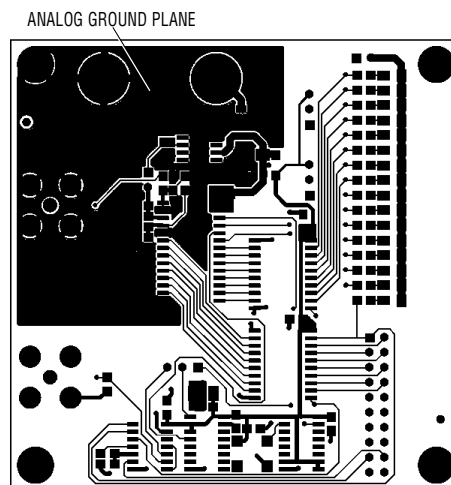
Figure 7b. The top side of the board has the components and shows the analog ground plane.
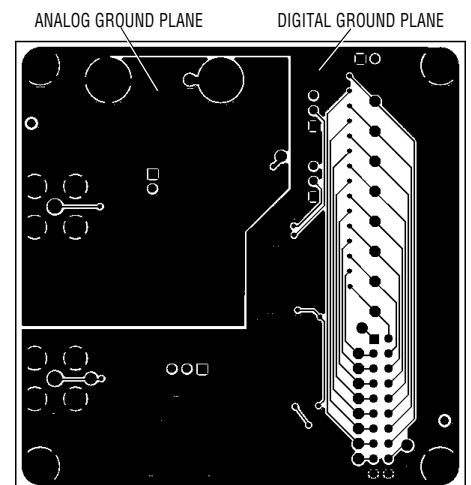
Figure 7c. The bottom side of the board shows how the analog and digital ground planes are isolated.
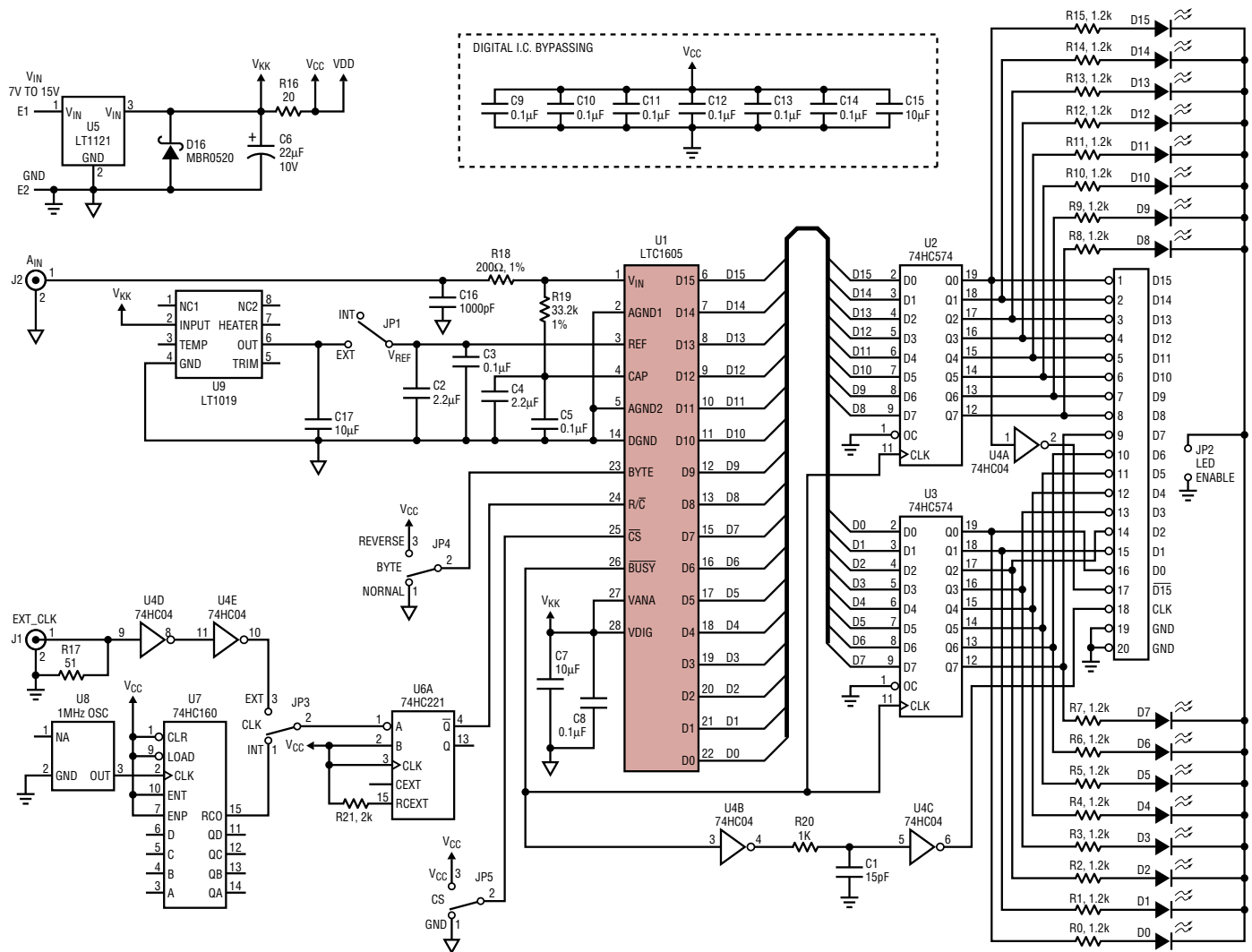
Figure 7d. LTC1605 suggested evaluation circuit schematic; this circuit includes output latches, conversion clock and an optional external reference.

are tied together at the power supply ground connection. In this evaluation circuit, after the start convert signal (R/$\overline{C}$) has gone low to start a conversion, it is brought back high 50ns later. This signal should be brought back high within 3µs after

Figure 8. A capacitor can be added to the external resistor network to form a simple lowpass filter. This will help prevent high frequency noise from coupling into the analog input.

the start of a conversion to ensure that no errors occur in the digitized result.

Applications

With its overvoltage protected ±10V analog input, the LTC1605 fits easily into industrial process control, power management and data acquisition board applications. In designs where wide dynamic range is required, one traditional way to implement this was to use a PGA with a lower resolution ADC. Now, with a 16-bit ADC, the PGA can be eliminated. For example, with a 12-bit ADC a PGA with a range of 1 to 16 would be required to cover the same range as a 16-bit ADC.

The LTC1605 has sufficient speed to be used in multiplexed applica-

tions. In such a system, there will typically be an analog multiplexer followed by a signal conditioning circuit, which may include filtering, programmable gain, and the like, and then the ADC. The LTC1605 needs to be driven from a low source impedance to prevent gain errors due to its 20kΩ input resistance.

The offset and full-scale error can be adjusted to zero using three external resistors along with two trim pots, as shown in Figure 9a. The full-scale error and offset for the LTC1605 have been factory trimmed with the two external resistors, R_A and R_B, in place. Figure 9b shows how the device can be connected if additional trimming is not needed.

New 14-Bit 800ksps ADC Upgrades 12-Bit Systems with 81.5dB SINAD, 95dB SFDR

by Dave Thomas and William C. Rempfer

Higher Dynamic Range ADCs

A new 14-bit 800ksps ADC, the LTC1419, satisfies the needs of new communications, spectral-analysis, instrumentation and data acquisition applications by providing an upgrade path to users of 12-bit converters. It provides outstanding 81.5dB SINAD (signal to noise and distortion ratio) and 95dB SFDR (spurious free dynamic range) for frequency-domain applications, and excellent ±1LSB DNL and no missing codes performance for time-domain applications.

LTC1419 Features

❏ Complete 14-bit, 800ksps ADC

❏ ±1LSB DNL and ±1.25LSB INL (max)

❏ 81.5dB SINAD and 95dB SFDR

❏ Low power—150mW on ±5V supplies

❏ Nap/Sleep power-down modes

❏ Small Footprint—28-pin SO or SSOP

The Big Brother of the LTC1410

The new LTC1419 is a 14-bit derivative of the LTC1410 ADC from LTC. It has a similar pinout and function, as shown in the block diagram in Figure 1. Inputs are received by the wideband differential sample-and-hold (S/H). This S/H is capable of sampling to Nyquist and beyond and operates with either differential or single-ended signals. In contrast to some converters, which must be driven differentially to perform well, this ADC operates equally well with single ended or differential signals. (To digitize a single-ended signal, simply ground the negative input.)
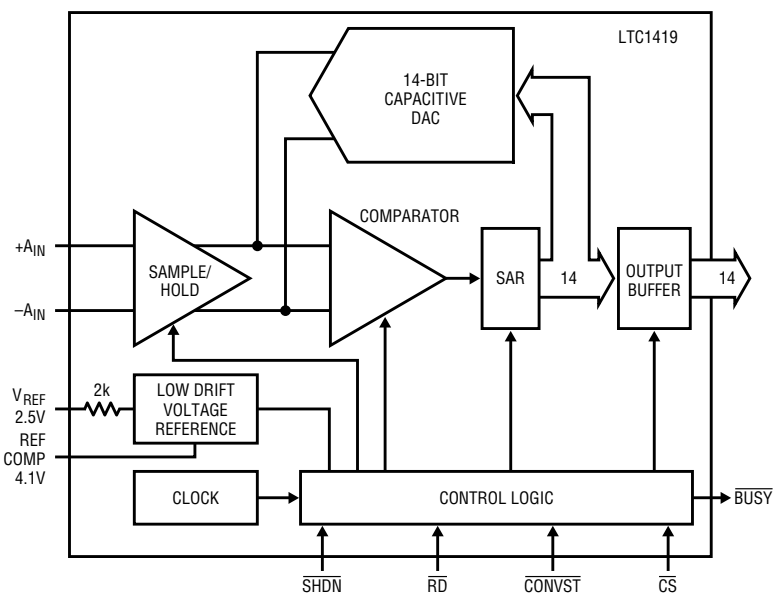
Figure 1. This complete 800ksps, 14-bit ADC has a wideband S/H that cleanly samples wideband input signals
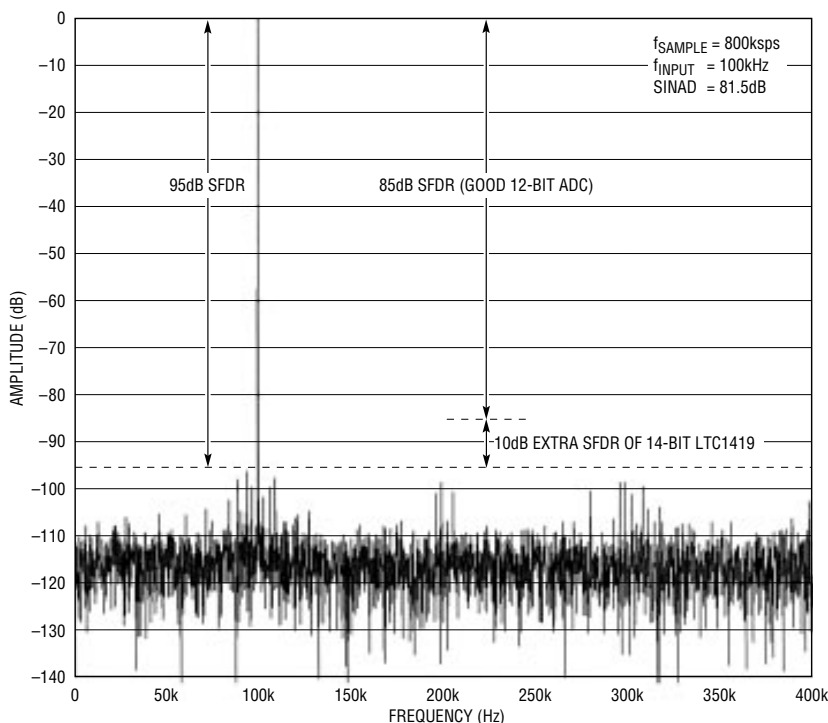
Figure 2. The LTC1419 gives a 10dB improvement in spectral purity over even the best 12-bit devices. This FFT shows the LTC1419's outstanding 81.5dB SINAD and 95dB SFDR.
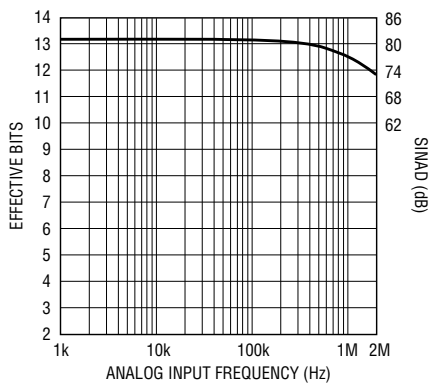
Figure 3. As the input signal frequency is increased, many ADCs start to loose spectral purity due to distortion or noise. The LTC1419 has essentially flat SINAD and effective bits out to Nyquist. Even when undersampling a 2MHz input, it maintains 12-bit performance.

The ADC uses a switched-capacitor SAR technique, similar to that of its predecessor, that yields excellent DC specifications and stability. It is a clean, simple to use design that delivers 800ksps conversion rate at low power levels.

The ADC has a flexible parallel I/O, which can interface to a DSP, a microprocessor, an ASIC or to dedicated logic. Conversions can be started either under command of a DSP or microprocessor or from an external

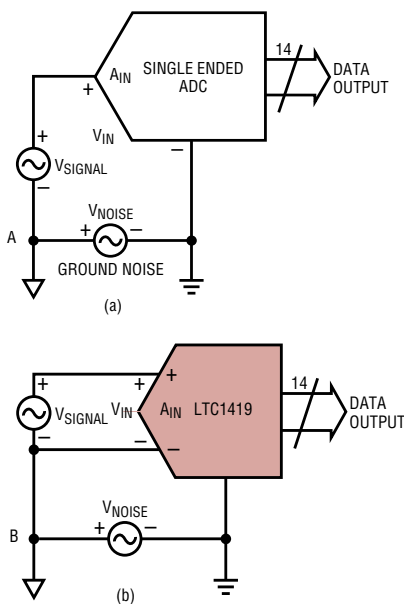**Figure 4. a) In high resolution ADC systems, noise sources such as ground noise and magnetic coupling can contaminate the ADC's input signal. b) The LTC1419's differential inputs can be used to reject this noise, even if it is at high frequencies.**

sample clock signal. An output disable allows the outputs to be three-stated.

The LTC1419, like the 12-bit LTC1410, operates from ±5V supplies and draws 150mW of power.

10dB Extra Dynamic Range for Signal Applications

The LTC1410 is probably the cleanest 12-bit ADC on the market. The part achieves 72dB SINAD and has an SFDR of better than 85dB. These numbers approach the theoretical limit for 12 bits. Figure 2 shows the improvements possible with the LTC1419. The 14-bit device achieves 81.5dB SINAD (an increase of roughly 10dB over the 12-bit device). The SFDR increases to 95dB. This gives the converter 10dB more resolving power to pick out small signals in communication and spectrum-analysis applications. This clean sampling capability is maintained even for wideband inputs. Figure 3 shows high effective bits and SINAD for inputs beyond Nyquist.

Four Times Improvement in DC Resolution

The 12-bit LTC1410 guarantees ±1LSB of integral and differential nonlinearity (INL and DNL). The 4096 steps over a 5V input range yield an LSB of 1.22mV. The new 14-bit part also maintains excellent linearity (±1LSB DNL, ±1.25LSB INL); resolution is increased and the LSB is reduced to 305μV.

Noise-Rejecting Differential Inputs

With its higher dynamic range and resolution, the LTC1419 can digitize signals more cleanly than previous devices. However, as the resolution increases and the noise floor drops, other system noises may show up unless precautions are taken. The differential input of the new ADC provides a way to keep noise out. Noise can be introduced in a number of ways including ground bounce, digital noise and magnetic and capacitive coupling (see Figure 4a). All of these sources can be reduced dra-

matically by measuring differentially from the signal source, as in Figure 4b. The high CMRR of the differential input (Figure 5) allows the LTC1419 to reject resulting common mode noise by over 60dB and maintain a clean signal.

Other Nice Features

Several other features make the LTC1419 flexible and easy to use:

❏ Both analog inputs have infinite DC input resistance, which makes them easy to multiplex or AC couple.

❏ The separate convert-start input pin allows precise control over the sampling instant. The S/H aperture delay is less than 1ns and the aperture jitter is below 1ps RMS.

❏ Conversion results are available immediately after a conversion and there is no latency in the data (no pipeline delay). This is ideal for both single shot and repetitive measurements.

❏ The low 150mW power dissipation can be reduced further using the ADC's Nap and Sleep power-down modes. Wake up from Nap mode is instantaneous. Sleep mode wake up time is several milliseconds.

❏ The LTC1419 is the industry's smallest high speed 14-bit converter: it is available in a 28-pin SSOP package.

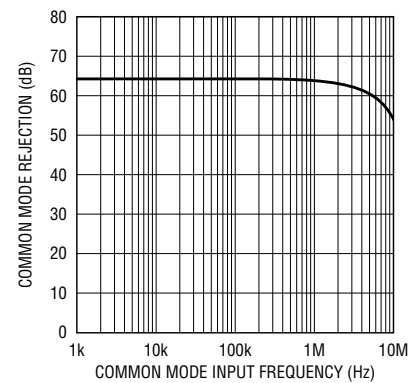**Figure 5. The common mode rejection of the analog inputs rejects common mode input noise frequencies to beyond 10MHz.**

The LT1495/LT1496:
1.5µA Rail-to-Rail Op Amps

by William Jett

Introduction

Micropower rail-to-rail amplifiers present an attractive solution for battery-powered and other low voltage circuitry. Low current is always desirable in battery-powered applications, and a rail-to-rail amplifier allows the entire supply range to be used by both the inputs and the output, maximizing the system's dynamic range. Circuits that require signal sensing near either supply rail are easier to implement using rail-to-rail amplifiers. However, until now, no amplifier combined precision offset and drift specifications with a maximum quiescent current of 1.5µA.

Operating on a minuscule 1.5µA per amplifier, the LT1495 dual and LT1496 quad rail-to-rail amplifiers consume almost no power while delivering precision performance associated with much higher current amplifiers. Input offset voltage is only 375µV maximum, with a maximum drift of 2µV/˚C, and input offset current is 100pA maximum. The low bias currents (1nA maximum) and low offset currents of these amplifiers permit the use of megohm-level source resistors without introducing significant errors. A minimum open-loop gain of

100V/mV guarantees that gain errors are small. The device characteristics change little over the supply range of 2.2V to ±15V: worst-case supply rejection is 90dB and the common mode rejection ratio is greater than 90dB. The LT1495 dual amplifier is available in the 8-pin SO and the 8-pin mini-DIP package. The LT1496 quad amplifier is available in 14-pin SO and 14-pin DIP.

The LT1495/LT1496 feature "over-the-top" operation: the ability to operate normally with the inputs above the positive supply. The devices also feature reverse-battery protection.

Start-Up Characteristics

Micropower op amps are sometimes not micropower during start-up, wreaking havoc on low current supplies. In the worst case, there may not be enough supply current available to take the system up to nominal voltages. Figure 1 shows a graph of LT1495 supply current versus supply voltage for the three limit cases of input offset that could occur during start-up. The circuits are shown in Figure 2. One circuit creates a positive offset, forcing the output to come up saturated high, another circuit creates a negative offset, forcing the output to come up saturated low and

Figure 2. Circuits for start-up characteristics

Figure 1. LT1495 supply current vs supply voltage for the three limit cases of input offset that could occur during start-up
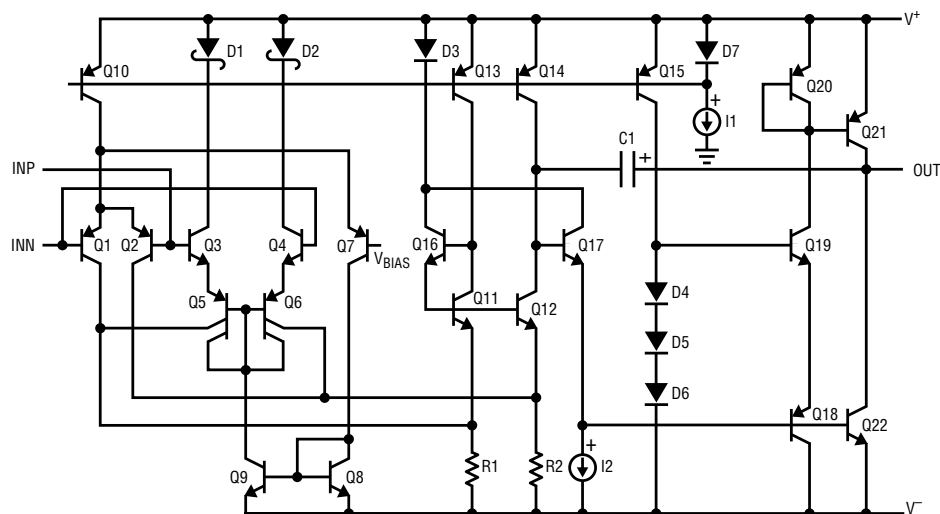
Figure 3. LT1495 simplified schematic
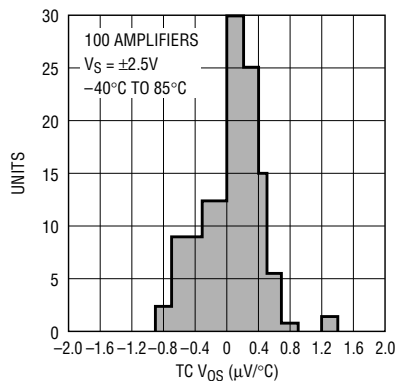
Figure 4. Input offset voltage drift distribution plot

Figure 5. 0nA–200nA current meter

the last brings up the output at half supply. In all cases, the supply current is well behaved. Supply current is highest with the output forced high, so if one amplifier is unused, it is best to force the output low or to half supply.

A Low Current Rail-to-Rail Architecture

The simplified schematic, Figure 3, details the circuit design approach of the LT1495/LT1496. The amplifier topology is a 3-stage design, consisting of a rail-to-rail input stage that continues to operate with the inputs above the positive rail, a folded-cascode second stage that develops most of the voltage gain, and a rail-to-rail common-emitter stage that provides the current gain.

The input stage is formed by two difference amps, Q1–Q2 and Q3–Q6. For signals with a common mode voltage between V_{EE} and (V_{CC} – 0.8V), Q1 and Q2 are active. When the input common mode exceeds (V_{CC} – 0.8V), Q7 turns on, diverting the current from difference amp Q1–Q2 to current mirror Q8–Q9. The current from Q9 biases on the other difference amp, consisting of PNPs Q5–Q6 and NPNs Q3–Q4. Though Q5–Q6 are driven from the emitters rather than the base, the basic difference amp action is the same. When the common mode voltage is between (V_{CC} – 0.8V) and V_{CC}, devices Q3 and Q4 act as followers, forming a buffer between the amplifier inputs and the emitters of the Q5–Q6. If the common mode voltage is taken above V_{CC}, Schottky diodes D1 and D2 reverse bias and devices Q3 and Q4 then act as diodes. The difference amp formed by Q5–Q6 operates normally, but the input bias current increases to the emitter current of Q5–Q6, which is typically 180nA.

The collector currents of the two input pairs are combined in the second stage consisting of Q11–Q16, which furnishes most of the voltage gain. Capacitor C1 sets the amplifier bandwidth. The output stage is configured for maximum swing by the use of common-emitter output devices Q21 and Q22. Diodes D4–D6 and current source Q15 set the output quiescent current.
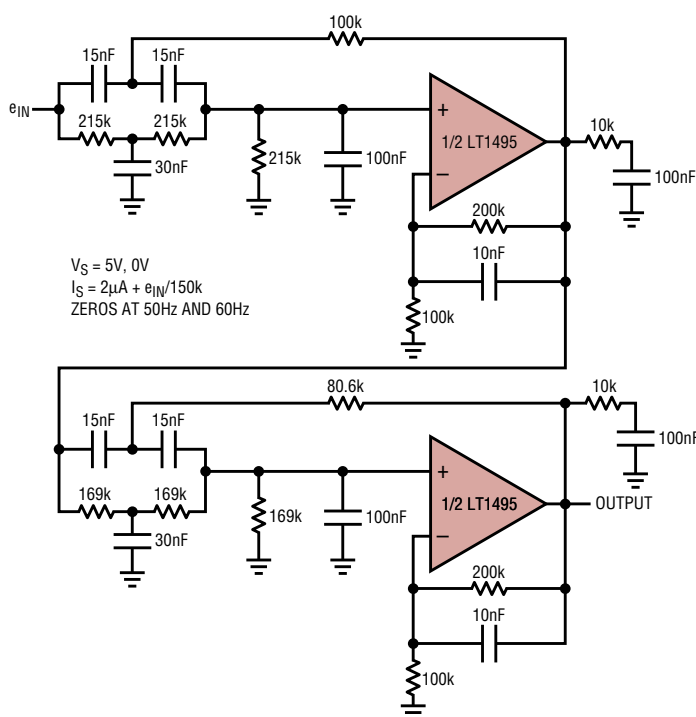
Figure 6. 6th order 10Hz elliptic lowpass filter
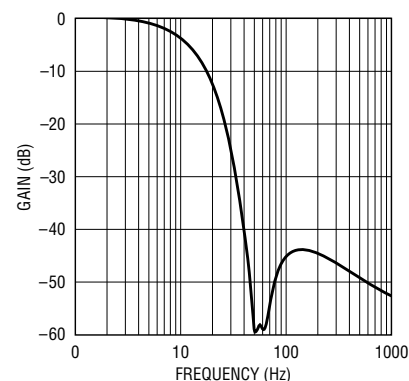
Figure 7. Frequency response of Figure 6's 6th order elliptic lowpass filter

Performance

Table 1 summarizes the performance of the LT1495/LT1496. As can be seen, operation is fully specified at 3V, 5V and ±15V. Input offset voltage drift is very low, guaranteed less than 2µV/˚C; a distribution plot is shown in Figure 4.

Applications

The ability to accommodate any input or output signal that falls within the amplifier supply range makes the LT1495/LT1496 very easy to use. The following applications highlight signal processing at low currents.

Nanoampere Meter

A simple 0nA–200nA meter operating from two flashlight cells or one lithium battery is shown in Figure 5. The readout is taken from a 0µA–200µA, 500Ω analog meter; the LT1495 supplies a current gain of 1000 in this application. The op amp is configured as a float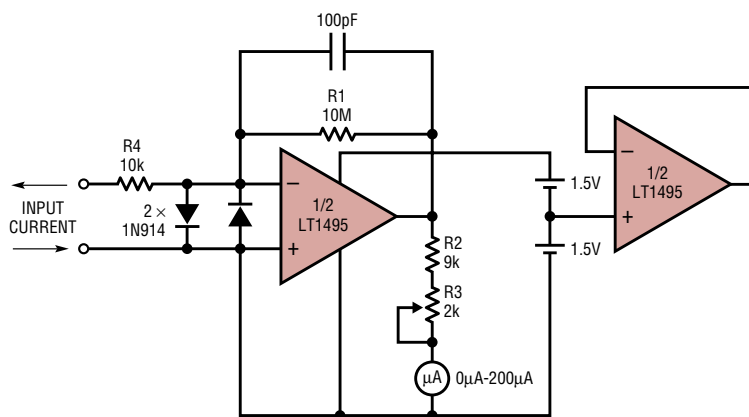ing I-to-I converter. It consumes only 3µA when not in use, so there is no need for an on/off switch. Resistors R1, R2 and R3 set the current gain. R3 provides a ±10% full-scale adjust for the meter movement. With a 3V supply, maximum current in the meter is limited by R2 + R3 to less than 300µA, protecting the movement. Diodes D1 and D2 and resistor R4 protect the inputs from faults up to 200V. Diode currents are below 1nA in normal operation, since the maximum voltage across the diodes is 375µV, the V_{OS} of the LT1495. C1 acts to stabilize the amplifier, compensating for capacitance between the inverting input and ground. The unused amplifier should be connected as shown for minimum supply current. Error terms from the amplifier (base currents, offset voltage) sum to less than 0.5% over the operating range, so the accuracy is limited by the analog meter movement.

6th Order, 10Hz Elliptic Lowpass Filter

Figure 6 shows a 6th order, 10Hz elliptic lowpass filter with zeros at 50Hz and 60Hz. Supply current is primarily determined by the DC load

on the amplifiers and is approximately $2µA + V_O/150k$ (9µA for $V_O = 1V$). The overall frequency response is shown in Figure 7. The notch depth of the zeros at 50Hz and 60Hz is nearly 60dB and the stopband attenuation is greater than 40dB out to 1kHz. As

with all RC filters, the filter characteristics are determined by the absolute values of the resistors and capacitors, so resistors should have a 1% tolerance or better and capacitors a 5% tolerance or better.

Table 1. LT1495/LT1496 key specifications: 25˚C

	$V_S = 5V, 0V$	$V_S = ±15V$	
	$V_S = 3V, 0V$		
Supply Current per Amplifier	1.5µA	2.0µA	Max
Input Offset Voltage	375µA ($V_S = 5V$)	575µV	Max
	475µV ($V_S = 3V$)		Max
Input Offset Drift	2µV/˚ C		Max
Input Noise Voltage (0.1Hz to 10Hz)	4µV$_{P-P}$	4µV$_{P-P}$	Typ
Input Bias Current	1000pA	1000pA	Max
Input Offset Current	100pA	100pA	Max
Open-Loop Gain ($R_L = 100k$)	100V/mV ($V_S = 5V$) 50V/mV ($V_S = 3V$)	100V/mV	Min Min
Common Mode Rejection Ratio			
$V_{CM} = 0V$ to 4V, $V_S = 5V$	90dB		Min
$V_{CM} = 0V$ to 10V, $V_S = 5V$	74dB		Min
$V_{CM} = –15V$ to 14V		100dB	Min
Power Supply Rejection Ratio			
$V_S = 2.2V$ to $V_S = 12V$	90dB		Min
$V_S = ±5V$ to $V_S = ±15V$		94dB	Min
Output Saturation Voltage: Low			
No Load	100mV		Max
$I_{SINK} = 100µA$	410mV		Max
$R_L = 100k$		500mV	Max
Output Saturation Voltage: High			
No Load	70mV		Max
$I_{SOURCE} = 100µA$	320mV		Max
$R_L = 100k$		380mV	Max
Short Circuit Current	700µA	700µA	Min
Slew Rate	0.4V/ms	0.4V/ms	Min
Gain-Bandwidth Product	3kHz	3kHz	Typ

The LTC1624: a Versatile, High Efficiency, SO-8 N-Channel Switching Regulator Controller

by Randy G. Flatness

Introduction

The LTC1624 is the newest member of Linear Technology's next generation of DC/DC controllers. This 8-pin controller uses the same constant frequency current mode architecture and Burst Mode operation as the LTC1435–LTC1439 controllers, but without the synchronous switch. The LTC1624, like the other members of the family, drives a cost-effective, external N-channel MOSFET for the topside switch and maintains low dropout operation previously available only with P-channel MOSFETs.

The LTC1624 can be configured to operate in all standard switching configurations, including boost, step-down, inverting and SEPIC, without a limitation on the output voltage. A wide input voltage range of 3.5V to 36V allows operation from a variety of power sources, from as few as four NiCd cells up though high voltage wall adapters. Tight load regulation, coupled with a reference voltage trimmed to 1%, provides very accurate output voltage control.

The 8-pin SO package, the need for few external components and N-channel drive make high efficiency DC/DC conversions possible in the extremely small PC board space available in today's portable electronics.

High Performance Architecture

The LTC1624 is a current mode switching regulator controller operating at an internally set frequency of 200kHz. A user selectable sense resistor (R_{SENSE}) sets the maximum
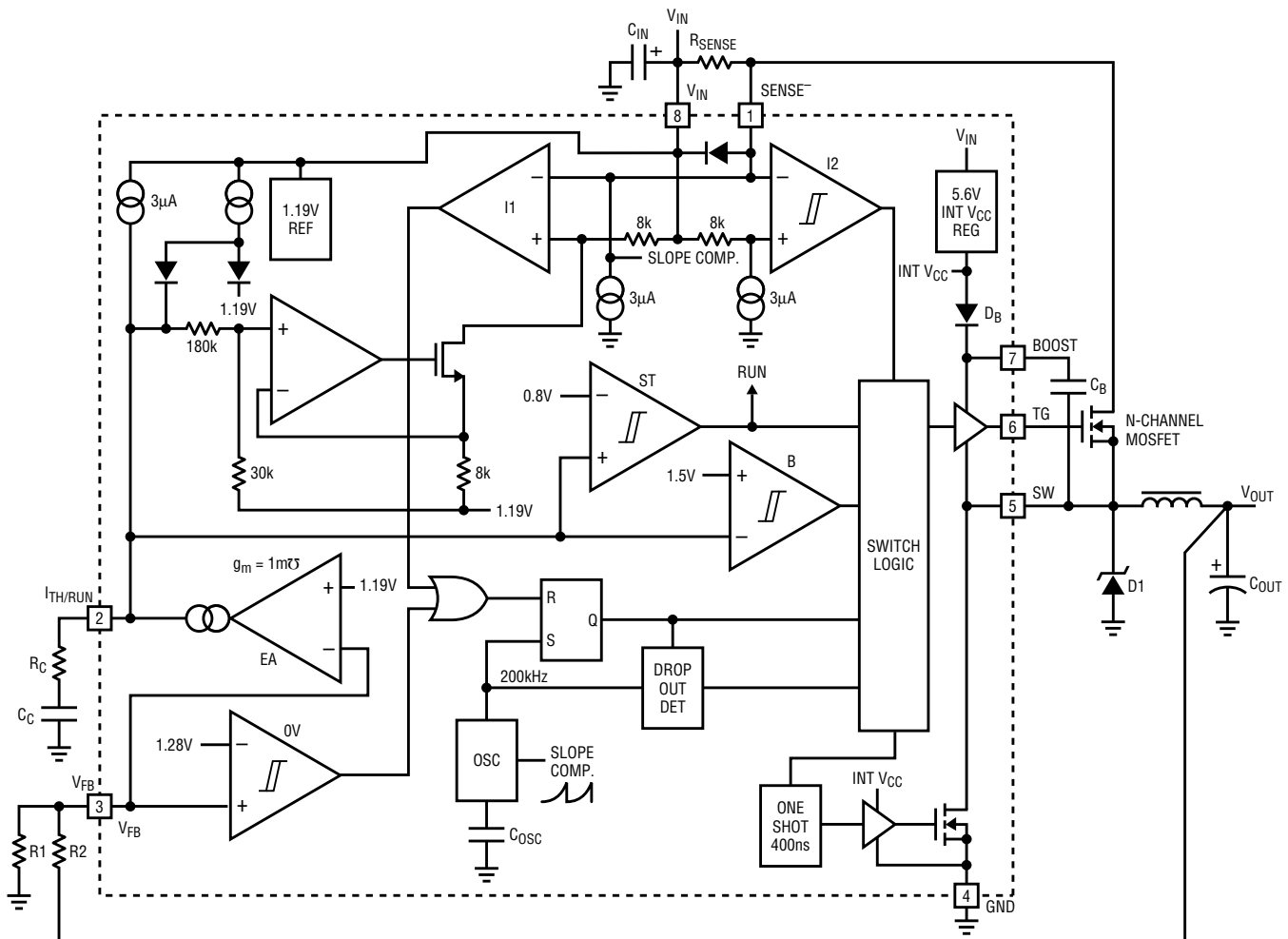
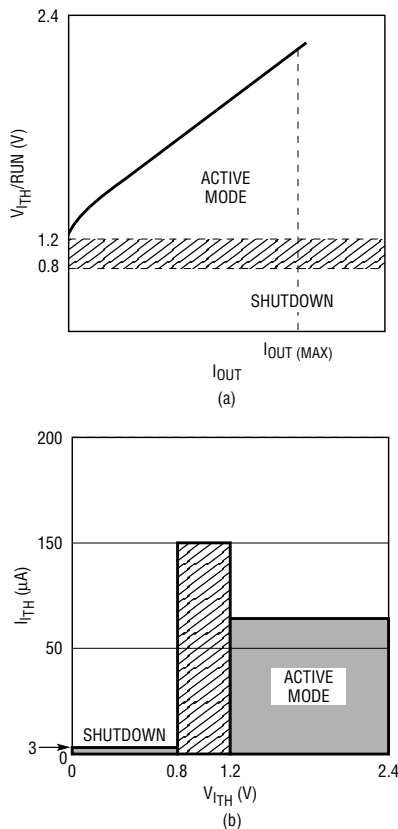

Figure 1. LTC1624 block diagram

Figure 2. I_{TH}/RUN pin characteristics

Figure 3. Driving the I_{TH}/RUN pin

current. Referencing the sense resistor to V_{IN} instead of V_{OUT} removes the limitation on maximum output voltage. (The LTC1435–LTC1439 have a maximum output voltage of 10V.) A block diagram of the LTC1624 configured as a step-down regulator is shown in Figure 1.

During normal operation, the top MOSFET is turned on during each cycle when the oscillator sets a latch, and turned off when the main current comparator resets the latch. The peak inductor current at which the current comparator resets the latch is controlled by the voltage on the I_{TH}/RUN pin, which is the output of the error amplifier. The error amplifier receives an output feedback voltage from an external resistive divider though the V_{FB} pin. When the load current increases, it causes a slight decrease in V_{FB} relative to the 1.19V reference, which in turn causes the I_{TH}/RUN voltage to increase until the average inductor current matches the new load current. After the top MOSFET is turned off, the internal bottom MOSFET is turned on during each
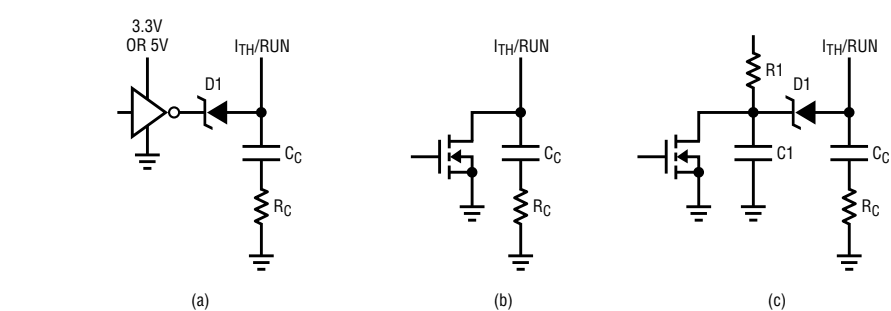
cycle for approximately 300ns–400ns to ensure that the bootstrap capacitor C_B is always recharged.

The value of R_{SENSE} is chosen based on the required output current. The LTC1624 current comparator has a maximum threshold of 160mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current (I_{MAX}) equal to the peak value less half the peak-to-peak ripple current, DI_L. For step-down applications, the value of the sense resistor is set to 100mV/$I_{OUT(MAX)}$. To prevent overcurrent during output short-circuit conditions, the operating frequency is dropped to around 30kHz to ensure the inductor's current safely decays in each cycle.

The LTC1624 includes protection against output overvoltage conditions or transients. An overvoltage comparator monitors the output voltage and forces the topside MOSFET off and keeps it off when the output voltage is greater than 7.5% of its regulated value.

Combined RUN/ Compensation/Soft-Start Pin

The I_{TH}/RUN pin is a multifunction pin, providing shutdown, control-loop compensation and optional soft-start. Internal slope compensation (required with constant frequency designs) coupled with external compensation (R_C, C_C in Figure 1) provides optimum load-step response. The peak inductor current is controlled by the voltage at the I_{TH}/RUN pin. The nominal range for the I_{TH}/RUN pin is from 1.2V to 2.4V with the load dependent characteristics shown in Figure 2a.

Pulling the I_{TH}/RUN pin below its 1.2V soft clamp voltage puts the LTC1624 into shutdown with a typical quiescent current of 15µA. Releasing the I_{TH}/RUN pin allows an internal 3µA current source to pull up the voltage on the I_{TH}/RUN pin, charging the compensation capacitor C_C. When the voltage on the I_{TH}/RUN pin reaches 0.8V, the main control loop is enabled with the I_{TH}/RUN voltage pulled up by the error amplifier, as shown in Figure 2b.

Soft-start can be implemented by increasing the voltage on the I_{TH}/RUN pin from 1.2V to its 2.4V maximum, because the internal current limit is also ramped at a proportional rate (See Figure 2). Soft-start reduces inrush surge currents from V_{IN} by gradually increasing the internal current limit. This pin can also be used to control power supply sequencing. Current limit begins at approximately 10mV/R_{SENSE} and ends at 100mv/R_{SENSE}. The circuit in Figure 3c shows how to implement soft-start. The capacitor C1 starts at 0V when V_{IN} is applied and diode D1 pulls the I_{TH}/RUN pin low. As C1 charges, the voltage on I_{TH}/RUN also increases at a proportional rate together with the current limit. If soft-start is not needed, the circuits in Figures 3a or 3b can be used. An open-drain MOSFET in Figure 3b directly pulls the I_{TH}/RUN to ground, forcing shutdown.

Loop compensation is accomplished with R_C and C_C. For step-down applications, the typical time constant created by R_C and C_C should be around 50kHz (1/4 the oscillator frequency) as a good starting point. The
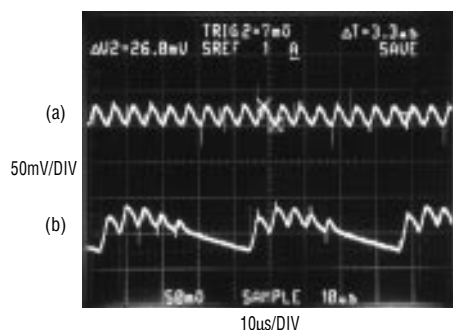
Figure 4. Output ripple: a) continuous mode;
b) Burst Mode

value of R_C should generally track R_{SENSE}. For example, for a 2A maximum output current, set R_{SENSE} = 0.05Ω, with R_C = 5.1k and C_C = 620pF. With a 4A output current, set R_{SENSE} = 0.025Ω, with R_C = 3k and C_C = 1000pF. Using these guidelines as a starting point, the final values of compensation components can be found using a load-transient step and observing the output voltage transient response.

To boost low current efficiency, the LTC1624 behaves like the LTC1435/LTC1438 during low current operation by using Burst Mode operation. When the load current falls to the point where the peak inductor current is approximately 20mV/R_{SENSE}, the topside MOSFET is held off and the output capacitor supports the load, initiating Burst Mode operation. During this phase the output voltage is decaying and the output of the error amp (I_{TH}/RUN pin) is increasing. The topside MOSFET is

not switched, saving power and boosting efficiency. When the I_{TH}/RUN pin voltage exceeds 1.5V the drive is returned to the topside MOSFET and the output voltage ramps up. Figure 4 shows the output voltage ripple for continuous mode at higher output currents (Trace A) and for Burst Mode operation at lower output currents (Trace B).

Floating MOSFET Driver

An internal 5.6V supply derived from V_{IN} provides power to drive the topside MOSFET (refer to Figure 1). The gate drive for the topside MOSFET originates from a floating driver operating from the BOOST pin to the SW pin. An external bootstrap capacitor (C_B) connected from BOOST to SW supplies the gate-drive voltage. Capacitor C_B is charged through an internal high voltage diode from the 5.6V supply when the SW pin is low. This eliminates the need for an external Schottky diode in most applications.

When the topside MOSFET is turned on, the driver places the voltage on C_B across the gate-source of the MOSFET. This enhances the MOSFET and turns on the top side switch. The switch node SW rises to V_{IN} and the BOOST pin rises to V_{IN} + 5V. A small internal N-channel MOSFET pulls the switch node (SW) to ground during each cycle after the topside MOSFET turns off ensuring the bootstrap capacitor is kept fully charged.

Figure 5. Efficiency comparison of synchronous and nonsynchronous step-down converters

Significant efficiency gains can be realized by supplying the topside driver operating voltage from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For 5V regulators this simply means connecting the BOOST pin though a small Schottky diode (like a CMDH-3) to V_{OUT}.

For operation with V_{IN} < 5V, higher gate-drive voltage and higher efficiency can be obtained by connecting a Schottky diode from V_{IN} to BOOST. This technique parallels the internal boost diode and increases the enhancement of the MOSFET. This limits the maximum input voltage to 8V so as not to exceed the maximum voltage from boost to switch of 8V.

Low Dropout

An important feature for extracting maximum energy from low voltage battery packs is low dropout. The LTC1147 (another 8-pin controller) achieves this by using a P-channel MOSFET switch that can operate at 100% duty cycle. The LTC1624 uses an N-channel MOSFET to accrue the benefits of lower $R_{DS(ON)}$ and lower cost than corresponding P-channel MOSFETs.

Driving N-channel MOSFETs requires periodic recharging of the bootstrap capacitor, C_B. This can only occur when the top MOSFET is turned off and the switch node is low (during the off-time). The ratio of maximum on-time to the clock period is defined as the duty cycle. The LTC1624 detects

Figure 6. High performance 3.3V/2A step-down DC/DC converter
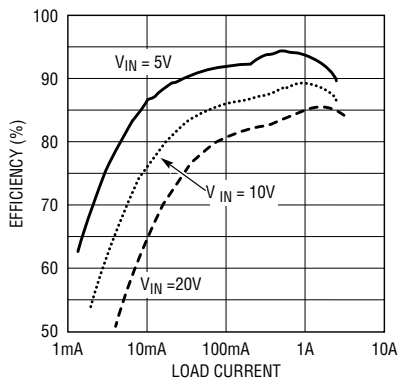
Figure 7. Efficiency plot for Figure 6's circuit

Figure 8. 12V/1A step-up converter

the number of clock cycles the top MOSFET is allowed to remain on. After two clock cycles, the topside is turned off and a minimum off-time is forced. In this mode the duty cycle is 95% and the topside is switching at $F_{OSC}/2$. This extends the maximum duty cycle from 90% to 95% and still guarantees that the bootstrap capacitor remains charged.

Giving Up the Synchronous Switch

The LTC1624 nonsynchronous N-channel controller saves switching losses (gate-charge current) of the synchronous MOSFET at the expense of increased loss due to the Schottky diode during some operating conditions. Printed circuit board area is minimized by fewer required external components and an 8-pin SO package footprint.

The LTC1624 controller shares the same loss-reducing techniques as other members of the LTC143X family. Figure 5 shows efficiency plots of two 3.3V converters, a nonsynchronous LTC1624 and a 16-pin synchronous

LTC1435 operating at V_{IN} = 10V. The same common external components and operating frequency are maintained for both circuits.

At low currents (I_{OUT} < 100mA), while in Burst Mode operation, the efficiency of the LTC1624 exceeds that of the LTC1435. This is due to saving gate-charge current by not switching the bottom synchronous MOSFET. At higher output currents, as expected, the Schottky diode loss dominates and the efficiency of the LTC1435 circuit is greater than that of the LTC1624 circuit.

At lower input voltages, when the duty cycle forces the topside MOSFET on longer, the loss due to the Schottky diode decreases and the efficiencies of the synchronous and nonsynchronous designs converge. At higher input voltages the efficiency difference in the low current region increasingly favors the nonsynchronous LTC1624, but at high currents the synchronous LTC1435 continues to win.

Minimum Externals, Maximum Versatility

The LTC1624 can be used in a wide variety of switching regulator applications, the most common being the step-down converter. Other switching regulator architectures include step-up, SEPIC and positive-to-negative converters.

The basic step-down converter is shown in Figure 6. This application shows a 3.3V/2A converter operating from an input voltage range of 4.5V to 25V. The efficiency for this circuit is shown in Figure 7.

Step-up and SEPIC applications require a low-side switch pulling the inductor to ground (see Figures 8 and 10). Since the source of the MOSFET must be grounded, the switch pin (SW) on the LTC1624 is also grounded in order for the driver to supply a gate-to-source signal to control the MOSFET. In these applications, the voltage on the boost pin is a constant 5V, resulting in a 0V–5V gate-drive

Figure 9. Efficiency plot for Figure 8's circuit

Figure 10. 12V/0.5A DC/DC converter operates from 5V–15V inputs

The LTC1514/LTC1515 Provide Low Power Step-Up/Step-Down DC/DC Conversion without Inductors

by Sam Nork

Introduction

Many applications must generate a regulated supply from an input source that may be above or below the desired regulated output voltage. Such applications place unique constraints on the DC/DC converter and, as a general rule, add complexity (and cost) to the power supply. A typical example is generating 5V from a 4-cell NiCd battery. When the batteries are fully charged, the input voltage is around 6V; when the batteries are near end of life, the input voltage may be as low as 3.6V. Maintaining a regulated 5V output for the life of the batteries typically requires an inductor-based DC/DC converter (for example, a SEPIC converter) or a complex hybrid step-up/step-down solution. The LTC1514/LTC1515 family of switched capacitor DC/DC converters handles this task with only three external capacitors (Figure 1).

A unique architecture allows the parts to accommodate a wide input voltage range (2.0V to 10V) and adjust the operating mode as needed to maintain regulation. As a result, the parts can be used with a wide variety of battery configurations and/or adapter voltages. Low power consumption (I_Q = 60µA typical) and low external parts count make the parts well suited for space-conscious low power a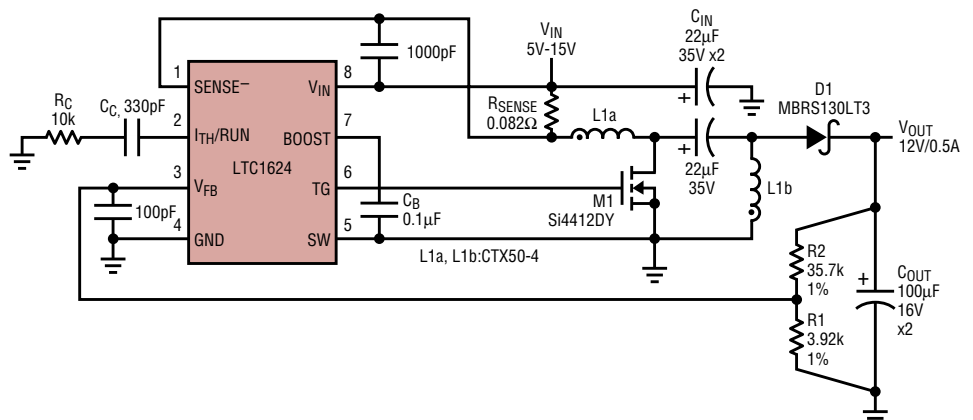pplications, such as cellular phones, PDAs and portable instruments. The parts come in adjustable and fixed output-voltage versions and include additional features such as power-on reset capability (LTC1515 family) and an uncommitted comparator that is kept alive in shutdown (LTC1514 family).

Regulator Operation

The parts combine the relatively simple architecture of a step-up voltage doubler with a gated-switch step-down regulator to create a simple-to-use step-up/step-down regulator. The trick, of course, is knowing when to step up and when to step down. The block diagram shown in Figure 3 illustrates how these parts function.

The regulator sections of both the LTC1514 and the LTC1515 consist of an oscillator, switch network (S1–S4), reference, comparator and control logic. Regulation is achieved by comparing the divided-down output voltage to the internal reference voltage. When the divided output drops below the reference voltage, the switch network is enabled to boost the output back into regulation. Hysteresis in the comparator forces the regulator to burst on and off, and causes approximately 100mV of peak-to-peak ripple to appear at the output. By enabling the regulator only when needed, the LTC1514 and LTC1515 are able to achieve high efficiencies with low output load currents.

The action of the switch network is controlled by internal circuitry that senses the voltage differential between V_{IN} and V_{OUT}. When the input voltage is lower than the output voltage, the switch network operates as a step-up voltage doubler with a free-running frequency of 650kHz (typical). When the input voltage is greater than the output, the switch network operates as a step-down gated switch. The net result is a stable, tightly regulated output supply that can tolerate widely varying input voltages and load transients.

Inrush Currents No Longer a Problem

Switched capacitor DC/DC converters are touted for their micropower operation and are generally used in light-load applications. However, despite their low power design and environment, they have two undesirable tendencies: 1) to pull very high inrush currents from the input supply during power-up; and 2) to generate high input and output current spikes
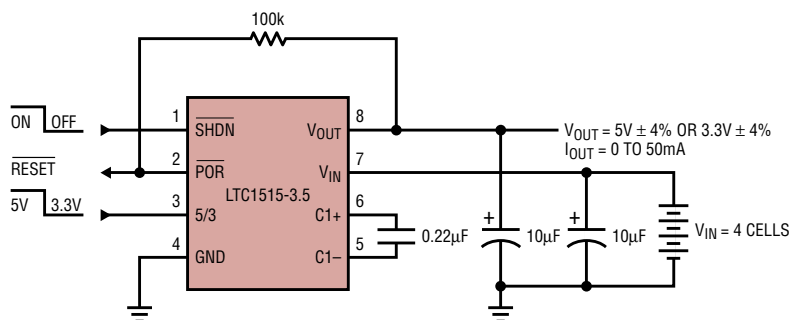
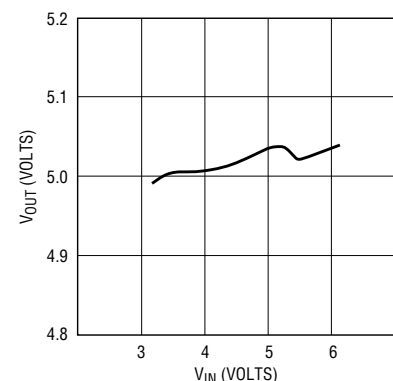**Figure 1. Programmable 5V/3.3V power supply with power-on reset**
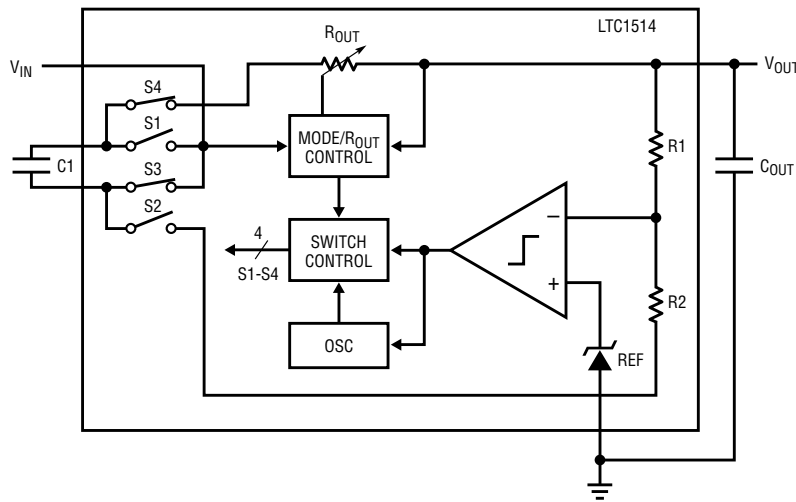
Figure 2. V_{OUT} vs V_{IN} for Figure 1's circuit
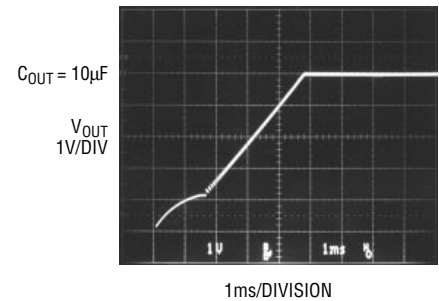
Figure 3. Simplified LTC1514/LTC1515 regulator block diagram

Figure 4. V_{OUT} during power-up

when large V_{IN} to V_{OUT} differentials are present. These traits can cause many bad things to happen. If the switched cap converter is being powered by another low power DC/DC converter, the sudden inrush current during power-up, which can easily reach several hundred milliamps, may disrupt regulation of the main power supply. High switching currents due to large V_{IN} to V_{OUT} differentials can cause excessive output ripple and/or poor regulation. As a result, most switched cap voltage converters have rather limited allowable V_{IN} to V_{OUT} differentials. These problems are addressed by the LTC1514/LTC1515.

Internal soft-start circuitry controls the rate at which V_{OUT} can be charged from 0V to its final regulated value (see scope photo, Figure 4). V_{OUT} typically changes from 0V to its final regulated value in a little under 5ms. This corresponds to an effective V_{OUT} charging current of only 12.5mA for a 10µF output capacitor (27.5mA for 22µF, and so forth). This method of controlling the average start-up current prevents any nasty disruptions on the input supply both during initial power-up and when coming out of shutdown.

Current spikes due to normal operation are mitigated by controlling the effective output impedance of the regulator. As the V_{IN} (or boosted V_{IN}) to V_{OUT} voltage differential grows, the effective output impedance (R_{OUT}) of the charge pump is automatically increased by internal voltage sensing

circuitry. This feature minimizes the current spike pulled from V_{IN} each time the switch network is enabled and helps to reduce output ripple over a wider V_{IN} range.

Additional Features

The LTC1515 family contains a power-on reset (POR) function. The $\overline{POR}$ pin is an open-drain output that pulls low when the output voltage is out of regulation. This feature can be used to prevent external circuitry from operating under invalid supply conditions. When V_{OUT} rises to within 6.5% of regulation, an internal timer is started, which releases $\overline{POR}$ (allows the pin to be pulled high) after 200ms (typical). In shutdown, the $\overline{POR}$ output is pulled low. In normal operation, an external pull-up resistor is used between the $\overline{POR}$ pin and V_{OUT}, as shown in Figure 1.

The LTC1514 contains an internal low-battery comparator and a reference that are kept active in shutdown. The comparator-trip voltage is easily programmed via an external resistor divider and has about 1% hysteresis for stability. Since the low-battery comparator is kept alive in shutdown, it may be used to protect batteries against deep discharge by shutting down the power supply when the battery voltage gets too low. It may also be used to implement a battery backup supply if the main supply fails. The open-drain comparator output allows for flexible interfacing between the LBO output and external logic.

The LTC1514/LTC1515 family also comes equipped with thermal shutdown and can survive an indefinite short circuit to ground. The short-
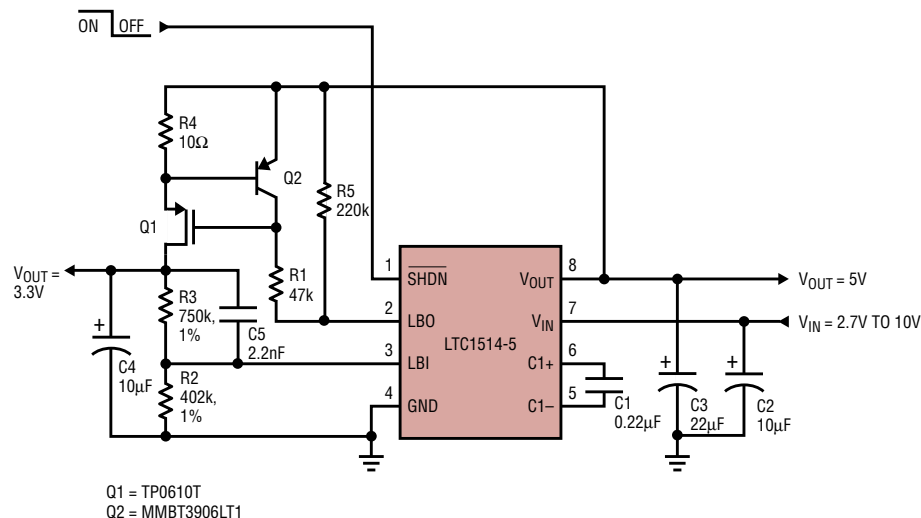

Q1 = TP0610T
Q2 = MMBT3906LT1

Figure 5. Using the low-battery comparator as a feedback comparator to produce an auxiliary 3.3V regulated output from the V_{OUT} of the LTC1514-5

RS485 Transceivers Operate at 10Mbps over Four Hundred Feet of Unshielded Twisted Pair

by Victor Fleury

Introduction

The LTC1685/LTC1686/LTC1687 family of RS485 transceivers can operate at data rates of >40Mbps over one hundred feet of category 5 unshielded twisted pair. These RS485 transceivers employ a unique architecture that guarantees excellent performance over process and temperature variations, with propagation delays for both the receiver and the driver of 18.5ns ±3.5ns. The receiver employs a fail-safe feature, over the entire 12V to –7V common mode range, whereby the receiver output remains in a HIGH state when the inputs are left open or shorted together. A novel short-circuit protection technique permits indefinite shorts (to either driver or receiver output) to power or ground while sourcing/sinking a maximum of 50mA.

Circuit Description

The timing performance of short channel CMOS circuitry can typically change significantly over fabrication and temperature variations. This is due in part to the large percentage variation in MOS channel length and to second-order transistor gain and threshold effects. For example, the propagation delay of other transceivers can vary by as much as 600% over process and temperature. In applications where high speed clock and data waveforms are sent over long distances, propagation delay and skew uncertainties can pose system design constraints and limit the maximum data rate. The LTC1685/LTC1686/LTC1687 line of high speed RS485 transceivers addresses this problem by guaranteeing the propagation to be 18.5ns ±3.5ns. The propagation delays change by ±20%, a better than tenfold improvement over other CMOS transceivers/receivers. Figure 1 shows a block diagram of the receiver used in the LTC1685/LTC1686/LTC1687 transceivers. Figure 2 shows a block diagram of the driver used in the transceivers. Note that the receiver and driver are both trimmed in order to guarantee the tight timing requirements. This is important because it minimizes the rise/fall skew of the receiver and the skew between the two driver outputs. The input resistor network is set up to allow the common mode to go as high as 12V and as low as –7V with a 5V power supply.

Predictable Propagation Delay and Low Skew

The inherent temperature and process tolerance make it possible to guarantee a ±3.5ns propagation-delay window. Temperature stability is accomplished by distributing the delay along the signal chain so that half of the delay increases with temperature and the other half decreases with temperature, independent of the amount of delay trimming. These circuits employ a novel current source whose current increases with temperature. Delay trimming takes out some of the effect of process variations. Note that both the receiver and driver also keep the input signal in differential form as far down the signal chain as possible. The differential architecture allows for very tight receiver and driver output skew.

High Data Rates over Unshielded Twisted Pair

The LTC1685/LTC1686/LTC1687 transceivers can have throughputs surpassing 40Mbps over one hundred feet of unshielded twisted pair (UTP).The tight propagation delay along with the low skew make these devices well suited for high speed
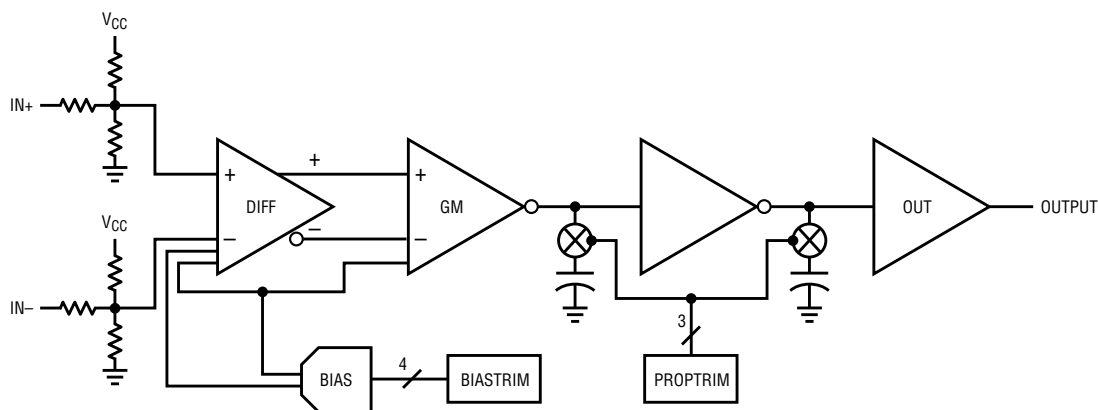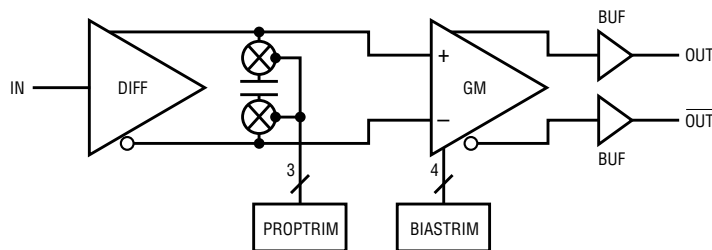

Figure 1. Receiver-section block diagram

Figure 2. Driver-section block diagram

Table 1. Performance characteristics of Belden 1588A 2-pair category 5 UTP

Average Impedance		100Ω ±15%
Maximum DC Resistance at 20°C		2.86Ω/100'
Maximum Attenuation	1MHz	0.61dB/100'
	10MHz	1.97dB/100'
	100MHz	6.67dB/100'

transmission over twisted-pair lines. Category 5 unshielded twisted pair cable can be used to transmit high data rates over long distances. The EIA/TIA568A standard specifies a minimum performance for category 5 cable. The cable used in the following experiments was Belden 1588A 2-pair category 5 UTP. Table 1 shows some of the performance characteristics of the cable.

The DC resistance of the cable will divide down the signal at all frequencies. The longer the cable, the higher the resistance and the larger the voltage division. The AC attenuation of the cable will further divide down the signal, with the highest frequency signal components, of course, being attenuated the most. Note that the cable impedance can vary by ±15%. Tweaking the termination of each individual cable with its actual impedance will yield best results; however, this might not be practical.

Experiments

We set up the LTC1685 transceiver to operate at different speeds at different cable distances. Note that the cable had two distinct twisted-pair sets. Only one of the two pairs was driven; the other pair was kept in high impedance or "listen" mode, when all stations connected to that particular pair are in receive mode. Even under these circumstances (one pair being driven, while the adjacent pair is in high impedance mode), the receivers connected to the high impedance cable maintain a HIGH output state without glitching.

The timing of the receivers works best if they are being driven by a 50% duty cycle square wave. This tends to keep a constant average voltage bias on the cable and on the internal nodes of the devices. A more stringent test, however, is to try to pass a single pulse at the highest data rate, thus not allowing the system to reach steady state. Figure 3 shows the test setup, with four LTC1685 transceivers: the LTC1685 on the top left is the only transceiver with the driver enabled; the other three transceivers
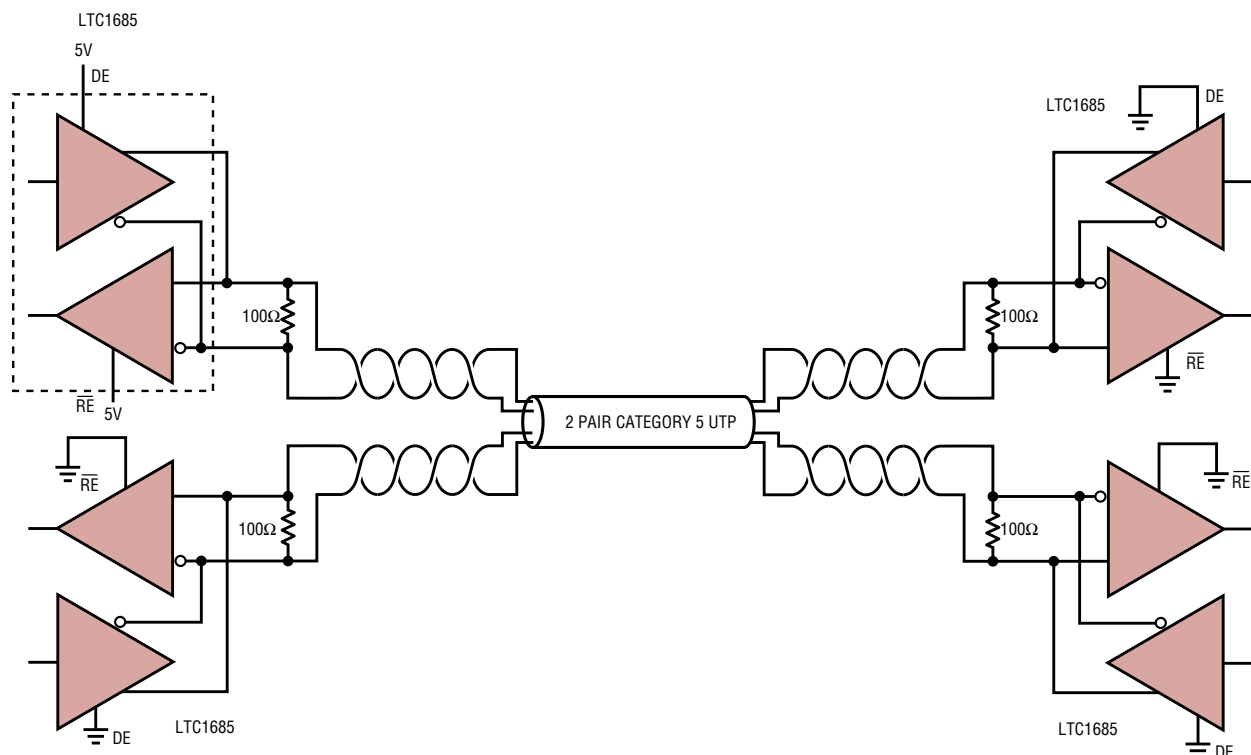

Figure 3. Test configuration

are set to receive mode only. All of the following traces are actual scope photographs.

One Hundred Feet, 40Mbps

Figure 4 shows a 25ns pulse transmitted over one hundred feet of two-pair, category 5 twisted-pair cable. The top trace is the input to the driver at the left end of the cable. The second trace is the driver output and the third trace is the receiver input, which shows the attenuation of the pulse at the end of one hundred feet of cable. Figure 5 shows the same configuration, but with a 40Mbps square wave as the input to the driver.

Four Hundred Feet, 10Mbps

Figure 6 shows a 100ns pulse (10Mbps) propagated over four hundred feet of category 5 UTP. The pulse width at the far end of the cable is slightly narrower than the pulse width at the driver output. Note the sharp edges on the receiver output, in spite of the heavily filtered inputs due to cable losses.

Four Thousand Feet, 1Mbps

Figure 7 shows a 1µs pulse propagated over four thousand feet of category 5 UTP. The top trace is the driver input. The 2nd trace is the output of an LTC1685 receiver, placed only one hundred feet away from the driver (not shown in diagram in Figure 3). The third trace is the differential input to the transceiver at the end of the four thousand feet of UTP.

Notice the effect of the parasitic DC resistance of the cable. The third trace waveform in this oscilloscope photograph was drawn at 1V/Div. This means that the four thousand feet UTP parasitic resistance has divided our signal by a factor of two (compare with the third trace of Figure 6, which is drawn at 2V/Div). Figure 8 shows a 1Mbps square wave propagated down the same four thousand feet of UTP.

Figure 4. 25ns pulse, 100 feet category 5 UTP

Figure 5. 40Mbps, 100 feet category 5 UTP
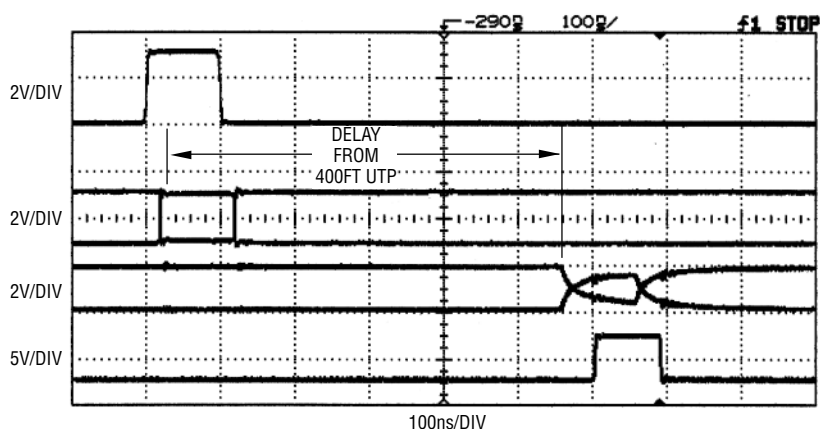
Figure 6. 100ns pulse, 400 feet category 5 UTP

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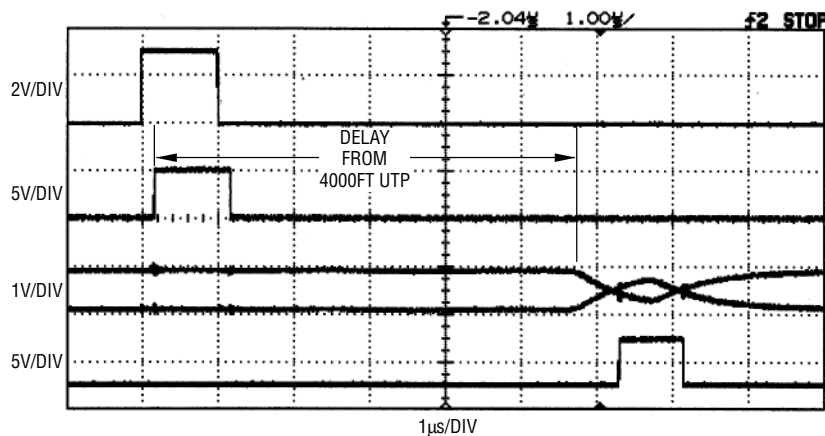
Figure 7. 1μs pulse, 4000 feet category 5 UTP
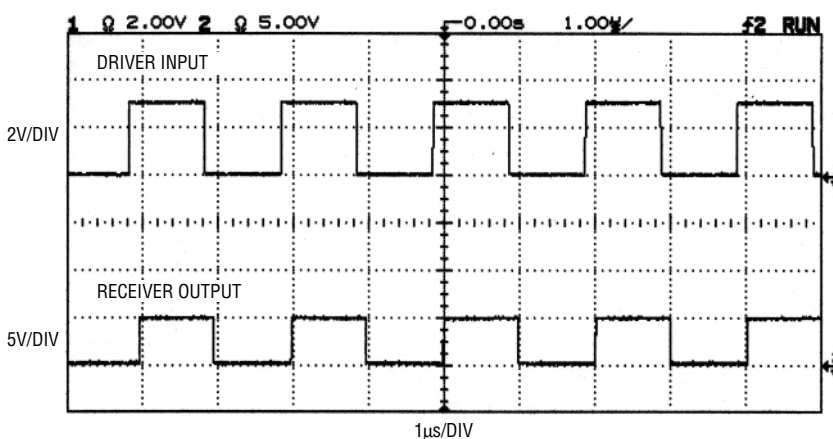
Figure 8. 1Mbps, 4000 feet category 5 UTP

Undriven Cable Pair

The cable used had two twisted-pair sets. One pair was driven, while the other pair was terminated at both ends but remained in high impedance. The undriven pair was tied to the inputs of an LTC1685 receiver. The two inputs of the LTC1685 thus appeared "shorted" together through the terminated cable. This in turn activated the fail-safe feature of the receiver and the receiver output remained high during all tests, despite the fact that the adjacent cable was switching at high frequencies (short distance) and low frequencies (long distance).

Other Features of the LTC1685 Family

❏ Novel short circuit protection: max 50mA without oscillating in and out of short-circuit mode, and automatically resetting when short is removed
❏ Receiver output will go high when receiver inputs are either floating or shorted
❏ Three-state outputs
❏ High input resistance (>22K) allows many devices on one line

Applications

These devices can be used for high speed transmission over twisted-pair cables. The RS485 common mode range allows flexibility in connecting systems with a ground potential difference or with power supply differences. They can be used in hubs, routers, bridges, repeaters, factory-floor controls and other applications.

Conclusion

The LTC1685/LTC1686/LTC1687 transceivers can work over a wide range of speed and over a wide range of cable distances. The novel architecture maintains a very tight propagation delay window for both the receiver and the driver. The precise timing, ruggedness and fail-safe features make it easy to use in wide variety of applications. *LT*

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Hot Swapping the PCI Bus

by James Herr, Paul Marshik
and Robert Reay

The Peripheral Component Interconnect (PCI) bus has become widely used in high volume personal computers and single-board computer designs. With a 32-bit data path and a bandwidth of up to 133MB/s, PCI offers the throughput demanded by the latest I/O and storage peripherals. Unfortunately, the original PCI specification does not require the bus to be hot swappable, so the system power must be turned off when a peripheral is inserted into or removed from a PCI slot.

With the migration of the PCI bus into servers, industrial computers and computer-telephony systems, the ability to plug a peripheral into a live PCI slot becomes mandatory. By using the LTC1421 to control the power supplies, and QuickSwitch® QS3384s to buffer the data bus, a peripheral can be inserted into a PCI slot without turning off the system power.

Inrush Current and Data Bus Problems

The problems with plugging a standard peripheral into a fully powered PCI slot are shown in Figure 1. When the peripheral is inserted, the supply bypass capacitors on the peripheral can draw huge transient currents from the PCI power bus as they charge. The

transient currents can cause permanent damage to the connector pins and board traces, and can cause glitches on the system supply that force other peripherals in the system to reset.

The second problem involves the diodes to V_{CC} at the inputs or outputs of most logic families. With the peripheral initially unpowered, the V_{CC} input to the logic gate is at ground potential. When the data bus pins make contact, the bus lines are clamped to ground through the diodes to V_{CC} and the data is corrupted. With current flowing into the V_{CC} diode, the logic gate may latch-up and destroy itself when power is applied.

Hot-Swappable PCI Slot Using the LTC1421

The circuitry for a hot-swappable PCI slot on the motherboard or backplane is shown in Figure 2. The power supplies for each PCI slot are controlled by an LTC1421 and four external FETs and the data bus is buffered by several QS3384 QuickSwitches or equivalent. A PCI power control ASIC, FPGA, microprocessor or the like controls all of the slots within the system.

The 12V, 5V, 3.3V and –12V supplies are controlled by placing external N-channel pass transistors, Q1–Q4,

in the power path. By ramping the gate of the pass transistors at a controlled rate, the transient surge current ($I = C \times dV/dt$) drawn from the PCI supplies can be limited to a safe value. The ramp rate for the positive supplies is set by $dV/dt = 20\mu A/C2$. The –12V supply ramp rate is set by R7 and C3; resistor R5 and transistor Q5 help transistor Q2 turn off quickly. Resistors R9, R10 and R11 prevent potential high frequency FET oscillations. Resistors R13 and R14 pull up PWRGD and $\overline{FAULT}$ to the proper logic level.

Sense resistors R1, R2 and R3 provide current-fault protection. When the voltage across R1 or R2 is greater than 50mV for more than 10ms, the LTC1421 circuit breaker is tripped. All of the FETs are immediately turned off and the $\overline{FAULT}$ pin is pulled low. The circuit breaker is reset by cycling the $\overline{POR}$ pin. The current-fault protection for the 3.3V supply is provided by resistive divider R6 and R8 and the uncommitted comparator in the LTC1421. Because the current levels on the –12V supply are so low, over-current protection is not necessary.

The QuickSwitch contains a low resistance N-channel FET placed in series with the data bus. The switch is turned off when the board is inserted and then enabled after the power is stable. The switch inputs and outputs do not have a parasitic diode back to V_{CC} and have very low capacitance.

System Timing

The system timing is shown in Figure 3. The PCI power controller senses when a board has been inserted into the PCI via the power-select bits. Alternatively, the user can inform the controller that a board has been
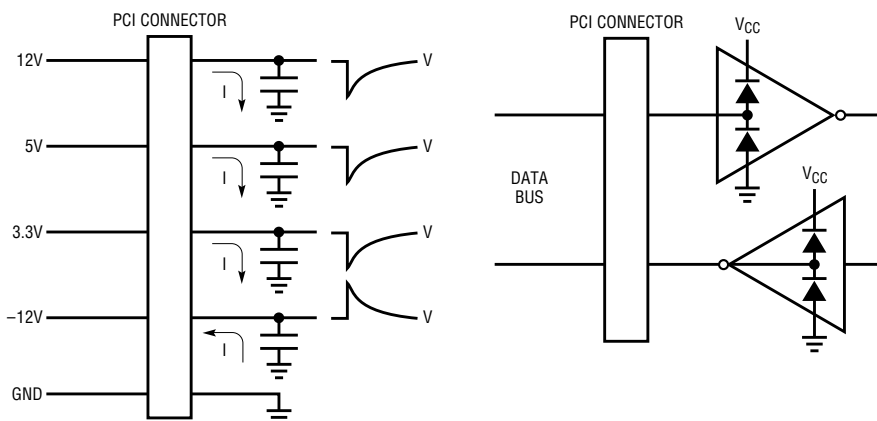
Figure 1. Problems with plugging a standard peripheral into a fully powered PCI slot
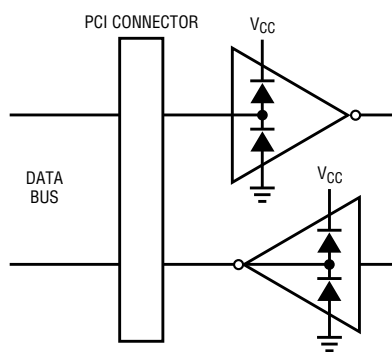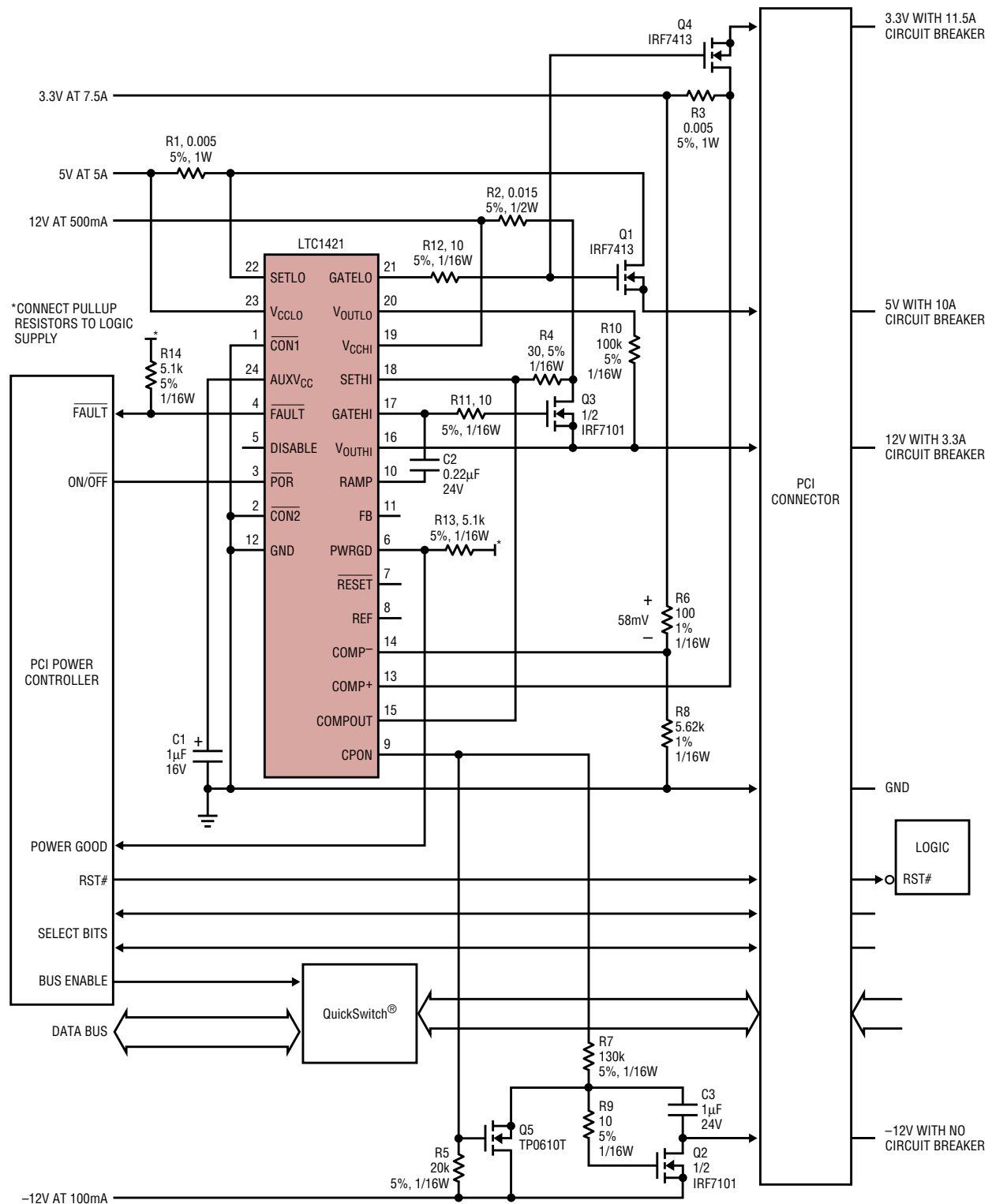
Figure 2. Hot-swappable PCI slot

inserted via the front panel or keyboard. The PCI controller holds the RST# pin low and disables the QuickSwitches, then turns on the LTC1421 via the $\overline{POR}$ pin. The power supplies turn on at a controlled rate and when the 12V supply is within 10% of its final value, the PWRGD signal pulls high. The PCI power controller waits one reset time-out period, then pulls RST# high and enables the QuickSwitches.

When the board is turned off, RST# is pulled low, the QuickSwitches are disabled and the LTC1421 turned off by pulling the $\overline{POR}$ pin low. After a 20ms delay, the external FETs are turned off and the supply voltages collapse.

Conclusion

Using the LTC1421 and a Quick-Switch, a PCI slot can be made hot swappable so the system power can remain on when a peripheral is inserted or removed. Up to now, the design of the Hot Swap circuitry has required the talents of an analog guru, but with the LTC1421, safe hot-swapping becomes as easy as hooking up an IC, a couple of power FETs and a handful of resistors and capacitors. ⊿⊺

> **Authors can be contacted
> at (408) 432-1900**
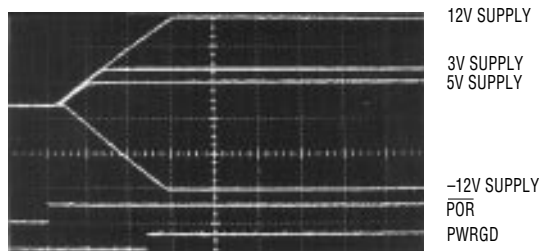
Figure 3a. System timing: power up
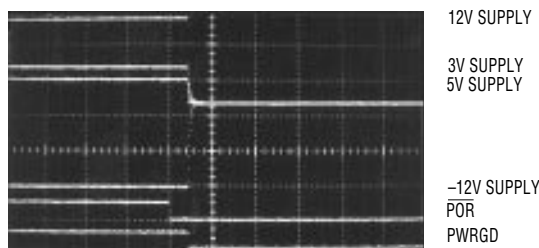
Figure 3b. System timing: power down
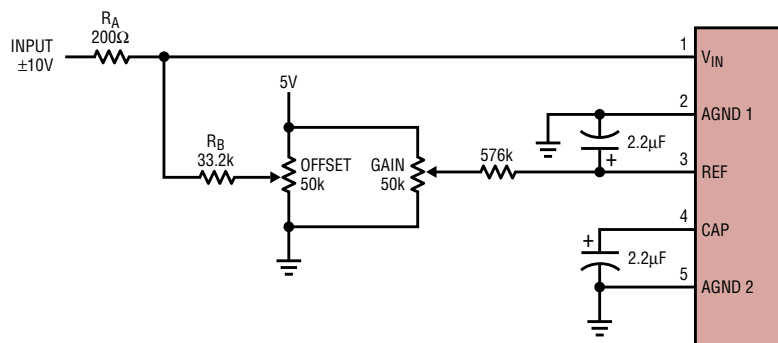
Figure 9a. Gain and offset errors can be reduced to zero by adding trimming resistors.
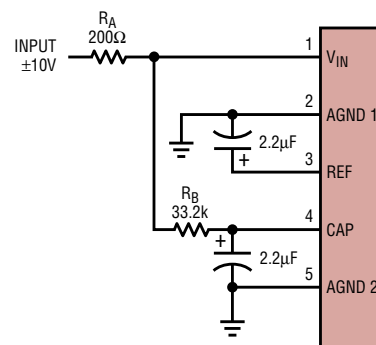
Figure 9b. If the specified gain and offset errors are adequate, connect the external resistors as shown.

Conclusion

The LTC1605 is a complete 16-bit ADC with a built-in sample-and-hold and reference. Its wide analog input range and DC accuracy make it a good candidate for industrial process-control applications. The LTC1605 is the first of many new 16-bit ADCs that will be introduced as Linear Technology continues to broaden its data acquisition product line. Having a selection of ADCs with 8, 10, 12, 14 and now 16-bits of resolution will make it easier for users to find the right ADC from Linear Technology for their applications. ⊿⊺

Time to Upgrade?

The new, low cost LTC1419 is the ideal converter to upgrade new 12-bit, high performance designs to 14 bits. Its exceptional dynamic performance gives a 10dB improvement in dynamic range compared to a the best 12-bit devices. Its low power and flexibility make it useful in a variety of time- and frequency-domain applications. This and the LTC1419's low cost and ultrasmall size make it the ideal candidate for designers who need the next step in ADC performance. ⊿⊺

Battery-Current Monitor with "Over-the-Top" Operation

The bidirectional current sensor shown in Figure 8 takes advantage of the extended common mode range of the LT1495 to sense currents into and out of a 12V battery while operating from a 5V supply. During the charge cycle, op amp A1 controls the current in Q1 so that the voltage drop across R_A is equal to $I_L \times R_{SENSE}$. This voltage is then amplified at the charge output by the ratio of R_A to R_B. During this cycle, amplifier A2 sees a negative offset, which keeps Q2 off and the discharge output low. During the discharge cycle, A2 and Q2 are active and operation is similar to that during the charge cycle.

$$V_O = I_L \left(\frac{R_B}{R_A} \right) R_{SENSE}$$

FOR $R_A = 1k$
$R_B = 10k$

$$\frac{V_O}{I_L} = \frac{1V}{A}$$
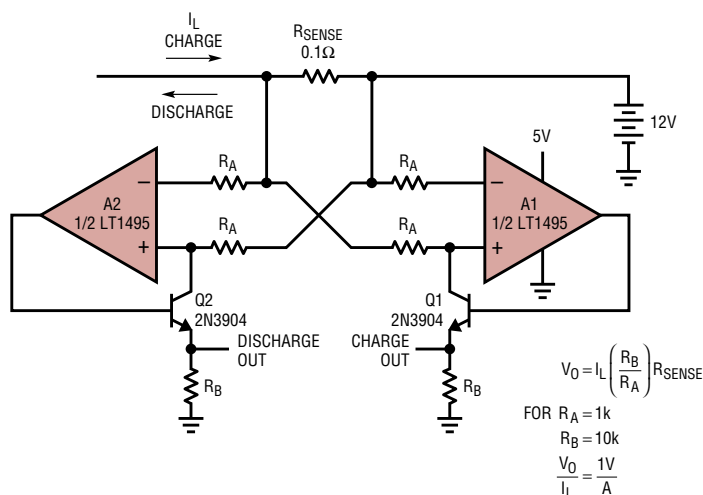
Figure 8. Battery-current monitor

Conclusions

The LT1495/LT1496 extends Linear Technology's range of rail-to-rail amplifier solutions to a truly micropower level. The combination of extremely low current and precision specifications provides designers with a versatile solution for battery-operated devices and other low power systems. ⨳

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level. A capacitor from boost to switch is still required, because this capacitor supplies the gate-charge currents.

The basic step-up converter is shown in Figure 8. The LTC1624 is used to create 12V/1A from a 5V source with the efficiency shown in Figure 9. Efficiency is above 90% from 20mA up to close to full load, dropping only to 89% at 1A.

In order to allow input voltages both above and below the output voltage, a SEPIC converter can be used. An example of the LTC1624 used as a 12V/0.5A SEPIC converter operating from an input range of 5V to 20V is shown in Figure 10.

Conclusion

The LTC1624 is the latest member of Linear Technology's family of constant-frequency, N-channel, high efficiency controllers. With only 8 pins, an internal boost diode and the ability to operate in multiple topologies, it can be used to implement a wide variety of different applications in a very small amount of space. The high performance of this controller, with its wide input range, 1% reference and tight load regulation, makes it ideal for next generation designs. ⨳

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circuit protection not only prevents the part from blowing up, but also limits the current pulled from the input supply during a fault condition. When V_{OUT} is held below 100mV by a short on the output, a 15mA current limit in the regulator output kicks in until the short goes away.

Dual Output Supply from a 2.7V to 10V Input

The circuit shown in Figure 5 uses the low-battery comparator as a feedback comparator to produce an auxiliary 3.3V regulated output from the V_{OUT} of the LTC1514-5. A feedback voltage divider formed by R2 and R3 connected to the comparator input (LBI) establishes the output voltage. The output of the comparator (LBO) enables the current source formed by Q1, Q2, R1 and R4. When the LBO pin is low, Q1 is turned on, allowing current to charge output capacitor C4. Local feedback formed by R4, Q1 and Q2 creates a constant current source from the 5V output to C4. Peak charging current is set by R4 and the V_{BE} of Q2, which also provides current limiting in the case of an output short to ground. R5 pulls the gate of Q1 high when the auxiliary output is in regulation. C5 is used to reduce output ripple. The combined output current from the 5V and 3.3V supplies is limited to 50mA. Since the regulator implements a hysteretic feedback loop in place of the traditional linear feedback loop, no compensation is needed for loop stability. Furthermore, the high gain of the comparator provides excellent load regulation and transient response.

Conclusion

With low operating current, low external parts count and robust protection features, the LTC1514 and LTC1515 are well-suited to low power step-up/step-down DC/DC conversion. The shutdown, POR and low-battery detect features provide additional value and functionality. The simplicity and versatility of these parts make them ideal for low power DC/DC conversion applications. ⨳

–48V to 5V DC/DC Converter Operates from the Telephone Line

by Gary Shockey

DC/DC converters for use inside the telephone handset require operation from the high source-impedance phone line. Additionally, the CCITT specifications call for on-hook power consumption of 25mW maximum. The DC/DC converter circuit presented here is 70% efficient at an input power of 25mW, providing 5V at 3.4mA. Controlled, low peak switch current ensures that the –48V input line does not experience excessive voltage drops during switching.

The circuit shown in Figure 1 operates as a flyback regulator with an auxiliary winding to provide power for the LT1316. To understand the operation of this circuit, examine Figure 1. When power is first applied, the LBI pin is low, causing the $\overline{SHDN}$ pin to be grounded through LBO. This places the part in shutdown mode and only the low-battery comparator remains active. During this state, V_{IN} rises at a rate determined by R1 and C1. The LT1316 draws only 6μA in shutdown mode; R1 needs to supply only this current, the current through R2 and R4, and C1's charging current. When LBI reaches 1.17V ($V_{IN} \approx 3.7V$) the LBO pin lets go of $\overline{SHDN}$ and the part enters the active mode. Once this state is reached, switching action begins and the output voltage begins to increase. As the device switches, the LT1316 V_{IN} pin draws current out of C1; V_{IN} then

T1 = DALE LPE-4841-A313, L PRI = 2mH
Q1 = ZETEX ZVN 4424A
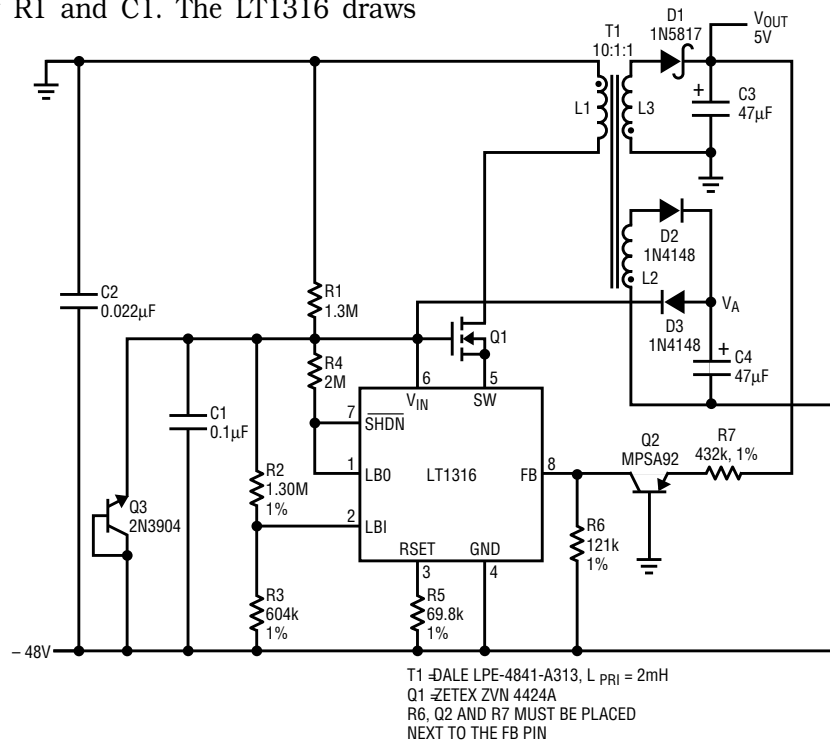R6, Q2 AND R7 MUST BE PLACED NEXT TO THE FB PIN
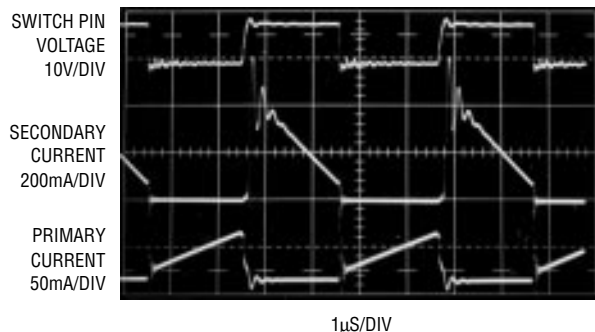
Figure 1. –48V to 5V flyback converter

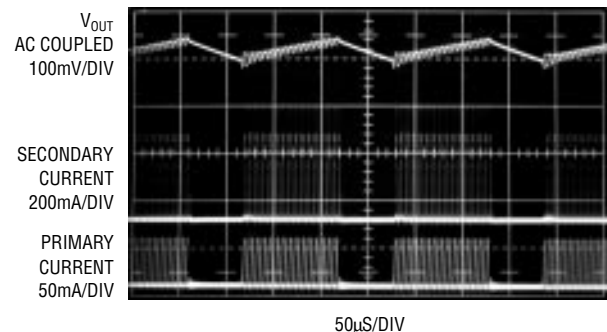**Figure 2. Switch voltage and current waveforms**

Figure 3. Output ripple voltage and current waveforms

Water Tank Pressure Sensing, a Fluid Solution

by Richard Markell

Introduction

Liquid sensors require a media compatible, solid state pressure sensor. The pressure range of the sensor is dependent on the height of the column or tank of fluid that must be sensed. This article describes the use of the E G & G IC Sensors Model 90 stainless steel diaphragm, 0 to 15psig sensor used to sense water height in a tank or column.

Because large chemical or water tanks are typically located outside in "tank farms," it is insufficient to provide only an analog interface to a digitization system for level sensing. This is because the very long wires required to interconnect the system cause IR drops, noise and other corruption of the analog signal. The solution to this problem is to implement a system that converts the analog to digital signals at the sensor. In this application, we implement a "liquid height to frequency converter."

Circuit Description

Figure 1 shows the analog front-end of the system, which includes the LT1121 linear regulator for powering the system. The LT1121 is a micropower, low dropout linear regulator with shutdown. For micropower applications of this or other circuits, the ability to shut down the entire system via a single power supply pin allows the system to operate only when taking data (perhaps every hour), conserving power and improving battery life.

In Figure 1, U3, the LT1121, converts 12V to 9V to power the system. The 12V may be obtained from a wall cube or batteries.

The LT1034, a 1.2V reference, is used with U1D, 1/4 of an LT1079 quad low power op amp, to provide a 1.5mA current source to the pressure sensor. The reference voltage is also divided down by R5, R8, R4 and the 10k potentiometer and used to offset the output amplifier, U2A, so that the signals are not too close to the supply rails.

Op amps U1A and U1B (each 1/4 of an LT1079) amplify the bridge pressure sensor's output and provide a differential signal to U2A (an LT1490). Note that U2A must be a rail-to-rail op amp. The system's analog output is taken from U2A's output.

Figure 3 plots the output voltage for the sensor system's analog front end versus the height of the water column that impinges on the pressure transducer. Note that the pressure change is independent of diameter of the water column, so that a tank of liquid would produce the same resulting output voltage. Figure 4 is a photograph of our test setup.

The remainder of the circuitry, shown in Figure 2, allows transmission of analog data over long distances. The circuit was designed by Jim Williams. The circuit takes a DC input from 0V to 5V and converts it to a frequency. For the pressure circuit in Figure 1, this translates to approximately 0Hz to 5kHz.

The voltage-to-frequency converter shown in Figure 2 has very low power consumption (26µA), 0.02 % linearity, 60ppm/°C drift and 40ppm/V power supply rejection.

In operation, C1 switches a charge pump, comprising Q5, Q6 and the 100pF capacitor, to maintain its negative input at 0V. The LT1004s and

Figure 1. Pressure-sensor amplifier
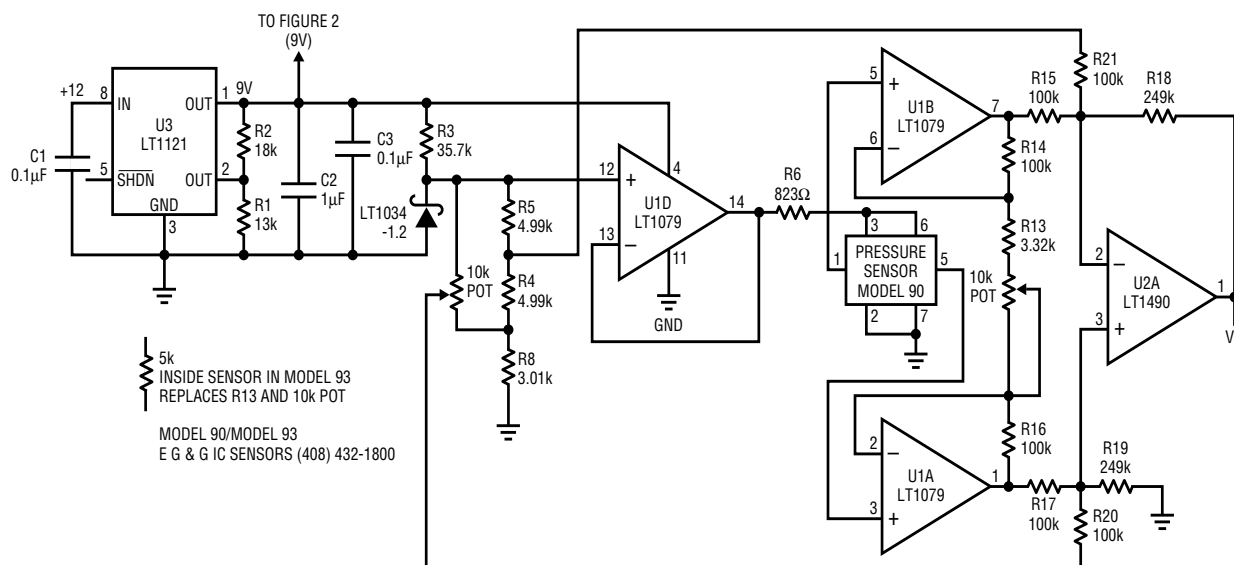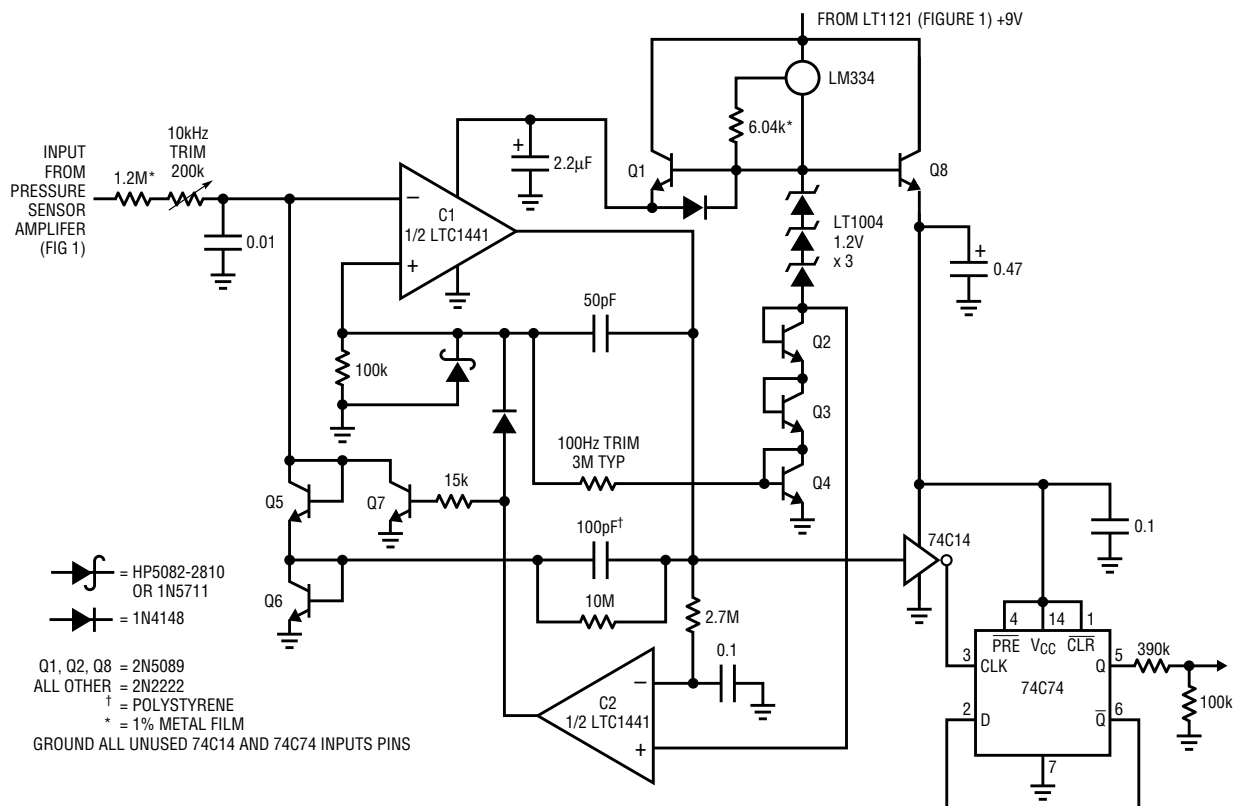
Figure 2. This 0.02% V/F converter requires only 26μA supply current.

associated components form a temperature-compensated reference for the charge pump. The 100pF capacitor charges to a fixed voltage; hence, the repetition rate is the circuit's only degree of freedom to maintain feedback. Comparator C1 pumps uniform packets of charge to its negative input at a repetition rate precisely proportional to the input-voltage-derived current. This action ensures that circuit output frequency is determined strictly and solely by the input voltage.

Figure 5 shows the output frequency versus column height for two

different Model 90 transducers. Note the straight lines, which are representative of excellent linearity.

Conclusion

A cost effective system is shown here consisting of a fluid pressure sensor, IC Sensors Model 90. This sensor's output is fed to signal processing electronics that convert the low level DC output of the bridge-based pressure sensor to a frequency in the audio range depending on the height of the fluid column impinging on the pressure transducer. *LT*

Figure 3. Output voltage vs column height
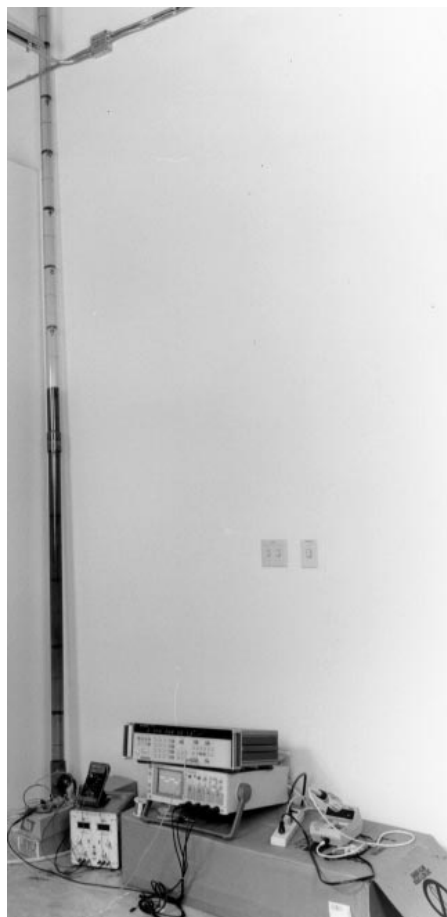
Figure 4. Test setup for water-column sensor
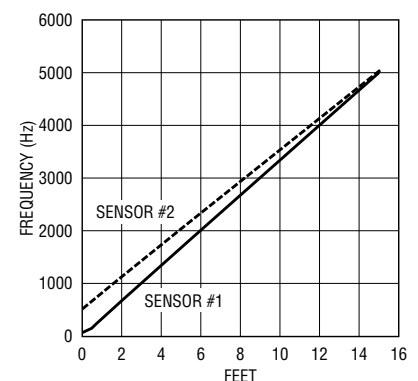
Figure 5. Output frequency vs column height for two Model 90 sensors

0.05µV/°C Chopped Amplifier Requires Only 5µA Supply Current

by Jim Williams

Figure 1 shows a chopped amplifier that requires only 5.5µA supply current. Offset Voltage is 5µV, with 0.05µV/°C drift. A gain exceeding 10^8 affords high accuracy, even at large closed-loop gains.

The micropower comparators (C1A and C1B) form a biphase 5Hz clock. The clock drives the input-related switches, causing an amplitude-modulated version of the DC input to appear at A1A's input. AC-coupled A1A takes a gain of 1000, presenting its output to a switched demodulator similar to the aforementioned modulator.

The demodulator output, a reconstructed, DC-amplified version of the circuit's input, is fed to A1B, a DC gain stage. A1B's output is fed back, via gain setting resistors, to the input modulator, closing a feedback loop around the entire amplifier. The configuration's DC gain is set by the feedback resistor's ratio, in this case 1000.

The circuit's internal AC coupling prevents A1's DC characteristics from influencing overall DC performance,

accounting for the extremely low offset uncertainty noted. The high open-loop gain permits 10ppm gain accuracy at a closed-loop gain of 1000.

The desired micropower operation and A1's bandwidth dictate the 5Hz clock rate. As such, the resultant overall bandwidth is *low*. Full-power bandwidth is 0.05Hz with a slew rate of about 1V/s. Clock-related noise, about 5µV, can be reduced by increasing C_{COMP}, with commensurate bandwidth reduction. ![LT]

Figure 1. 0.05µV/°C chopped amplifier requires only 5µA supply current

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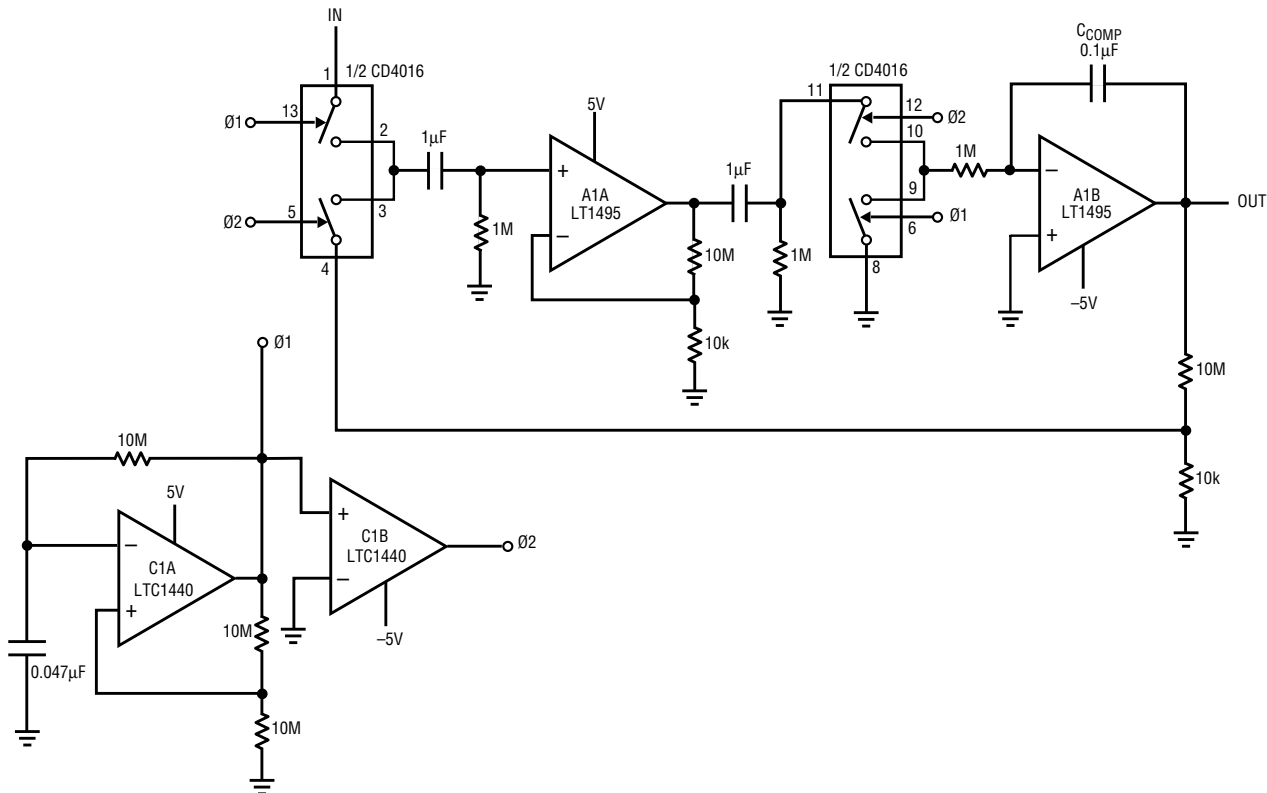
Making –5V 14-Bit Quiet

by Kevin R. Hoskins

Many high performance data acquisition systems reap multiple benefits when using ±5V supplies rather than a single 5V supply. These benefits include the ability to handle larger signal magnitudes than is possible with a single 5V supply. This increases a system's dynamic range and helps improve the signal-to-noise ratio. Operating on ±5V also increases headroom, which is important for signal conditioning. Compared to operating on 5V, conditioning circuitry operating on ±5V has twice the headroom, allowing it to easily handle ±2.5V signals without clipping. Additionally, the greater headroom avoids the limitations of rail-to-rail operation and widens the selection of high performance operational amplifiers and analog-to-digital converters, such as the LTC1419.

Although a switching or charge-pump power supply is an efficient way to create a –5V supply from a single 5V supply, they are not generally recommended for use with ADCs. Typical ADCs have inadequate PSRR, which decreases with increasing frequency. This poor PSRR performance cannot sufficiently attenuate the noise created by switching or charge-pump supplies. However, LTC's new family of ADCs, here represented by the LTC1419, has excellent PSRR. This family make it easy to achieve high performance data conversion, even at 14 bits, using a switch-based regulator for a –5V supply.

The LTC1419's high PSRR is shown in Figure 1. It shows that when operating on ±5V, the negative and positive PSRR are typically 80dB and 90dB, respectively, up to 200kHz for a 100mV ripple voltage. Combined with proper layout, the LTC1419's high PSRR allows it to convert signals without signal degradation while using switching regulators and charge pumps to generate its –5V supply. Applications including high speed communications, high resolution signal processing and wideband multiplexing benefit from the LTC1419's advantages—its 20MHz S/H bandwidth, 800ksps conversion rate and 14-bit resolution. This Design Idea shows two supply designs that are quiet enough to use with the LTC1419.
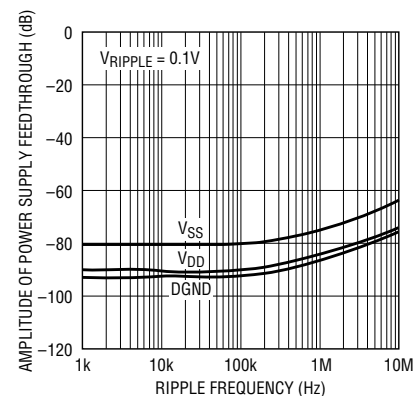
Figure 1. The LTC1419's positive supply PSRR of 80dB and negative supply PSRR of 90dB to 200kHz is a significant contribution to this ADC's wideband conversion performance and 80dB SINAD.

Low Noise Cuk Converter

The switching regulator shown in Figure 1 is configured as a Cuk converter, creating –5V from 5V. This configuration has the advantage of a small triangular switching-current waveform through the secondary inductor. This current waveform is continuous, producing much less harmonic content than is created by a typical positive-to-negative voltage converter, with its rectangular switching cur-
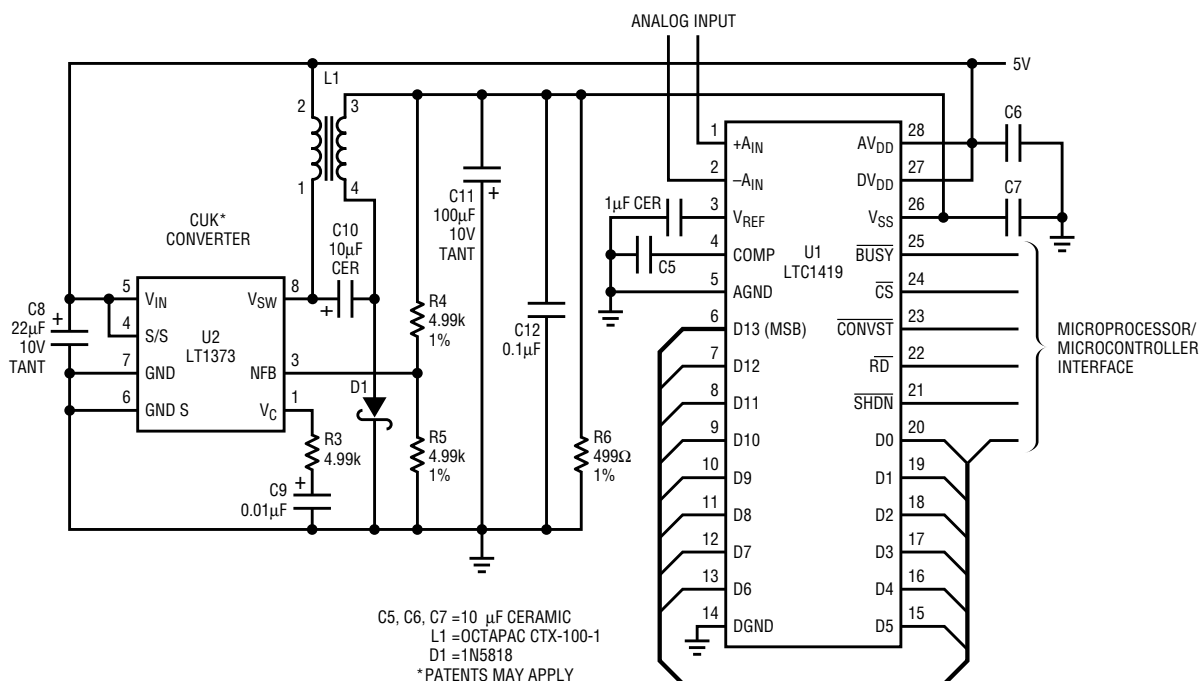
Figure 2. The LTC1419's 80dB PSRR allows the LTC1373 to generate the –5V and power the ADC without signal-conversion degradation.
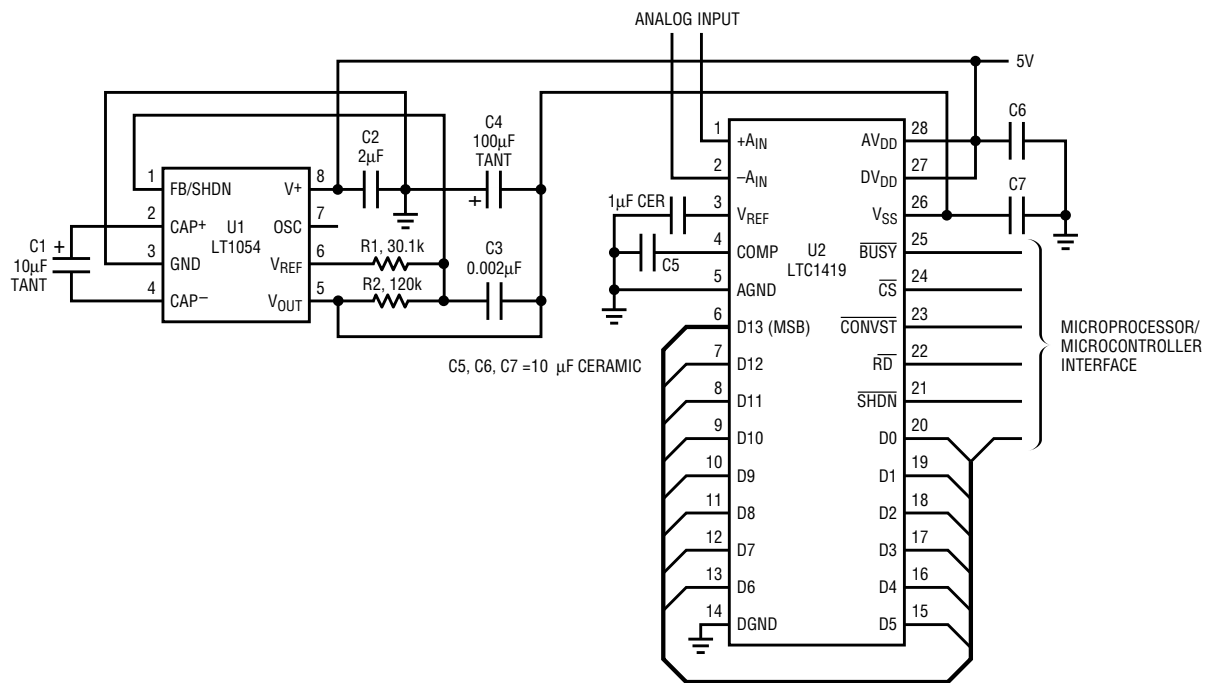
Figure 3. The LTC1419's high negative supply PSRR also allows the use of the LT1054 regulated charge pump to generate –5V without loss of performance.

rent waveform. With the components shown, the LT1373 operates continuously with load currents above 10mA. Because the LTC1419s typically draw 18mA of negative supply current, the LT1373 will always operate in the quiet continuous mode.

Regulated Charge Pump Converter

The LTC1419's negative PSRR also allows the use of charge pumps to create –5V. The circuit shown in Figure 3 uses the LT1054 regulated charge pump. This circuit has the advantage of reduced board space, since it lacks an inductor and requires fewer passive components.

Performance Results

What is the effect of using either of these switch-based supplies on the LTC1419's conversion performance? The FFTs in Figures 4–6 show the excellent results. Figure 4 is an FFT of a typical LTC1419 operating on ±5V from a lab supply and converting a full-scale 91kHz sine wave at 800ksps. The noise floor is approximately 114dB below full scale, the second harmonic's amplitude is approximately 90dB below full scale and the
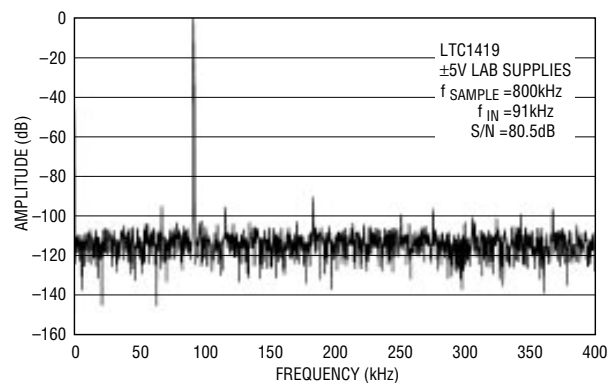
Figure 4. This FFT of an LTC1419 powered by a ±5V lab supply shows a SINAD of 80.5dB for a 91kHz input at a 800ksps sampling rate.
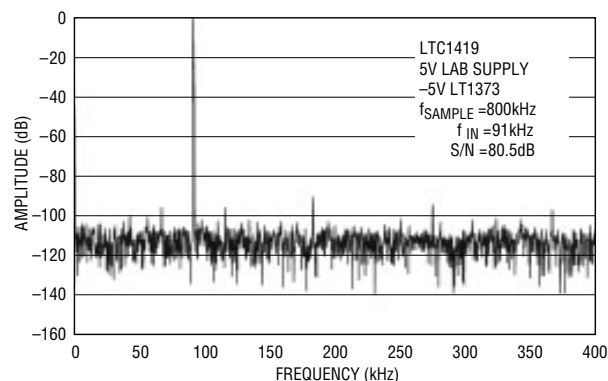
Figure 5. When the LTC1419's –5V supply is generated by an LT1373 switching regulator, the SINAD (80.5dB), the noise floor and the 91kHz fundamental's harmonic components remain essentially the same as those shown in Figure 4.

SINAD is 80.5dB. Figure 5 shows the FFT of the same LTC1419 operating on a 5V lab supply and –5V from the LT1373 circuit. The noise floor and the second harmonic's amplitude remain the same relative to full scale and the SINAD remains the same at 80.5dB. Figure 6 shows the LTC1419's response when its –5V is generated by the LT1054 circuit. As with the LT1373 circuit, the noise floor and the amplitude of harmonics remain the same and the SINAD is 80.8dB. ☆
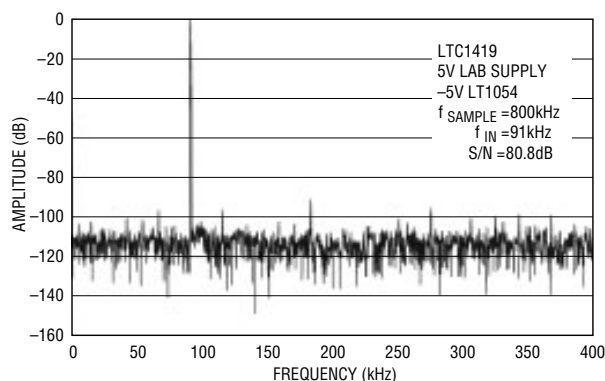
Figure 6. When the LTC1419's –5V supply is generated by an LT1054 inverter, the SINAD (80.8dB), the noise floor and the 91kHz fundamental's harmonic components again remain unchanged from those shown in Figure 4.
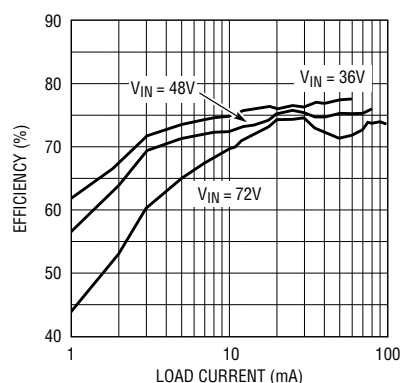
Figure 4. Efficiency vs load current

decreases sufficiently to trip the low-battery detector, stopping the switching. Start-up proceeds in this irregular fashion until, eventually, the voltage at V_A increases to 5V. (V_A is the same as V_{OUT}, because L2 and L3 have the same number of turns.) After start-up, current is supplied to the LT1316 from V_A rather than from the –48V rail, increasing efficiency. V_{OUT} must not be loaded until it reaches 5V or the circuit will not start.

During each switch cycle, current in the transformer primary ramps up until current limit is reached (See Figures 2 and 3). This peak switch current can be set by adjusting R5. The circuit shown uses a 69.8kΩ resistor to give a peak switch current of 50mA. Increasing R5 decreases the current limit. Secondary peak current will be approximately equal to the primary peak current multiplied by the transformer turns ratio. The FB pin has a sense voltage of 1.23V and V_{OUT} can be set by the following formula:

$$V_{OUT} = 1.23(R7/R6) + 0.6V.$$
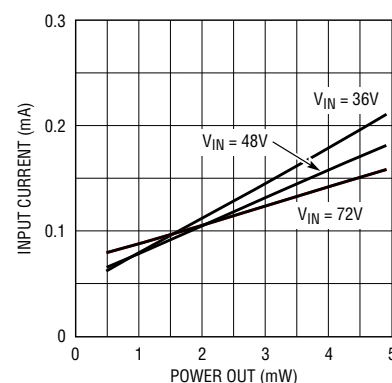
Figure 5. Input current vs power out

Efficiency versus load current is detailed in Figure 4. Note that for the range of 4mA to 80mA, 70% efficiency or greater is achieved. Figure 5 shows input current versus output power. Less than 80µA quiescent current flows when the converter supplies 0.5mW over the 36V–72V range. ☆

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Understanding and Applying Voltage References: Part One

by Mitchell Lee

Specifying the right reference and applying it correctly is a more difficult task than one might first surmise, considering that references are only 2- or 3-terminal devices. Although the word "accuracy" is most often spoken in reference to references, it is dangerous to use this word too freely because it can mean different things to different people. Even more perplexing is the fact that a reference classified as a dog in one application is a panacea in another. This article will familiarize the reader with the various aspects of reference "accuracy" and present some tips on extracting maximum performance from any reference.

As with other specialized electronic fields, the field of monolithic references has its own vocabulary. We've already learned the first word in our reference vocabulary, "accuracy." This is the yardstick with which references are graded and compared. Unfortunately, there are at least five or six good units for gauging accuracy. To keep you from reaching a full understanding of the topic, industry pundits use a special technique called "unit-hopping" to confuse and confound everyone from newcomer to seasoned veteran. You mention an accuracy figure and the pundit quickly hops to a new unit so that you cannot follow his line of reasoning. Figure 1 neutralizes the pundits' callous intentions and allows its possessor to unit-hop with equal ease and full comprehension. Refer to Figure 1 as you read this article.

Today's IC reference technology is divided along two lines: bandgap references, which balance the temperature coefficient of a forward-biased diode junction against that of a ΔV_{BE} (see sidebar on page 33); and buried Zeners, which use subsurface breakdown to achieve outstanding long-term stability and low noise. With few exceptions, both reference types use additional on-chip circuitry to further minimize temperature drift and trim output voltage to an exact value. Bandgap references are generally used in systems of up to 12 bits; buried Zeners take over from there in higher accuracy systems.

In circuits and systems, monolithic references face competition from discrete Zener diodes and 3-terminal voltage regulators only where accuracy is not a concern. 5% Zeners and 3% voltage regulators are commonplace; these represent 4- or 5-bit accuracy. At the other end of the spectrum—laboratory standards—the performance of the best monolithic references is exceeded only by saturated Weston cells and Josephson arrays, leaving monolithic references in command of every conceivable circuit and system application.

Reference accuracy comprises multiple electrical specifications. These are summarized in Table 1. Most commonly specified by circuit designers is *initial accuracy*. This is a measure of the output voltage error expressed in percent or in volts. Initial accuracy is specified at room temperature (25°C), with a fixed input voltage and zero load current, or for shunt references, a fixed bias current.

Tight initial accuracy is a concern in systems where calibration is either inconvenient or impossible. More commonly, absolute accuracy is only a secondary concern, as a final trim is performed on the finished product to reconcile the summation of all system inaccuracies. A final trim affects considerable cost savings by eliminating the need for tight initial accuracy in every reference, DAC, ADC, amplifier and transducer in the system.

Monolithic reference initial accuracy ranges from 0.02% to 1%, representing 1LSB error in 6-bit to 12-bit systems. Weston cells and
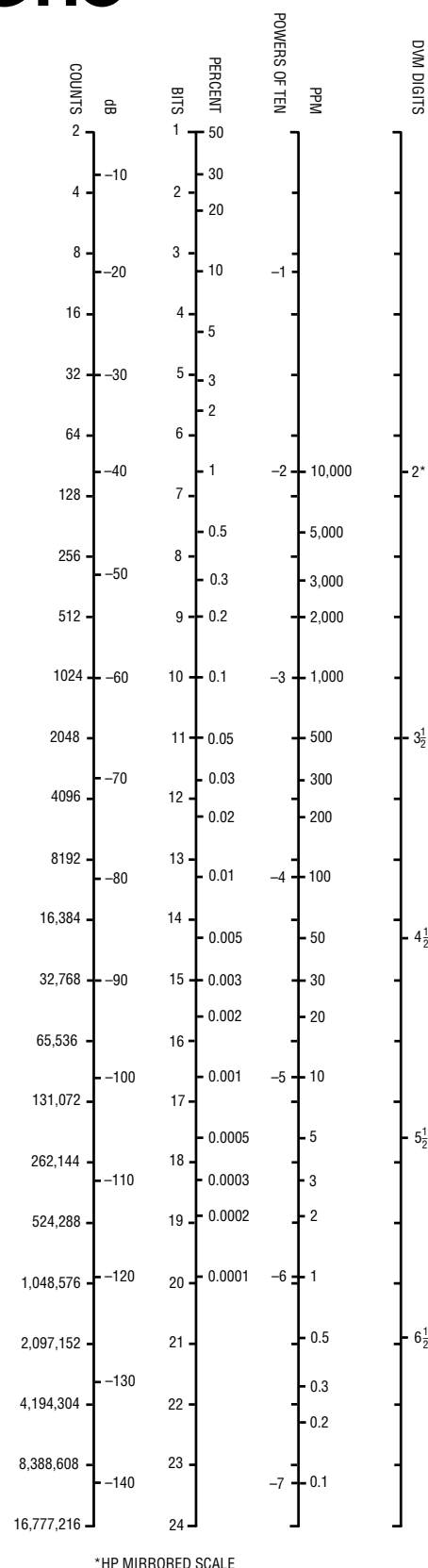

Figure 1. Accuracy translator

*HP MIRRORED SCALE

ΔV_{BE}: Integrated Circuit Workhorse

It is, perhaps, a cruel fate for IC designers that no single IC device or structure is invariant with changes in temperature. Various combinations of devices have been devised to stabilize circuits against changes in temperature. As explained in the text, Zener-based references use a Zener and a forward-biased diode connected in series to achieve near-zero temperature coefficient, and a bandgap relies on a ΔV_{BE} in series with a forward-biased diode.

An indispensable technique in integrated circuit design, the ΔV_{BE} is not widely known in other fields. Before explaining the theory of ΔV_{BE}, let's skip ahead to the two most important results: two identical diode (or base-emitter) junctions running different currents produce different voltage drops. The ratio of the currents controls the absolute value of the offset voltage. Further, this offset has a predictable, positive temperature coefficient of approximately 3.4µV/°C for each room-temperature millivolt of offset. By combining the positive TC of a ΔV_{BE} with the negative TC of a diode drop, a zero TC bandgap reference is formed. As we shall soon see, it takes a ΔV_{BE} offset of 650mV to cancel the –2.18mV/°C TC of a hypothetical diode*.

Two transistors (or diodes) produce an offset given by the following equation:

$$\Delta V_{BE} = V_{BE}1 - V_{BE}2$$
$$= (kT/q) \ln(Je1/Je2) \qquad (1)$$

where ΔV_{BE} = offset voltage, k = Boltzmann's constant (1.381×10^{-23} Joules/K), T = absolute tem-
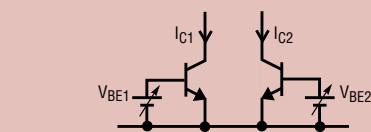
Figure A. The current ratio required to produce a certain V_{BE} offset is defined by equations (1) and (2).

perature (298K at room), q = charge of an electron (1.6×10^{-19} Coulombs), and Je = emitter current density. The actual units of area used to calculate Je1 and Je2 cancel each other, so that only the area ratio is important. Similarly, only the current ratio is important. If we restrict ourselves to using two identical transistors, Equation (1) reduces to

$$\Delta V_{BE} = V_{BE}1 - V_{BE}2$$
$$= (kT/q) \ln(I_C1/I_C2) \qquad (2)$$

where I_C = collector current (see Figure A). The temperature coefficient is given by

$$TC = d\Delta V_{BE}/dT$$
$$= (k/q) \ln(I_C1/I_C2) \qquad (3)$$

where k/q = 86.3µV/°C.

Calculating the current ratio required to produce +2.18mV/°C (corresponding to 650mV offset) we

find that it is unmanageably large, about 9.44×10^{10}:1. In practice, a much smaller offset is generated by a ΔV_{BE} cell and then amplified to 650mV. As an example, see Figure B. Using a 10:1 current ratio**, we find a room temperature offset from Equation (2) of 59.2mV, and a temperature coefficient of 199µV/°C. Applying a gain of slightly less than eleven brings us to 650mV and +2.18mV/°C.

Adding a PNP emitter follower to the output of this circuit forms a crude "bandgap" reference, with an output voltage equal to the sum of 650mV and the PNP's V_{BE}. Assuming V_{BE} = 600mV, the output would be 1.25V. The reference could be further improved by trimming the gain of eleven so that the ΔV_{BE} exactly canceled the PNP's base-emitter temperature coefficient. IC bandgap references are constructed in a similar way. *LT*

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*The numbers have been massaged for those that want to reproduce the calculations.

**or a combination of current and area scaling to achieve a 10:1 current density ratio in Equation (1).
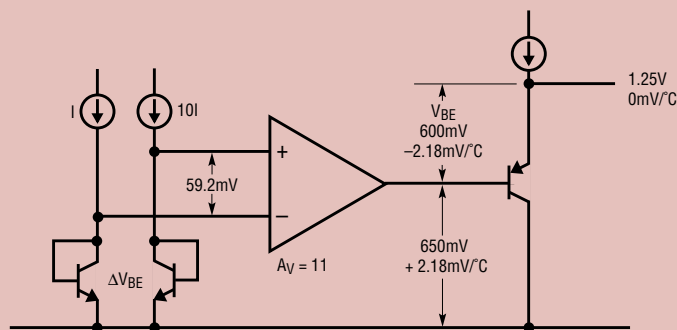
Figure B. A bandgap reference is formed by stacking a ΔV_{BE} generator and a V_{BE}.

Josephson arrays clock in at 1ppm–10ppm and 0.02ppm initial accuracy, respectively (0.02ppm is less than 1LSB error in a 25-bit system).

Temperature-induced changes in reference output voltage can quickly overshadow a tight initial accuracy specification. Considerable effort is therefore expended to minimize the

temperature coefficient (tempco) of a reference. Most references are guaranteed in the range of 2ppm/°C to 40ppm/°C, with a few devices falling outside this range. A properly applied LTZ1000 temperature stabilized reference can demonstrate 0.05ppm/°C.

Tempco is specified as an average over the operating temperature range

in units of ppm/°C or mV/°C. This average is calculated in what is called the "box" method. Figure 2 shows how box method tempco figures are defined and calculated. The reference in question (LT1019 bandgap) is tested over the specified operating temperature range. The minimum and maximum recorded output voltages

are applied to the equation shown, resulting in an average temperature coefficient expressed in V/°C. This is further manipulated to find ppm/°C, as used in the data sheet. The tempco is an average over the operating range, rather than an incremental slope measured at any specific point. In the case of the LT1021 and LT1236, the incremental slope at 25°C is also guaranteed.

A data sheet figure for tempco can be used to directly calculate the output voltage tolerance over the entire operating temperature range. A device with a tempco of 10ppm/°C, specified for 0°C to 70°C, could drift up to 700ppm from the initial value (about 3 counts in a 12-bit system). A 0.1% reference with 700ppm tempco error is guaranteed 0.17% accurate over its entire operating temperature range.

Two exceptions to this rule are the LT1004 and LT1034, which simply guarantee absolute output voltage accuracy over the entire operating temperature range. The LT1009 and LT1029 use a combination of the two, called the "bow tie" or "butterfly" method (see the LT1009 data sheet for a detailed explanation).

Neither the bandgap nor buried Zener, in their basic form, are inherently low drift. Special on-chip circuitry is used to improve the tempco of the reference core. A buried Zener is first-order compensated against temperature changes by adding a P-N junction diode. The Zener itself measures +2mV/°C and the diode –2mV/°C. The combination of the two in series cancel to about 0.2mV/°C
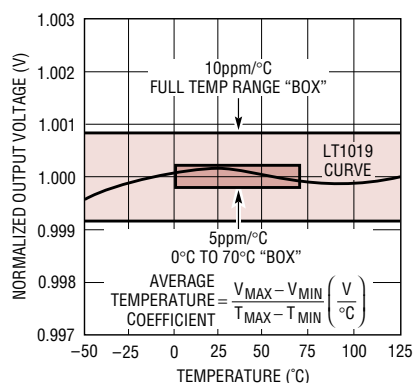
Figure 2. The box method expresses absolute output accuracy over temperature as a drift term.

Table 1. Reference accuracy specifications

Parameter	Description	Preferred Unit(s)
Initial Accuracy	Initial output voltage at 25°C	V, %
Temperature Coefficient	$\dfrac{V_{MAX} - V_{MIN}}{\text{TOTAL TEMPERATURE RANGE}}$	ppm/°C
Long-Term Stability	Change in output vs time measured over 1000 hours or more	ppm/$\sqrt{kh}$
Noise	0.1Hz to 10Hz	μV_{P-P}, ppm_{P-P}
	10Hz to 1kHz	μV_{RMS}, ppm_{RMS}

(≈30ppm/°C) out of a total of 7V. Interestingly, this is very close to the tempco of a saturated Weston cell, which measures –40μV/°C, or –39ppm/°C. Weston cells are held in a temperature-controlled bath; monolithic buried Zener references are further compensated against temperature changes by carefully adding fractional V_{BE} and/or ΔV_{BE} terms to the output. Post-manufacturing trims are used on both bandgap and buried Zener products to further minimize tempco of the finished reference.

Another detractor from accuracy is *long-term stability*. The output of a reference changes, usually in one direction, as it ages. The effect is logarithmic; that is, the output changes less and less as time progresses. The units of long-term stability, ppm/$\sqrt{kh}$ (kh = 1000 hours), reflect the logarithmic decline of the output change vs time. Because long-term changes in the output are small and occur over the course of months or years, it is impossible to devise an affordable manufacturing test to guarantee the true stability of all references. Instead, this parameter is characterized by aging dozens of units in a temperature-controlled chamber at 25°C to 30°C for 1000 hours or more. Note that the absolute temperature is unimportant, but it must remain invariant during the course of the test. Mathematically extrapolating long-term stability data from high temperature, accelerated life tests leads to erroneously optimistic room temperature results.

When long-term stability is guaranteed, it is done by means of a 4-week burn-in, during which multiple output voltage measurements are made. Even with this elaborate, costly procedure, the guaranteed limit is about three to four times the typical drift.

Unless the product is designed for frequent calibration or is relatively low performance, long-term stability may be an important aspect of reference performance. Products designed for a long calibration cycle must hold their accuracy for extended periods of time without intervention. These products demand references with good long-term stability. You can expect buried Zeners to perform better than 20ppm/$\sqrt{kh}$, and bandgaps between 20ppm and 50ppm/$\sqrt{kh}$. Some of this drift is attributed to the trim and compensation circuitry wrapped around the reference core. The LTZ1000 dispenses with trim and compensation overhead in favor of an on-chip heater. The remaining Zener/diode core drifts 0.5ppm/$\sqrt{kh}$ in the first year of operation, approaching the stability of a Weston cell.

Most of the long-term stability figures shown in LTC reference data sheets are for devices in metal can packages, where assembly and package stresses are minimized. You can expect somewhat less performance for the same reference in a plastic package.

One last factor that affects accuracy is short-term variation of output voltage, otherwise known as noise.

Table 2. True to late twentieth century form, LTC references offer many choices.

Part	Bandgap	Buried Zener	Series	Shunt	1.25V	2.5V	4.5V	5.0V	7.0V	10V	Trim
LT1004	✓			✓	✓	✓					
LT1009	✓			✓		✓					✓
LT1019	✓		✓	✓		✓	✓	✓		✓	✓
LT1021		✓	✓	(7V, 10V)				✓	**	✓	✓
LT1027		✓	✓					✓			✓
LT1029	✓			✓				✓			✓
LT1031		✓	✓	✓						✓	
LT1034	✓	*		✓	✓	✓			*		
LT1236		✓	✓	(10V only)				✓		✓	✓
LT1460	✓		✓			✓		✓		✓	
LT1634	✓			✓	✓						
LTZ1000		✓		✓					7.2		

*The LT1034 bandgap reference includes a shunt-mode buried Zener.
**The LT1021-7 cannot be trimmed.

Reference noise is typically characterized over two frequency ranges: 0.1Hz to 10Hz for short-term, peak-to-peak drift, and 10Hz to 1kHz for total "wideband" RMS noise. Noise voltage is usually proportional to output voltage, so the output noise expressed in ppm is constant for all voltage options of any given reference. Wideband noise ranges from 4ppm–16ppm RMS for bandgap references, to 0.17ppm–0.5ppm RMS for buried Zeners. Noise improves with increased reference current, regardless of reference type. But since the reference core operating current is set internally, the noise characteristics cannot be changed except by external filtering (the LT1027 features a noise filtering pin). The LT1034 and LTZ1000 buried Zeners are externally accessible, allowing the user to increase the bias current and reduce noise.

Adding output bypassing or external compensation will affect the character of a reference's noise. In particular, if the compensation is "peaky," the spot noise will likely rise to a peak somewhere in the 100Hz to 10kHz range. Critical damping will eliminate this noise peak.

Reference noise can affect the dynamic range of a high resolution system, obscuring small signals. Low frequency noise also complicates the measurement of output voltage. Modern, high accuracy digital voltmeters can average many readings to help filter low frequency noise effects and provide a stable reading of a reference's true output voltage.

Essential Features

There are two styles of references: shunt, functionally equivalent to a Zener diode; and series, not unlike a 3-terminal regulator. Bandgaps and buried Zeners are available in both configurations (see Figure 3). Some series references are designed to also operate in shunt mode by simply biasing the output pin and leaving the input pin open circuit. Series-mode references have the advantage that they draw only load and quiescent current from the input supply, whereas shunt references must be biased with a current that exceeds the sum of the maximum quiescent and maximum expected load currents. Since they are biased by a resistor, shunt references can operate on a very wide range of input voltages.

About half of LTC's reference offerings include a pin for external (customer) trimming. Some are designed for precision trimming of the reference output, whereas others have a wide trim range, allowing the output voltage to be adjusted several percent above or below the intended operating point.

Many voltage options are available for both bandgaps and buried Zeners. Table 2 shows the voltage options for each LTC reference, plus a summary of reference type, operating modes and external trim option.
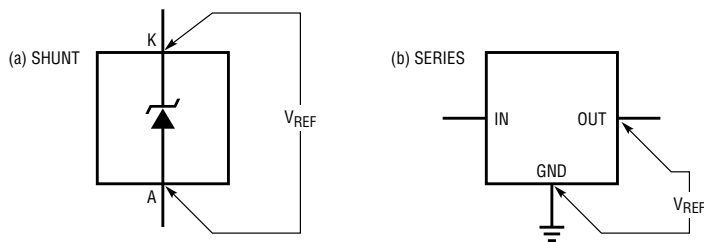
Figure 3. References are supplied in either 2-terminal Zener style (a) or 3-terminal voltage regulator style (b).

Figure 4. The LT1009 is optimized for rapid settling at power-up.

If load current steps must be handled, transient response is important. Transient response varies widely from reference to reference and comprises three distinct qualities: turn-on characteristics, small-signal output impedance at high frequency and settling behavior when subjected to a fast, transient load. References exhibit these qualities because almost all contain an amplifier to buffer and/or scale the output.

The LT1009 is optimized for fast start-up characteristics, and it settles in a little over 1µs, as shown in Figure 4. For some references, optimum settling is obtained with an external compensation network. As shown in Figure 5, a 2µF/2Ω damper optimizes the settling and high frequency output impedance of an LT1019 reference. Fastest settling is obtained with an LT1027, which settles to 13 bits accuracy in 2µs. This impressive feat is illustrated by the oscillograph of Figure 6, which clearly shows the output recovering from a 10mA load step.

Reference Pitfalls

References look deceptively simple to use, but like any other precision product, maximum performance is not necessarily easy to achieve. Here are a few common pitfalls reference users face, and ways to beat them.
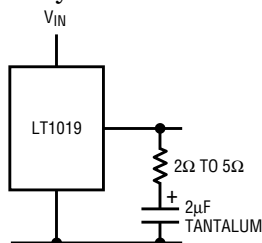
Current-Hungry Loads

Most references are specified for maximum load currents (or shunt currents) of 10mA–20mA. Nevertheless, best performance is not obtained by running the reference at maximum current. A number of effects, including thermal gradients across the die and thermocouples formed between the leads and external circuit connections, may limit the short-term stability of the output voltage. Adding an external pass transistor, as shown in Figure 7, removes the load current from the reference. For loads greater than 300µA, the pass transistor carries almost all of the current and eliminates short-term thermal drift. This circuit is also useful for applications requiring more than 20mA, and easily supports up to 100mA, limited only by transistor beta and dissipation.

"NC" Pins

If references need only two or three external connections, why are they supplied in 8-pin packages? There are several reasons, but the one we'll cover here is post-package trimming. To guarantee tight output tolerances, some factory trimming is necessary after the device has been packaged. In packaged form we no longer have

direct access to the die, so the extra pins on an 8-pin package are used to effect post-package trimming.

For some ICs, "NC" means "this pin is floating, you can hook it up to whatever you want." In the case of a reference, it means "don't connect anything to this pin." That includes ESD and board leakage, as well as intentional connections. External connections will, at best, cause output voltage shifts and, at worst, permanently shift the output voltage out of spec.

A similar caution applies to the TRIM pin on references with adjustable outputs. The TRIM pin is akin to an amplifier's summing node; do not inject current into a TRIM pin—unless you want to trim the output, of course. Here board leakage or capacitive coupling to noise sources are pitfalls to avoid. *LT*

This article will conclude in the August issue of *Linear Technology*; if you can't wait for the thrill-packed conclusion, you can order the second half by checking the appropriate box on the response card.

Figure 5. Optimum settling realized with RC compensation at output

Figure 6. The LT1027 is optimized for fast settling in response to load steps.

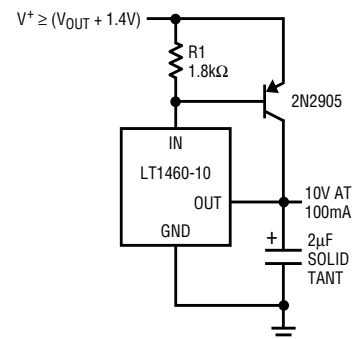Figure 7. An external transistor is useful for boosting output current as well as for removing load current from the reference. This trick works on all 3-terminal references.

New Device Cameos

LT1635 Micropower Op Amp and Reference

The LT1635 is a new analog building block that includes a high quality op amp, precision reference and reference buffer. The LT1635 combines precision specifications with single-supply micropower operation. An important feature of the device is operation on an unusually low 1.2V single supply, or dual supplies of up to ±5V; the LT1635 consumes a mere 130µA of supply current.

The input common mode range of the op amp includes ground and incorporates phase-reversal protection to prevent false outputs from occurring when the input is below the negative supply. The rail-to-rail output stage can swing to within 15mV of each rail with no load and can deliver 20mA output current while driving to within 400mV of either supply. The gain bandwidth of the op amp is 200kHz; it is unity gain stable with up to 1000pF of load capacitance.

The 0.2V precision bandgap reference is referred to V⁻ and includes a buffer amplifier to enhance the flexibility of the LT1635. The reference and buffer combine to achieve a drift of only 30ppm/˚C, a load regulation of 150ppm/mA and a line regulation of 20ppm/V.

The LT1635 is offered in SO-8 and 8-pin DIP packages, in both commercial and industrial temperature grades, and has been optimized for both single 5V and ± 5V operation.

LT1492/LT1493: 550µA, 5MHz, 3V/µs Single-Supply, Precision Dual and Quad Op Amps

The LT1492 and LT1493 dual and quad precision operational amplifiers are ideal for low power and single-supply applications that require DC accuracy, high speed and high output current.

The LT1492/LT1493 operate over a wide supply range of 2.5V to 36V total and draw a maximum supply current of only 550µA. The devices feature 5MHz gain bandwidth, a slew rate of 3V/µs and can deliver a minimum of 20mA output-drive current.

In addition to the aforementioned AC specifications, the LT1492/LT1493 have excellent DC specs. With less than 180µV of input offset voltage, 100nA input bias current and 20nA offset current, the LT1492/LT1493 eliminate trims in most systems. A minimum open-loop voltage gain (A_{VOL}) of 1500V/mV (V_S = ±15V, R_L = 5k) ensures a very small gain error. Furthermore, the inputs can be driven beyond the supplies without damage or phase reversal of the output.

The LT1492 is available in plastic 8-pin DIP and SO-8 packages with the standard dual op amp pinout. The LT1493 is available in 16-pin SO package.

LTC1540 Ultralow Power Comparator and Reference

The LTC1540 is an ultralow power comparator with a built-in reference. The comparator draws only 0.35µA supply current with a 5V power supply and features an internal, 1.182V (±2%) reference. It also has programmable hysteresis and a TTL/CMOS output that can sink or source current. The reference output can drive a bypass capacitor of up to 0.01µF without oscillation and can source up to 1mA and sink up to 20µA.

The comparator operates from a single 2V–11V supply or dual ±1V to ±5.5V supplies. Comparator hysteresis is easily programmed using two resistors and the HYST pin. The comparator's input range extends from the negative supply to within 1.3V of the positive supply.

The LTC1540 is pin compatible with the LTC1440. It is available in 8-pin SO and MSOP packages.

Ultralow I_Q LTC1474/ LTC1475 High Efficiency Step-Down DC/DC Converters Now Available with Fixed Output Voltages

The LTC1474/LTC1475, featuring 3V–18V operation, 10µA typical quiescent current and a tiny 8-pin MSOP package, are now available in fixed 3.3V and 5V output versions. The LTC1474-3.3 and LTC1474-5 contain internal feedback resistors trimmed for output voltages of 3.3V and 5V, respectively. As with the adjustable version, they are controlled by a RUN pin and feature a low-battery comparator that remains active in shutdown. The LTC1475-3.3 and LTC1474-5 have all of the above features, plus an ON/OFF latch for push-button control of power. The adjustable versions of the LTC1474 and LTC1475 are also available.

All six members of the LTC1474/ LTC1475 family feature operating efficiencies exceeding 90% and a combination of cycle-by-cycle inductor current control and ultralow quiescent current previously unavailable in switching regulators. Strapping two pins together defines a 400mA peak inductor current with no external current sense resistor, allowing output currents of up to 300mA . By adding an inexpensive external resistor, the user can program the peak inductor current to be as low as 10mA, for efficient low current operation with small inductors.

The LTC1474/LTC1475 are ideal for many quiescent-current sensitive applications, such as battery-powered, handheld devices, keep-alive power supplies and industrial 4–20mA loops. In addition to the small-footprint MS8 package, all device types are also available in the standard 8-lead SO package.

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> at (408) 432-1900

LTC1439: a 40% Smaller Package for LTC's Full-Function, Low Noise, Multiple Output Controller

The LTC1439 is now offered in a narrower and shorter "G" package, measuring $0.2'' \times 0.5''$, down from the $0.3'' \times 0.6''$. "GW" package. The total package "footprint" including the pins has been reduced from $0.4'' \times 0.6''$ to $0.3'' \times 0.5''$, a 40% PC board savings.

The LTC1439 offers the most compact power supply system solution for applications requiring a constant-frequency, dual controller with a 1% guaranteed reference and 1% load and line regulation over its entire operating temperature range. The Adaptive Power™ output stage maximizes efficiency while maintaining constant frequency operation by dynamically switching between two optimally sized N-channel output power MOSFETs, depending upon loading conditions. This technique delivers true constant frequency operation over two decades of output current—down to typically 1% of the designed maximum output load. This technique eliminates the possibility of audible artifacts that can be produced by the switching power supply's inductor or transformer under noncontinuous inductor operation. The controller switches over to Burst Mode operation at very low output currents, maximizing efficiency when a system is in standby mode. External frequency compensation ensures optimal transient response and overall loop stability in a variety of applications and topologies. A power-on reset output holds its output low for system reset for 65,536 clock cycles (typically 300ms) after the first controller's output has risen to 95% of its final output voltage. An auxiliary linear regulator with an external pass device is capable of supplying any required voltage/current combination that might be required for the power supply system. An extra comparator whose negative input is tied to the internal reference is available to be used for a low-battery comparator or other system function. The first controller can be pin selected to provide a 5V or a 3.3V output and the second controller can be programmed to be a 5V, 3.3V or an adjustable output having a range of from 1.2V to 9V. The controllers have logic-controlled independent shutdown and programmable soft-start. A true phase-locked loop can lock the "constant" frequency over a 2:1 range or can be used for frequency shifting or spread-spectrum operation. *LT*

*for
the latest information
on LTC products,
visit
www.linear-tech.com*

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

DESIGN TOOLS

Applications on Disk

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp.   Available at no charge

SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim.   Available at no charge

SwitcherCAD™ — The SwitcherCAD program is a powerful PC software tool that aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. 144 page manual included. $20.00

SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

Micropower SwitcherCAD™ — The MicropowerSCAD program is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components which surround the DC/DC converter. In the case of a battery supply, MicropowerSCAD can perform a battery life simulation. 44 page manual included. $20.00

MicropowerSCAD supports the following LTC micropower DC/DC converters: LT1073, LT1107, LT1108, LT1109, LT1109A, LT1110, LT1111, LT1173, LTC1174, LT1300, LT1301 and LT1303.

Technical Books

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook, Vol II — This 1248 page supplement to the 1990 Linear Databook is a collection of all products introduced in 1991 and 1992. The catalog contains full data sheets for over 140 devices. The 1992 Linear Databook, Vol II is a companion to the 1990 Linear Databook, which should not be discarded. $10.00

1994 Linear Databook, Vol III —This 1826 page supplement to the 1990 and 1992 Linear Databooks is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The 1994 Linear Databook Vol III is a companion to the 1990 and 1992 Linear Databooks, which should not be discarded. $10.00

1995 Linear Databook, Vol IV —This 1152 page supplement to the 1990, 1992 and 1994 Linear Databooks is a collection of all products introduced since 1994. A total of 80 product data sheets are included with updated selection guides. The 1995 Linear Databook Vol IV is a companion to the 1990, 1992 and 1994 Linear Databooks, which should not be discarded. $10.00

1996 Linear Databook, Vol V —This 1152 page supplement to the 1990, 1992, 1994 and 1995 Linear Databooks is a collection of all products introduced since 1995. A total of 65 product data sheets are included with updated selection guides. The 1996 Linear Databook Vol V is a companion to the 1990, 1992, 1994 and 1995 Linear Databooks, which should not be discarded. $10.00

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