LINEAR TECHNOLOGY

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LTC1406: 8-Bit, 20MHz ADC Offers 250MHz Input Bandwidth and Tiny Footprint

by Jeff Huehn

LTC Goes High Speed

Everyone knows about Linear Technology's linear and switching regulators, but over the last several years Linear has built an impressive family of data conversion products. With the recent introduction of fast 12-bit and 14-bit ADCs, and, most recently, a 16-bit part, the family continues to expand. Now, the newest member of the LTC converter family, the LTC1406, takes LTC in a new direction: high speed for communications and video conversion.

LTC1406 Features

- ❑ 20Msps sample rate, 8-bit parallel output
- ❑ 250MHz internal sample-and-hold
- ❑ 48.5dB S/(N + D) and 62dB THD
- ❑ 7.0 effective bits at 70MHz
- ❑ ±1LSB DNL and INL Max
- ❑ Low power with power-down mode
- ❑ Small footprint: 24-pin narrow SSOP package

Why Use Linear Technology?

There are other 8-bit, 20Msps converters on the market, so why use the LTC1406? The LTC1406 has several significant advantages over its seemingly similar competitors.

Wide Input Bandwidth for Communications

One very useful advantage is the extremely wideband sample-and-hold. The 250MHz input bandwidth of the LTC1406 allows for undersampling of very high frequency signals. Coupled with its excellent distortion, the LTC1406 has better high frequency undersampling performance than any other 8-bit, 20MHz part on the market. The signal-to-(noise + distortion) ratio is a nearly ideal 48.5dB for low frequencies; it stays flat all the way out to 10MHz. Even at 70MHz, well beyond the Nyquist frequency of 10MHz, the signal-to-(noise + distortion) ratio is still close to 44dB, which is equivalent to 7.0 ENOBs (effective number of bits). Figure 1 illustrates this outstanding performance along with the spurious free dynamic range (SFDR). For applications in communications, or any application that depends on high dynamic range and a high number of effective bits at very high input frequencies, the LTC1406 outperforms the competition.

Small Footprint

Is board space a problem? The LTC1406 is also the smallest 8-bit, 20MHz part available. It comes in the tiny GN-24 package that occupies only 52mm^2 (only 1.75 times the size of an

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Issue Highlights

Our cover article for this issue introduces the LTC1406, a high speed 8-bit ADC intended for communications and video-conversion applications. It features a 20Msps sample rate, 8-bit parallel output, a 250MHz internal sample-and-hold and excellent noise and distortion specs.

Two other new data converters are also introduced in this issue: the LTC1401 and LTC1404 are low power, 12-bit serial ADCs. The LTC1401 operates on a 3V supply and samples at 200ksps. The LTC1404 is a pin-compatible upgrade of the LTC1400. It samples at 600ksps and operates on either single 5V or ±5V supplies. These devices provide the highest throughput per square area of board space of any 12-bit ADC on the market.

This issue debuts a new instrumentation amp and two new op amp families: the LT1167 is the next-generation instrumentation amplifier designed to replace the previous generation of monolithic instrumentation amps, as well as discrete, multiple–op amp solutions. The gain of the LT1167 is set by the absolute value of one external resistor. Gain error depends on the ratio of one external resistor to the value of the LT1167's internal, laser-trimmed resistors, which are trimmed to better than 0.1%.

The LT1638 and LT1639 are Linear Technology's latest general-purpose, low power, dual and quad rail-to-rail operational amplifiers. The circuit topology of the LT1638 is based on Linear Technology's popular LT1490/LT1491 op amps, with substantial improvements in speed. The LT1638 is five times faster than the LT1490. The LT1638/LT1639 are "tough" op amps, with a variety of features that make them ideal for general-purpose applications.

The LT1630/LT1632 duals and LT1631/LT1633 quads are the newest members of Linear Technology's family of precision rail-to-rail op amps, which provide the best combination of AC performance and DC precision over the widest range of supply voltages. The LT1630/LT1631 deliver a 30MHz gain-bandwidth product, a 10V/µs slew rate and 6nV/$\sqrt{Hz}$ input-voltage noise. Optimized for higher speed applications, the LT1632/LT1633 have a 45MHz gain-bandwidth product, a 45V/µs slew rate and 12nV/$\sqrt{Hz}$ input voltage noise.

Expanding LTC's line of products to support the SMBus standard, we debut the LTC1710, which features two SMBus controlled 0.4Ω switches in an MSOP-8 package. The LTC1710 is a complete solution for delivering power to portable-equipment peripherals without external switches.

Rounding out the selection of new parts introduced in this issue, we debut the LT1394, an ultrafast, low power, single-supply comparator. The LT1394 is the first product made with LTC's new 6GHz complementary bipolar process.

In our Design Ideas section, we present a variety of power conversion ideas: a high isolation converter that achieves 3750V_{RMS} isolation with the LT1172 and off-the-shelf magnetics, a wide input range, low voltage flyback regulator based on the LTC1624, a positive to negative converter for –48V telecommunications applications, a bootstrapped synchronous boost converter using the LTC1266, a battery-powered buck-boost converter that requires no magnetics and a number of battery converter circuits based on the LT1610 micropower DC/DC converter. We also include a design primer for creating lowpass filters with added notches using the LTC1562 quad Operational Filter™ IC, and an optimized low power, low distortion ADSL line driver based on the LT1207.

LTC in the News...

Linear Technology Reports Another Quarter of Record Sales and Profits

"This was a good March quarter for us," said Robert H. Swanson, president and CEO of Linear Technology. "We achieved strong quarterly financial performance culminating in record return on sales. Recent difficulties experienced by some technology companies regarding slowing demand in Asia and in computer markets worldwide have us cautious going forward. However, our product, geographic and end-market diversity and our good March quarter performance should enable continued sequential sales and profits growth in the upcoming June quarter."

On the strength of the Company's third quarter results, it was named the "Stock of the Day" by the *San Jose Mercury News* in its April 16, 1998 edition. LTC also received prominent attention in the *San Jose Mercury News*'s annual "Silicon Valley 150" report. The report included a feature article on LTC in which Elias Moosa, an analyst for BancAmerica Robertson Stephens, praised it as "truly among the premier chip companies"; the report also ranked Linear Technology as among the top twenty Silicon Valley firms for return on sales and market capitalization.

Net sales for the third quarter ended March 29, 1998, were $125,982,000, an increase of 33% over net sales of $95,033,000 for the third quarter of the previous year. The Company also reported record net income for the quarter of $47,174,000 or $0.59 diluted earnings per share, an increase of 39% from $33,980,000 or $0.43 diluted earnings per share, reported for the third quarter of last year. A cash dividend of $0.06 will be paid on May 13, 1998 to shareholders of record on April 24, 1998.

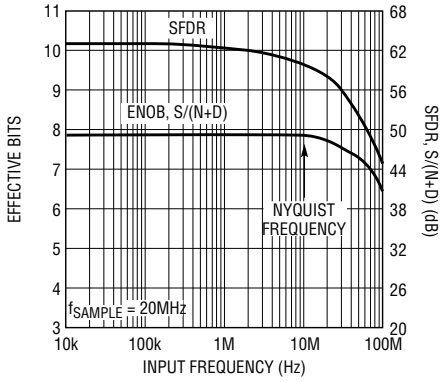


Figure 1. LTC1406 SINAD and SFDR plot shows 7 effective bits at 70MHz input frequency.

LTC1406, continued from page 1

SO-8 package). It also requires only three surface mount bypass capacitors, one for the analog, digital, and output logic supplies, one for the reference input (V_{REF}) and one for the V_{BIAS} pin, resulting in a small layout footprint in addition to a small package.

Low Power Shutdown Mode

The low power consumption of the LTC1406 can be reduced even further by taking advantage of the Shutdown mode. Taking the $\overline{SHDN}$ pin low powers down the converter and bias circuitry so that the part draws only a tiny leakage current from the supply. This can reduce power consumption in portable and battery-powered equipment whenever the converter is idle.

Overrange/ Underrange Detection

Another feature unique to the LTC1406 is the ability to detect an overrange or underrange condition using the Overflow/Underflow bit. The OF/UF output will transition from 0 to 1 at 1LSB below the 0000 0000 to 0000 0001 transition and 1LSB above the 1111 1110 to 1111 1111 transition, providing a clear indicator that the input signal is outside the full-scale conversion range of the converter. This can be used as a flag when trimming the input span to maximize the signal-to-noise ratio. For imaging applications where the output of a CCD varies from pixel to pixel, for communications applications where the magnitude of the input signal is constantly changing or for any application where the input span varies, the LTC1406 makes it easy to optimize performance.

Ease of Use with Flexibility

Trying to make a high speed data converter perform used to be somewhere near the magic end of the "science–magic scale." It was also generally true that the more flexibility (the more options the user had for connecting the part), the more difficult it was to get the part to work properly. The LTC1406 changes that: it was designed to make it easy to get good performance and to be very easy to use without sacrificing flexibility. It starts with very simple, straightforward connections. A power supply, a reference, a clock and an input are all you need to start converting high speed signals into ones and zeros.

Connecting the supply voltage is a good example of the simplicity and flexibility built into the LTC1406. In the simplest configuration, connect the analog, digital and output logic supplies together to a single 5V supply and bypass capacitor and you're done. If you need to interface with 3V logic, the LTC1406 is ready for that too. The logic inputs are set up to work equally well with 3V or 5V signals and the output logic supply (O_{VDD}) can be connected to a separate 3V supply to provide 3V data out. This eliminates the need for circuitry to level shift a 3V clock up to 5V and/or level shift the entire 5V data bus back down to 3V.

The reference is also easier to provide. Rather than the conventional half-flash architecture that requires two reference voltages, two bypass capacitors and two buffer amplifiers for the top and bottom of the reference ladder, the LTC1406 requires only one 2.5V reference and bypass capacitor. This is really an advantage when changing or trimming the input span. Instead of moving both the top and bottom voltages to obtain the correct span, the single 2.5V reference functions as a gain control. It also requires less current, and therefore less power, from the reference, since there is no resistive ladder to drive. The typical reference current required is about 1mA (5mW) compared to about 7mA (35mW) for most of the half-flash architectures.

Flexible Analog Inputs

Easy to Drive

One of the strongest features of the LTC1406 is the structure of the inputs. The inputs are very easy to drive. Following the rising clock edge, the LTC1406 goes into track mode and, like other converters, the inputs draw a small current spike to charge the input sampling capacitors. However, the input capacitance is typically one-fourth that of competitive parts, so the current spike necessary to charge them is much smaller. While the clock is high, the voltage across the sampling capacitors will track the voltage on the inputs. Again, this small input capacitance makes the inputs much easier to drive, particularly for high input frequencies. Reducing the capacitive load by 70%–80% greatly reduces the input-buffer-amplifier requirement and may eliminate the need for a buffer amplifier altogether.

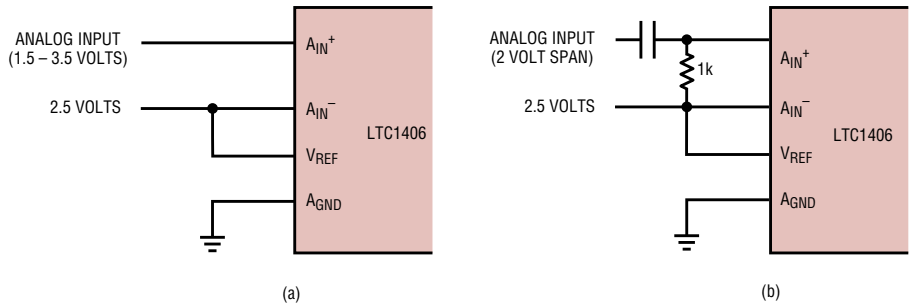


Figure 2. (a) Using A_{IN}+ as the input and connecting A_{IN}– to V_{REF} yields an input span of 1.5V–3.5V. (b) AC coupling the input yields a 2V AC-coupled span.

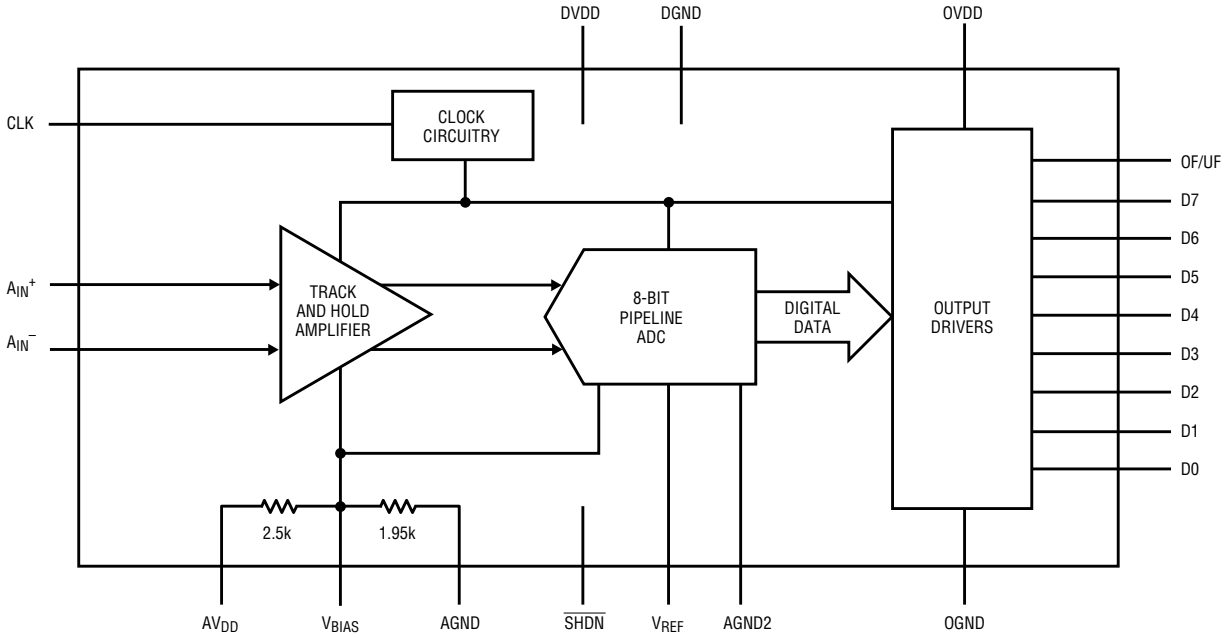


Figure 3. The LTC1406has a wideband differential track-and-hold that can capture input signals of up to 230MHz. The separate output supply and grounding pins allow for easy interface to 3V logic.

On the falling clock edge, the part samples the input voltage; the inputs draw only a small leakage current while the clock is low.

Differential or Single-Ended

The LTC1406's inputs are truly differential; they will always convert the difference between A_{IN}+ and A_{IN}–. The maximum output code (1111 1111) occurs when A_{IN}+ – (A_{IN}–) = 1V and the minimum output code (0000 0000) occurs when A_{IN}+ – (A_{IN}–) = –1V. These differential inputs also have outstanding common mode rejection, so that any noise or unwanted signal that is common to both inputs will be rejected. However, the inputs need not be driven differentially to achieve good performance. If a differential signal is present, the differential inputs can be connected directly. If the input signal is single ended, there is no need for a complicated transformer to create a differential signal; the LTC1406 will handle a single-ended signal as easily as a differential signal. The A_{IN}– input can be tied to a common mode voltage and A_{IN}+ becomes the signal input, with a ±1V span centered around A_{IN}–. Again, to simplify the hookup A_{IN}– can be connected to V_{REF} resulting in an input span of 1.5V–3.5V as shown in Figure 2a.

Rail-to-Rail Common Mode

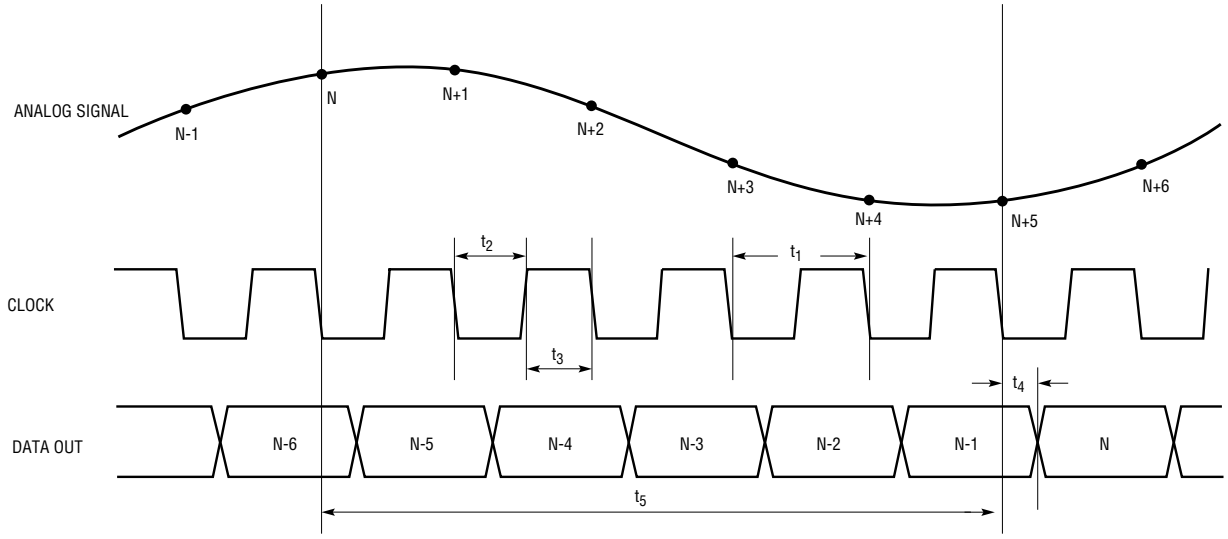
Another nice feature of the LTC1406 input structure is that the inputs have a common mode range that extends to either rail. In single-ended mode, the 2V input span can extend from 0V–2V to 3V–5V. The ±1V differential-input span can also extend between the rails. This allows for direct coupling to a wide range of inputs without any additional circuitry. In addition, the input can be AC coupled to allow for a 2V input span centered around virtually any common mode voltage (see Figure 2b).

Keys to Using High Speed ADCs

The LTC1406 uses an internal sample-and-hold and a pipeline quantizing architecture to convert an analog signal to an 8-bit parallel output. The input is sampled on the falling clock edge, converted into an internal differential voltage and fed into a comparator to determine the most significant bit. The result of that decision is subtracted from the sample and the residue is multiplied by two and then passed on to the next stage via a similar sample-and-hold. This continues down the eight pipeline stages. The comparator outputs are then combined in a digital error-correction circuit into an 8-bit parallel word. Figure 3 is a block diagram of the LTC1406.

The one-bit-per-stage pipeline architecture of the LTC1406 is very similar to the half-flash or subranging architecture (sometimes also referred to as pipeline, the difference being the number of bits determined in each comparator cycle) used in other 8-bit, 20MHz converters. However, if you are more familiar with the successive approximation register (SAR) architecture used in many lower speed, higher resolution converters (including most of Linear Technology's converters), there are some things you need to know about high speed ADCs.

Almost all high speed converters have latency in the output data. This is defined as the delay, usually expressed as a number of clock cycles, from the sampling of the analog input to the appearance of the conversion data on the digital outputs. The most common architecture for 8-bit, 20MHz converters, the half-flash, typically has a delay of 2.5 clock cycles. The



		MIN	TYP	UNITS
t_1	CLOCK PERIOD	50		ns
t_2	PULSE WIDTH LOW	25		ns
t_3	PULSE WIDTH HIGH	25		ns
t_4	OUTPUT DELAY		15	ns
t_5	DATA LATENCY		5	CYCLES

Figure 4. As with all pipeline ADCs, there is latency in the output data. Output data is available from the LTC1406 5 cycles after the input is sampled and the conversion starts.

data latency of the LTC1406, as well as other 8-bit, one-bit-per-stage, pipeline converters, is five clock cycles. Each falling clock edge samples the input and starts a conversion. The digital representation of that sample will be available as an 8-bit parallel word following the fifth falling edge after the start of conversion. So although each conversion takes five clock cycles, a new conversion result is available on each falling edge. Figure 4 clearly illustrates the relationship between the sampled analog input and when the output data is available.

Another important consideration when using a high speed converter is the sampling clock. Most high speed converters use both phases of the clock, so it is critical to maintain a 50% duty cycle. During each clock phase, half of the stages of the ADC are sampling and half are amplifying. At conversion speeds below the maximum conversion rate, the duty cycle can deviate from 50% with no degradation in performance. At the maximum conversion rate it is important to maintain a 50% duty cycle clock. It is also important to provide a clock that has low jitter and fast rise and fall times (<2ns).

Finally, much of the internal circuitry operates dynamically, resulting in two important consequences. First, as with most high speed ADCs, there is a lower limit on the conversion speed. The minimum conversion speed of the LTC1406 is 10kHz. Second, some high speed ADCs, including the LTC1406, are dynamically biased and the bias must be periodically refreshed. Under normal, free-running conversion conditions, the bias is refreshed during each clock cycle. However, when power is first applied or the clock stops for longer than 100µs (for example, in Shutdown mode), the part must typically be clocked for 20 clock cycles at a sample rate of greater than 10kHz before the output data will be valid.

Easy, Clean, Small Layout

One of the reasons that high speed converters can de difficult to use is that the board layout becomes extremely critical for high input frequencies. The layout in Figure 5 shows how easy it is to get a clean, tight layout using the LTC1406 even when connecting the output logic to the digital supply and ground—it's almost automatic. It also illustrates the advantage of the tiny GN-24 package relative to the standard SO-24. The pinout is designed for a smooth flow from analog input signal to digital output. All of the supplies, reference, and analog inputs are located on one side of the part and the clock input and digital data outputs are on the other. This allows for easy separation of the analog and digital ground planes and helps to prevent digital noise from coupling into the analog inputs. As mentioned earlier, the LTC1406 requires very few external components and the pinout is designed to allow the bypass capacitors to be located very close to the package. This close bypassing minimizes lead inductance and sensitivity to currents flowing in the ground plane, which can be critical when the whole system is clocking at 20MHz.

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The LT1167: Precision, Low Cost, Low Power Instrumentation Amplifier Requires a Single Gain-Set Resistor

by Alexander Strong

Introduction

The LT1167 is the next-generation instrumentation amplifier designed to replace the previous generation of monolithic instrumentation amps, as well as discrete, multiple op amp solutions. Instrumentation amplifiers differ from operational amplifiers in that they can amplify input signals that are not ground referenced. The output of an instrumentation amplifier is referenced to an external voltage that is independent of the input. Conversely, the output voltage of an op amp, due to the nature of its feedback, is referenced to the differential and common mode input voltage.

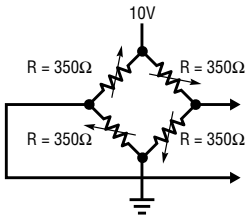
A separate ground reference and the high CMRR of the LT1167 instrumentation amplifier reduce the effect of the input common mode voltage on the output signal. The closed-loop gain of an op amp and of most instrumentation amps is set by a resistor ratio; the gain of the LT1167 is set by the absolute value of one external resistor. Gain error depends on the ratio of one external resistor to the value of the LT1167's internal, laser-trimmed resistors, which are trimmed to better than 0.1%. Once the gain is set, it is expected to remain constant when the output voltage or output current changes. Any change in gain with output swing will show up as gain nonlinearity.

Parameters such as gain error, voltage offset and CMRR are a function of trimming. Gain nonlinearity cannot be trimmed; it is a function of careful design and die layout. The use of common centroid geometries and isothermal layout cancels the errors due to die stress and thermal gradients. If this is not done correctly, all the trimming in the world will not improve performance.

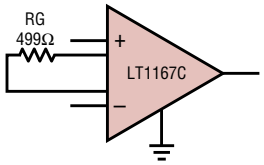
Input Protection

Instrumentation amplifiers must survive in a hostile environment. Not only does the LT1167 have to endure ESD during handling (power off) but it must also survive excessive voltage during operation. The inputs of the LT1167 have low leakage internal diodes from each input to the supplies. These diodes have a maximum current rating of 20mA and protect the IC when the input voltage exceeds the supply rails. Precision and indestructibility are combined when an external 20k resistor is placed in series with each input. There is little offset voltage penalty because the 320pA offset current from the LT1167 multiplied by the 20k input resistors contributes only 6.4µV additional offset. With the 20k resistors, the LT1167 can handle both ±400VDC input faults and ESD spikes over 4kV. This meets the IEC 1004-2 level 2 European standard.

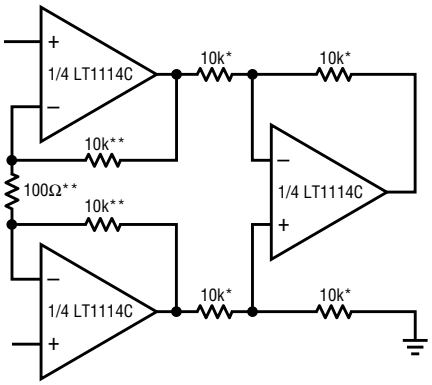
The low noise voltage of 7.5nV$\sqrt{Hz}$ is achieved by idling a large portion of the 0.9mA supply current in the input stage. Input bias current is not compromised due to the use of superbeta transistors, current-cancellation circuitry and trimming. The LT1167's input bias current is better than that of a JFET input stage at only 350pA maximum at room temperature; it does not double for every 10°C. The LT1167 is also trimmed for critical DC parameters, such as input offset voltage and CMRR. These trims allow the amplifier to achieve very high DC accuracy; total input-referred offset voltage is only 60µV and CMRR is better than 110dB at a gain of ten. Worst-case input offset is at a gain of one; it is guaranteed to be less than 240µV for the prime grade. The LT1167 is offered in 8-pin PDIP and SO packages, saving significant board space compared to discrete designs. With these advantages, the LT1167 will easily find its way into many applications.



PRECISION BRIDGE TRANSDUCER



LT1167 MONOLITHIC
INSTRUMENTATION AMPLIFIER, G = 100
SUPPLY CURRENT = 1.3mA MAX



"ROLL YOUR OWN" INSTRUMENTATION AMP, G = 100
*0.02% RESISTOR MATCH, 3PPM/°C TRACKING
**DISCRETE 1%RESISTOR, 100PPM/°C TRACKING
SUPPLY CURRENT = 1.35mA FOR THREE AMPLIFIERS

Figure 1. "Roll your own" vs LT1167

Table 1a. "Roll your own" vs LT1167 error budget

Error Source	LT1167 Circuit Calculations	"Roll Your Own" Circuit Calculations	Error (PPM) of Full Scale	
			LT1167	"Roll Your Own"
Absolute Accuracy at T_A = 25° C				
Input Offset Current	$I_{OS} \times R_S/V_{FS}$	$I_{OS} \times R_S/V_{FS}$	4	4
Input Offset Voltage	V_{OSI}/V_{FS}	$\Delta V_{OS}/V_{FS}$	3000	6500
Output Offset Voltage	$V_{OSO}/G/V_{FS}$	$V_{OS} \times NG/G/V_{FS}$	150	75
CMRR	$CMRR \times V_{CM}/V_{FS}$	$RM \times V_{CM}/G/V_{FS}$	790	500
Total Absolute Error			3944	7079
Drift to 85° C				
Input Offset Voltage Drift	$TCV_{OSI} \times \Delta T/V_{FS}$	$TC\Delta V_{OS} \times \Delta T/V_{FS}$	1200	5700
Output Offset Voltage Drift	$TCV_{OSO} \times \Delta T/G/V_{FS}$	$TCV_{OS} \times NG \times \Delta T/G/V_{FS}$	180	78
Gain Drift	$(TCG + TCR) \times \Delta T$	$TCRM \times \Delta T$	3,600	6000
Total Drift Error			4980	11,778
Resolution				
Gain Nonlinearity	GNL	RNL	15	10
Typical 0.1Hz–10Hz Voltage Noise	e_n/V_{FS}	$e_n \times \sqrt{2}/V_{FS}$	14	21
Total Resolution Error			29	31
Grand Total Error			8953	18,888

"Roll Your Own"—Discrete vs Monolithic LT1167 Error Budget Analysis

The LT1167 offers performance superior to that of "roll your own," three–op amp discrete designs. A typical application that amplifies and buffers a bridge transducer's differential output is shown in Figure 1. The amplifier, with its gain set to one hundred, amplifies a differential, full-scale output voltage of 20mV over the industrial temperature range. The discrete instrumentation amp uses the best precision, low power, superbeta quad op amp available, the LT1114. This comparison demonstrates that the LT1167 outperforms a discrete instrumentation amplifier using a state-of-the-art op amp. The error budget comparison in Table 1 shows how various errors are calculated and referenced to the bridge's full-scale output of 20mV. The table shows that some of the greatest differences in error between the LT1167 and the discrete solution are input offset voltage, input offset voltage drift and CMRR. Expensive precision resistor arrays that can deliver 0.02%

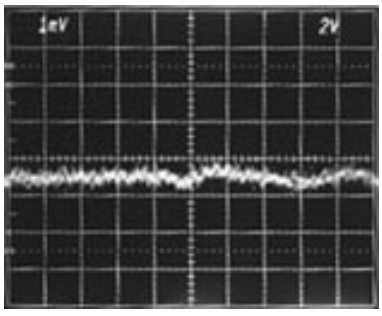


Figure 2. LT1167 gain nonlinearity: R_C = 1k; V_O = ±10V

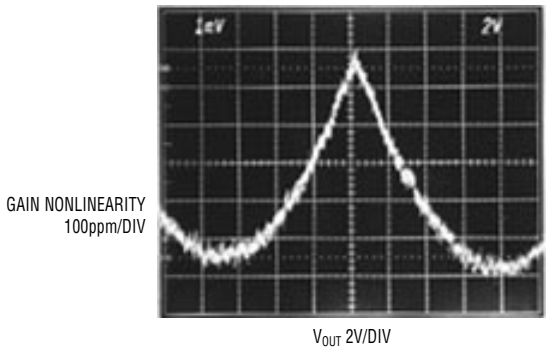


Figure 3. Gain nonlinearity of a previous generation instrumentation amp: R_C = 1k; V_O = ±10V

matching are required to match the LT1167's CMRR performance. The total error for the LT1167 solution is much lower than that of the discrete solution. The LT1167 has other advantages over a discrete design, including lower power dissipation, lower component cost and smaller size. The clear advantage goes to the LT1167.

LT1167 vs the Competition

What was said about the LT1167 when compared to discrete solutions is also applicable to previous IC instrumentation amplifiers. Improvements in circuit design and common centroid layout greatly enhance the CMRR, PSRR, gain error and nonlinearity over competitive IC solutions. The LT1167 has a 10dB improvement for CMRR and a 20dB improvement in PSRR for the worst-case condition of unity gain. Gain error is better than 0.1% for all gains up to one hundred, which is a 2.5× to 5× improvement over previous ICs. This gain error is maintained even when the output has to drive heavy loads, thanks to improvements in common centroid layout. The LT1167 maintains excellent performance even when driving heavy loads. Figure 2 is a photo of the LT1167 in a gain of one thousand driving a 1k load. Figure 3 is a previous generation IC instrumentation amplifier in the same condition. You can see why a 10k load resister and not a 1k resistor was specified for older ICs.

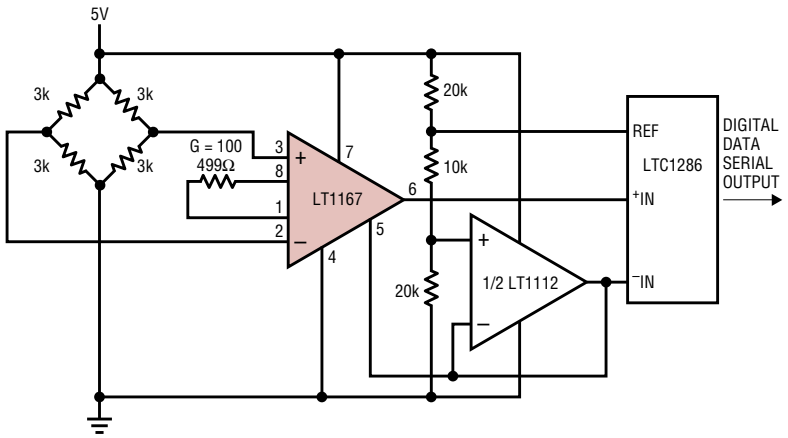


Figure 4. Single-supply pressure monitor

Table 1b. Terms used in Table 1a

Term	LT1167 Spec	LT1114C Spec	Comment
I_{OS}	450pA	500pA	Input Offset Current
R_S	350Ω/2	350Ω/2	Source Resistance
V_{FS}	20mV	20mV	Full-Scale Input Voltage
V_{OSI}	60µV	N/A	Input Offset Voltage
ΔV_{OS}	N/A	130µV	Input Offset Voltage Match
V_{OSO}	300µV	N/A	Output Offset Voltage
V_{OS}	N/A	75µV	Offset Voltage
NG	N/A	2V/V	Noise Gain of Output Op Amp
G	100V/V	100V/V	Gain
CMRR	110dB (3.16ppm)	N/A	Common Mode Rejection Ratio
V_{CM}	5V	5V	Common Mode Voltage
RM	NA	0.02%	Resistor Match
TCV_{OSI}	0.4V/°C	N/A	Temperature Coefficient of Input Offset Voltage
ΔT	60°C	60°C	Change in Temperature
$TC\Delta V_{OS}$	N/A	1.9µV/°C	Temperature Coefficient of Offset Voltage Match
TCV_{OSO}	6µV/°C	N/A	Temperature Coefficient of Output Offset Voltage
TCV_{OS}	N/A	1.3µV/°C	Temperature Coefficient of Offset Voltage
TCG	50ppm/°C	N/A	Temperature Coefficient of Gain
TCR	10ppm/°C	N/A	Temperature Coefficient of Resistance
TCRM	N/A	100ppm/°C	Temperature Coefficient of Resistor Match
GNL	15ppm	N/A	Gain Nonlinearity
RNL	N/A	10ppm	Resistor Nonlinearity
e_n	$0.28\mu V_{P-P}$	$0.3\mu V_{P-P}$	0.1Hz–10Hz Voltage Noise

Low I_B Favors High Impedance Bridges, Lowers Dissipation

The LT1167's low supply current, low supply voltage operation and low input bias current (350pA max) allow it to fit nicely into battery powered applications. Low overall power dissipation necessitates using higher impedance bridges. Figure 4 shows the LT1167 connected to a 3kΩ bridge's differential output. The bridge's impedance is almost an order of magnitude higher than that of the bridge used in the error-budget table. The picoampere input bias currents will still keep the error caused by offset current to a negligible level. The LT1112 level shifts the LT1167's reference pin and the ADC's analog ground pins above ground. This is necessary in single-supply applications because the output cannot swing to ground. The LT1167's and LT1112's

combined power dissipation is still less than the bridge's. This circuit's total supply current is just 3mA.

ADC Signal Conditioning

The LT1167 is shown in Figure 5 changing a differential signal into a single-ended signal. The single-ended signal is then filtered with a passive 1st order RC lowpass filter and applied to the LTC1400 12-bit analog-to-digital converter (ADC). The LT1167's output stage can easily drive the ADC's small nominal input capacitance, preserving signal integrity. Figure 6 shows two FFTs of the amplifier/ADC's output. Figures 6a and 6b show the results of operating the LT1167 at unity gain and a gain of ten, respectively. This results in a typical SINAD of 70.6dB.

Current Source

Figure 7 shows a simple, accurate, low power programmable current source. The differential voltage across pins 2 and 3 is mirrored across R_G. The voltage across R_G is amplified and applied across R1, defining the output current. The 50µA bias current flowing from pin 5 is buffered by the LT1464 JFET operational amplifier, which increases the resolution of the current source to 3pA.

Nerve-Impulse Amplifier

The LT1167's low current noise makes it ideal for ECG monitors that have MΩ source impedances. Demonstrating the LT1167's ability to amplify low level signals, the circuit in Figure 8 takes advantage of the amplifier's high gain and low noise operation. This circuit amplifies the low level nerve impulse signals received from a patient at pins 2 and 3 of the LT1167. R_G and the parallel combination of R3 and R4 set a gain of ten. The potential on LT1112's pin 1 creates a ground for the common mode signal. The LT1167's high CMRR of 110db ensures that the desired differential signal is amplified and unwanted common mode signals are attenuated. Since the DC portion of the signal is not important, R6 and C2 make up a 0.3Hz highpass filter. The AC signal at LT1112's pin 5 is amplified by a gain of 101 set by R7/R8 + 1. The parallel combination of C3 and R7 forms a lowpass filter that decreases this gain at frequencies above 1kHz.

The ability to operate at ±3V on 0.9mA of supply current makes the LT1167 ideal for battery-powered applications. Total supply current for this application is 1.7mA. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

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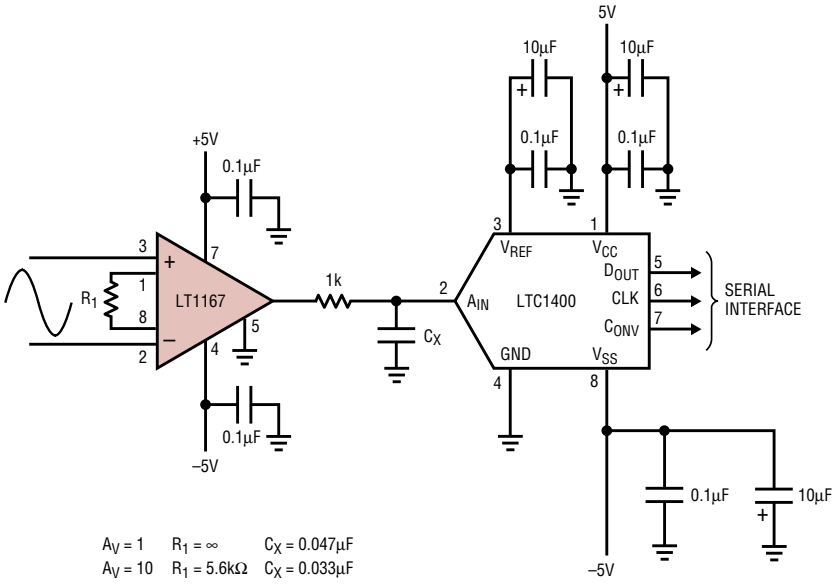

Figure 5. The LT1167 converting differential signals to single-ended signals; the LT1167 is ideal for driving the LTC1400.

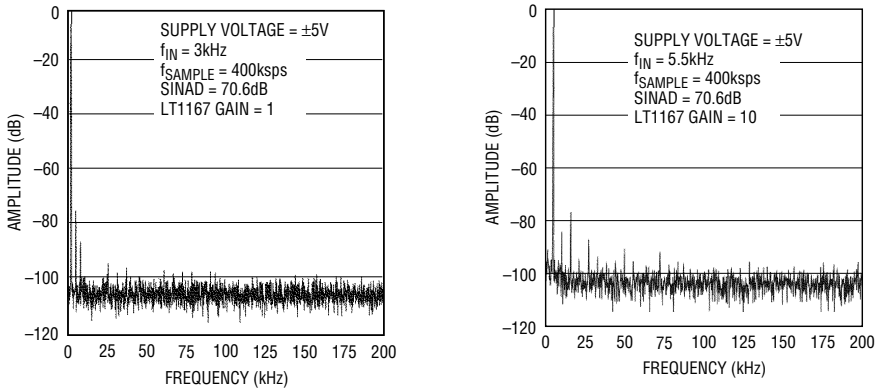

Figure 6. Operating at a gain of one (left) or ten (right), Figure 5's circuit achieves 12-bit operation with a SINAD of 70.6dB

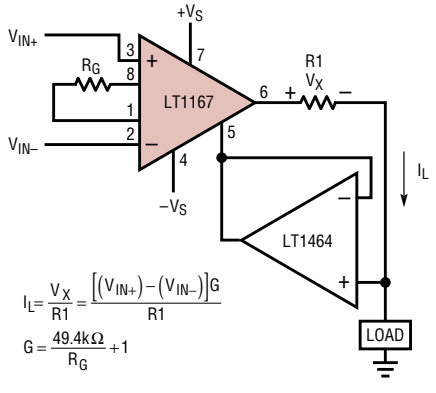

Figure 7. Precision current source

200µA, 1.2MHz Rail-to-Rail Op Amps Have Over-The-Top Inputs

by Raj Ramchandani

Introduction

The LT1638 is Linear Technology's latest general-purpose, low power, dual rail-to-rail operational amplifier; the LT1639 is a quad version. The circuit topology of the LT1638 is based on Linear Technology's popular LT1490/LT1491 op amps, with substantial improvements in speed. The LT1638 is five times faster than the LT1490. The LT1638/LT1639 are "tough" op amps, with a variety of features that make them ideal for general-purpose applications. A unique input stage allows the LT1638 to be operated with input common mode voltages up to 44V above the negative rail. The LT1638 dual and LT1639 quad op amps operate on all single and split supplies with a total voltage of 2.5V to 44V. These amplifiers are reverse-battery protected and draw no current for reverse supplies up to 18V. For single 5V supply operation, typical specifications include 200µV input offset voltage, 15nA input bias current, 1nA input offset current, open-loop voltage gain of 1500V/mV, 0.4V/µs slew rate, 98dB common mode rejection ratio and 100dB power supply rejection ratio. The output can swing within 30mV of the positive rail and within 5mV of the negative rail with no load. The gain-bandwidth product is 1.2MHz and the part is stable with capacitive loads up to 200pF under all loading conditions. Additional performance specifications are shown in Table 1.

The LT1638 dual is available with industry standard pinout in 8-pin MSOP, SO and miniDIP packages. The LT1639 quad is available with industry-standard pinout in 14-pin SO and 14-pin miniDIP packages.

Input-Stage Architecture

The input stage of the LT1638 is shown in Figure 1. Like the LT1490 rail-to-rail op amp, the LT1638 uses two input stages to achieve rail-to-rail capability. Device Q7 controls which stage is active by steering the tail current between the two stages as a function of input common mode voltage. The LT1638 has three modes of operation. For input common mode voltages between V_{EE} and (V_{CC} – 1V), the PNP stage (Q5–Q6) is active and Q7 and the NPN stage (Q1–Q4) are off. Since Q7 is off , the entire 10µA of tail current will flow through the PNP stage (Q5–Q6). The input bias current is the base current of Q5 or Q6, typically 15nA, as shown in Figure 2. The input offset voltage for this stage is trimmed to less then 300µV. As the input common mode voltage is increased above V_{CC} – 1V, Q7 turns on, diverting the tail current from the PNP stage to the NPN stage. When the PNP stage is completely off, the 10µA tail current will flow through the current mirror D3–Q8. The 10µA current through Q8 sets the bias for the NPN input stage. In the NPN stage, Q1 and Q2 serve as emitter followers, driving the differential pair formed by Q3 and Q4. Further increases in the common mode voltage will cause Q1 and Q2 to saturate due to the forward voltage of D1 and D2. This will cause the input bias current to increase, as shown in Figure 2. At $V_{CM} = V_{CC}$ the input bias current is typically 1µA and the untrimmed input offset voltage is typically 600µV. As Figure 2 shows, when $V_{CM} = V_{CC}$ the NPN input stage is beginning to saturate but is not yet fully saturated. When V_{CM} is approximately 200mV above V_{CC}, the Schottky diodes will reverse bias, causing Q1 and Q2 to fully saturate. The Schottkys, in combination with the input devices Q1 and Q2, will cause Q1's and Q2's base current to equal their

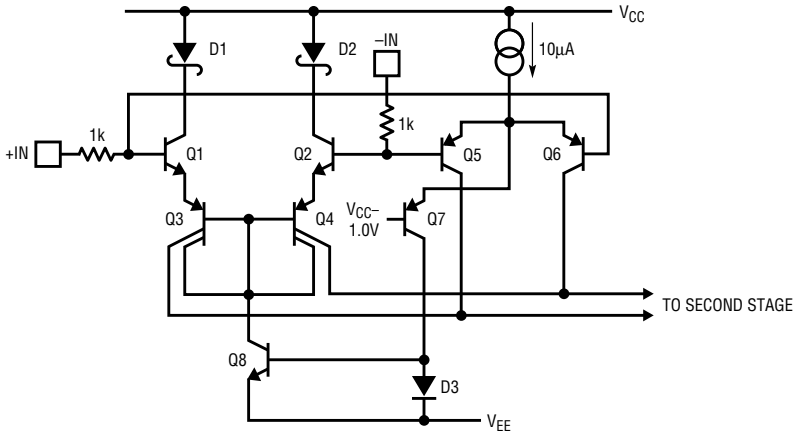

Figure 1. LT1638 input stage

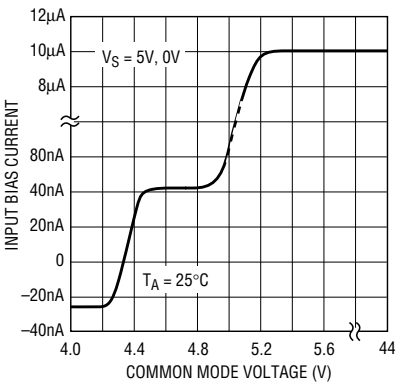

Figure 2. Input bias current vs common mode voltage

Table 1. LT1638/LT1639 typical DC performance, 25°C

Parameter	Conditions	V_S = 3V	V_S = 5V	V_S = ±15V
Offset Voltage	$V_{CM} = V_{EE}$ to (V_{CC} – 1V)	200µV	200µV	200µV
	$V_{CM} = V_{EE}$ + 44V	600µV	600µV	600µV
Input Bias Current	$V_{CM} = V_{EE}$ to (V_{CC} – 1V)	15nA	15nA	15nA
	$V_{CM} = V_{EE}$ + 44V	10µA	10µA	10µA
Input Offset Current	$V_{CM} = V_{EE}$ to (V_{CC} – 1V)	1nA	1nA	1nA
	$V_{CM} = V_{EE}$ + 44V	200nA	200nA	200nA
CMRR	$V_{CM} = V_{EE}$ to (V_{CC} – 1V)	98dB	98dB	98dB
	$V_{CM} = V_{EE}$ + 44V	88dB	88dB	88dB
Open-Loop Gain	R_L = 10k	1500k	1500k	500k
Output Voltage (Low)	No Load	5mV	5mV	–14.995V
	I_{SINK} = 10mA	500mV	500mV	–14.5V
Output Voltage (High)	No Load	2.965V	4.965V	14.965V
	I_{SOURCE} = 10mA	2.6V	4.6V	14.6V
Output Current	Source	15mA	25mA	40mA
	Sink	25mA	25mA	40mA
Supply Current per Amp		190µA	190µA	240µA

emitter current when the input stage is saturated, typically 10µA. The device can operate with the input common mode as high as 44V above the negative rail. The input offset voltage for this mode of operation is typically 600µV.

Reverse-Battery Protection

The LT1638 and LT1639 can withstand typical reverse supply voltages of 40V and are guaranteed to withstand reverse supply voltages up to 18V. The input stage incorporates phase-reversal protection to prevent the output from phase reversing when the input is forced up to 22V below the negative supply. Input-protection resistors also limit the current from becoming excessive when the input is forced up to this extreme.

An Over-The-Top Application

The battery-current monitor shown in Figure 3 demonstrates the LT1638's ability to operate with its inputs above the positive rail. In this application, a conventional amplifier would be limited to a battery voltage between 5V and ground, but the LT1638 can handle battery voltages as high as 44V. The LT1638 can be shut down by removing V_{CC}. With V_{CC} removed, the input leakage is less then 0.1nA. No damage to the LT1639 will result from inserting the 12V battery backward.

When the battery is charging, amplifier B senses the voltage drop across R_S. The output of amplifier B causes Q_B to drain sufficient current through R_B to balance the inputs of amplifier B. Likewise, amplifier A and Q_A form a closed loop when the battery is discharging. The current through Q_A or Q_B is proportional to the current in R_S. This current flows into R_G and is converted into a voltage. Amplifier D buffers and amplifies the voltage across R_G. Amplifier C compares the outputs of amplifier A and amplifier B to determine the polarity of current through R_S. The scale factor for V_{OUT} with S1 open is 1V/A. With S1 closed the scale factor is 1V/100mA and currents as low as 5mA can be measured.

Conclusion

The LT1638 is an ideal candidate for general purpose op amp applications. With its Over-The-Top capability, reverse-battery protection and rail-to-rail input and output features, the LT1638/LT1639 is suitable for multiple applications.

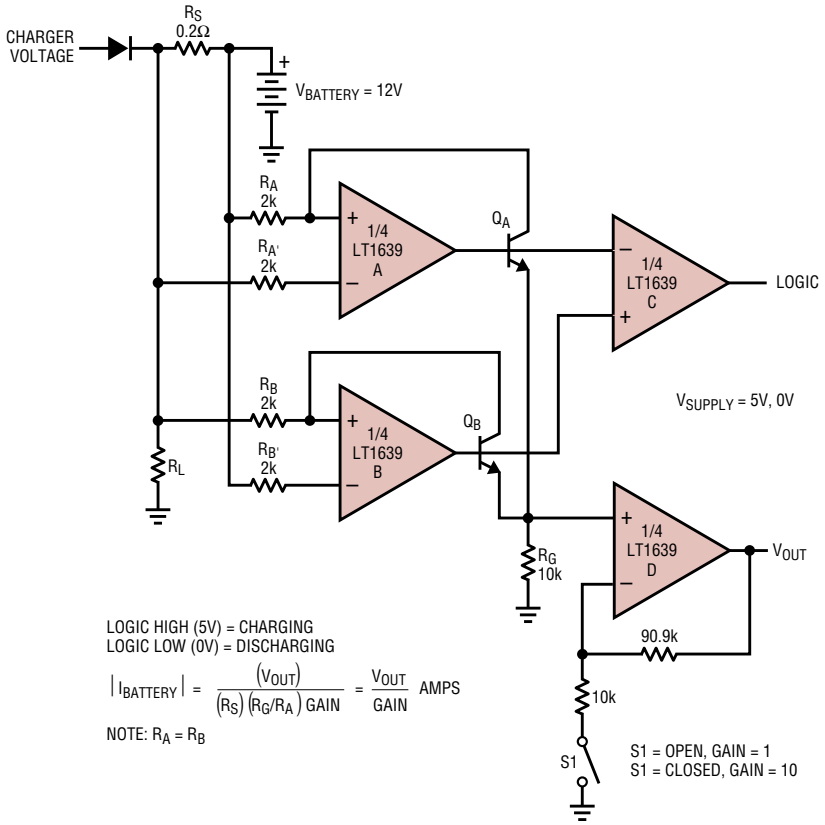

Figure 3. LT1638 battery current monitor—an Over-The-Top application

LTC1710: Two 0.4Ω Switches with SMBus Control Fit into Tiny MSOP-8 Package

by Peter Guan

Introduction

The LTC1710 SMBus dual switch is a complete solution for supplying power to portable-equipment peripherals without the need for external switches. Two internal high-side N-channel switches, each capable of delivering 300mA at an $R_{DS(ON)}$ of 0.4Ω, are available in the tiny MSOP-8 package. With a low standby current of 14µA, the LTC1710 operates on an input voltage of 2.7V to 5.5V while maintaining the SMBus-specified 0.6V V_{IL} and 1.4V V_{IH} input thresholds.

Figure 1 shows a typical application of the LTC1710 switching two different SMBus peripherals. Figure 2 shows a block diagram of the LTC1710 architecture, which can be broken down into four basic building blocks: the two N-channel power MOSFETs, the regulated charge-pump driver, the power-on reset and undervoltage-lockout units and the SMBus interface components.

Two 0.4Ω Switches in MSOP-8

To fully enhance the power switches, the LTC1710 uses a charge-pump tripler to boost and regulate the gate drive of each switch. Running at about 300kHz, each charge pump is programmed to supply a ramped voltage to the gate of the switch, so that it turns on slowly and smoothly, avoiding large current spikes into the load. Since the charge pumps drive only the gates of the switches, only a small amount of current is needed; hence, the charge-pump caps are integrated on the IC.

The drains of the two N-channel switches are independent of each other. Switch 1's drain is connected to V_{CC}, but the potential of switch 0's drain can be anywhere between V_{CC} and GND. As a result, SMBus peripherals requiring different input voltages can be simultaneously switched by the LTC1710 (Figure 3).

Though unlikely in normal operating conditions, if the internal switches become extremely hot as a result of sourcing too much output current, an internal thermal shutdown circuit becomes active at around 120°C and turns off the switch outputs temporarily until the temperature drops by about 15°C.

Power-On Reset and Undervoltage Lockout

To ensure that the LTC1710 starts up with both switches off, an internal power-on reset (POR) signal inhibits operation until about 300µs after V_{CC} crosses the undervoltage lockout threshold (UVLO, typically 2V). The circuit also includes some hysteresis and delay to avoid nuisance resets. Once operation begins, V_{CC} must drop below the UVLO threshold for at least 100µs to trigger another POR sequence.

Three-State Programmable Address Pin

To identify itself on the SMBus, the LTC1710 has a three-state programmable address pin (AD1) that can be tied directly to V_{CC}, to GND or to $V_{CC}/2$ with the help of two 1M resistors. To conserve standby current, it's preferable to tie the address pin to either V_{CC} or GND. The third state of $V_{CC}/2$ should be used only when more than two addresses are needed on the bus. The three available addresses are 1011000 (AD1 = GND), 1011010 (AD1 = V_{CC}) and 1011001 (AD1 = $V_{CC}/2$). Notice that the five MSBs of the LTC1710 addresses are hardwired to 10110XX, which, according to the SMBus specifications, places the LTC1710 directly in the reserved address range for power-plane switching.

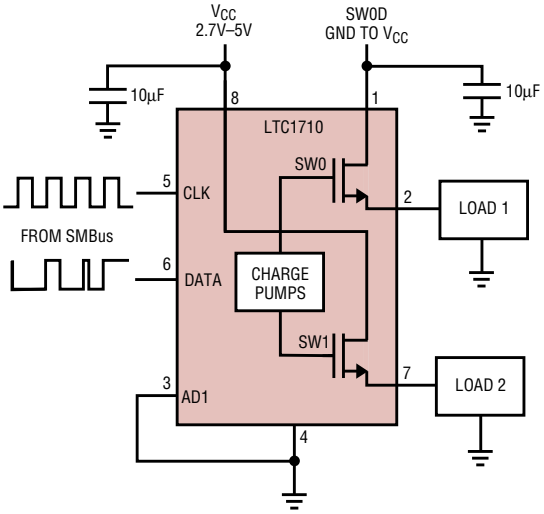

Figure 1. Typical application: the LTC1710 switches two SMBus peripherals.

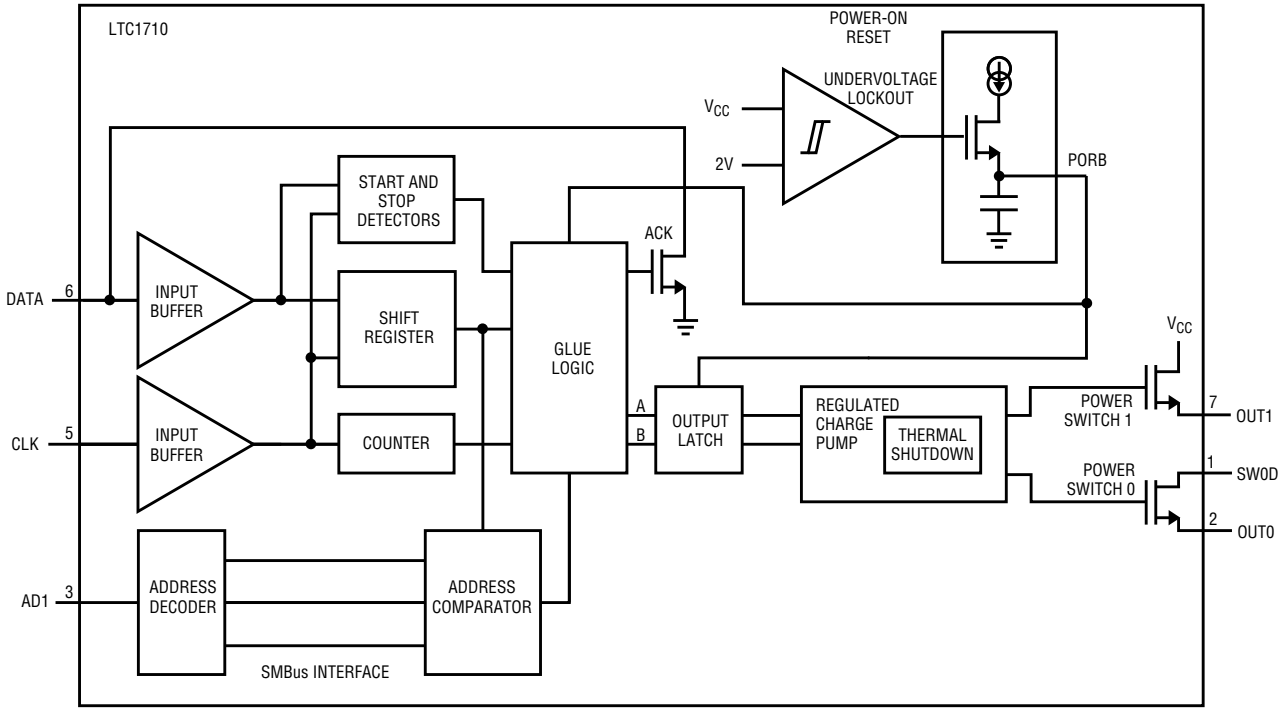

Figure 2. LTC1710 block diagram

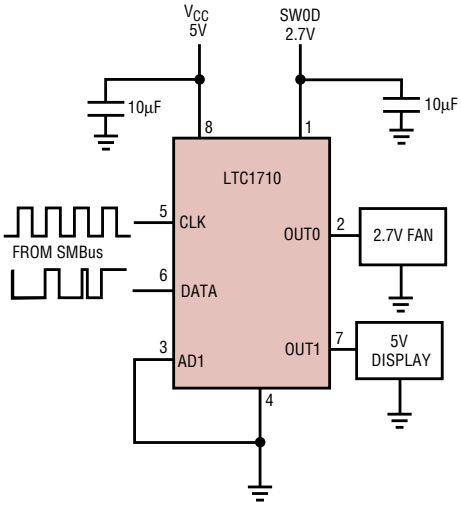

Figure 3. The LTC1710 switches two SMBus peripherals with different input voltages.

SMBus Operation

The SMBus is a serial bus interface that uses only two bus lines, DATA and CLK, to control low power peripheral devices in portable equipment. The LTC1710 is a slave-only device that uses the Send Byte protocol of the SMBus for communication. The master of the bus initiates communication to its slave devices with the Start signal, which is the switching of the DATA line from high to low while CLK is high. Upon detecting this Start signal, all slave devices on the bus, including the LTC1710, wake up and get ready to shift in the data that will follow. Beginning on the next rising CLK edge, the master sends out the first byte. The first seven bits of this byte consist of the address of the slave with which the master wishes to communicate. The last bit indicates whether the following command will be a read (logic one) or write (logic zero). Since the LTC1710 is a slave device that can only be written to by a master, it will ignore the read command, even if the address matches. If the first byte does match, then the LTC1710 will acknowledge proper reception to the master by pulling the DATA line low during the next CLK cycle. The master then sends the command byte with its two LSBs as the controlling signal for the switch outputs. A logic one turns on the internal charge pump to drive up the gate voltage and the output. A logic zero shuts down the charge pump and discharges the output to zero. After reception of the second byte, the LTC1710 again acknowledges the master by pulling DATA low for the next CLK cycle. At this point, valid data is shifted into the output latch of the LTC1710. However, the output switch won't be enabled until the Stop signal (DATA going from low to high while CLK is high) is detected. With this double buffering feature of

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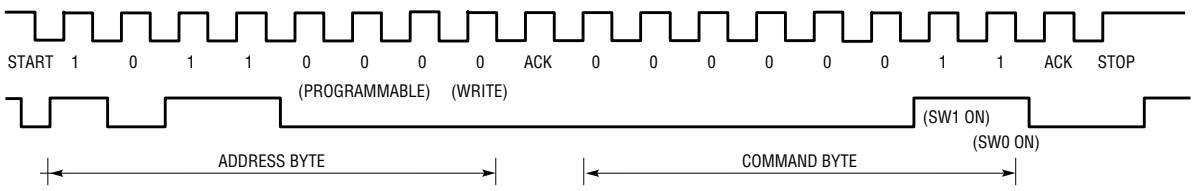


Figure 4. SMBus Send Byte protocol

Low Distortion Rail-to-Rail Op Amps Have 0.003% THD with 100kHz Signal

by Danh Tran

Introduction

The LT1630/LT1632 duals and LT1631/LT1633 quads are the newest members of Linear Technology's family of rail-to-rail op amps, which provide the best combination of AC performance and DC precision over the widest range of supply voltages. The LT1630/LT1631 deliver a 30MHz gain-bandwidth product, a 10V/µs slew rate and 6nV/√Hz input-voltage noise. Optimized for higher speed applications, the LT1632/LT1633 have a 45MHz gain-bandwidth product, a 45V/µs slew rate and 12nV/√Hz input voltage noise. In a low supply environment, these op amps maximize system dynamic range and precision. The very large open loop gain of these devices (a few million) virtually eliminates gain error. Because input offset error is so important on low supplies, it is guaranteed over the whole rail-to-rail input range. To achieve this, these amplifiers use an LTC proprietary trim algorithm to minimize the input offset at two common mode voltages, one at the negative supply and the other at the positive supply. To make designing with these amplifiers straightforward, their performance is fully specified for 3V, 5V and ±15V supplies.

Device Characteristics

The LT1630/LT1631 have a gain-bandwidth product of 30MHz, a 10V/µs slew rate and a low input noise voltage of 6nV/√Hz. With a 4.1mA typical supply current per amplifier, the LT1630/LT1631 can sink or source currents in excess of 50mA on a ±15V supply, allowing them to drive low impedance loads. Input offset voltage with a 5V supply is specified at 525µV maximum over the entire input range; a minimum open loop gain of 500,000 ensures a very small gain error. To maximize common mode rejection, the LT1630/LT1631 also employ a patented trim technique that keeps the input offset shift to less than 525µV when the input common mode voltage is varied from rail-to-rail. The output can swing to within 40mV to either rail while providing 0.5mA output current. Furthermore, the device's characteristics change very little over the supply range of 3V to ±15V: the worst-case supply rejection is 87dB and the typical gain-bandwidth product is constant at 30MHz. The LT1630/LT1631 have only 0.003% THD with a 100kHz signal while operating on a low supply voltage, as shown in Figure 1.

Optimized for higher frequency and slew rate applications, the LT1632/LT1633 deliver a gain-bandwidth product of 45MHz, a slew rate of 45V/µs and an input voltage noise of 12nV/√Hz. These devices consume 4.6mA of supply current per amplifier and have a short-circuit current of 70mA operating on a ±15V supply. The input offset voltage is guaranteed to be less than 1350µV over the whole input range and the open loop gain is specified to be greater than 450,000 on a 5V supply. Also, using the proprietary trim technique, the LT1632/LT1633 is guaranteed to have an input-offset shift of less than 1500µV when the input common mode voltage is varied from rail-to-rail. Like the LT1630/LT1631, the LT1632/LT1633's characteristics don't change much over the specified supply range of 3V to ±15V. Figure 2 illustrates the large-signal response of LT1632 with various loads for a 5V supply. Figure 3 shows the harmonic distortion of LT1632 with a 1.25MHz sinusoidal signal. Table 1 summarizes the performance of these newest rail-to-rail amplifiers.

The LT1630/LT1632 dual amplifiers are available in either 8-pin SO or 8-pin miniDIP packages. The LT1631/LT1633 quad amplifiers are available in the 14-pin SO.

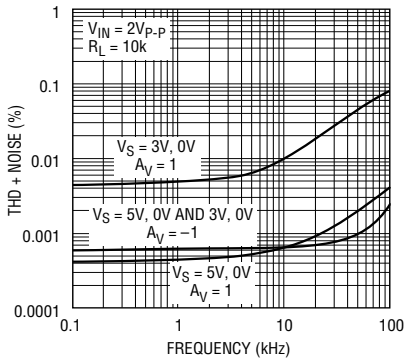


Figure 1. LT1630 total harmonic distortion + noise vs frequency

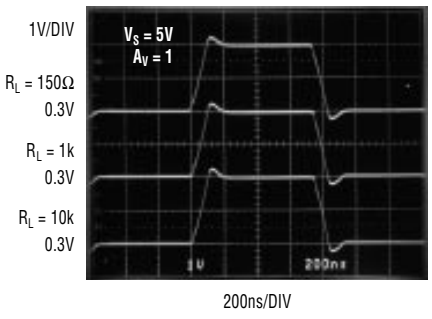


Figure 2. LT1632 large-signal response

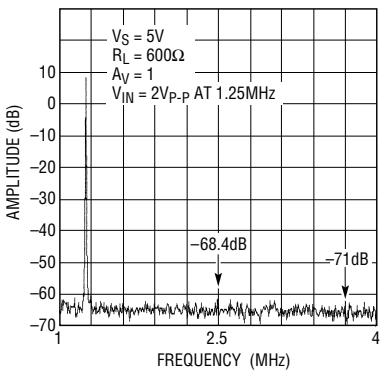


Figure 3. LT1632 harmonic distortion

Table 1. Amplifier characteristics: V_S = 5V, 25°C

Parameter		LT1630/LT1631	LT1632/LT1633	
Gain-Bandwidth Product		30MHz	45MHz	Typ
Slew Rate	V_S = ±15V	10V/µs	45V/µs	Typ
Input Noise Voltage		6nV/√Hz	12nV/√Hz	Typ
Offset Voltage	V_{CM} = V–, V+	<525µV	<1350µV	Max
Offset Voltage Shift	V_{CM} = V–, V+	<525µV	<1500µV	Max
Open Loop Gain	R_L = 10k	500k	450k	Min
Input Bias Current	V_{CM} = V–, V+	1µA	2.2µA	Max
Input Offset Current	V_{CM} = V–, V+	150nA	440nA	Max
Output Voltage Swing to Rail	No Load	15mV	15mV	Typ
	I_O = 20mA	900mV	900mV	Typ
Short-Circuit Current	V_S = 5V	±40mA	±40mA	Typ
	V_S = ±15V	±70mA	±70mA	Typ
Operating Supply Voltage Range		2.7V–30V	2.7V–30V	
Specified Supply Voltages		3V, 5V, ±15V	3V, 5V, ±15V	

The Rail-to-Rail Architecture

Figure 4 shows the simplified schematic of these amplifiers. The circuit is composed of three distinct stages: an input stage, an intermediate stage and an output stage. The input stage consists of two differential amplifiers, a PNP stage (Q1–Q2) and an NPN stage (Q3–Q4), that are active over different portions of the input common mode range. Each input stage is trimmed for minimum offset voltage and maximum common mode rejection. The intermediate stage is a folded cascode configuration formed by Q8–Q12, which provides most of the voltage gain. A pair of complementary common emitter devices, Q14–Q15, creates an output stage which can swing from rail to rail. The amplifiers are fabricated on Linear Technology's proprietary complementary bipolar process, which ensures that the output devices, Q14 and Q15, possess a very similar DC and AC characteristics.

Let's first examine the input stage. Transistor Q5 switches tail current I_1 between the two input stages. When the input common mode voltage, V_{CM}, is between the negative supply and 1.5V below positive supply, Q5 is reverse biased and the PNP differential pair Q1–Q2 is active. As V_{CM} moves further toward the positive supply, Q5 will be forward biased and steer the tail current I_1 through the current mirror Q6–Q7 to activate the NPN differential pair. The PNP pair becomes inactive for the rest of the input common mode range, up to the positive supply. The input stages are protected by a pair of back-to-back diodes D5–D6. When a differential voltage of more than 0.7V is applied to the inputs, these diodes will turn on, preventing the emitter-base breakdown of the input transistors. To prevent the output from reversing polarity when the input voltage exceeds the power supplies, two pairs of crossing diodes, D1–D4, are employed. When the input voltage exceeds either supply by approximately 700mV, D1–D2 or D3–D4 will turn on and force the output to the proper polarity.

The collector currents of the input pairs are combined at the intermediate stage, consisting of Q8–Q12. Most of the voltage gain of the amplifier is generated in this stage. Its output is then buffered and applied to output transistors Q14 and Q15. Capacitors C1 and C2 form local feedback loops at the output stage to lower the output impedance at high frequency.

Applications

The ability to accommodate any input and output signals that fall within the device' s supplies makes these amplifiers very easy to use. They exhibit a very good transient response and can drive low impedance loads, which makes them suitable for high performance applications. The following applications demonstrate the versatility of these amplifiers.

400kHz 4th Order Butterworth Filter for 3V Operation

The circuit shown in Figure 5 makes use of the low voltage operation and the wide bandwidth of the LT1630 to create a 400kHz 4th order lowpass filter with a 3V supply. The amplifiers are configured in the inverting mode for the lowest distortion and the output can swing rail-to-rail for the

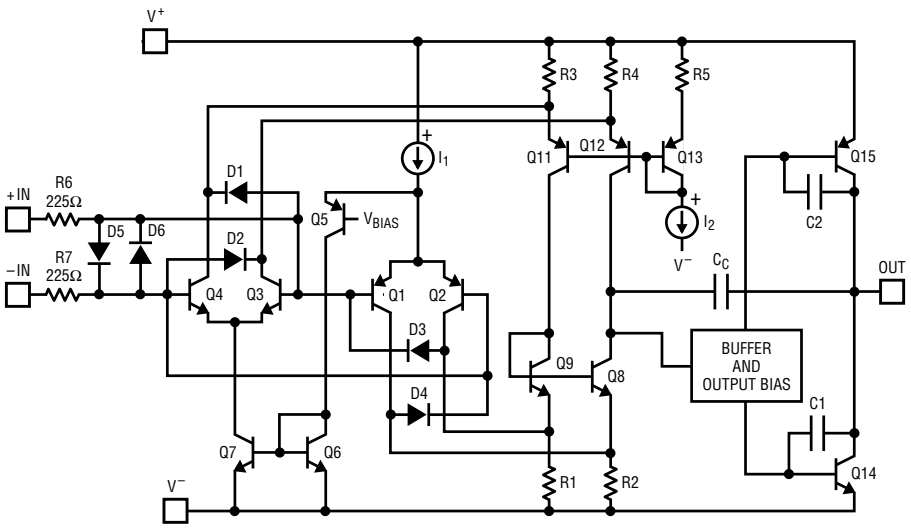


Figure 4. LT1630 simplified schematic

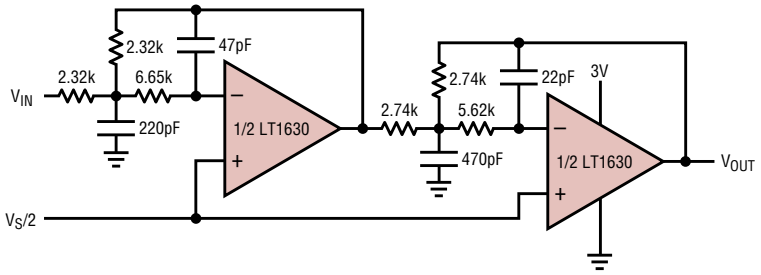


Figure 5. Single-supply, 400kHz, 4th order Butterworth filter

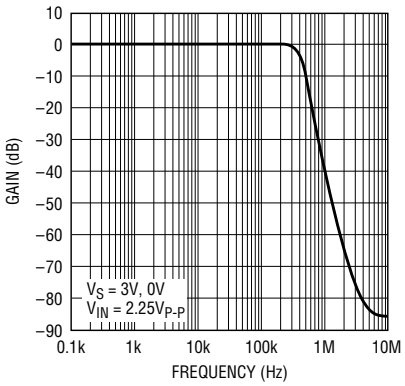


Figure 6. Frequency response of filter in Figure 5

maximum dynamic range. Figure 6 displays the frequency response of the filter. Stopband attenuation is greater than 85dB at 10MHz. With a $2.25V_{P-P}$, 100kHz input signal, the filter has harmonic distortion products of less than –87dBc.

40dB Gain, 550kHz Instrumentation Amplifier

An instrumentation amplifier with a rail-to-rail output swing, operating from a 3V supply, can be constructed with the LT1632, as shown in Figure 7. The amplifier has a nominal gain of 100, which can be adjusted with resistor R5. The DC output level is equal to the input voltage (V_{IN}) between the two inputs multiplied by the gain of 100. Common mode range can be calculated by the equations shown with Figure 7. For example, the common mode range is from 0.15V to 2.65V if the output voltage is at one-half of the 3V supply. The common mode rejection is greater than 110dB at 100Hz when trimmed with resistor R1. Figure 8 shows the amplifier's cutoff frequency of 550kHz.

Conclusion

The LT1630–LT1633 family of rail-to-rail amplifiers extends the performance of rail-to-rail operation by offering high speed characteristics combined with precision. The combination of low distortion, high slew rate and wide bandwidth allows these amplifiers to be used in applications where the signal amplitude could be as large as the power supplies, and where both AC and DC performance are required. These amplifiers maintain their precision by specifying the input offset over the whole input common mode range and by having the typical open loop gain of a few million. These characteristics, combined with a wide supply operation and a large output current capability, make these amplifiers truly versatile and ideal for demanding applications.

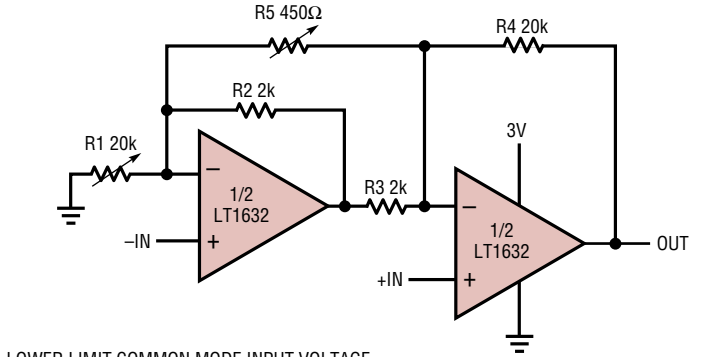


Figure 7. Single-supply instrumentation amplifier

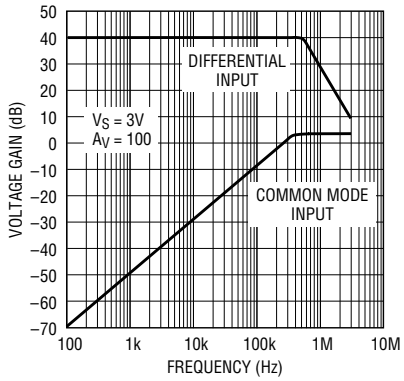


Figure 8. Frequency response of Figure 7's instrumentation amplifier

High Speed SO-8 12-Bit ADCs Run on 5V or 3V

by Ricky Chow and Teo Yang Long

Introduction

Advancing the leading edge of high speed, low power 12-bit serial ADCs in SO-8, LTC introduces the LTC1401 and LTC1404. The LTC1401 is a single 3V supply, 200ksps 12-bit ADC. The LTC1404 is a pin-to-pin compatible upgrade of the existing LTC1400. It samples at 600ksps on either single 5V or ±5V supplies. Both of these devices are small in size but big in features. They achieve speeds that are far ahead of the pack. Once again, LTC has rewritten the record for the highest throughput per square area of board space of any 12-bit ADC on the market. Both devices satisfy tomorrow's digitally based signal-processing requirements while achieving a minimum footprint.

Full ADC Features in an SO-8 Package

3V, 5V or ±5V Supplies

The LTC1401 provides a complete 200ksps unipolar A/D solution operating on a single supply as low as 2.7V. The typical supply current is 5mA and the analog input range is from 0V to 2.048V, yielding an LSB of 0.5mV. Unlike the LTC1400 and LTC1404, the unipolar LTC1401 replaces the unused negative supply pin with a power-down input. The user can power the chip down immediately by pulling this pin low. Like the LTC1400, the LTC1404 operates on a single 5V or ±5V supplies and consumes about 15mA. The analog input signal range is automatically determined by the supply voltage. If V_{SS} is connected to ground, the chip operates in unipolar mode and accepts analog signals between 0V and 4.096V. If V_{SS} is connected to a –5V supply, the chip enters bipolar mode, in which case the input range is ±2.048V. In either mode, the LSB is 1mV. Figure 1 shows a typical application for LTC1401 or LTC1404.

Reference, S/H and Serial I/O

The common features shared by both devices include a precision internal reference, which can be overdriven externally, and high frequency S/H circuitry. The high impedance analog input can be driven through a MUX without adding any DC errors due to on-resistance. The low input capacitance allows fast acquisition time for the sample-and-hold, even with high source impedance. There is a simple 3-wire digital interface to the host computer, DSP or microcontroller. The interface consists of a serial input clock (CLK), data output (D_{OUT}) and a convert-input start (CONV) signal. The CONV input allows precise control of each sample conversion, so vital to DSP applications that require precise sampling. The rising CLK edge synchronizes all the ADC events to make sure that none of the ADC's critical comparisons occur simultaneously with a clock edge or data-out transition. The D_{OUT} pin is at high impedance when the ADC is not converting. During operation, it first pipes out a REFRDY bit and follows this with the 12-bit serial data. Figure 2 shows the block diagram and the digital timing. The block diagram illustrates the pinout and functional differences between the LTC1401 and LTC1404. The REFRDY bit indicates that the internal reference is ready for conversion. REFRDY is a logic 1 if the reference is valid; otherwise it outputs a 0. This bit indicator becomes a very useful feature when the chip is toggling between the active and power-down modes.

NAP and SLEEP Shutdown Modes

The combination of CLK and CONV signals serves another very important function. The ADCs can be placed in NAP or SLEEP mode with the proper manipulation of these two input signals. Figure 3 shows the power-down

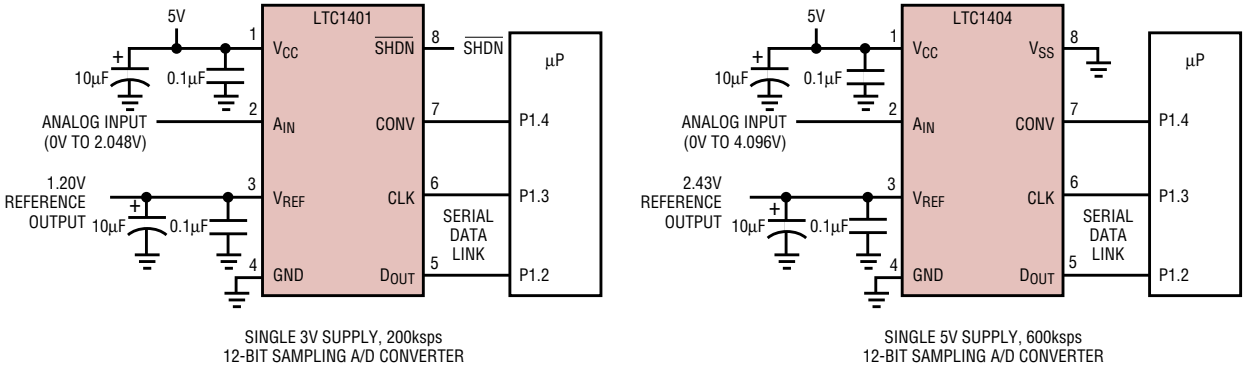


Figure 1. LTC1401 and LTC1404 typical applications

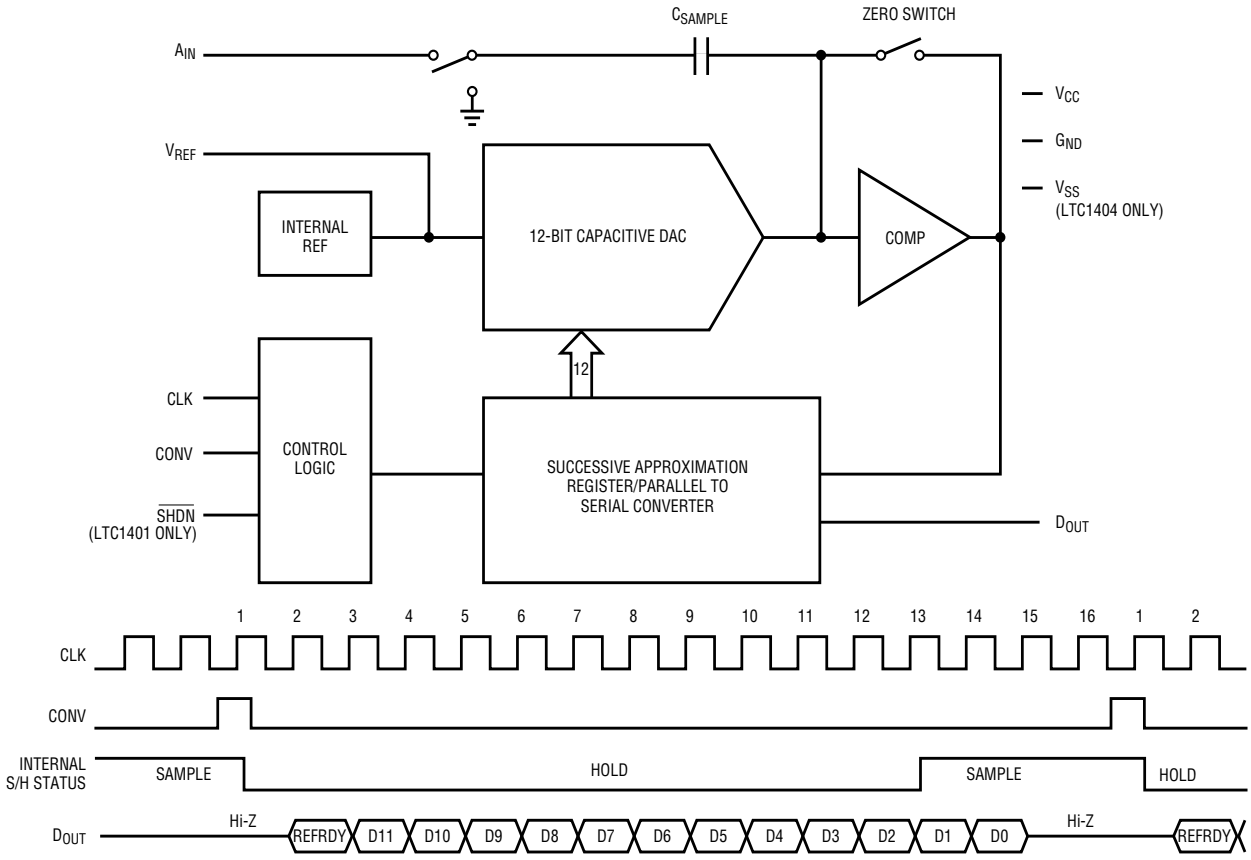
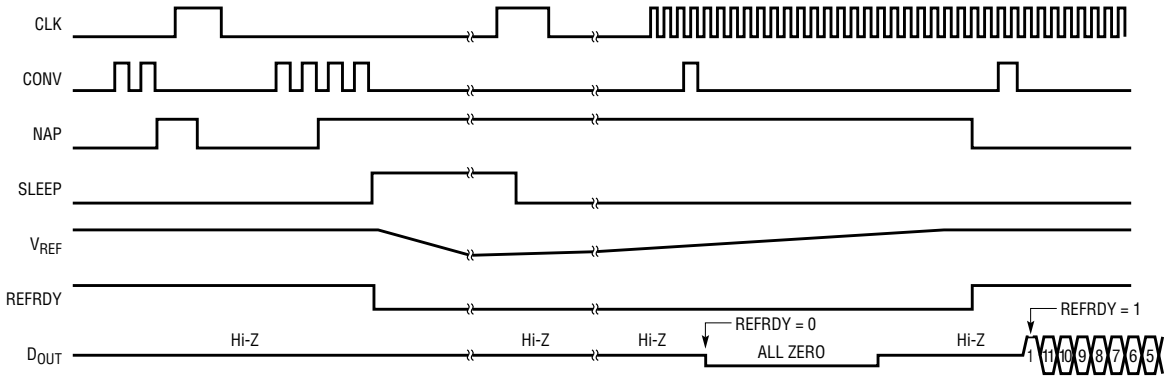


Figure 2. Block and timing diagrams

timing waveform. With CLK held at a logic low, two consecutive CONV pulses activate NAP mode and shut down all internal circuitry except the reference, which fully charges the external bypass capacitor; the REFRDY bit is high. Under this condition, the supply currents for the LTC1401 and LTC1404 are 500µA and 1.3mA, respectively. Either ADC can be reawakened quickly to resume conversion. If the ADC is not reawakened and CLK is still held low, another two consecutive CONV pulses (a total of four pulses) activate the SLEEP mode and shut down the reference; the charge on its bypass capacitors goes to zero and the REFRDY bit goes low, reducing the supply current to 6.5µA for the LTC1401 and 8µA for the LTC1404. Figure 4 shows the power supply consumption of the LTC1404 in its various operating modes.

Reference Ready Indicator

In NAP or SLEEP mode, the first rising CLK edge returns the ADC to normal operation. When SLEEP is deactivated on the LTC1404, the internal reference is first powered up and the reference capacitor is slowly charged. Since the LTC1404 has limited source-current capability to charge the capacitor, a finite time is needed and this time depends on the capacitance value. Guesswork as to when the



NOTE: NAP AND SLEEP ARE INTERNAL SIGNALS; REFRDY APPEARS AS THE FIRST BIT IN THE D_{OUT} WORD.

Figure 3. NAP and SLEEP mode waveforms

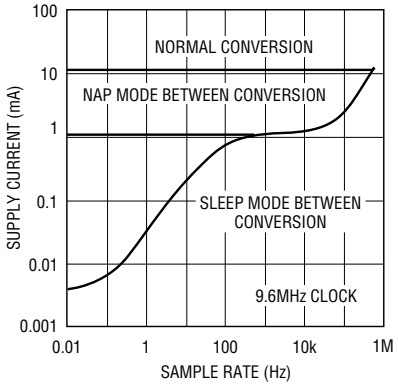


Figure 4. LTC1404 power consumption in various operating modes

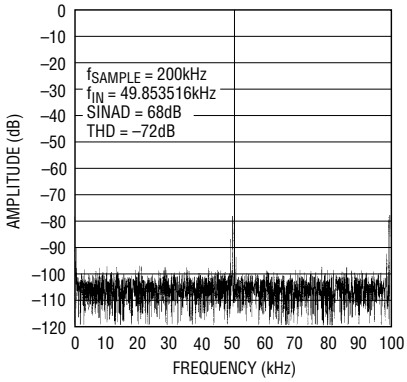


Figure 5a. LTC1401 FFT

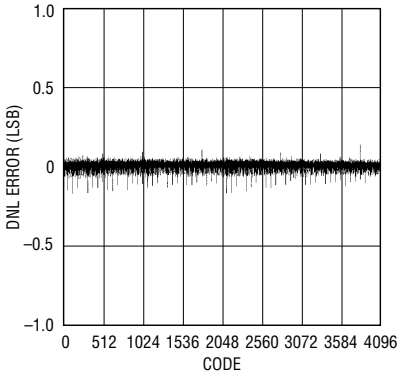


Figure 5b. LTC1401 DNL error

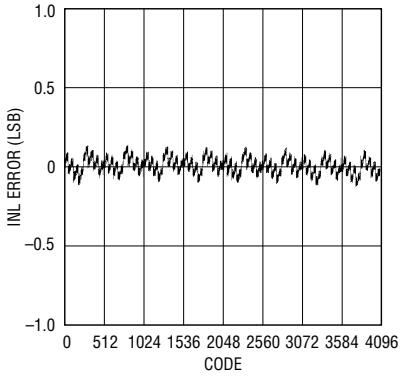


Figure 5c. LTC1401 INL error

capacitor is fully charged is eliminated by monitoring the REFRDY bit. The REFRDY bit guarantees that the reference is steady and the digital result is correct. Some competing ADCs need an off-chip reference. With these parts, it is up to the system designer to come up with a way to put the reference to sleep and to determine just how long it takes to wake up. Because of board-level variations or varying reference loading conditions, the converted output may not be correct because of different reference wake-up times. With their proprietary power-down scheme, the high speed LTC1401 and LTC1404 can save more power when operating at low sampling rates than some "micropower" ADCs without a power-down feature.

Easy to Apply

Ground Plane

As with other high resolution, high speed ADCs, the LTC1401/LTC1404 needs some basic attention to layout details. These include grounding, bypassing and lead inductance. The best performance is achieved when the LTC1401/LTC1404 is applied as an analog device and powered from an analog supply. Its ground pin should be connected to an analog ground plane. This ground plane should have only one connection to the system ground. This prevents system-ground currents from taking a short cut through the analog ground. This single connection should be made to a point near the ADC ground pin. Alternatively, a 10Ω resistor or a ferrite bead jumper instead of a direct short may help to reduce the digital noise.

Supply Bypassing

Noise on the power supply can cause ADC errors. At low frequencies, the converter has very good power supply rejection, but as frequency increases, all converters lose the ability to reject power-supply noise. To eliminate power-supply noise, the LTC1401/LTC1404 V_{CC} pin should be bypassed directly to the analog ground plane with a good 10µF AVX capacitor in parallel with a 0.1µF ceramic; for better results, another 10µF AVX capacitor can be added. At 600ksps, the LTC1404's CLK frequency can be as high as 9.6MHz. Some poor quality capacitors can lose more than 80% of their capacitance in this frequency range. Therefore, it is important to consult the manufacturer's data sheet before selecting a capacitor. For the LTC1404, at 600ksps, every bit decision must be determined within 104ns (9.6MHz). During this short time interval, the supply disturbance due to CLK transition must settle, the ADC must update its DAC, make a comparator decision, latch the new DAC information and output the serial data. Both of these ADCs have only one power supply pin, which is connected to both the internal analog and digital circuitry. Any ringing due to poor bypassing, parasitic trace inductance, CLK and CONV over/undershoot or unnecessary D_{OUT} current loading can cause ADC errors. Narrow power supply traces should be avoided. Their comparatively high inductance can lead to compromised bypass performance and conversion errors. The input signals for the CLK and CONV pins should be terminated properly. The D_{OUT} signal should be buffered if necessary to drive a long trace or heavy load.

DC and AC Performance

With these basic concerns in mind, it is not difficult to obtain the best performance from the LTC1401 and LTC1404. The DC performance of the LTC1401 and LTC1404 includes ±1LSB INL and DNL. No missing codes are guaranteed over temperature. In addition to these excellent DC specifications, these devices have curvature-corrected 1.20V (LTC1401) or 2.43V (LTC1404) precision references. For high frequency conversion applications, the LTC1401 and LTC1404 excel, with outstanding AC performance. Figures 5 and 6 show the performance of the LTC1401 and LTC1404, respectively.

continued on page 24

A 7ns, 6mA, Single-Supply Comparator Fabricated on Linear's 6GHz Complementary Bipolar Process

by Jim Williams and Brian Hamilton

Introduction

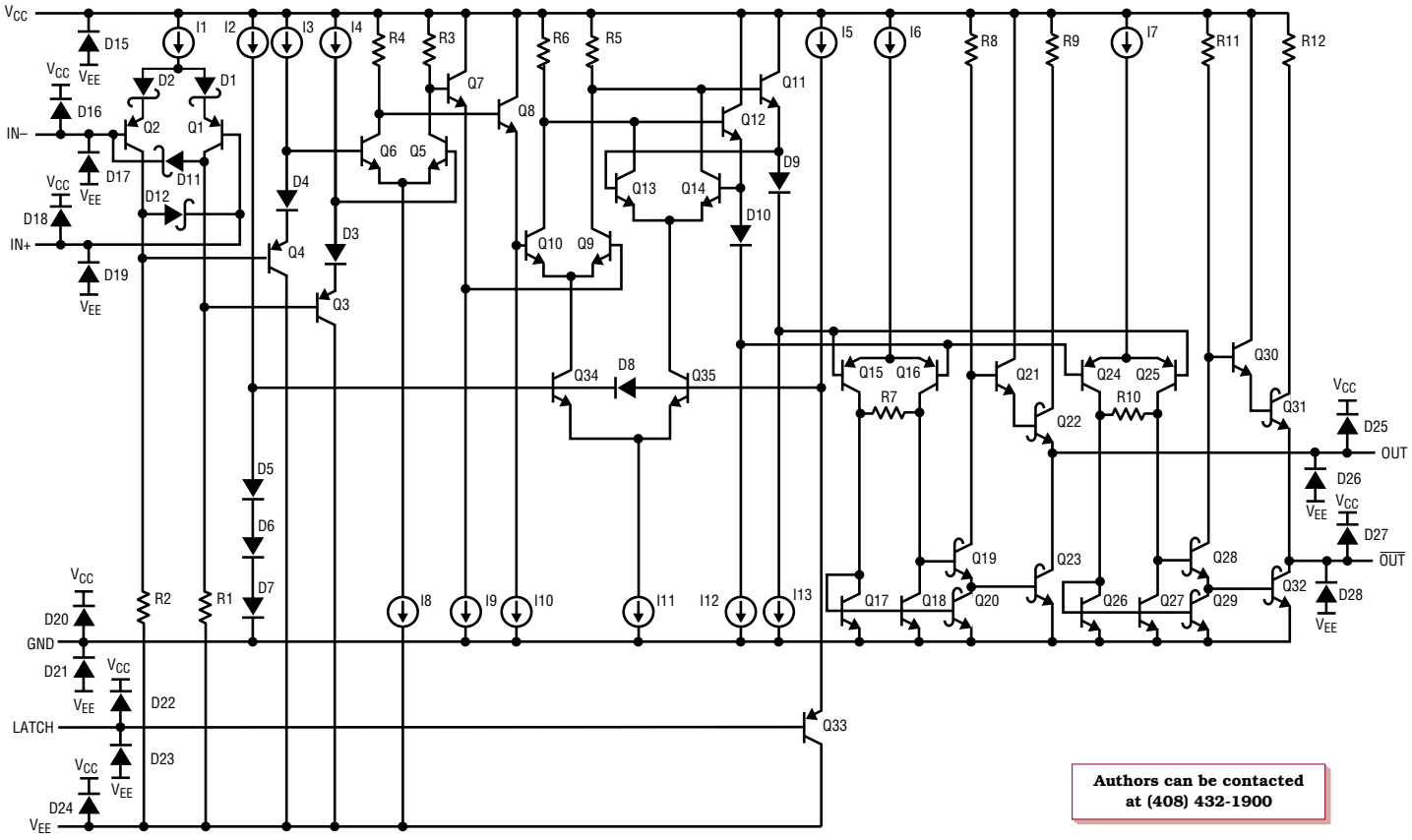
The LT1394 is an ultrafast (7ns), low power (6mA), single-supply comparator designed to operate on either 5V or ±5V supplies. It has a maximum offset voltage of 2.5mV, complementary TTL compatible outputs and output latch capability. The LT1394 is the first product made with Linear Technology's 6GHz complementary bipolar technology. This fine-line geometry process results in a product with dramatically improved speed and power compared to industry-standard comparators developed in slower NPN-only technologies.

These features combine to make the LT1394 well suited for applications such as high performance NTSC crystal oscillators, single-supply voltage-to-frequency converters and high speed, high accuracy level detectors. The LT1394 is offered in SO-8 and is pin compatible with the industry-standard LT1016 and LT1116 comparators.

Circuit Description

A simplified schematic of the LT1394 can be seen in Figure 1. There are differential inputs (+IN/–IN), differential outputs (OUT/$\overline{OUT}$), a latch input (LATCH) and three power supply pins (V_{EE}, V_{CC} and GND). The circuit topology consists of a differential input stage, a level-shifting gain stage, a latch stage and complementary output stages. The complementary output stages offer improved flexibility for the user; the latch stage provides superior sampling accuracy of the input signal without the need for an external latch.

The input stage of the LT1394 uses a PNP differential pair (Q1–Q2) with Schottky diodes in the emitters (D1–D2) and resistive loads (R1–R2). The Schottky diodes in series with the emitters allow differential input voltages that are greater than the base-emitter breakdown of the input transistors. Two additional Schottky



Authors can be contacted at (408) 432-1900

Figure 1. LT1394 simplified schematic

diodes (D11–D12) prevent output phase reversal when either input is taken far enough below V_{EE} to forward bias the base-collector junction of its corresponding PNP input transistor. To allow single-supply operation, the input stage has been designed to have small voltage swings across load resistors R1 and R2. This ensures that the input PNPs will not saturate with the LT1394 inputs at V_{EE}.

The signal path remains differential as it is buffered and level shifted via transistors Q3–Q4 and diodes D3–D4. The level shift prevents current source I_8 from saturating. The second gain stage, comprising transistors Q5–Q6 and resistors R3–R4, takes additional gain while level shifting the signal back to V_{CC}. The differential output of the second gain stage is buffered by transistors Q7–Q8, which then drive the latch stage.

In the latch stage, transistors Q9–Q10 and resistors R5–R6 act as a third gain stage. Q11–Q12 buffer the signal at resistors R5–R6, driving another differential pair (Q13–Q14). Q13 and Q14, when activated, provide positive feedback to resistors R5–R6, creating the latch. When the LATCH pin is low, the LT1394 is in flow-through or GAIN mode. Current I_{11} is steered through Q34, activating the Q9–Q10 differential pair. When the LATCH pin is high, the LT1394 is in LATCH mode. Current I_{11} is steered through Q35, activating the Q13–Q14 differential pair. The output of the gain/latch stage has additional level shifting from the emitters of transistors Q11–Q12 via diodes D9–D10. This level shifting prevents the output stage current sources I_6 and I_7 from saturating.

The LT1394 provides complementary outputs by using two identical output stages connected in opposite phases. Examining the output circuitry for the OUT pin, a PNP differential pair (Q15–Q16) is driven from the outputs of the latch stage. When I_6's current is steered through Q16, it drives R7 and the base of Q19. R7 improves switching speed by reducing the gain of the differential pair Q15–Q16 and lowering the impedance at the base of Q19. Q19's emitter current then drives the base of Q23, turning it on until the OUT pin has been pulled low and Q23's Schottky clamp diode has turned on. Conversely, if I_6's current is steered through Q15, it allows R8 to pull up the Darlington-connected output transistors Q21 and Q22, bringing the OUT pin high. For faster output switching times, Q15's collector current flows into the Q17/Q18/Q20 current mirror. Q20's collector current helps turn off Q23, whereas the collector current of Q18 helps turn off Q19.

Linear Technology's 6GHz Complementary Bipolar Technology

Linear Technology's 6GHz complementary bipolar technology (6GHz ComBi) features vertical NPN and PNP transistors with similar frequency response and gain characteristics. Both the NPN and PNP transistors feature polysilicon emitters for improved gain, a collector-to-emitter breakdown voltage (BV_{CEO}) greater than 12V and a unity gain frequency (f_T) of 6GHz. The PNP transistors have a nominal current gain (β) of about 45, while the NPNs have a β of about 100.

In addition to the transistors, the 6GHz ComBi technology includes diode, resistor and capacitor structures. Schottky barrier diodes with low parasitic capacitance and high breakdown voltage are included for high speed voltage clamping and breakdown protection of transistors. Low parasitic capacitance polysilicon resistors are included for use in high speed signal paths. High resistivity diffused resistors are used for biasing and low power circuitry. Polysilicon-oxide-metal capacitors offer low parasitic capacitance, high capacitance density and low series resistance for good high frequency performance.

When compared to a typical 30V complementary bipolar process, the reduction of transistor BV_{CEO} from 30V to 12V has many benefits for applications that do not require higher supply voltages. Dramatically reduced depletion widths within the transistor allow a 50% decrease in area. This area reduction improves speed by lowering parasitic capacitances associated with the transistor. The reduced voltage requirement also allows a thinner, richer epitaxial (epi) region. This change to the epi region dramatically reduces the collector resistance of the transistors, resulting in smaller

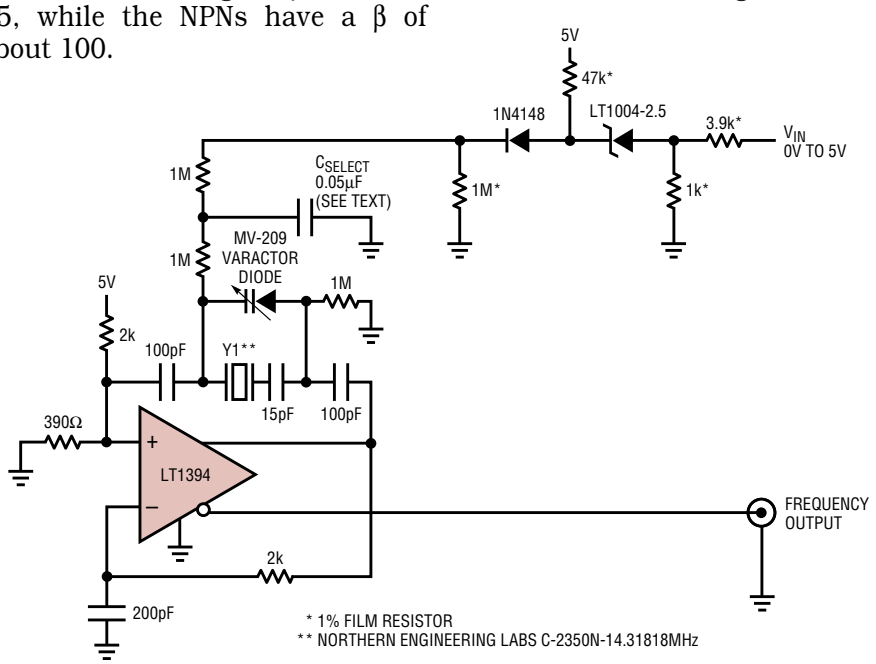


Figure 2. A 4× NTSC subcarrier voltage tunable crystal oscillator; tuning range and bandwidth accommodate a variety of phase-locked loops.

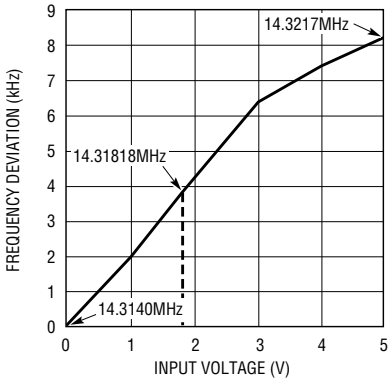


Figure 3. Control voltage vs output frequency for Figure 2; tuning deviation from the center frequency exceeds ±240ppm.

transistors for a given current level. With this significant reduction in transistor size, interconnects using a single metallization layer becomes much more difficult and would generate significant parasitic capacitance. Because of this, the 6GHz ComBi process utilizes two levels of metallization.

Applications

4× NTSC Voltage-Tunable Crystal Oscillator

The first of three representative applications for the LT1394 can be seen in Figure 2. This circuit is a crystal oscillator with voltage tuning of the output frequency. This application makes use of the LT1394's high speed, complementary outputs and single-supply 5V operation. Such voltage controlled crystal oscillators (VCXO) are often employed where slight variation of a stable carrier is required. This example is specifically intended to provide a 4× NTSC subcarrier tunable oscillator suitable for phase locking.

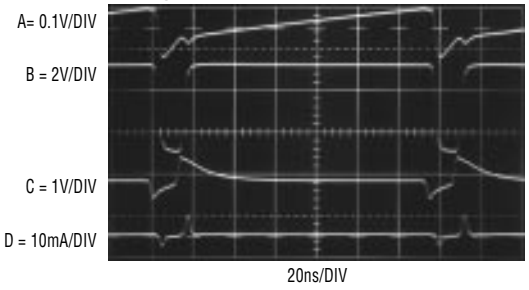


Figure 5. Waveforms for the 10MHz voltage-to-frequency converter; charge pump–based feedback provides linearity and fast response to input.

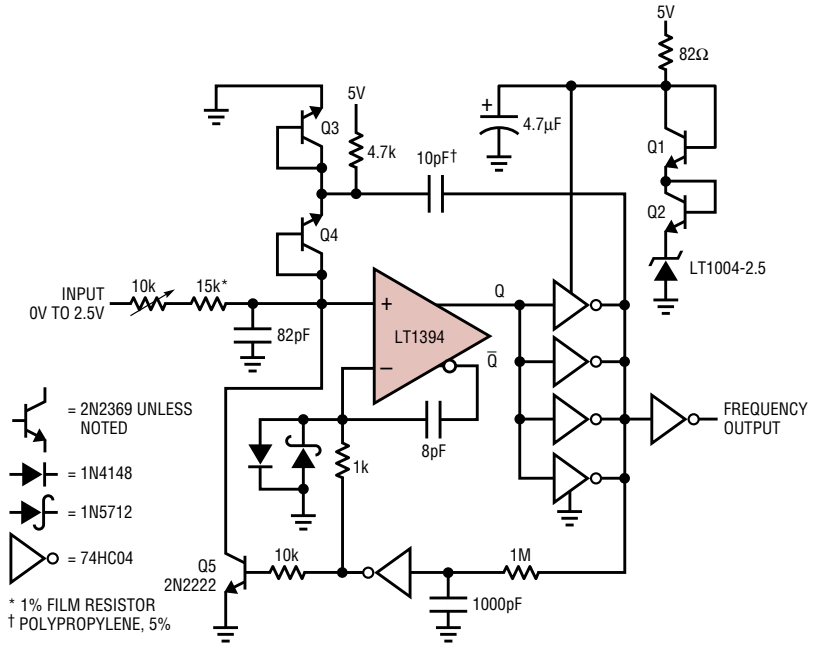


Figure 4. This simple charge pump–based 10MHz voltage-to-frequency converter has 40dB dynamic range and operates from a 5V supply.

The resistors at the LT1394's positive input set a DC bias point of 840mV. The 2kΩ– 200pF path sets up phase-shifted negative feedback, putting the DC output in the active region with a gain of 35 at the oscillation frequency. The crystal's path provides resonant positive feedback and stable oscillation occurs. The varactor diode is biased from the tuning input. The tuning network is arranged so that a 0V to 5V drive provides a reasonably symmetric, broad tuning range around the 14.31818MHz center frequency. The capacitor labeled C_{SELECT} sets the tuning bandwidth. It should be picked to complement loop response in phase-locking applications. Figure 3 is a plot of frequency deviation versus tuning input voltage. Tuning deviation from the 4× NTSC 14.31818MHz center frequency ex-

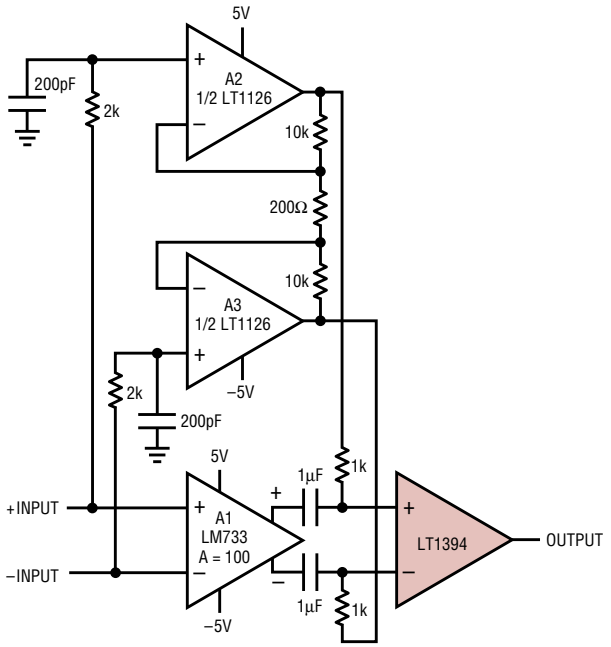


Figure 6. Parallel preamplified paths allow 18ns response to 500µV overdrive.

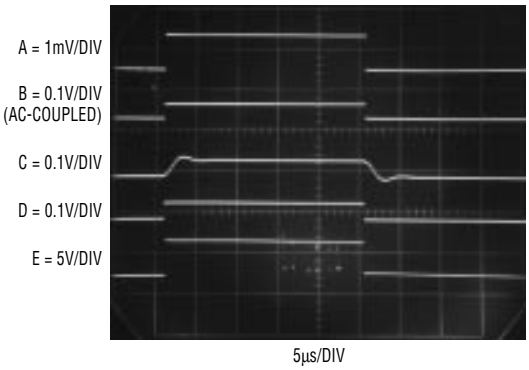


Figure 7. 500µV input (Trace A) is split into wideband and low frequency gain paths (Traces B and C) and recombined (Trace D). Trace E is the level-detector output.

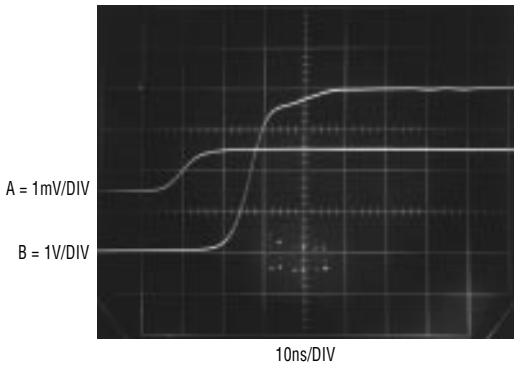


Figure 8. Parallel-path level detector shows 18ns response (Trace B) to 500µV overdrive (Trace A).

ceeds ±240ppm for a 0V to 5V tuning range.

Simple 10MHz Single-Supply V/F Converter

A second application for the LT1394 is shown in Figure 4. It is a simple 10MHz single-supply voltage-to-frequency converter that makes use of the LT1394's speed, single-supply operation and complementary outputs. A 0V to 2.5V input produces a 0Hz to 10MHz output with 40dB of dynamic range, 1% linearity and 400 ppm/°C gain drift. Power supply rejection is 0.5% for 4.75V to 5.25V supply excursions.

To understand circuit operation, assume the LT1394's positive input is slightly below its negative input. The circuit's input voltage causes a positive-going ramp at the comparator's positive input (Trace A, Figure 5). The Q output is low, forcing the CMOS inverter outputs high. This allows current flow from diode Q1's collector, through the CMOS inverter supply pin, to the 10pF capacitor. The 4.7µF capacitor provides high frequency bypass, maintaining low impedance at Q1's collector. Diode connected Q3 provides a path to ground. The voltage to which the 10pF capacitor charges is a function of Q1's collector potential and Q3's drop. When the ramp at the comparator's positive input goes high enough, the Q output goes high and the paralleled inverters switch low (Trace B). This action pulls current from the 82pF capacitor at the input via the Q1–10pF route (Trace D). This current removal resets the LT1394's positive input ramp to a potential slightly below ground, forcing the Q output low and the paralleled inverters high. The 8pF capacitor at the LT1394's inverting output furnishes AC positive feedback to the negative input (Trace C). This ensures that the Q output remains high long enough for a complete discharge of the 10pF capacitor. The Schottky diode prevents the LT1394's input from being driven outside its negative common mode limit. When the 8pF capacitor's feedback decays, the LT1394 again switches and the entire cycle repeats. The oscillation frequency depends entirely upon the input-derived current. The LT1004 is the circuit's voltage reference, with Q1 and Q2 temperature compensating Q3 and Q4.

Start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, the LT1394's output goes high, causing the paralleled inverters to go low. After a time determined by the 1MΩ–1000pF RC, the associated lone inverter goes high. This lifts the LT1394's negative input and grounds the positive input with Q5, initiating normal circuit action.

To calibrate this circuit, apply 2.5V and adjust the 10k potentiometer for a 10MHz output.

18ns 500µV Level Detector

The ultimate limitation on comparator sensitivity is available gain. Unfortunately, increasing gain invariably involves giving up speed. The gain vs speed trade-off in fast comparators is usually a practical compromise designed to satisfy most applications. Some situations, however, require more sensitivity (that is, higher gain) with minimal effect on speed. Figure 6's circuit adds a differential preamplifier ahead of the LT1394, increasing gain. This permits 500µV comparisons in 18ns. A parallel-path DC stabilization approach eliminates preamplifier drift as an error source. A1 is the differential amplifier, operating at a gain of 100. Its output is AC coupled to the LT1394. A1 has poorly defined DC characteristics, necessitating some form of DC correction. A2 and A3, operating at a differential gain of 100, provide this function. They differentially sense a band-limited version of A1's inputs and feed DC and low frequency amplified information to the comparator. The low frequency roll-off of A1's signal path complements A2–A3's high frequency roll-off. The summation of these two signal channels at the LT1394's inputs results in flat response from DC to high frequency.

Figure 7 shows waveforms for the high sensitivity level detector. Trace A is a 500µV overdrive on a 1mV step applied to the circuit's positive input (negative input grounded). Trace B shows the resulting amplified step at A1's positive output. Trace C is A2's

band-limited output. A1's wideband output combines with A2's DC-corrected information to yield the correct, amplified composite signal at the LT1394's positive input in Trace D. The LT1394's output is Trace E. Figure 8 details circuit propagation delay. The output responds in 18ns to a 500µV overdrive on a 1mV step. Figure 9 plots response time versus overdrive. As might be expected, propagation delay decreases at higher overdrives. A1's noise limits usable sensitivity.

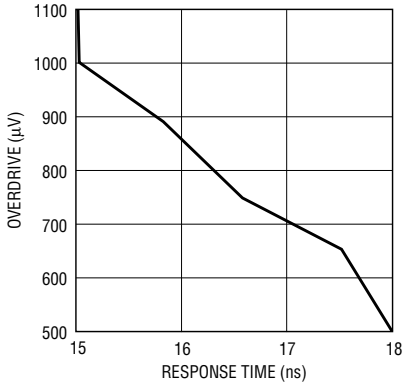


Figure 9. Response time vs overdrive for the composite level detector

Conclusion

Innovative circuit design, coupled with Linear Technology's 6GHz complementary bipolar process simultaneously achieves the seemingly contradictory goals of high speed and low power. The LT1394 is easy to use, thanks to its single-supply capability and complementary outputs. Additional LT1394 applications appear in the forthcoming Linear Technology Application Note, *A Seven Nanosecond Comparator for Single Supply Operation.*

LTC1401/LTC1404, continued from page 19

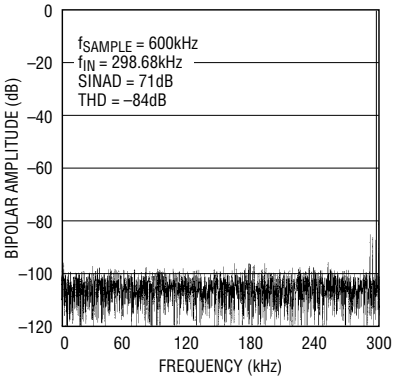


Figure 6a. LTC1404 FFT

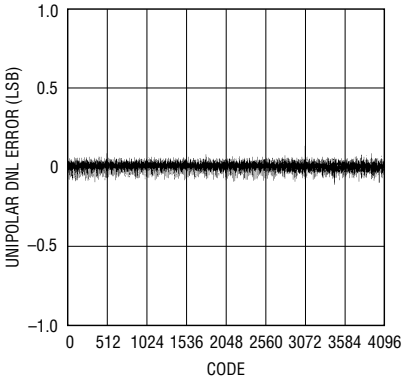


Figure 6b. LTC1404 DNL error

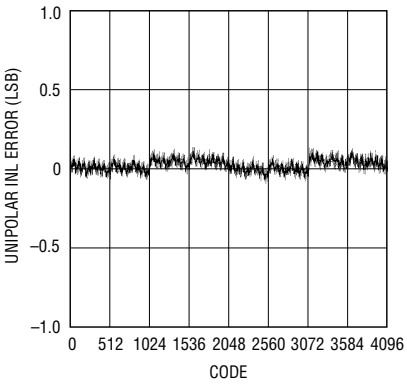


Figure 6c. LTC1404 INL error

Applications

The LTC1401 and LTC1404 will find applications in telecommunications, digital signal processing, portable-computer data acquisition boards and high speed or multiplexed data acquisition.

In telecommunication applications such as HDSL (high-bit-rate digital subscriber line interface), high speed and low power dissipation are a must because the systems are usually powered by the phone line itself. Excellent dynamic performance is required of the ADC's sample-and-hold. The serial interface minimizes the number of signal lines that must be routed, thereby saving significant board space. The 600ksps LTC1404, with its SO-8 footprint, is an excellent choice for HDSL applications. At 584ksps, with 2B1Q coding, the LTC1404 receives at 2.048Mbps over two wires.

Another common use of ADCs is in data acquisition applications. System designers have always faced problems in optimizing data acquisition applications for speed, size, power and cost, especially in the case of portable designs. The high sample rate, the high level of functional integration and the low cost of these converters make them ideal choices for these applications. The LTC1401 and LTC1404 can be easily interfaced to a low cost MUX (for example, a CD4051, 74HC4051 or LTC1391) through their high impedance inputs. The high input impedance of these ADCs eliminates the need for a buffer between the MUX and the ADC, resulting in savings of both cost and board space.

Conclusion

The new LTC1401 and LTC1404 come with full ADC performance and an easy-to-use serial interface. These complete, stand alone, high speed, low power devices will simplify the job of system designers.

LTC1406, continued from page 5

Clean, Wideband Undersampling Performance

All of the features and advantages of the LTC1406 wouldn't mean a thing without outstanding performance. Fortunately, the LTC1406 has it. Extremely low noise combined with low distortion and wide input bandwidth make the LTC1406 a great performer over an extremely wide range of input frequencies. As shown in Figure 1, the signal-to-(noise + distortion) ratio stays nearly flat out to 10MHz. Figure 6 shows a FFT plot for an input frequency of 30MHz and provides an even clearer picture of the low distortion and high spurious free dynamic range for frequencies beyond the Nyquist frequency of 10MHz.

Conclusion

The LTC1406 has everything high speed designers need: wide input bandwidth, great high frequency and undersampling performance, the smallest package of any 8-bit, 20MHz converter available and a host of features that make it easy to use and easy to get maximum performance. Linear Technology and the LTC1406 will be welcome additions to high speed data conversion.

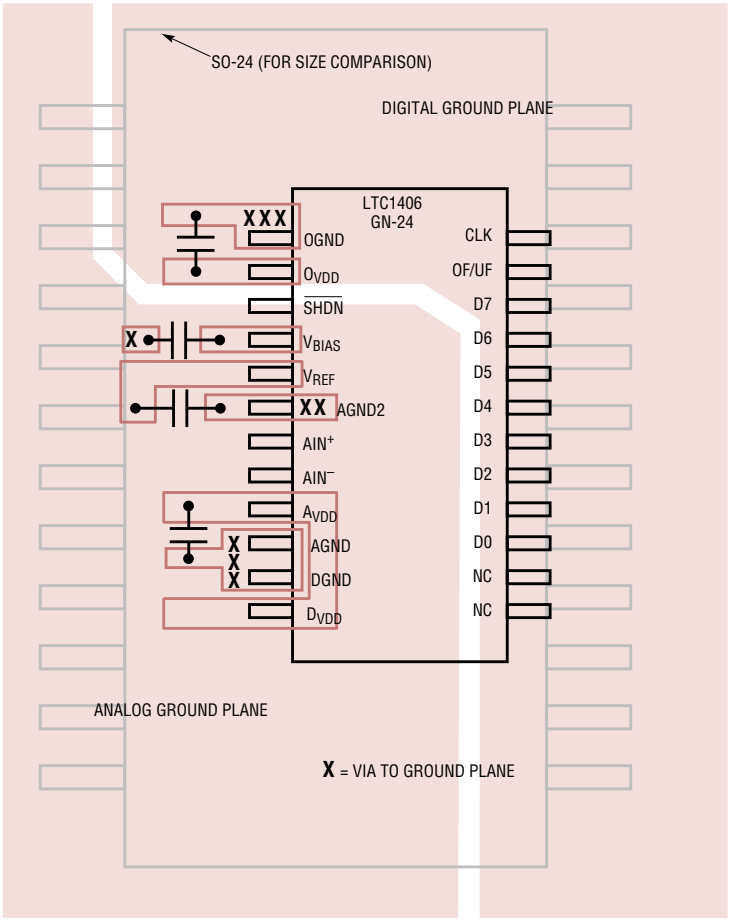


Figure 5. The tiny footprint of the LTC1406 saves board spacecompared to an SO-24. A clean layout includes short bypass loops and separation of analog and digital signals

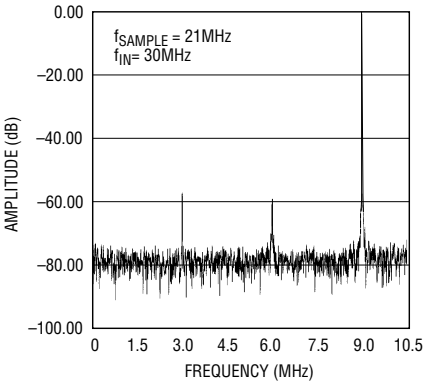


Figure 6. An FFT plot of the LTC1406 shows outstanding performance for high input frequencies: the S/(N + D) si 47dB and the SFDR is 56dB for an input frequency of 30MHz.

LTC1710, continued from page 13

the output latch in the LTC1710, the Stop signal not only indicates an end to the Send Byte protocol, but can also be used to synchronize the output executions of several differently addressed SMBus peripherals whose valid data were also loaded into their respective output latches at different times without a Stop signal being sent. However, if a Start or Stop signal is detected in the middle of a byte transmission, the LTC1710 will regard it as an error and reject all previous data. An example of a Send Byte protocol is provided in Figure 4.

Conclusion

With two built-in 0.4Ω power switches in an MSOP-8 or SO-8 package and a low standby current (typically 14µA), the LTC1710 is an ideal and complete solution for delivering up to 300mA of current to SMBus peripherals in today's complex portable equipment.

High Isolation Converter Uses Off-the-Shelf Magnetics

by Mitchell Lee

Isolated flyback converters usually evoke thoughts (or bitter memories) of custom transformers, slipped delivery schedules and agency approval problems. Off-the-shelf flyback transformers are available from several vendors, but these carry isolation ratings of only 300V–500V, and, rarely, of up to 1kV. Flyback transformers with isolation ratings of $3750V_{RMS}$ are impossible to find, and if an application requires this level of isolation, an expensive, custom design is likely the only solution.

Gate-drive transformers, designed to couple switching regulator controllers to MOSFET gates, are readily available from stock with high isolation ratings and low cost. These are wound on ungapped cores and have very high inductance (500µH to 2mH), and will quickly saturate in a normal flyback converter circuit. It is possible to use a gate-drive transformer in a forward converter, but an optoisolator or a tertiary winding is needed for feedback. Another topology that can utilize a gate drive transformer is the uncoupled SEPIC.

Figure 1 shows a complete schematic for a converter based on the uncoupled SEPIC. The converter operates from a 12V battery-backed input supply and outputs 24V at 200mA. The key feature is that the second coil is not a coil at all, but rather an off-the-shelf gate drive transformer. This component offers $3750V_{RMS}$ isolation and full VDE approval, and functions flawlessly in SEPIC service.

Feedback is derived from the primary winding, through D3. R1 acts to filter the leakage-inductance spike at switch turn-off, and C4 smooths the recovered feedback voltage. Note that the transformer is wound 1:1; C4 peak detects a voltage roughly equal to the output. Sizing R1 and C4 is a trade-off between minimum load and load regulation. As shown, a minimum load of 3600Ω is recommended. Output regulation is shown in Figure 2. Line regulation from 10V to 20V input at full load is 0.13%/V.

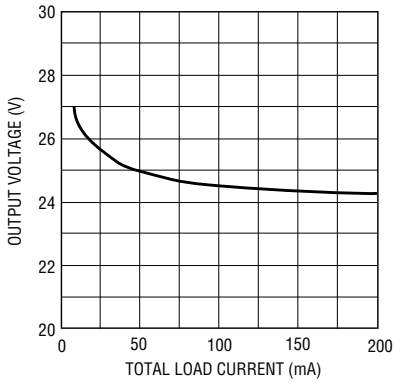


Figure 2. Output regulation for Figure 1's circuit

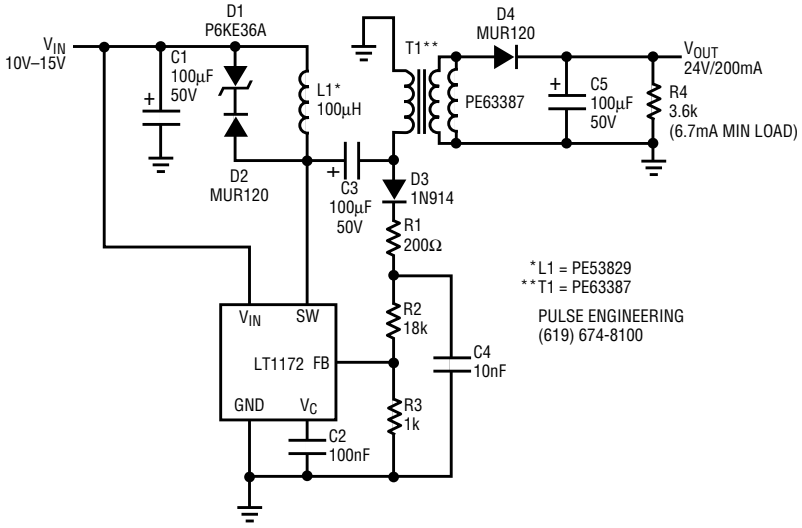


Figure 1. 24V/200mA bulk supply with $3750V_{RMS}$ isolation

Wide-Input-Range, Low Voltage Flyback Regulator

by Kurk Mathews

Many new switching regulators are designed with a specific application or topology in mind. If your requirements happen to fall within these parameters, all is well. Unfortunately, when faced with unusual requirements, the designer is often forced to choose bare-bones, universal regulators. The LTC1624 overcomes these issues by providing a full featured regulator that can operate in the step-down (buck), step-up (boost), buck-boost or flyback mode.

The functional diagram in Figure 1 reveals the flexibility of this device. This constant-frequency current mode controller includes a high-side differential current sense amplifier and a floating high current N-Channel MOSFET driver. In the buck mode, an external bootstrap capacitor between the BOOST and SW pins works in conjunction with the internal 5.6V regulator and diode to provide a regulated supply for a high-side driver. In the boost, buck-boost or flyback mode, the SW pin is grounded, providing drive for a low-side MOSFET.

An example of a wide-input-range flyback is shown in Figure 2. The circuit provides ±50V at 75mA from a 4.75 to 24V source. The sum of line-, load- and cross-regulation is better than ±5%. The SW pin voltage is controlled by the internal 5.6V regulator, allowing the input voltage to be above Q1's 16V maximum gate-to-source voltage rating. 200kHz fixed frequency operation minimizes the size of T1. The R-C snubber formed by C1 and R1 in combination with T1's low leakage inductance keeps Q1's drain voltage well below its 100V rating. To improve cross-regulation, Q2, R2 and R3 were included to disable

continued on page 31

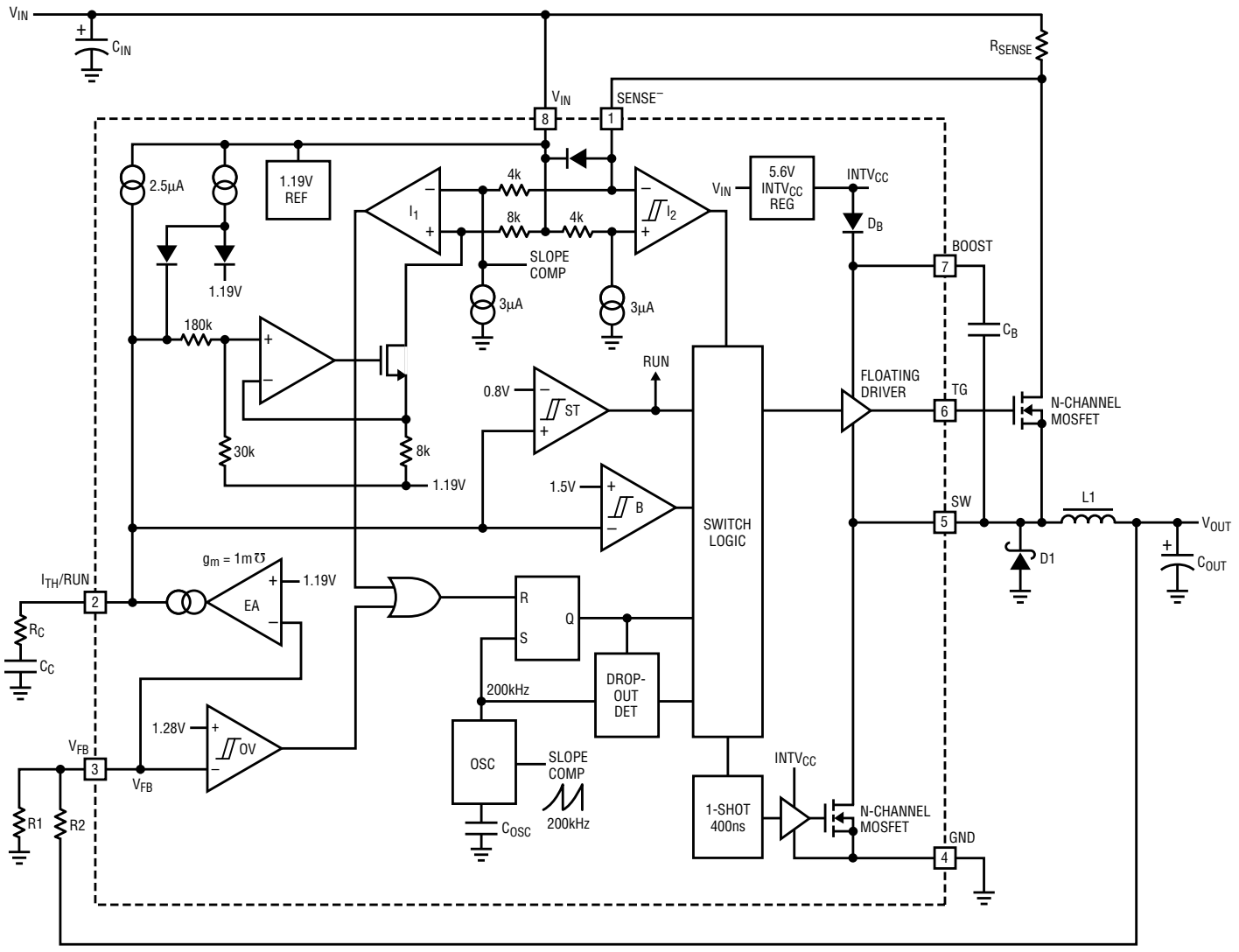


Figure 1. LTC1624 function diagram

How to Design High Order Filters with Stopband Notches Using the LTC1562 Quad Operational Filter (Part 1)

by Nello Sevastopoulos

This is the first in a series of articles describing applications of the LTC1562 connected as a lowpass, highpass or bandpass filter with added stopband notches to increase selectivity. Part 1 covers lowpass filters.

Lowpass filters with stopband notches are useful in applications seeking steep attenuation in the vicinity of the cutoff frequency. When compared to classical all-pole realizations (such as Butterworth or Chebyshev) they are more "efficient"; that is, they meet a given attenuation requirement with the least number of poles.

Lowpass filters with stopband notches (broadly referred to as "elliptics" or "Cauers") can be designed with the aid of some literature or with commercially available software. The new FilterCAD™ for Windows® program, supplied free of charge by Linear Technology Corporation, is an excellent example.

For instance, a 100kHz lowpass filter with a 0.1dB passband ripple and 40dB attenuation at 200kHz can be realized with a 6th order Chebyshev or a 4th order textbook elliptic. Curves A and B of Figure 1 illustrate the respective amplitude responses.

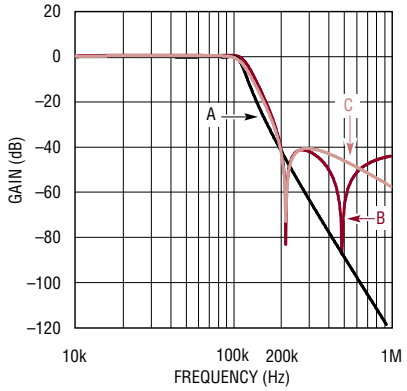


Figure 1. Amplitude responses of 6th order Chebychev (A), 4th order textbook elliptic (B) and modified 4th order elliptic (C) lowpass filters

When considering the practical implementation of the filters of Figure 1 (curves A and B), in the author's experience, it is easier to implement the higher order all-pole filter (curve A), rather than the 4th order version with the stopband notches. The realization of deep stopband notches may result in hardware complexity. This is especially true if a discrete R-C active implementation is chosen and if a single 5V supply and a wide input dynamic range are required.

Nevertheless, curve C of Figure 1 is of particular interest because of its rather simple hardware implementation. Curve C is derived from the classical elliptic response, curve B, where the high frequency notch is "pushed" to infinity and the highest Q pole pair is readjusted to maintain passband flattness. The penalty is the slight gain roll-off at the cutoff frequency, which, for many applications, is acceptable. For sake of simplicity the amplitude response of the filter of Figure 1, curve C, is called a "p-e" (pseudo-elliptic) response.

Figure 2 illustrates the group delay responses of the three filters of Figure 1, with the same curve letter designations. The group delay of curve C is the flattest.

Hardware Implementation

High order filter realizations were a subject of passionate interest in the 1960s and '70s. One very popular method, which stems from the simplicity of its hardware implementation, consists of decomposing a high order filter polynomial into cascaded second and first order polynomials. Each polynomial is then implemented with commercially available active and passive components. The major drawback of the "cascaded" method is the relatively high Q of at least one of the 2nd order sections and the resulting requirement for precision components for its realization.

Using the "cascading" principle outlined above, the "p-e" response of curve c, Figure 1, can be treated as a self-contained 4th order block and two (or more) of these blocks can be cascaded to form an 8th order (or higher) lowpass filter with two (or more) stop-band notches. This interesting novelty is driven by the simplicity of its hardware realization; it requires, however, the transformation of an 8th order classical elliptic lowpass response into two cascaded 4th order "p-e" responses.

Figure 3 shows a compact hardware implementation of the 4th order "p-e" filter using one half of the LTC1562 quad Operational Filter IC, which was introduced in the February 1998 issue of *Linear Technology* magazine.[1] Two 2nd order sections form the 4th order filter function. A phase-shifting external capacitor, C_{IN1}, and a feedforward path through resistor R_{FF2}, create the desired notch.

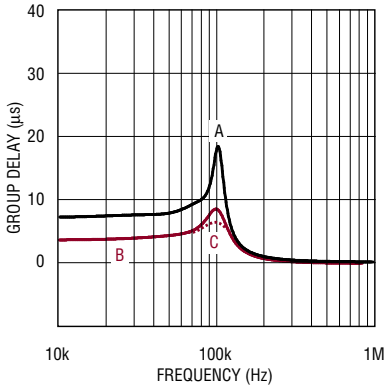


Figure 2. Group-delay responses corresponding to the amplitude responses of Figure 1.

To make the circuit technique of Figure 3 intuitively obvious, consider the following:

A signal of a given frequency can be notched if it is phase shifted by 180 degrees and then summed with itself. If the summation is governed by equal gains, a complete signal cancellation occurs and the notch depth, at least in theory, is infinite.

A phase shift of 180 degrees at a single frequency, f_O, is easily provided by a second order inverting bandpass filter; hence, in Figure 3, if C_{IN1} equals zero, a notch is formed as the bandpass output (pin 2) is summed with the input via (R_{IN2}, R_{FF2}). Moreover, if the summation has equal gains (1), the notch should, in theory, have infinite depth.

$$R_{FF2} = R_{IN2} \bullet (R_{IN1}/R_{Q1}) \qquad (1)$$

In Figure 3, an external capacitor, C_{IN1}, is added to provide additional phase lead, so that the frequency of the notch is higher than the center frequency, f_{O1}, of the second order section used to create it.

The notch frequency, f_{n1}, is directly proportional to the center frequency, f_{O1}, and indirectly proportional to the time constant ($R_{IN1} \bullet C_{IN1}$) divided by the ($R_{Q1} \bullet C$) (C is an internal capacitor of 159pF); therefore:

$$f_{n1} = f_{O1}\sqrt{1 - \frac{1}{\frac{R_{IN1} \bullet C_{IN1}}{R_{Q1} \bullet C}}} \qquad (2)$$

A step-by-step algorithm for building compact "p-e" lowpass filters with the new LTC1562 quad Operational Filter building block is outlined below:

Start with a set of two (lowpass) pole pairs and one finite stopband notch. Arrange the pole pairs in ascending order of Q values.

Example 1:
f_{O1} = 113.76kHz, Q1 = 2.28, f_{n1} = 224.7kHz, f_{O2} = 85.8kHz, Q2 = 0.64, $f_{n2} = \infty$;

1. Calculate the frequency-setting resistor, R21:

   $R21 = (100kHz/f_{O1})^2 \bullet 10k\Omega$
   (choose the closest 1% value)
   R21 = 7.68k (1%)

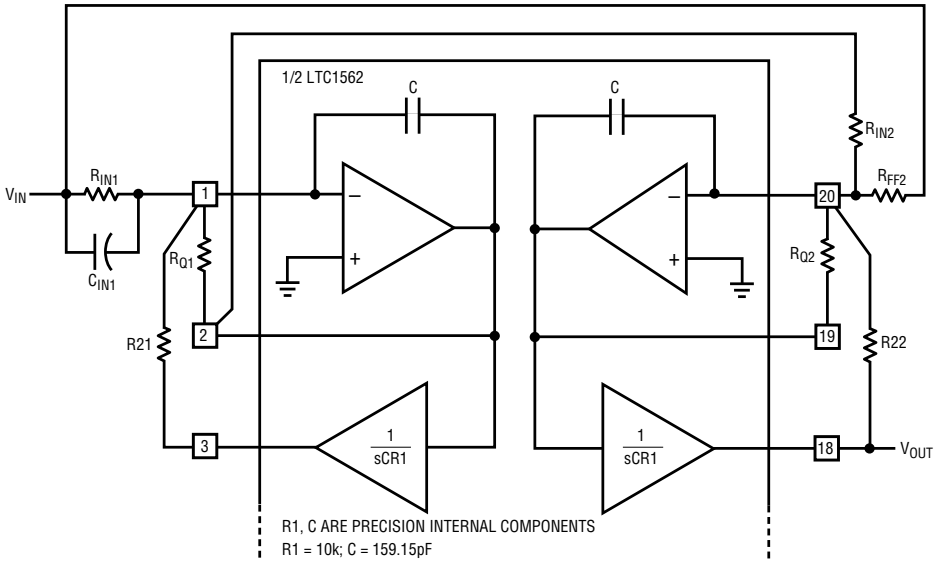


Figure 3. Hardware implementation of a 4th order pseudo-elliptic filter using one-half of an LTC1562 quad Operational Filter IC

2. Calculate the Q-setting resistor, R_{Q1}:

   $R_{Q1} = Q1 \bullet \sqrt{(R21 \bullet 10k)}$
   (choose the closest 1% value)
   R_{Q1} = 20k (1%)

Note: The calculations for R21 and R_{Q1} are from the LTC1562 Data Sheet; they are applicable to any 2nd order section using the LTC1562 proprietary architecture.

3. Calculate the input resistor, R_{IN1}, from the following expression:

$$R_{IN1} = Q1 \bullet \sqrt{[R_{Q1} \bullet (1 - \left(\frac{f_{O1}}{f_{n1}}\right)^2)]^2 + (R21 \bullet 10k\Omega)}$$

R_{IN1} = 39.36k

Make sure that R_{IN1} > R21; If not, make R_{IN1} = R21 and proceed to Step 4a.

Note: $R21/R_{IN1}$ is the DC gain from the input to the lowpass output of the first building block, pin 3. The expression for R_{IN1} ensures optimum dynamic behavior of all nodes of the LTC1562.

4a. Use the value of R_{IN1}, calculated above, and calculate the value of the input capacitor C_{IN1} from the notch equation (2).

$C_{IN1} = 159.15pF \bullet \{(R_{Q1}/R_{IN1}) \bullet [(1 - (f_{O1}/f_{n1})^2]\}$
C_{IN1} = 60.14pF

Use a commercially available NPO-type 0402 surface mount capacitor with the value nearest the ideal value of C_{IN1} calculated above. For instance, if $C_{IN1\ (ideal)}$ is 60.14pF, choose an off-the-shelf 56pF standard value.

4b. Recalculate the value of R_{IN1} after a C_{IN1} of 56pF is chosen.

$R_{IN1} = (C_{IN1(ideal)} \bullet R_{IN1(ideal)})/C_{IN(NPO, 0402)}$
(choose the closest 1% value)
R_{IN1} = 42.2k (1%)

5. Calculate the frequency- and Q-setting resistors R22, R_{Q2}, as done in steps 1 and 2, above. Choose the closest 1% standard resistor values.

   R22 = 13.3k (1%); R_{Q2} = 7.32k (1%)

6. Calculate the feedforward resistor, R_{FF2}:

   R_{FF2} = R22/(DC gain),
   R_{FF2} = 13.3k
   DC gain = V_{OUT}/V_{IN} (DC) = 1

7. Calculate the input resistor R_{IN2}, to satisfy the gain condition for the notch (1).

   $R_{IN2} = R_{FF2} \bullet (R_{Q1}/R_{IN1})$
   R_{IN2} = 6.34k (1%)

Make the practical value of R_{IN2} as close as possible to the value calculated above; otherwise, the stopband notch depth will be affected.

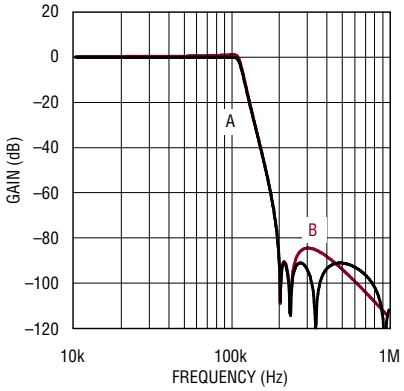


Figure 4. Amplitude responses of 8th order 100kHz elliptic lowpass filters comprising four cascaded 2nd order biquad sections (A) and the filter after the two highest notch frequencies are raised to infinity

An Example Using FilterCAD

The following is a comprehensive example of how to synthesize and realize a complex lowpass filter using two "p-e" 4th order sections in cascade. FilterCAD for Windows will be used to synthesize the filter.

A classical 8th order, 100kHz lowpass elliptic filter with theoretical passband ripple, A_{MAX}, of 0.005dB, and a minimum stopband attenuation, A_{MIN}, of 85dB at twice cutoff, can be synthesized by cascading four biquadratic 2nd order sections, as shown in Table 1. Each biquadratic section comprises a complex pole pair of center frequency f_O, and an imaginary zero pair of notch frequency f_n. The amplitude response is shown in Figure 4, curve A. The filter above is easily transformed into two cascadable 4th order "p-e" sections by performing the following steps.

1. Set the two highest notch frequencies to infinity and expect a decrease in stopband attenuation as well as gain peaking in the vicinity of the cutoff frequency (Figure 4, curve B).
2. Use the interactive capability of FilterCAD to increase the frequency of the right hand notch (Figure 5 curve C), until the stopband ripple has equal peaks.
3. Use the interactive capability of FilterCAD to flatten the passband by lowering the Qs. Start with the highest Q, then proceed with the second highest, then the third.

Table 2 illustrates the parameters of the transformed filter. Compared to Table 1, two notch frequencies are set to infinity, one notch frequency has been increased and the three highest Qs have been reduced. Figure 5, curve C, illustrates the amplitude response of the transformed filter. The original filter shown in Figure 4 is also shown in Figure 5, curve A, for comparison. The main difference between curves A and C is the theoretical stopband attenuation. Curve C, with its lower Q, will also exhibit improved transient behavior.

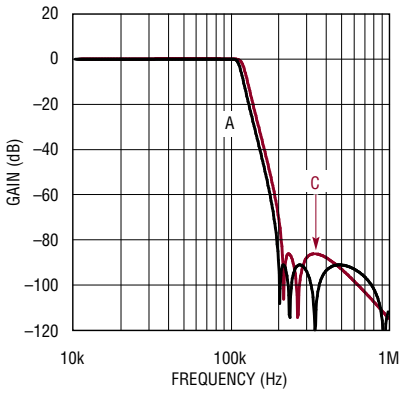


Figure 5. Comparison of original 8th order 100kHz elliptic filter (A) and filter transformed by FilterCAD into two cascaded 4th order "p-e" sections (C)

A Practical Case

The high Qs of the previous synthesized filters ensure, at least in theory, passband flatness all the way up to the cutoff frequency. In practice, errors occur in the vicinity of the filter cutoff. They are most often manifested as gain peaking and they are caused by the tolerances of the passive components and the finite bandwidth of the active circuitry. The gain peaking at the filter cutoff can be addressed by predistorting the high Q section, that is, by intentionally lowering the Q so that the theoretical response will show some gain rolloff at the cutoff frequency.

The synthesized filter of Table 2 can be efficiently realized by two cascaded "p-e" 4th order sections, as illustrated in the block diagram, Figure 6. Note the arrangement of the pole-zero pairs of Figure 6 and compare it with Table 2. In Table 2, the sections appear in order of increasing f_O and Q. In Figure 6, within each 4th order "p-e" filter, the 2nd order section with the highest Q is placed first; the 4th order "p-e" filter containing the highest Q is cascaded last. The notches (f_{n1} and f_{n2}) are so arranged that the highest frequency notch is formed from the pole pair whose center frequency (f_O) is closest to the filter cutoff frequency. For example, the 250kHz notch is placed with the 99.99kHz pole pair. This nonobvious arrangement allows for a stopband attenuation approaching the theoretical values. The highest Q of 5.87 is

Table 1. Parameters of 8th order, 100kHz lowpass elliptic filter synthesized by cascading four biquadratic 2nd order sections

f_0	Q	f_n
61.8049e3	0.5471	957.9224e3
81.2817e3	0.9230	343.0259e3
99.9948.e3	1.9047	235.4796e3
109.8890e3	6.4428	203.3896e3

Table 2. Parameters of Table 1's filter transformed into two cascadable, 4th order "p-e" sections

f_0	Q	f_n
61.8000e3	0.5471	∞
81.2800e3	0.9046	∞
99.9900.e3	1.7555	250.6400e3
109.8800e3	5.874	203.3900e3

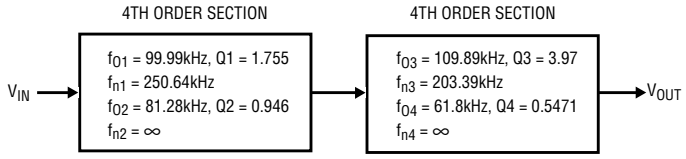


Figure 6. Realization of Table 2's filter with two cascaded 4th order "p-e" sections

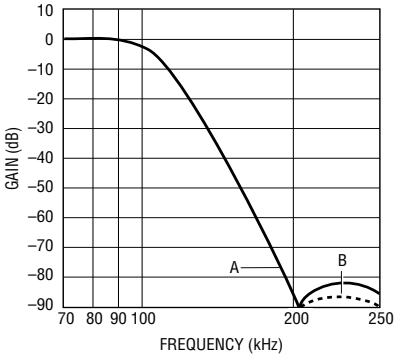


Figure 7. Amplitude response of Figure 7's filter before (A) and after (B) R_{Q1} was lowered to 16.2k to better define the notch.

reduced to 3.97 for reasons mentioned above and for improving the transient response of the circuit. See Figure 7 for the amplitude response; note the slight rolloff at the cutoff frequency. Figure 8 shows the complete hardware realization using all four sections of an LTC1562 continuous-time quad Operational Filter IC. The algorithm outlined above was followed to calculate the values of the external passive components. The circuit occupies as much real estate as a U.S. dime. This is quite significant considering the cumbersome alternative of a fully discrete realization with op amps, Rs and Cs.

Experimental Results

Figure 7, curve A, shows the amplitude response of the filter hardware illustrated in Figure 8. No attempt was made to adjust any component. Both notches are fully resolved, but due to the tolerances of the components and the finite bandwidth of the active circuitry, the stopband attenuation, although impressive, is 2dB above the theoretical value. Subsequently, the value of R_{Q1} was lowered to 16.2k (curve B) to better define the first notch. The filter reaches attenuation levels beyond 85dB all the way up to 0.5MHz input frequencies. The measured attenuation at 1MHz was still better than 78dB. The dynamic range of the circuit is quite impressive: the measured wideband noise was 40µV_{RMS} and the THD for 1V_{RMS} and 50kHz input signal was better than –80dB.

[1] Hauser, Max. "Universal Continuous-Time Filter Challenges Discrete Designs." *Linear Technology* VIII:1 (February 1998), p.1.

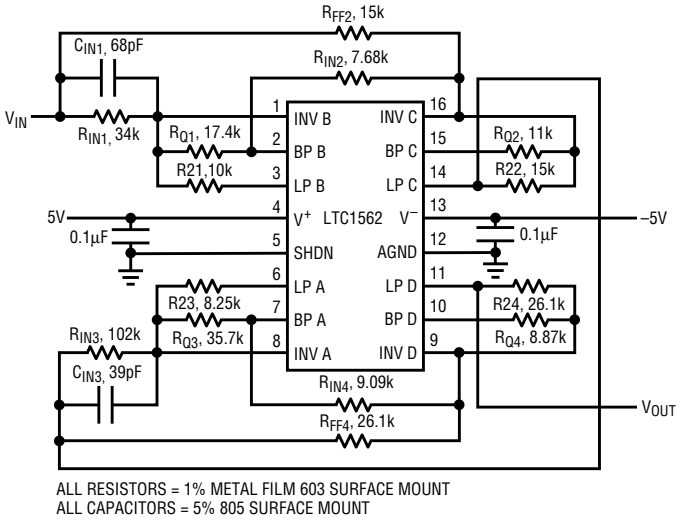


Figure 8. Hardware realization of the filter in Figure 6, using all four sections of an LTC1562.

Flyback, continued from page 27

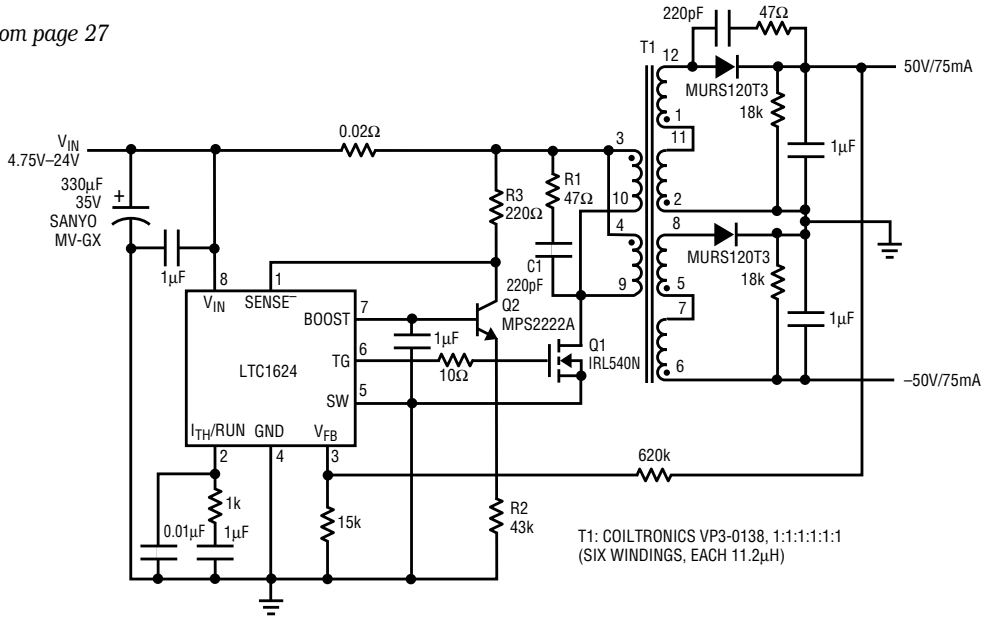


Figure 2. Wide-input-range flyback regulator provides ±50V at 75mA.

Burst Mode™ operation (a feature that improves efficiency at light load conditions by skipping switching cycles). The LTC1624's 95% maximum duty cycle accommodates the 5-to-1 input voltage range. Finally, by reconfiguring T1's secondaries, a variety of output configurations, such as 24V out (four windings in parallel), single 50V/150mA or a single 100V output, are possible with this same basic circuit.

LT1610 Micropower Step-Up DC/DC Converter Runs at 1.7MHz

by Steve Pietkiewicz

Introduction

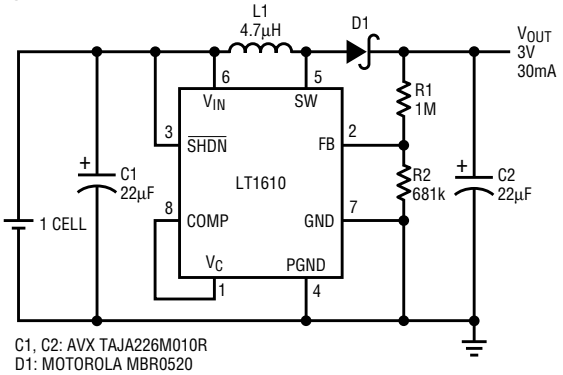
When designing portable electronics, be it a pager, handheld computer or cell phone, "footprint" is one of the most important specifications of any component. Most such products use at least one DC/DC converter to generate regulated voltages from a battery. The LT1610, a micropower DC/DC converter IC, addresses the issue of footprint in several ways. First, the switching frequency is 1.7MHz, allowing the use of small, inexpensive, minimal-height inductors and capacitors. Second, the frequency-compensation components have been integrated, eliminating the requirement for an external RC network in most applications. Finally, the device comes in LTC's 8-lead MSOP package, one-half the size of the 8-lead SO package.

The LT1610's input voltage ranges from 1V to 8V, and the 30V, 300mA switch allows several different configurations, such as boost, SEPIC and flyback, to be successfully implemented. Output voltage can be up to 28V in boost mode. Operating quiescent current is 50µA unloaded; grounding the shutdown pin reduces the current to 0.5µA. The device can generate 3V at 30mA from a single (1V) cell, or 5V at 100mA from two cells (2V). Configured as a Li-Ion cell to 3.3V SEPIC converter, the LT1610 can deliver 100mA. In boost mode, efficiency ranges from 60% at a 100µA load to 83% at full load.

Single-Cell to 3V DC/DC Converter

A 1V to 3V boost converter is shown in Figure 1. The specified components take up very little board space. The 4.7µH Murata inductor specified measures 2.5mm by 3.2mm and is only 2mm high. The 22µF AVX "A" case tantalum capacitors measure 1.6mm by 3.2mm and are 1.6mm tall. Circuit efficiency, which reaches 77%, is detailed in Figure 2. Transient response to a 1mA to 31mA load step is pictured in Figure 3. The device features Burst Mode operation at light loads. This can be seen at a load of 1mA. When the load is increased to 31mA, the device shifts to constant-frequency switching and peak switch current is controlled to achieve output regulation.

continued on page 35



C1, C2: AVX TAJA226M010R
D1: MOTOROLA MBR0520
L1: MURATA LQH3C4R7M24

Figure 1. Single cell to 3V converter delivers 30mA.

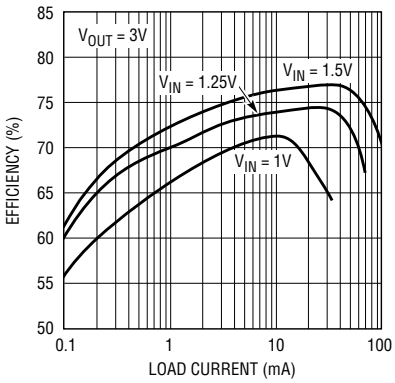


Figure 2. Single-cell converter efficiency reaches 77%.

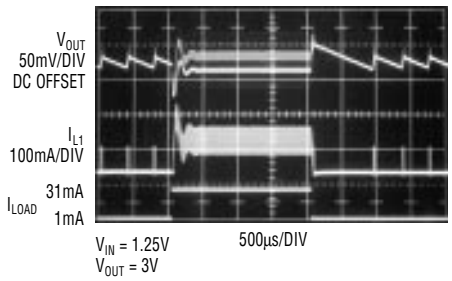
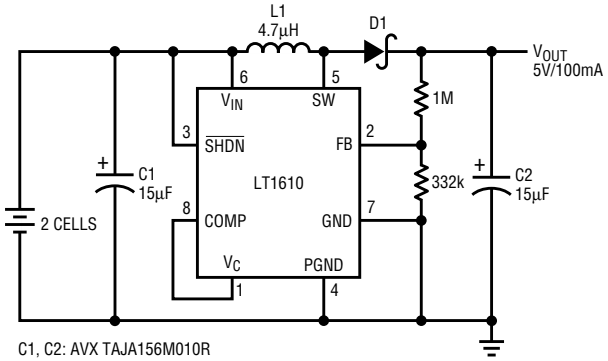


Figure 3. Transient load response of single-cell converter, load stepped from 1mA to 31mA



C1, C2: AVX TAJA156M010R
D1: MOTOROLA MBR0520
L1: SUMIDA CD43-4R7
MURATA LQH3C4R7M24

Figure 4. 2 cell to 5V converter delivers 100mA at 2V input.

An Optimized, Low Distortion, Lower Power ADSL Line Driver Using the LT1207

by Adolfo A. Garcia

Introduction

High speed ADSL modems require high output voltage/current, high speed operational amplifiers to deliver large signals under peak conditions depending upon the characteristics of the line code used. In the ADSL market, two prevalent codes are in use: DMT (discrete multitone) and CAP (carrierless amplitude/phase) modulation. DMT modulation uses a large number of phase-locked carriers to transmit data over cable. As a result, current DMT systems for ADSL exhibit high crest factors (peak to RMS) of 5.33:1. CAP-based systems, on the other hand, use single-carrier modulation and exhibit lower crest factors of 3:1. In these ADSL systems, data is transmitted over two separate frequency bands and at different RMS power levels. The lower frequency band, labeled "upstream," is defined by a 30kHz to 140kHz spectral band with the upper frequency band, labeled "downstream," defined by a 170kHz to 1.5MHz spectral band. In these systems, the RMS signal power transmitted over the downstream band is 20dBm. The RMS signal power transmitted over the upstream band is 13dBm and the reference impedance level for ADSL systems in general is 100Ω.

Even though the transmitted RMS power is fairly low, large crest factors produce large peak signal/power levels that must be cleanly processed to avoid bit-error-rate degradation. DMT systems require 70dBc dynamic performance under peak conditions; CAP-based systems require 60dBc dynamic performance. Table 1 summarizes peak voltage and current levels required for DMT- and CAP-based systems.

To handle these peak signal levels, current solutions in the marketplace use amplifiers with very high quiescent currents—35mA or more. To generate the required peak output voltage drive, these amplifiers are commonly operated from ±15V supplies and, as a result, can produce a zero-load power dissipation over 1 Watt. It is this high static power dissipation that prevents modem manufacturers from implementing multiline modem cards in the central office because of the large amount of PC board area required to heat sink the device.

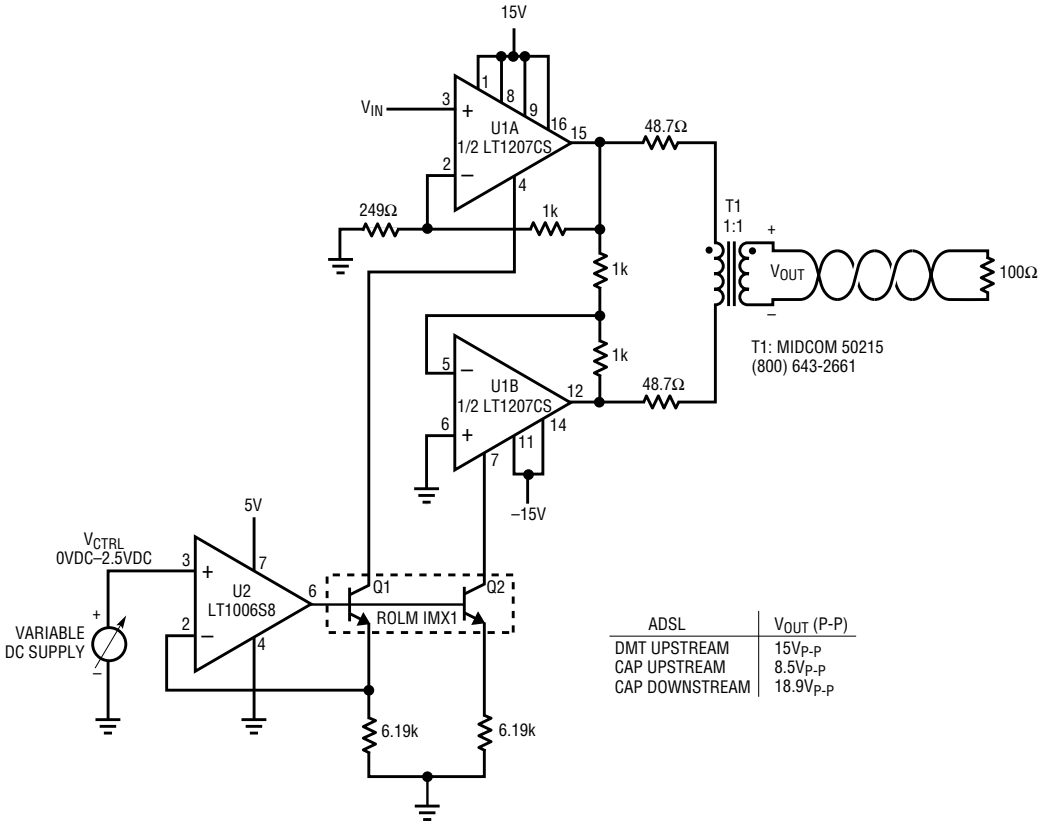


Figure 1. A versatile, high performance, LT1207-based differential ADSL transmitter with amplifier quiescent current control

Table 1. Peak voltage and current levels for DMT- and CAP-based systems

ADSL	Nominal Transmit Power	Peak Voltage	Peak Current
DMT Upstream	13dBm	$15V_{P-P}$	$150mA_{P-P}$
CAP Upstream	13dBm	$8.5V_{P-P}$	$85mA_{P-P}$
CAP Downstream	20dBm	$18.9V_{P-P}$	$189mA_{P-P}$

The circuit in Figure 1 builds upon differential line driver design ideas first illustrated in the May 1996 issue of *Linear Technology* magazine[1] with a twist to address the issue of static and dynamic power dissipation in line-driver amplifiers.

Line-Driver Quiescent Current Control

Line-driver amplifiers expend a significant amount of power to deliver signal power to the load (otherwise known as dynamic power dissipation). Of the total power dissipated by an amplifier, 50% to 60% of the power consumed can come from static power dissipation. Reducing the quiescent power without sacrificing speed or performance allows the line driver circuit to run cooler and use less pc board area—two factors that are very important in the implementation of multiline high speed modem cards.

A unique feature in the LT1207 family of CFAs (for example, the LT1210 and the LT1206) is the ability to control amplifier quiescent current via the SHUTDOWN pin. Originally intended to be used with an external resistor connected to GND or with an open-collector/-drain device under digital control, a programmable current sink can be used to change the bias current to properly match the power dissipation in the amplifiers to the dynamic requirements of the application.

To use this feature, an amplifier-quiescent-current control loop circuit has been added to the basic differential line driver circuit shown in Figure 1. The control loop consists of U2, Q1/Q2 (a dual matched NPN transistor), and a pair of 6.19k resistors. These components are combined to form two matched current sinks designed to operate from 0µA to 400µA. Over this control current range, the quiescent current of the LT1207's internal CFAs can be set from 200µA to 18mA each.

A DC voltage of 0V to 2.5V is applied to U2's noninverting input to set amplifier quiescent current. As designed for the LT1207CS, the control circuit's transfer characteristic is 7.2mA/V. Thus, a zero-volt setting on V_{CTRL} places both amplifiers in a shutdown state, where the amplifier supply current drops to less than 200µA for each. A 2.5V setting on V_{CTRL} biases both amplifiers to their maximum supply current. If a DC voltage source or a voltage-output DAC is not available for the control circuit, a housekeeping microcontroller's timer output can generate a PWM signal that can be filtered and then used as the DC control voltage.

Performance

The circuit in Figure 1 was evaluated at each of the three peak output levels shown in the table. For ADSL upstream applications, a 100kHz single-tone sine wave was used to evaluate the line driver's harmonic distortion performance as a function of amplifier quiescent current control. In each of the three cases, the output signal was attenuated to obtain maximum sensitivity from the HP4195A network analyzer used for the measurements.

Figure 2 illustrates the dynamic performance of the line driver circuit at an output level of $15V_{P-P}$ into the 100Ω load. The 3rd order harmonic distortion (3HD) is approximately 70dBc (sufficient for peak-power DMT remote-terminal operation); this was achieved with an amplifier quiescent current of 6mA each. With an output level of $8.5V_{P-P}$ for CAP-based remote-terminal applications, the circuit exhibits 64dBc dynamic performance (shown in Figure 3), with the line-driver amplifiers operating at 2mA each. The presence of a pronounced 2nd order artifact (2HD) is indicative of current starvation in the line-driver amplifier core. Incrementally increasing the supply current of the amplifier is effective in reducing this 2nd order harmonic distortion.

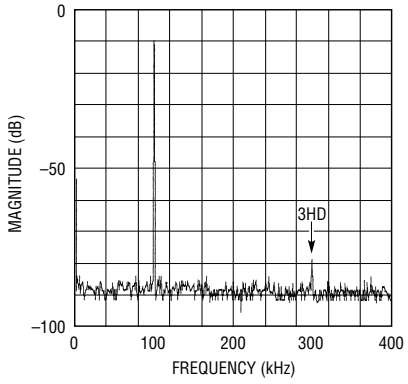


Figure 2. Harmonic distortion performance of Figure 1's circuit with a 100kHz sine wave at $15V_{P-P}$ into 100Ω

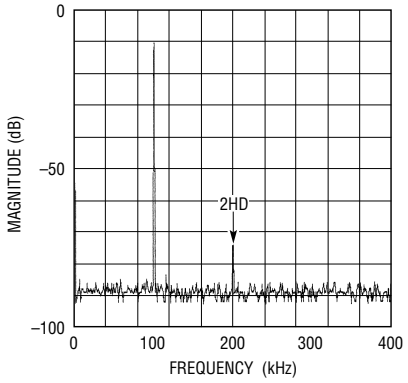


Figure 3. Harmonic distortion performance of Figure 1's circuit with a 100kHz sine wave at $8.5V_{P-P}$ into 100Ω

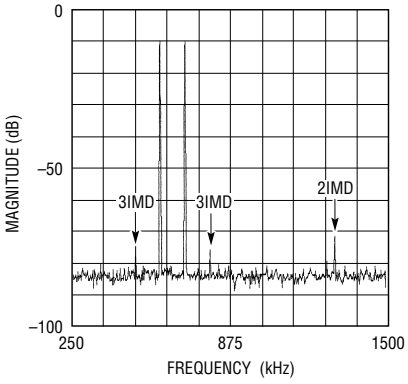


Figure 4. 2-tone intermodulation distortion performance of Figure 1's circuit (See text for additional details.)

Although single-tone distortion measurements are a good indicator of circuit performance in single-carrier applications, they do not provide any insight into amplifier linearity when processing more that one tone at a time. An effective tool in gauging dynamic performance in these applications is 2-tone intermodulation. Figure 4 illustrates the performance of Figure 1's circuit with two sine waves at 600kHz and 700kHz. The frequency spectrum displayed is representative of both DMT and CAP downstream operation, and the two tones were chosen to show both 2nd and 3rd order IMD products (2IMD and 3IMD) that fall in-band. With a 1:1 turns-ratio transformer, the output level of the circuit was adjusted to produce an $18.9V_{P-P}$ envelope across the 100Ω load. This output voltage level implies a peak differential voltage across the line driver outputs of approximately $38V_{P-P}$. With each amplifier operating at a supply current of 13mA, the circuit achieves a spur-free dynamic performance of 63dBc, sufficient for peak power operation in CAP-based systems. Improved performance at lower supply currents can be achieved with a transformer turns ratio greater than 1:1, whereby amplifier output current drive is substituted for amplifier output voltage drive.

Conclusion

Under DC voltage or digital control, the quiescent supply current of the line-driver CFAs can be adjusted (statically or dynamically) to reduce their static power dissipation without sacrificing either downstream or upstream dynamic performance. In addition, this supply-current control can be coupled with a reduction of the line-driver supply voltage to reduce an amplifier's dynamic power dissipation. The supply voltage should not be reduced below a level that causes the amplifier output stage to clip the peak transmitted signal, however. The best method for gauging dynamic performance is to monitor the bit-error-rate (BER) performance of the modem. Under normal DMT or CAP operation (downstream or upstream), the supply voltage and quiescent currents of the line-driver amplifiers can be reduced until the system BER degrades beyond an acceptable minimum.

For additional information on a complete line of driver solutions, featuring the LT1210 (1.1A), the LT1206 (250mA) and the LT1497 (125mA), please consult the LTC factory.

Note:

[1] Hoskins, Kevin. "The LT1207: An Elegant Dual 60MHz, 250mA Current Feedback Amplifier." *Linear Technology* VI:2 (May 1996), pp. 9–13.

LT1610, continued from page 32

2-Cell to 5V DC/DC Converter

By simply changing the feedback resistor values, the LT1610 can generate 5V. Figure 4's circuit generates 5V at a load of up to 100mA from a 2-cell input. Figure 5's graph shows efficiency the of the circuit, which reaches 83%. This circuit is also suitable for 3.3V to 5V conversion, supplying over 200mA.

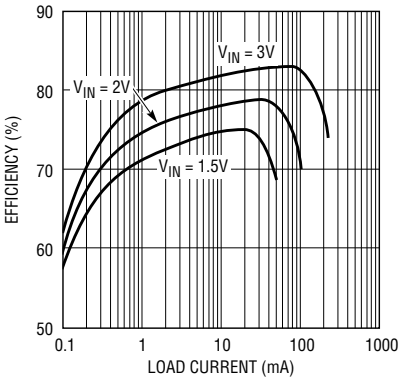


Figure 5. 2-cell converter efficiency reaches 83%.

Li-Ion to 3.3V SEPIC Converter

Figure 6 employs the SEPIC (single ended primary inductance converter) topology to provide a regulated 3.3V output from an input that can range above or below the output voltage. Although the circuit requires two inductors and a ceramic coupling capacitor, the total footprint of this solution is still attractive compared with alternative methods of generating 3.3V, such as a boost converter followed by a linear regulator. The circuit can supply up to 100mA. Efficiency, while lower than that of a standard boost converter, reaches approximately 73%. Unlike a boost converter, this topology provides input-to-output isolation. The output is completely disconnected from the battery in shutdown mode, preventing inadvertent battery discharge through the load. The LT1610's sub-µA shutdown current reduces standby losses, increasing battery life.

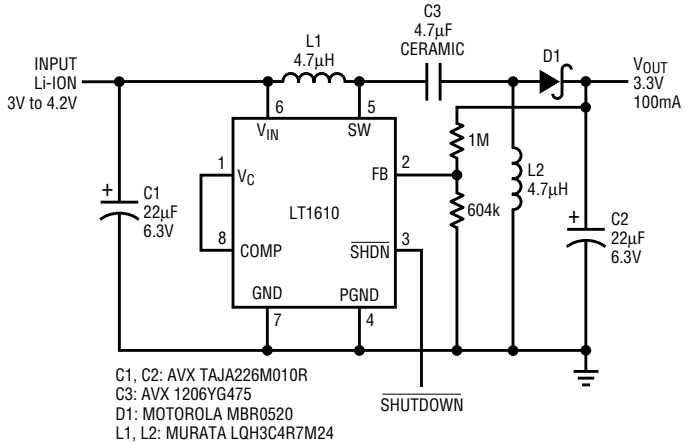


Figure 6. Li-Ion to 3.3V SEPIC converter delivers 100mA.

Positive-to-Negative Converter Powers –48V Telecom Circuits

by Mitchell Lee

If you're designing a system that interfaces to telecom equipment, chances are you'll need a –48V supply. The circuit in Figure 1 supplies up to 6W at –48V and scales to more than 12W with higher power components. Based on the Cúk topology, the converter exhibits excellent efficiency over a wide range of loading conditions (see Figure 2).

The LT1171's error amplifier is designed for positive-boost applications, and hence its gain and reference are of the wrong phase and polarity for sensing an inverted output. In this application, the error amplifier is simply bypassed and feedback is applied at the compensation (V_C) pin. Zener diode D2 senses the output, pulling down on Q1 and the V_C pin, in response to small increases in output voltage. Pulling down on the V_C pin reduces peak switch current, and constitutes negative feedback. If the output is a little low, the Zener's diminished feedback signal is overcome by an internal 200µA current source at the V_C pin, thereby increasing peak switch current and restoring the output voltage.

The combination of the LT1171 and the VP-2 series VERSA-PAC™ coil (CTX02-13836) are suited for 120mA output current as shown. For lighter loads of up to 60mA, use the LT1172 and a VP-1-series equivalent to the coil shown. For up to 15W, use the LT1171 and a VP-5 equivalent. High voltage versions of the LT1170 family (-HV) allow inputs of up to 20V without exceeding the peak switch-voltage rating.

This converter starts working at 2.7V and will regulate –48V at reduced power. You can add undervoltage lockout by inserting a Zener diode (V_Z = $V_{LOCKOUT}$ – 2.7V) between the input supply and the LT1172's V_{IN} pin.

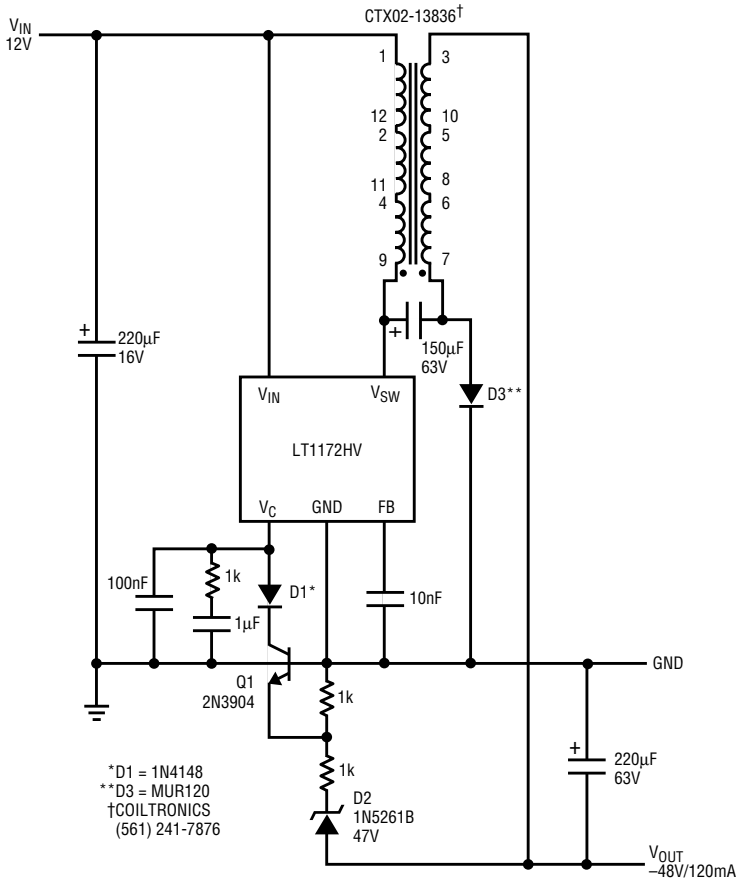


Figure 1. 12V to –48V features good efficiency over a wide range of loads.

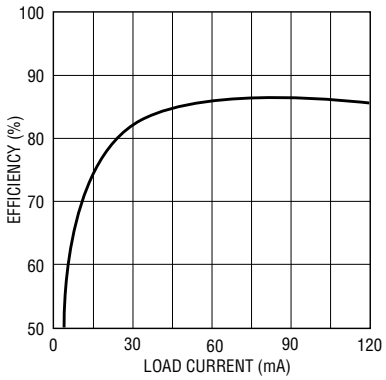


Figure 2. Converter efficiency rises to 80% at only 20mA load.

VERSA-PAC is a trademark of Coiltronics, Inc.

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

Bootstrapped Synchronous Boost Converter Operates at 1.8V Input

by Tom Gross

Some applications, such as those powered by batteries or solar cells, see their input voltage decrease as they operate. The circuit in Figure 1 maintains the maximum load current as the input voltage drops. The regulator boosts a 2.5V–4.2V input to 5V. The maximum load current is 2A (10W of output power).

The circuit is a bootstrapped synchronous boost regulator using an LTC1266 synchronous regulator controller. Diodes D2 through D5 allow the circuit to start-up using the (low) input voltage and then to be powered during normal operation by the higher output voltage. The crucial elements in this circuit are the switches: two IRF7401 N-channel MOSFETs. These MOSFETs are fully enhanced at very low gate-to-source voltages (at 2V of V_{GS}, the peak drain current is rated at 15A). The low enhancement voltages allow the circuit to start up at low input voltages (crucial for low series-cell-count, battery-powered applications). Diodes D3 and D4, along with capacitor C2, form a charge-pump circuit, which the controller uses for the MOSFETs' gate drive. The switches are driven by an LTC1266 synchronous regulator controller.

Because the circuit is powered from the 5V output, it will still operate if the input supply voltage drops below the minimum input voltage of the IC. This bootstrapping allows the circuit to start up even when the input voltage is below the minimum input voltage of the IC (3.5V). With a 1A load, the regulator operates down to 1.8V.

Figure 2 shows the efficiency of the regulator versus the input voltage at three different load currents. At 2A of load current, efficiency drops as the input voltage is decreased due to the higher power losses in the inductor. A larger inductor will increase efficiency and/or allow for larger load currents. The efficiency with the indicated inductor is good, averaging 87% overall. Higher efficiency will help to increase the run time of battery-powered applications.

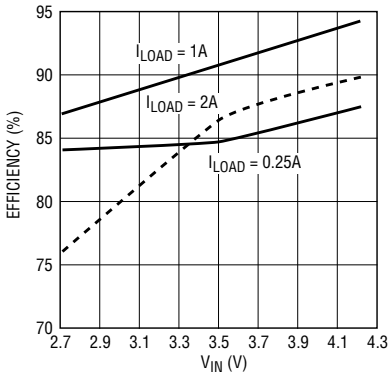


Figure 2. Efficiency of Figure 1's circuit

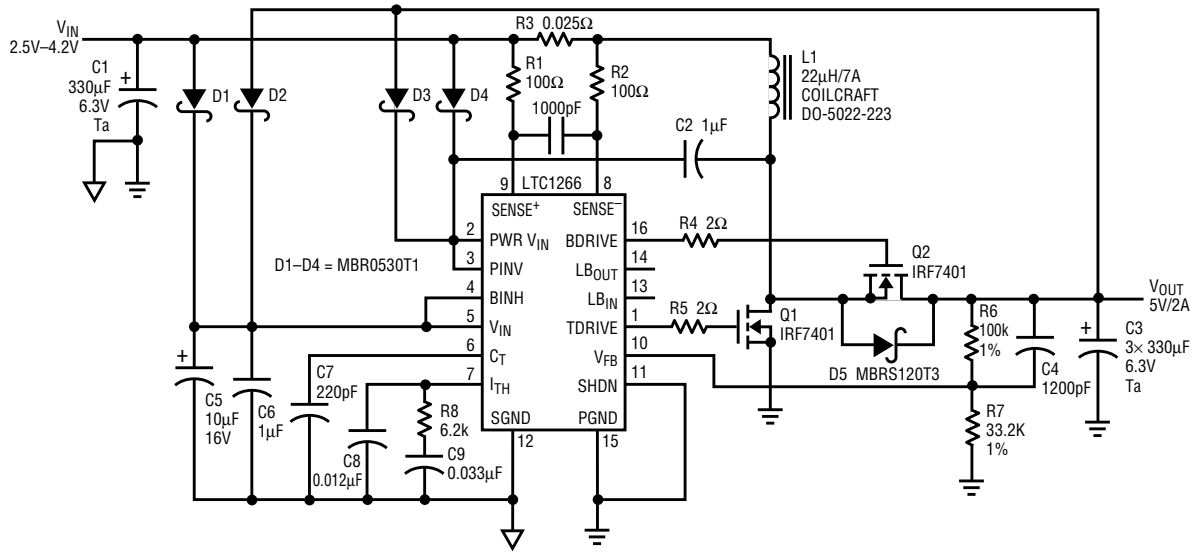


Figure 1. Bootstrapped synchronous boost converter

Battery-Powered Buck-Boost Converter Requires No Magnetics

by John Seago

One of the problems that designers of portable equipment face is generating a regulated voltage that is between the charged and discharged voltage of a battery pack. As an example, when generating a 3.3V output from a 3-cell battery pack, the regulator input voltage changes from about 4.5V at full charge to about 2.7V when discharged. At full charge, the regulator must step down the input voltage, and when the battery voltage drops below 3.3V, the regulator must step up the voltage. The same problem occurs when a 5V output is required from a four-cell input voltage that varies from about 3.6V to 6V. Ordinarily, a flyback or SEPIC configuration is required to solve this problem.

The LTC1515 switched capacitor DC/DC converter, can provide this buck-boost function for load currents up to 50mA with only three external capacitors. The circuit shown in Figure 1 will provide a regulated 3.3V output from a three-cell input or a 5V output from a four-cell input. Connecting the 5/3 pin to V_{IN} will program the output to 5V, whereas grounding the 5/3 pin programs the output to 3.3V.

The absence of bulky magnetics provides another benefit: this circuit requires only 0.07 square inches of board space in those applications where components can be mounted on both sides of the board. The addition of R1 provides a power-on-reset flag that goes high 200ms after the output reaches 93.5% of its programmed value. The $\overline{SHDN}$ pin allows the output to be turned on or off with a 3V logic signal.

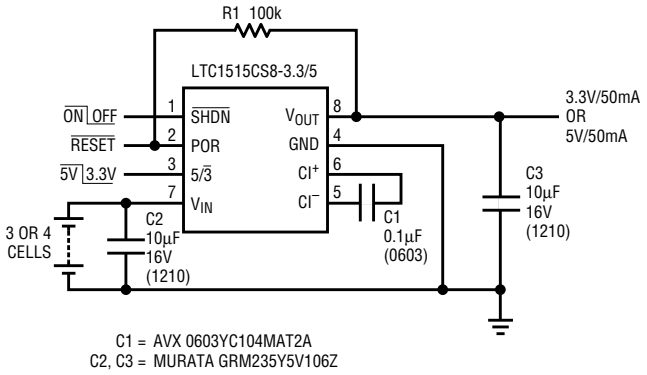


Figure 1. Battery-powered buck-boost converter

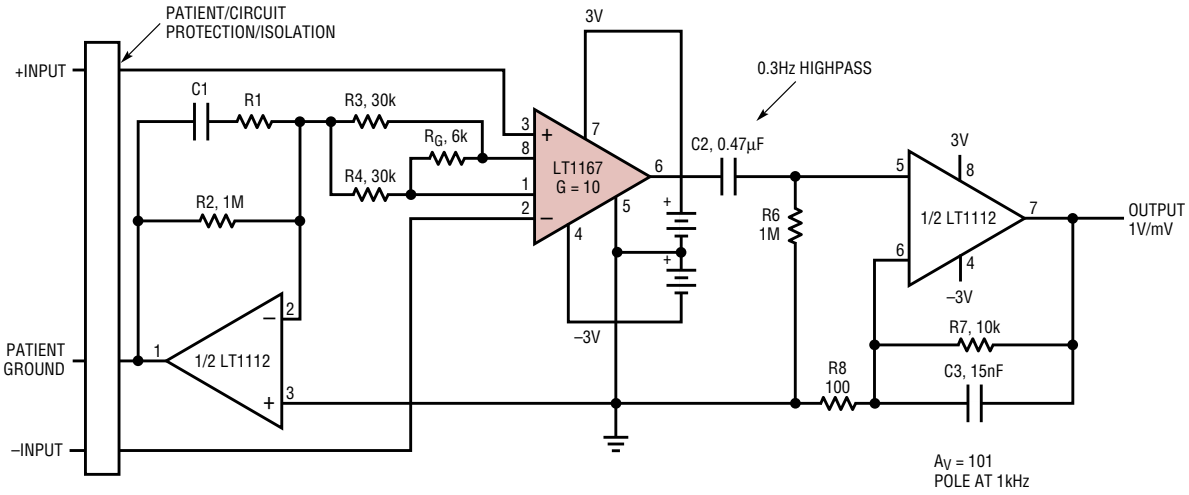


Figure 8. Medical ECG monitor

LT1167, continued from page 9

Conclusion

The LT1167 instrumentation amplifier delivers the best precision, lowest noise, highest fault tolerance, plus the ease of use provided by single-resistor gain setting. The LT1167 is offered in 8-pin PDIP and SO packages. The SO uses significantly less board space than discrete designs. With these advantages and the ability to operate over a wide range of supply voltages at a quiescent current of 0.9mA, the LT1167 is appropriate for a wide range of applications.

DESIGN TOOLS

Applications on Disk

FilterCAD™ 2.0 CD-ROM — This CD is a powerful filter design tool that supports all of Linear Technology's high performance switched capacitor filters. Included is FilterView™, a document navigator that allows you to quickly find Linear Technology monolithic filter data sheets, the FilterCAD manual, application notes, design notes and *Linear Technology* magazine articles. It *does not* have to be installed to run FilterCAD. It is not necessary to use FilterView to view the documents, as they are standard .PDF files, readable with any version of Adobe Acrobat™. FilterCAD runs on Windows® 3.1 or Windows 95. FilterView requires Windows 95. The FilterCAD program itself is also available on the web and will be included on the new LinearView™ CD. Available at no charge.

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp. Available at no charge

SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim. Available at no charge

SwitcherCAD™ — The SwitcherCAD program is a powerful PC software tool that aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. 144 page manual included. $20.00

SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

Micropower SwitcherCAD™ — The MicropowerSCAD program is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components which surround the DC/DC converter. In the case of a battery supply, MicropowerSCAD can perform a battery life simulation. 44 page manual included. $20.00

MicropowerSCAD supports the following LTC micropower DC/DC converters: LT1073, LT1107, LT1108, LT1109, LT1109A, LT1110, LT1111, LT1173, LTC1174, LT1300, LT1301 and LT1303.

Technical Books

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook, Vol II — This 1248 page supplement to the 1990 Linear Databook is a collection of all products introduced in 1991 and 1992. The catalog contains full data sheets for over 140 devices. The 1992 Linear Databook, Vol II is a companion to the 1990 Linear Databook, which should not be discarded. $10.00

1994 Linear Databook, Vol III —This 1826 page supplement to the 1990 and 1992 Linear Databooks is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The 1994 Linear Databook Vol III is a companion to the 1990 and 1992 Linear Databooks, which should not be discarded. $10.00

1995 Linear Databook, Vol IV —This 1152 page supplement to the 1990, 1992 and 1994 Linear Databooks is a collection of all products introduced since 1994. A total of 80 product data sheets are included with updated selection guides. The 1995 Linear Databook Vol IV is a companion to the 1990, 1992 and 1994 Linear Databooks, which should not be discarded. $10.00

1996 Linear Databook, Vol V —This 1152 page supplement to the 1990, 1992, 1994 and 1995 Linear Databooks is a collection of all products introduced since 1995. A total of 65 product data sheets are included with updated selection guides. The 1996 Linear Databook Vol V is a companion to the 1990, 1992, 1994 and 1995 Linear Databooks, which should not be discarded. $10.00

1997 Linear Databook, Vol VI —This 1360 page supplement to the 1990, 1992, 1994, 1995 and 1996 Linear Databooks is a collection of all products introduced since 1996. A total of 79 product data sheets are included with updated selection guides. The 1997 Linear Databook Vol VI is a companion to the 1990, 1992, 1994, 1995 and 1996 Linear Databooks, which should not be discarded. $10.00

1990 Linear Applications Handbook, Volume I — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook, Volume II — Continues the stream of "real world" linear circuitry initiated by the 1990 Handbook. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. References and articles from non-LTC publications that we have found useful are also included. $20.00

1997 Linear Applications Handbook, Volume III — This 976 page handbook maintains the practical outlook and tutorial nature of previous efforts, while broadening topic selection. This new book includes Application Notes 55 through 69 and Design Notes 70 through 144. Subjects include switching regulators, measurement and control circuits, filters, video designs, interface, data converters, power products, battery chargers and CCFL inverters. An extensive subject index references circuits in LTC data sheets, design notes, application notes and *Linear Technology* magazines. $20.00

Interface Product Handbook — This 424 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422, V.35 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, mixed RS232 and RS485 devices, 10kV ESD protection of RS232 devices and surface mount packages. Available at no charge

Power Solutions Brochure — This 84 page collection of circuits contains real-life solutions for common power supply design problems. There are over 88 circuits, including descriptions, graphs and performance specifications. Topics covered include battery chargers, PCMCIA power management, microprocessor power supplies, portable equipment power supplies, micropower DC/DC, step-up and step-down switching regulators, off-line switching regulators, linear regulators and switched capacitor conversion. Available at no charge

High Speed Amplifier Solutions Brochure — This 72 page collection of circuits contains real-life solutions for problems that require high speed amplifiers. There are 82 circuits including descriptions, graphs and performance specifications. Topics covered include basic amplifiers, video-related applications circuits, instrumentation, DAC and photodiode amplifiers, filters, variable gain, oscillators and current sources and other unusual application circuits. Available at no charge

Data Conversion Solutions Brochure — This 64 page collection of data conversion circuits, products and selection guides serves as excellent reference for the data acquisition system designer. Over 60 products are showcased, solving problems in low power, small size and high performance data conversion applications—with performance graphs and specifications. Topics covered include ADCs, DACs, voltage references and analog multiplexers. A complete glossary defines data conversion specifications; a list of selected application and design notes is also included. Available at no charge

Telecommunications Solutions Brochure — This 72 page collection of circuits, new products and selection guides covers a wide variety of products targeted for the telecommunications industry. Circuits solving real life problems are shown for central office switching, cellular phone, base station and other telecom applications. New products introduced include high speed amplifiers, A/D converters, power products, interface transceivers and filters. Reference material includes a telecommunications glossary, serial interface standards, protocol information and a complete list of key application notes and design notes. Available at no charge

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CD-ROM Catalog

LinearView — LinearView™ CD-ROM version 3.0 is Linear Technology's latest interactive CD-ROM. It allows you to instantly access thousands of pages of product and applications information, covering Linear Technology's complete line of high performance analog products, with easy-to-use search tools.

The LinearView CD-ROM includes the complete product specifications from Linear Technology's Databook library (Volumes I–VI) and the complete Applications Handbook collection (Volumes I–III). Our extensive collection of Design Notes and the complete collection of *Linear Technology* magazine are also included.

A powerful search engine built into the LinearView CD-ROM enables you to select parts by various criteria, such as device parameters, keywords or part numbers. All product categories are represented: data conversion, references, amplifiers, power products, filters and interface circuits. Up-to-date versions of Linear Technology's software design tools, SwitcherCAD, Micropower SwitcherCAD, FilterCAD, Noise Disk and Spice Macromodel library, are also included. Everything you need to know about Linear Technology's products and applications is readily accessible via LinearView. LinearView runs under Windows 3.1, Windows 95 and Macintosh® System 7.0 or later.

Available **this Summer** at no charge.

World Wide Web Site

Linear Technology Corporation's customers can now quickly and conveniently find and retrieve the latest technical information covering the Company's products on LTC's new internet web site. Located at www.linear-tech.com, this site allows anyone with internet access and a web browser to search through all of LTC's technical publications, including data sheets, application notes, design notes, *Linear Technology* magazine issues and other LTC publications, to find information on LTC parts and applications circuits. Other areas within the site include help, news and information about Linear Technology and its sales offices.

Other web sites usually require the visitor to download large document files to see if they contain the desired information. This is cumbersome and inconvenient. To save you time and ensure that you receive the correct information the first time, the first page of each data sheet, application note and *Linear Technology* magazine is recreated in a fast, download-friendly format. This allows you to determine whether the document is what you need, before downloading the entire file.

The site is searchable by criteria such as part numbers, functions, topics and applications. The search is performed on a user-defined combination of data sheets, application notes, design notes and *Linear Technology* magazine articles. Any data sheet, application note, design note or magazine article can be downloaded or faxed back. (Files are downloaded in Adobe Acrobat PDF format; you will need a copy of Acrobat Reader to view or print them. The site includes a link from which you can download this program.)

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