LINEAR TECHNOLOGY

Third-Generation DC/DC Controllers Reduce Size and Cost

by Randy G. Flatness

Introduction

The LTC1735 and LTC1736 are the newest members of Linear Technology's third generation of DC/DC controllers. These controllers use the same constant frequency, current mode architecture and Burst Mode™ operation as the previous generation LTC1435–LTC1437 controllers but with improved features. With OPTI-LOOP™ compensation, new protection circuitry, tighter load regulation and strong MOSFET drivers, these controllers are ideal for the current and future generations of CPU power applications.

The LTC1735 is pin compatible with the previous generation LTC1435/LTC1435A controllers with only minor external component changes.

Protection features include internal foldback current limiting, output overvoltage crowbar and optional short-circuit shutdown. The 0.8V±1% reference allows the low output voltages and 1% accuracy that will be demanded by future microprocessors. The operating frequency (synchronizable up to 500kHz) is set by an external capacitor, allowing maximum flexibility in optimizing efficiency.

The LTC1736 has all of the features of the LTC1735, plus voltage programming for CPU power, in a 24-lead SSOP package. The output voltage in LTC1736 applications is programmed by a 5-bit digital-to-analog converter (DAC) that adjusts the out-

Figure 1. LTC1736 evaluation circuit: a complete 5V–24V to 0.9V–2V/12A converter in 2.15in² of PC board space

Issue Highlights

Happy New Year and welcome to the ninth volume of *Linear Technology* magazine.

This issue is heavy on power products: our cover article introduces the LTC1735 and LTC1736, the newest members of Linear Technology's third generation of DC/DC controllers. These controllers use the same current mode architecture with constant frequency and Burst Mode operation as the LTC1435–LTC1437 controllers but with improved features. With OPTI-LOOP compensation, new protection circuitry, tighter load regulation and strong MOSFET drivers, these controllers are ideal for the current and future generations of CPU power applications.

This issue debuts the LTC1530, a synchronous buck regulator controller in the SO-8 package. The LTC1530 is a small, versatile controller that is usable in numerous topologies and over a wide range of power levels. In basic buck applications, the LTC1530 permits the designer to realize very simple, low parts count designs that require minimal real estate. With a little ingenuity, it is possible to develop circuits different than those that the part's designers intended, but which give excellent performance nonetheless.

The LT®1505 is a constant-current, constant-voltage, current mode switching battery charger using the synchronous buck topology. Its output voltage is preset for 3–4 Li-Ion cells, but can be programmed from 1V to 21V. It features a 0.5% voltage reference, low dropout operation, programmable wall adapter current limiting and efficiencies to 94%.

Rounding out our selection of switchers are the LT1611 and LT1613. These current mode, constant frequency devices contain internal 36V switches capable of generating output power in the range of 400mW to 2W, in a 5-lead SOT-23 package. The LT1613 has a standard positive feedback pin and is designed to regulate positive voltages. The LT1611 has a novel feedback scheme designed to directly regulate negative output voltages without the use of level-shifting circuitry.

In the filter arena, we premier the LTC1562-2, an extended-frequency version of the LTC1562 quadruple 2nd order, universal, continuous-time filter, described in the February 1998 issue. The LTC1562 introduced Operational Filter™ building blocks, which satisfy diverse filter requirements and applications compactly. The LTC1562-2 has the same block diagram, pinout and packaging as the original LTC1562, but is optimized for higher filter frequencies: 20kHz to 300kHz. Besides covering a full octave of frequencies (150kHz–300kHz) above the range of the LTC1562, the LTC1562-2 also overlaps the LTC1562's utility in the range 20kHz to 150kHz. In this frequency range, the LTC1562-2 typically shows reduced large-signal distortion at a cost of slightly more noise than with the LTC1562.

We also introduce a new data converter: the LTC1597 16-bit parallel, current output, low glitch, multiplying DAC. The LTC1597 has outstanding 1LSB linearity over temperature, ultralow glitch impulse, on-chip 4-quadrant feedback resistors, low power consumption, asynchronous clear and a versatile parallel interface. For 14-bit systems, its pin compatible counterpart, the LTC1591, is an ideal solution. Combined with the LT1468 op amp (introduced in the November 1998 issue), the LTC1597 provides the best in its class, 1.7μs settling time to 0.0015%, while maintaining superb DC linearity specifications. Two rail-to-rail, voltage output DACs can be found in the Design Information section: the 14-bit LTC1658 and the 16-bit LTC1655; these DACs have a flexible 3-wire serial interface that is SPI/QSPI and MICROWIRE™ compatible. They provide a convenient upgrade path for users of LTC's 12-bit voltage output DAC family.

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This issue features a rich selection of Design Ideas, including four different power conversion circuits and the second in a series of articles on designing high order filters with stopband notches using the LTC1562 filter ICs.

The issue concludes with six New Device Cameos. **LT**

put voltage from 0.925V to 2.00V, according to Intel mobile VID specifications.

Details

The LTC1735 and LTC1736 are synchronous step-down switching regulator controllers that drive external N-Channel power MOSFETs using a programmable fixed frequency OPTI-LOOP architecture. OPTI-LOOP compensation effectively removes the constraints placed on C_{OUT} by other controllers for proper operation (such as limits on low ESRs). A maximum duty cycle limit of 99% provides low dropout operation, which extends operating time in battery operated systems. A forced-continuous control pin reduces noise and RF interference and can assist secondary winding regulation by disabling Burst Mode when the main output is lightly loaded. Soft-start is provided by an external capacitor that can be used to properly sequence supplies. The operating current level is user-programmable via an external current sense resistor. A wide input-supply range allows operation from 3.5V to 30V (36V maximum).

Protection

New internal protection features in the LTC1735 and LTC1736 controllers include foldback current limiting, short circuit detection, short-circuit latch-off and overvoltage protection. These features protect the PC board, the MOSFETs and the load itself (the CPU) against faults.
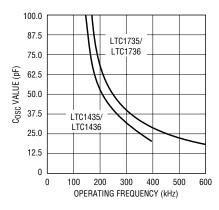

Figure 2. C_{OSC} value vs frequency for the LTC1435/36 and the LTC1735/36

Fault Protection: Overcurrent Latch-Off

The RUN/SS pin, in addition to providing soft-start capability, also provides the ability to shut off the controller and latch off when an overcurrent condition is detected. The RUN/SS capacitor, C_{SS}, (refer to Figure 5) is used initially to turn on and limit the inrush current of the controller. After the controller has been started and given adequate time to charge the output capacitor and provide full load current, C_{SS} is used as a short-circuit timer. If the output voltage falls to less than 70% of its nominal output voltage after C_{SS} reaches 4.2V, it is assumed that the output is in a severe overcurrent and/or short-circuit condition and C_{SS} begins discharging. If the condition lasts for a long enough period, as determined by the size of C_{SS}, the controller will be shut down until the RUN/SS pin voltage is recycled.

This built-in latch-off can be overridden by providing >5µA at a compliance of 4V to the RUN/SS pin (refer to the LTC1735/LTC1736 Data Sheet for details). This external current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition.

Why should you defeat overcurrent latch-off? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off. Defeating this feature will allow easy troubleshooting of the circuit and PC layout. The internal short-circuit detection and foldback current limiting still remain active, thereby protecting the power supply system from failure. After the design is complete, you can decide whether to enable the latch-off feature.

Fault Protection: Current Limit and Current Foldback

The LTC1735/LTC1736 current comparator has a maximum sense voltage of 75mV, resulting in a maximum MOSFET current of 75mV/R_{SENSE}. The LTC1735/LTC1736 includes current foldback to help further limit load current when the output is shorted to ground. If the output falls by more than one-half, the maximum sense voltage is progressively lowered from 75mV to 30mV. Under short-circuit conditions with very low duty cycle, the LTC1735/LTC1736 will begin cycle skipping in order to limit the short-circuit current. In this situation, the bottom MOSFET will be on most of the time, conducting the current. The average short-circuit current will be approximately 30mV/ R_{SENSE}. Note that this function is always active and is independent of the short circuit latch-off.

Fault Protection: Output Overvoltage Protection (OVP)

An output overvoltage crowbar turns on the synchronous MOSFET to blow a system fuse in the input lead when

Operating Condition	Soft Latch	Hard Latch
Fast Transients	Controls Overshoot	Latches Off
Output Shorted to 5V	Output Clamped at OVP	Latches Off
VID Voltage Decrease	Regulates New Voltage	Latches Off
Noise	Controls Output	Latches Off
Shorted Top MOSFET	Bottom MOSFET Overloads	Bottom MOSFET Overloads
Output Voltage Can Reverse	No	Yes
When Overload is Removed	Resumes Normal Operation	Remains Latched Off
Troubleshooting Faults	Easy DC Measurements	Difficult; May Require Digital Oscilloscopes

Table 1. Overvoltage protection comparison

Table 2. FCB possible states

FCB Pin	Condition
DC Voltage: 0V–0.7V	Burst Disabled/ Forced Continuous, Current Reversal Enabled
DC Voltage: > 0.9V	Burst Mode, No Current Reversal
Feedback Resistors	Regulating a Secondary Winding
($V_{FCBSYNC}$ > 1.5V)	Burst Mode Disabled, No Current Reversal

the output of the regulator rises much higher than nominal levels. The crowbar can cause huge currents to flow, greater than in normal operation. This feature is designed to protect against a shorted top MOSFET or short circuits to higher supply rails; it does not protect against a failure of the controller itself.

Previous latching crowbar schemes for overvoltage protection have a number of problems (see Table 1). One of the most obvious, not to mention most annoying, is nuisance trips caused by noise or transients momentarily exceeding the OVP threshold. Each time that this occurs with latching OVP, a manual reset is required to restart the regulator. Far more subtle is the resulting output voltage reversal. When the synchronous MOSFET latches on, a large reverse current is loaded into the inductor while the output capacitor is discharging. When the output voltage reaches zero, it does not stop there, but rather continues to go negative until the reverse inductor current is
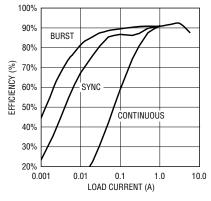

100%
90%
80% BURST
70%
60% SYNC
50%
40% CONTINUOUS
30%
20%
0.001 0.01 0.1 1.0 10.0
LOAD CURRENT (A)
EFFICIENCY (%)

Figure 3. Efficiency vs load current for three modes of operation

depleted. This requires a sizable Schottky diode across the output to prevent excessive negative voltage on the output capacitor and load.

A further problem on the horizon for latching OVP circuits is their incompatibility with on-the-fly CPU core voltage changes. If an output voltage is reprogrammed from a higher voltage to a lower voltage, the OVP will temporarily indicate a fault, since the output capacitor will momentarily hold the previous, higher output voltage. With latching OVP, the result will be another latch-off, with a manual reset required to attain the new output voltage. To prevent this problem, the OVP threshold must be set above the maximum programmable output voltage, which would do little good when the output voltage was programmed near the bottom of its range.

In order to avoid these problems with traditional latching OVP circuits, the LTC1735 and LTC1736 use a new "soft latch" OVP circuit. Regardless of operating mode, the synchronous MOSFET is forced on whenever the output voltage exceeds the regulation point by more than 7.5%. However, if the voltage then returns to a safe level, normal operation is allowed to resume, thereby preventing latch-off caused by noise or voltage reprogramming. Only in the case of a true fault, such as a shorted top MOSFET, will the synchronous MOSFET remain

latched on until the input voltage collapses or the system fuse blows.

The new soft latch OVP also provides protection and easy diagnosis of other overvoltage faults, such as a lower supply rail shorted to a higher voltage. In this scenario, the output voltage of the higher regulator is pulled down to the OVP voltage of the soft-latched regulator, allowing the problem to be easily diagnosed with DC measurements. On the other hand, latching OVP provides only a millisecond glimpse of the fault as it latches off, forcing the use of expensive digital oscilloscopes for troubleshooting.

Three Operating Modes/One Pin: Sync, Burst Disable and Secondary Regulation

The FCB pin is a multifunction pin that controls the operation of the synchronous MOSFET and is an input for external clock synchronization. When the FCB pin drops below its 0.8V threshold, continuous mode operation is forced. In this case, the top and bottom MOSFETs continue to be driven synchronously regardless of the load on the main output. Burst Mode operation is disabled and current reversal is allowed in the inductor.

In addition to providing a logic input to force continuous synchronous operation and external

Table 3. Comparison of LTC1735/36 controllers with LTC1435A/36A-PLL controllers

Parameter	LTC1735/1736	LTC1435A/1436A-PLL
Reference	0.8V	1.19V
Load Regulation	0.1% Typ, 0.2% Max	0.5% Typ 0.8% Max
Max Current Sense	75mV	150mV
Minimum On-Time	200ns	300ns
Synchronizable	Yes	LTC1436A-PLL Only
Int V_{CC} Voltage	5.2V (7V Max)	5V (10V Max)
Power Good Output	LTC1736 Only	LTC1436A/36A-PLL Only
Current Foldback	Internal	External
Output OV Protection	Yes	No
Output OI Latch-Off	Optional	No
Packages	SO16, GN16/G24	SO16, G16/GN24
MOSFET Drivers	3×	1×

Table 4. VID output voltage programming

B4	B3	B2	B1	B0	V_{OUT} (V)
0	0	0	0	0	2.000V
0	0	0	0	1	1.950V
0	0	0	1	0	1.900V
0	0	0	1	1	1.850V
0	0	1	0	0	1.800V
0	0	1	0	1	1.750V
0	0	1	1	0	1.700V
0	0	1	1	1	1.650V
0	1	0	0	0	1.600V
0	1	0	0	1	1.550V
0	1	0	1	0	1.500V
0	1	0	1	1	1.450V
0	1	1	0	0	1.400V
0	1	1	0	1	1.350V
0	1	1	1	0	1.300V
0	1	1	1	1	*
1	0	0	0	0	1.275V
1	0	0	0	1	1.250V
1	0	0	1	0	1.225V
1	0	0	1	1	1.200V
1	0	1	0	0	1.175V
1	0	1	0	1	1.150V
1	0	1	1	0	1.125V
1	0	1	1	1	1.100V
1	1	0	0	0	1.075V
1	1	0	0	1	1.050V
1	1	0	1	0	1.025V
1	1	0	1	1	1.000V
1	1	1	0	0	0.975V
1	1	1	0	1	0.950V
1	1	1	1	0	0.925V
1	1	1	1	1	**

Note: *, ** represent codes without a defined output voltage as specified in Intel specifications. The LTC1736 interprets these codes as a valid inputs and produces output voltage as follows: [01111]=1.250V, [11111]=0.900V.

synchronization, the FCB pin provides a means to regulate a flyback winding output. It can force continuous synchronous operation when needed by the flyback winding, regardless of the primary output load. In order to prevent erratic operation if no external connections are made, the FCB pin is pulled high by a 0.25µA internal current source.

The LTC1735 internal oscillator can be synchronized to an external oscillator by applying a clock signal of at least $1.5V_{P-P}$ to the FCB pin. When synchronized to an external frequency, Burst Mode operation is disabled but cycle skipping occurs at low load currents since current reversal is inhibited. The bottom gate will come on every 10 clock cycles to ensure that the bootstrap cap is kept refreshed and to keep the frequency above the audio range. The rising edge of an external clock applied to the FCB pin starts a new cycle.

The range of synchronization is from $0.9 \times f_O$ to $1.3 \times f_O$, with f_O set by C_{OSC}. Attempting to synchronize to a higher frequency than $1.3 \times f_O$ can result in inadequate slope compensation and cause loop instability with high duty cycles. If loop instability is observed while synchronized, additional slope compensation can be obtained by simply decreasing C_{OSC}. A plot of operating frequency versus C_{OSC} value is shown in Figure 2.

Table 2 summarizes the possible states available on the FCB pin.

Figure 3 gives a comparison of efficiencies in a regulator for the three operating modes: forced continuous operation, pulse skipping mode (synchronized at $f = f_O$) and Burst Mode operation.

Figure 4. MOSFET gate-charge current vs frequency

Converting to the LTC1735

The LTC1735 is pin compatible with the LTC1435/LTC1435A, with minor component changes. Table 3 shows the differences between the two controllers. The important items to note are:

1. The LTC1735 has a 0.8V reference (versus 1.19V for the LTC1435) that allows lower output voltage operation (down to 0.8V). Thus, the output feedback divider will have to be recalculated for the same output voltage.

2. The LTC1735's maximum current sense voltage is half that of the LTC1435. This reduces the power lost in the sense resistor by half. Hence, for the same maximum output current, the current sense resistor must be cut in half.

Figure 5. High efficiency 1.6V/9A CPU power supply

3. The gate drivers of the LTC1735 are 3× the strength of those in the LTC1435. This equates to faster rise and fall times for driving the same MOSFETs plus the capability to drive larger MOSFETs with less efficiency loss due to transition losses.
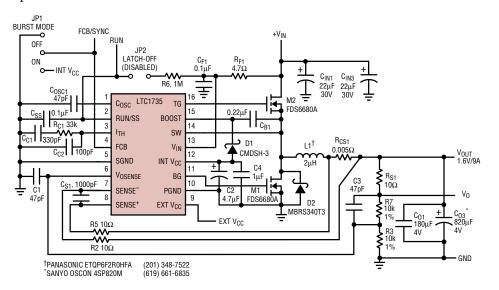
Speed

The LTC1735/LTC1736 are designed to be used in higher current applications than the LTC1435 family. Stronger gate drives allow paralleling multiple MOSFETs or higher operating frequencies. The LTC1735 has been optimized for low output voltage operation by reducing the minimum on-time to less than 200ns. Remember, though, that transition losses can still impose significant efficiency penalties at high input voltages and high frequencies. Just because the LTC1735 can operate at frequencies above 300kHz doesn't mean it should. Figure 4 shows a plot of MOSFET charge current versus frequency.

Linear Current Comparator Operation

Since the trend in the marketplace has forced output voltages to lower and lower values, the current sense inputs have been optimized for low voltage operation. The current sense comparator has a linear response characteristic, without discontinuities, from 0V to 6V output voltages. In the LTC1435/LTC1435A, two input stages are used to cover this range, so an overlap exists together with a transition region. The LTC1735/LTC1736 uses only one input stage and includes slope compensation that operates over the full output voltage range. This allows the LTC1735/LTC1736 to be operated in grounded R_{SENSE} applications as well.

LTC1736 Additional Features

The LTC1736 includes all the features of the LTC1735, plus 5-bit mobile VID control and a power-good comparator in a 24-lead SSOP package. The window comparator monitors the output voltage and its open-drain output is pulled low when the divided

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voltage is *not* within ±7.5% of the 0.8V reference voltage.

The output voltage is digitally set to levels between 0.925V and 2.00V using the voltage identification (VID) inputs B0–B4. The internal 5-bit DAC configured as a precision resistive voltage divider sets the output voltage in 50mV or 25mV increments according to Table 4. The VID codes (00000–11110) are compatible with the Intel mobile Pentium® II processor. The LSB (B0) represents 50mV increments in the upper voltage range (2.00V–1.30V) and 25mV increments in the lower voltage range (1.275V–0.925V). The MSB is B4. When all bits are low or grounded, the output voltage is 2.00V.

The LTC1736 also has remote sense capability. The top of the internal resistive divider is connected to V_{OSENSE} and is referenced to the SGND pin. This allows a Kelvin connection for remotely sensing the output voltage directly across the load, eliminating any PC board trace resistance errors.

Applications

Figure 5 shows a 1.6V/9A application using the LTC1735. The input voltage can range from 6V to 26V. Figure 6 shows a VID application using the LTC1736 optimized for output voltages of 1.6V to 1.3V with a 5V to 24V input voltage range.

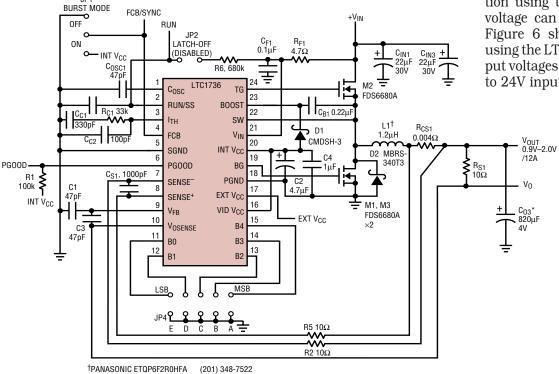†PANASONIC ETQP6F2R0HFA   (201) 348-7522
*PANASONIC EEFVEOG181R

Figure 6. High efficiency, VID programmable, 0.9V–2.0V/12A CPU power supply

New Universal Continuous-Time Filter with Extended Frequency Range

by Max W. Hauser

Introduction

The original LTC1562, described in the February 1998 issue of this magazine, is a compact, quadruple 2nd order, universal, continuous-time filter that is DC accurate and user programmable for the 10kHz–150kHz frequency range. The LTC1562 introduced Operational Filter building blocks, whose virtual-ground input, rail-to-rail outputs and precision internal R and C components satisfy diverse filter requirements and applications compactly.[1, 2, 3]

The design of the LTC1562 entailed choices in the internal R and C values and internal amplifiers, and these elements were optimized to minimize wideband noise. The LTC1562-2 is a new product with the same block diagram, pinout and packaging, but optimized for higher filter frequencies: 20kHz to 300kHz. The internal precision R and C components and amplifiers are different in the LTC1562-2. Besides covering a full octave of frequencies (150kHz–300kHz) above the range of the LTC1562, the LTC1562-2 also overlaps the LTC1562's utility in the range 20kHz to 150kHz. In this frequency range, the LTC1562-2 typically shows reduced large-signal distortion at a cost of slightly more noise than with the LTC1562. For example, a 100kHz dual 4th order Butterworth lowpass filter with a ±5V supply, built with the LTC1562-2 and lightly loaded, exhibited 2nd-harmonic distortion of –103dB and 3rd-harmonic distortion of –112dB at 20kHz with an output of $1V_{RMS}$ ($2.8V_{P-P}$), and maintained low distortion even with output swings approaching the full supply voltage (–83dB total harmonic distortion, or THD, at $9.7V_{P-P}$ output).

The LTC1562-2 is, therefore, the product of choice for applications above 150kHz as well as for applications in the 20kHz–150kHz range that are especially distortion sensitive. Both the LTC1562 and the LTC1562-2 can replace LC filters or filters built from high performance op amps and precision capacitors and resistors, with a total surface mount board area of $155mm^2$ ($0.24in^2$)—smaller than a dime (the smallest US coin).

Comparison to the LTC1562

The LTC1562-2 both resembles and differs from the LTC1562 as follows:

❏ The parts have identical pin configurations and block diagrams (four independently programmable 2nd order Operational Filter blocks with virtual-ground inputs and rail-to-rail outputs).

❏ In both products, the user can program the filter's center-frequency parameter (f_0) over a wide range, using resistor values that vary as the desired f_0 changes up or down from a *design-center* value. In the LTC1562, this design-center f_0 is 100kHz; for the LTC1562-2, the value is 200kHz.

❏ The LTC1562 is optimized for lower noise, the LTC1562-2 for higher frequencies. Thus, a single LTC1562 section can deliver 103dB SNR in 200kHz bandwidth ($Q = 1$), whereas a single LTC1562-2 section supports 99dB SNR in 400kHz.
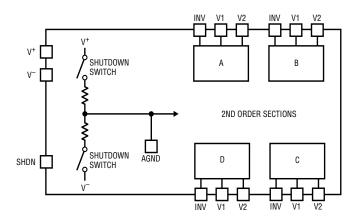

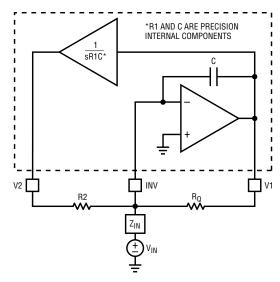Figure 1. LTC1562-2 block diagram

Figure 2. Single 2nd order Operational Filter section (inside dashed line) with external components added: resistor for Z_{IN} gives lowpass at V2, bandpass at V1; capacitor for Z_{IN} gives bandpass at V2, highpass at V1.

❑ Each chip contains precision R and C components equivalent to eight 0.25% tolerance capacitors and four 0.5% tolerance resistors, as well as twelve op amps with rail-to-rail outputs and excellent high frequency linearity.

❑ Both circuits operate from nominal 5V to 10V total supplies (single or split). Single-supply applications can use a half-supply, ground-reference voltage generated on the chip.

❑ Both chips feature a power-down mode that drops the power supply current to zero, except for reverse junction leakages (on the order of 1µA total).

*V^- ALSO AT PINS 4, 7, 14 & 17
ALL RESISTORS 1% METAL FILM

Figure 3. Dual 4th order 200kHz Butterworth lowpass filter

What the LTC1562-2 Can Do

Figure 1 is an overall diagram and Figure 2 a per-section diagram for the LTC1562-2. These are identical to the diagrams for the LTC1562, except for the values of the internal precision components in Figure 2. In the LTC1562-2, R1 is 7958Ω and C is 100pF. External resistors can be combined with an LTC1562-2 section, as shown in Figure 2, to define a second order filter response with standardized parameters f_0, Q and gain. Design equations and procedures appear in the LTC1562-2 data sheet. For example, in Figure 2, R2 sets f_0; R_Q, a multiple of R2, sets Q; and Z_{IN} sets both the gain and the block's function. The 3-terminal blocks minimize the number of external parts necessary for complete 2nd order sections with programmable f_0, Q and gain.

A resistor for Z_{IN} in Figure 2 gives simultaneous lowpass (at V3) and bandpass (at V1) responses. The data sheet describes other ways to exploit the virtual ground INV input. For example, because the V1 output in Figure 2 shows a phase shift of 180° at the user-set center frequency, f_0, summing a V1 output with a feedforward path from the signal source yields a notch response,[2] or with different weighting, allpass (phase equalization), as used in Figure 5
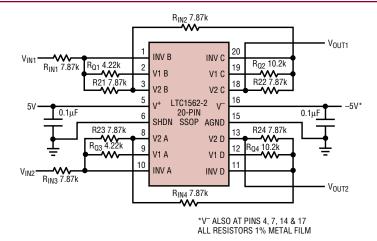
later in this article. Using capacitors together with the INV input's summing capability provides further powerful techniques for zero and notch responses (which, in turn, enable elliptic highpass and lowpass filtering). For example, the two outputs of each 2nd order section have a 90° phase difference, so summing V1 through a capacitor and V2 through a resistor, into another section's virtual-ground input, gives the same notch or allpass option mentioned above but without devoting an additional section for phase shift.[4] Figures 5 and 9, described later, use this RC notch method. Moreover, a capacitor for Z_{IN} in Figure 2 yields simultaneous *highpass* and bandpass responses; the capacitor sets voltage gain, not critical frequencies, with a relationship of the form Gain = C_{IN}/100pF in the LTC1562-2. Low level signals can exploit the built-in gain capability, which raises filter SNR with low input voltage amplitudes. Such abilities to tailor the use of each block and its built-in time constants are reminiscent of an operational amplifier—whence the term "operational filter."

DC performance includes a typical lowpass input-to-output offset of 3mV and outputs that swing (under load) to within approximately 100mV of each supply rail. An internal half-supply reference point (the AGND pin) generates a reference voltage for the inputs and outputs in single-supply

applications. The shutdown (SHDN) pin accepts CMOS logic levels and in 20µs puts the LTC1562-2 into a "sleep" mode, in which the chip consumes approximately 1µA (the part will default to this state if the pin is left open). The 16-pin dies is packaged in a 20-pin SSOP (the extra pins in the SSOP are substrate connections, to be returned to the negative supply for best performance).

The following application examples are tailored for specific corner frequencies, which can be modified by properly scaling the external components, as described in the data sheet and in LTC1562 application articles.[2, 3] Expert application assistance can be obtained by calling us at 408-954-8400, x3761. Pin numbers in the figures that follow are for the 20-pin SSOP package, where pins 4, 7, 14 and 17 (not shown) are always tied to the negative power supply rail. As with other filters, achieving low noise and distortion levels requires electrically clean construction (as well as equipment that can measure such performance).

Dual 4th Order 200kHz Butterworth Lowpass Filter

Each half of the circuit in Figure 3 provides a classic 4th order lowpass gain roll-off (24dB per octave) with a maximally flat passband. This schematic includes power supply connections for a split ±5V supply, one of the options available for any LTC1562-2
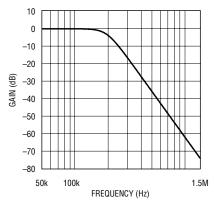
Figure 4. Frequency response of one of the two filters in Figure 3

*V⁻ ALSO AT PINS 4, 7, 14 & 17
ALL RESISTORS 1% METAL FILM

Figure 5. 256kHz linear-phase 6th order lowpass filter

application (Figure 5, in a different application, illustrates connections for a single 5V supply). The circuit of Figure 3 is a higher frequency variation of a 100kHz dual 4th order Butterworth lowpass filter using the LTC1562, which appeared in the February 1998 *Linear Technology* magazine,[1] as well as in the LTC1562 data sheet. Figure 4 shows the measured frequency response for one of the two filters in Figure 3. This ±5V circuit supports rail-to-rail inputs and outputs, with output noise of approximately $60\mu V_{RMS}$, for a maximum SNR of 95dB (compared to 100dB with the LTC1562 equivalent at half as much bandwidth). THD in a $1V_{RMS}$ output $(2.8V_{P-P})$ was measured as –87dB at 50kHz and –72dB at 100kHz.

256kHz Phase-Linearized 6th Order Lowpass Filter

Data communication and some signal antialiasing and reconstruction applications demand filters with controlled phase (or time-domain)
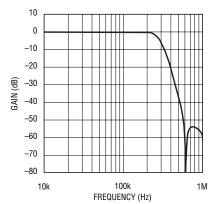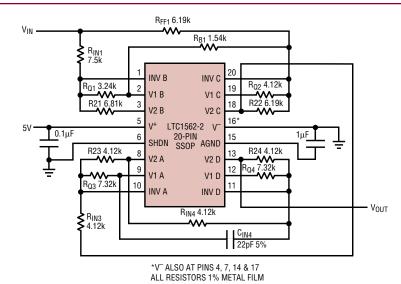
responses. The circuit in Figure 5 realizes a root-raised-cosine lowpass gain response (Figure 6). For data communications, this filter's time-domain pulse response (Figure 7) approximates, in *continuous time*, the ideal Nyquist-type property of crossing zero at a time interval that is equal to $1/(2f_C)$. When used as a pulse-shaping filter, this response has the special property of producing minimal intersymbol interference (ISI) among successive data pulses at a data rate of $2f_C$ (512 kbits/second or ksymbols/second for Figure 5) while simultaneously limiting the transmitted spectrum to a bandwidth approaching the theoretical minimum, which is f_C.[5] Also, data or signal acquisition (before A/D conversion) or reconstruction (after D/A conversion) can benefit from the linear-phase (that is, constant-group-delay) response (typically ±300ns group

delay variation over the passband from 0 to f_C, evident in Figure 8).

The filter in Figure 5 achieves these properties by preceding a 6th order lowpass section (the C, A, and D quarters of the LTC1562-2 chip, in that sequence) with a 2nd order allpass response to linearize the phase. This combination illustrates two practical uses of the virtual-ground inputs in the LTC1562-2. Combining two feedforward paths (R_{FF1} from the input and R_{B1} from a bandpass section in the "B" quarter of the LTC1562-2) yields the allpass equalization. Subsequently, R_{IN4} and C_{IN4} sum together two signals with 90° phase difference from the two outputs of the "A" quarter, with an additional 90° phase difference caused by the capacitor, to achieve a stopband notch at a desired frequency.[4] Figure 5 operates from a single supply voltage from 5V to 10V (the AGND pin furnishes a built-in
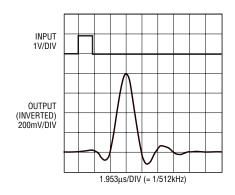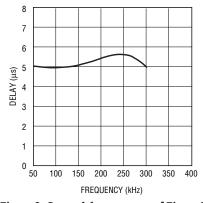

Figure 6. Gain response of Figure 5's circuit
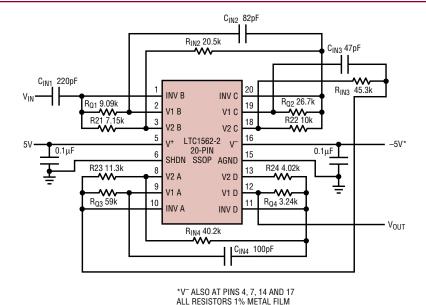

Figure 7. Time-domain response of Figure 5's circuit

Figure 8. Group delay response of Figure 5's circuit

*V⁻ ALSO AT PINS 4, 7, 14 AND 17
ALL RESISTORS 1% METAL FILM
ALL CAPACITORS 5% STANDARD VALUES

Figure 9. 175kHz 8th order elliptic highpass filter

Figure 10. Frequency response of Figure 9's circuit

half-supply ground reference) and exhibits –80dB THD at 50kHz for a 500mV$_{RMS}$ output with a 5V supply.

175kHz 8th Order Elliptic Highpass Filter

In Figure 9, three response notches below the cutoff frequency suppress the stopband and permit a narrow transition band in a 175kHz highpass filter, whose measured frequency response appears in Figure 10. Each notch is produced by summing two 180°-different currents into a virtual-ground "INV" summing input, one current passing through an R$_{IN}$ and the other (from a voltage 90° different

from the first) through a C$_{IN}$.[4] This circuit exhibits only 44µV$_{RMS}$ of output noise over a 1MHz bandwidth and THD of –70dB with a 200kHz signal, 0.5V$_{P-P}$ output, operating from a 5V total supply.

400kHz Dual 6th Order Lowpass Filter

Although it is outside the 300kHz f$_0$ limit recommended for best accuracy, this dual 6th order 400kHz Butterworth lowpass filter (Figure 11) illustrates an extreme of bandwidth available from the LTC1562-2 with some compromises. The high f$_0$ requires unusually small resistor val-
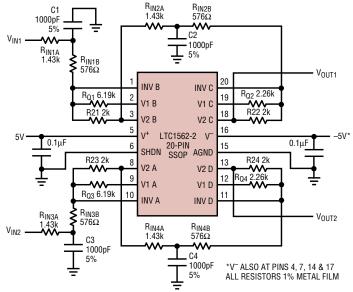
ues, resulting in heavier loading and an increase in distortion from the LTC1562-2; it was also necessary to adjust the R$_Q$ resistors in Figure 11 downwards to correct for Q enhancement encountered when the designed f$_0$ is very high.

The circuit of Figure 11 supplements the eight poles of filtering in the LTC1562-2 by driving all four of the virtual-ground INV inputs from R-C-R "T" networks (in place of resistors) and thus obtaining additional real poles (a method described in the original LTC1562 application article[1] and data sheet). Two such real poles replace the Q = 0.518 pole pair of a conventional 6th order Butterworth pole configuration, to good accuracy. The measured frequency response of one 6th order section appears in Figure 12. With ±5V power, this circuit permits rail-to-rail inputs and outputs and exhibits THD, at 1V$_{RMS}$ (2.8V$_{P-P}$) output, of –92dB at 50kHz and –79dB at 100kHz. Output noise

Figure 11. 400kHz dual 6th order Butterworth lowpass filter

*V⁻ ALSO AT PINS 4, 7, 14 & 17
ALL RESISTORS 1% METAL FILM

Figure 12. Frequency response of Figure 11's circuit

SOT-23 Switching Regulators Deliver Low Noise Outputs in a Small Footprint

by Steve Pietkiewicz

Introduction

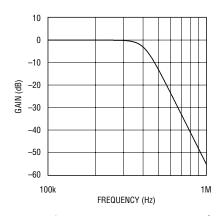As portable electronics designers continue to press for reduction in component sizes, Linear Technology introduces the LT1611 and LT1613 SOT-23 switching regulators. These current mode, constant frequency devices contain internal 36V switches capable of generating output power in the range of 400mW to 2W, in a 5-lead SOT-23 package. The LT1613 has a standard positive feedback pin and is designed to regulate positive voltages. The LT1611 has a novel feedback scheme designed to directly regulate negative output voltages without the use of level-shifting circuitry. Boost, single-ended primary inductance converters (SEPIC) and inverting configurations are possible with the LT1613 and LT1611. The high voltage switch allows hard-to-do, yet popular DC/DC converter functions like four cells to 5V, 5V to –5V, 5V to –15V or 5V to 15V to be easily realized.

Both devices switch at a frequency of 1.4MHz, allowing the use of tiny inductors and capacitors. Many of the components specified for use with the LT1613 and LT1611 are 2mm or less in height, providing a low profile solution. The input voltage range is 1V to 10V, with 2mA quiescent current. In shutdown mode, the quiescent current drops to 0.5µA. The
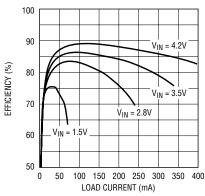

Figure 2. Efficiency of Figure 1's boost converter

constant frequency switching produces low amplitude output ripple that is easy to filter, unlike the low frequency ripple typical of pulse-skipping or PFM type converters. Internally compensated current mode control provides good transient response.

LT1613 Boost Converter Provides a 5V Output

Figure 1's circuit details a boost converter that delivers 5V at 200mA from a 3.3V input. The input can range from 1.5V to 4.5V, making the circuit usable from a variety of input sources, such as a 2- or 3-cell battery, single Li-Ion cell or 3.3V supply. Efficiency, shown in Figure 2, reaches 88% from a 4.2V input. Start-up waveforms from a 3.3V input into a 47Ω load are

pictured in Figure 3; the converter reaches regulation in approximately 250µs. The device requires some bulk capacitance due to the internal compensation network used. A 10µF ceramic output capacitor can be used with the addition of a phase-lead capacitor paralleled with R1; this capacitor is typically in the 10pF–100pF range.

LT1613 5V to 15V Boost Converter

By changing the value of the resistive divider, a 15V supply can be generated in a similar manner to the 5V converter shown in Figure 1. Figure 4 depicts the converter. L1's value has been changed to 10µH to provide the same di/dt slope with a higher input voltage. The converter delivers 15V at 60mA from a 5V input, at efficiencies up to 85%, as shown in the efficiency graph of Figure 5.

LT1613 4-Cell to 5V SEPIC

A 4-cell battery presents a unique challenge to the DC/DC converter designer. A fresh battery measures about 6.5V, above the 5V output, while at end of life the battery voltage will measure 3.5V, below the 5V output. Simple switching regulator topologies like boost or buck can only increase or decrease an input voltage,

L1: MURATA LQH3C4R7M24   (814) 237-1431
OR SUMIDA CD43-4R7   (847) 956-0666
C1, C2: AVX TAJA156M010R   (803) 946-0362
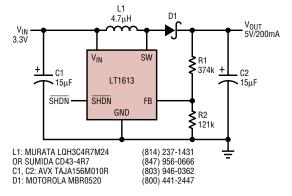D1: MOTOROLA MBR0520   (800) 441-2447

Figure 1. This boost converter steps up a 1.5V to 4.2V input to 5V. It can deliver 250mA from a 3.3V input.

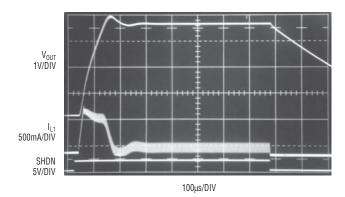
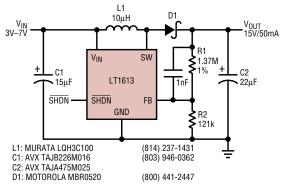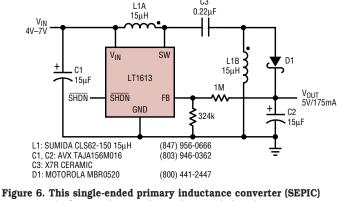Figure 3. Boost converter start-up with 3.3V input into a 50Ω load

Figure 4. This 4-cell to 15V boost converter can deliver 50mA from a 3V input.

L1: MURATA LQH3C100   (814) 237-1431
C1: AVX TAJB226M016   (803) 946-0362
C2: AVX TAJA475M025
D1: MOTOROLA MBR0520   (800) 441-2447

Figure 6. This single-ended primary inductance converter (SEPIC) generates 5V from an input voltage above or below 5V.

L1: SUMIDA CLS62-150 15μH   (847) 956-0666
C1, C2: AVX TAJA156M016   (803) 946-0362
C3: X7R CERAMIC
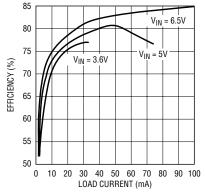D1: MOTOROLA MBR0520   (800) 441-2447

Figure 5. Efficiency of Figure 4's circuit

which will not do the trick in this situation. The solution is a SEPIC. A dual-winding inductor or two separate inductors are required to make this converter. Figure 6 details the circuit. A Sumida CLS62-150 15μH dual inductor is specified in the application, although two 15μH units can be used instead. Up to 125mA can be generated from a 3.6V input. Figure 7's graph shows converter efficiency, which peaks at 77%. Transient response with a 5mA to 105mA load step is pictured in Figure 8. The converter settles to final value inside

200μs, with a maximum perturbation under 200mV. The double trace of V_{OUT} under load in Figure 8 is actually switching ripple at 1.4MHz caused by the ESR of output capacitor C2. A better (lower ESR) output capacitor will decrease the output ripple.

LT1611 5V to –5V Inverting Converter

A low noise –5V output can be generated using an inverting topology with the LT1611. This circuit, shown in Figure 9, bears some similarity to the SEPIC described above, but the output is in series with the second inductor. This results in a very low noise output. The circuit can deliver –5V at up to 150mA from a 5V input, or up to 100mA from a 3V input. Efficiency, described in Figure 10, peaks at 75%. Figure 11 illustrates the start-up waveforms. During start-up, the switch-current increases to approximately 1A. At this current, the inductance of the Sumida unit decreases, resulting in the increased

Figure 7. Efficiency of Figure 6's SEPIC reaches 77%.

ripple current noticeable in the switch-current trace of Figure 11. After the circuit has reached regulation, the ripple current decreases by about a factor of two. Switching waveforms with a 100mA load are shown in Figure 12. Output voltage ripple is caused by ripple current in the inductor multiplied by output capacitor ESR.

Although the $20mV_{P-P}$ ripple pictured in Figure 12 is low, significant improvement can be obtained by judicious component selection. Figure 13 details the same 5 to –5V

200μs/DIV

Figure 8. SEPIC transient response at 5V input with a 5mA to 105mA load step

L1: SUMIDA CLS62-220 22μH   (847) 956-0666
C1, C2: AVX TAJB226010   (803) 946-0362
C3: X7R CERAMIC
D1: MOTOROLA MBR0520   (800) 441-2447

Figure 9. This inverting converter delivers –5V at 150mA from a 5V input.

Figure 10. 5V to –5V inverting converter efficiency reaches 76%.

Figure 11. 5V to –5V inverting converter start-up into a 47Ω load

Figure 12. Switching waveforms of inverting converter with 100mA load

converter function with better output capacitors. Now, output ripple measures just $4mV_{P-P}$. Additionally, transient response is improved by the addition of phase lead capacitor C5. Figure 14 depicts load transient response of a 25mA to 125mA load step. Maximum perturbation is under 30mV and the converter reaches final value in approximately 250µs.

It is important to take notice of how Figures 9 and 13 are drawn. D1's cathode is returned to the LT1611's GND pin before both connect to the ground plane. This connection combines the current of the switch and diode, which conduct on alternate phases. The summation of both currents equals a current with no abrupt changes, minimizing di/dt induced voltages caused by the few nanohenries of inductance in the ground plane. This summed current is then depos-

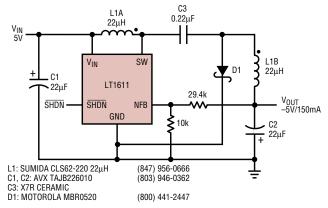ited into the ground plane. If this technique is not followed, 100mV spikes can appear at the converter output (I speak from experience: my first several breadboards had this problem).

Many systems, such as personal computers, have a 12V supply available. Although the LT1611 V_{IN} pin

has a 10V maximum, the 36V switch allows a 12V supply to be used for the inductor while the LT1611's V_{IN} pin is still driven from 5V, as indicated in Figure 13. Significantly more output power can be obtained in this manner, as illustrated in the efficiency graph of Figure 15.

Figure 13. Low noise inverting converter; component selection and feedforward capacitor C5 reduce noise to $4mV_{P-P}$.

Figure 14. Transient response of low noise inverting converter is under 30mV for a 25mA to 125mA load step. Steady-state output ripple is $4mV_{P-P}$.

Versatile New Switching Regulator Fits in SO-8

by Craig Varga

Introduction

Linear Technology recently introduced the LTC1530 synchronous buck regulator controller. Although packaged in an 8-pin SO, it has proven to be remarkably capable and versatile. The part is loosely based on the popular LTC1430, but with numerous enhancements. Features include current limiting that senses the voltage across the $R_{DS(ON)}$ of the high-side MOSFET (no sense resistor required), built in soft-start, 1% accurate reference, gate drivers capable of handling large MOSFETs, and micropower shutdown. The error amplifier transconductance is higher than that of previous generation parts and is trimmed for accuracy and stabilized over temperature. The I_{MAX} curren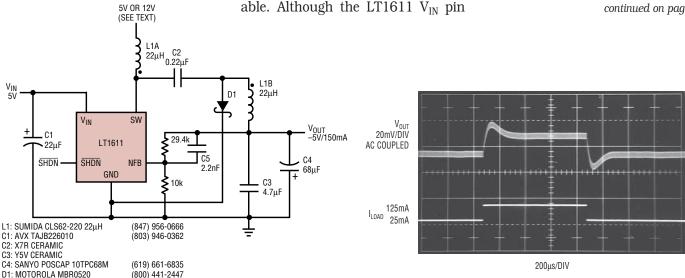t, which programs current limit, has a positive temperature coefficient to help cancel the positive temperature coefficient of the MOSFET's $R_{DS(ON)}$. This allows for more consistent current limit over temperature. Although intended primarily for buck regulator designs, the part has been successfully designed into boost, positive-to-negative and negative-to-positive converters.

A Quick Look at the Insides

Figure 1 is the basic block diagram. The LTC1530 is a voltage mode control, synchronous buck regulator controller. An on-chip oscillator generates a 300kHz ramp waveform. The output of the error amplifier is compared to this ramp by the PWM comparator. So far, nothing extraordinary. Current-limit circuitry, however, is a little more unusual.

Instead of the traditional current sense resistor, the LTC1530 relies on the $R_{DS(ON)}$ of the high-side MOSFET as its source of load current information. This saves the space, cost and the power dissipation of an additional resistor in the power path. The programming current (I_{MAX}) has a positive temperature coefficient that approximates the positive TC of a MOSFET's $R_{DS(ON)}$. This tends to flatten the current-limit trip point as a function of temperature. In a slight overload, the LTC1530 provides "square current limiting." In other words, the regulator starts to look like a current source. In the event of a significant overload, should the output fall to less than one-half of the nominal output voltage, the soft-start capacitor will be discharged very quickly. This forces
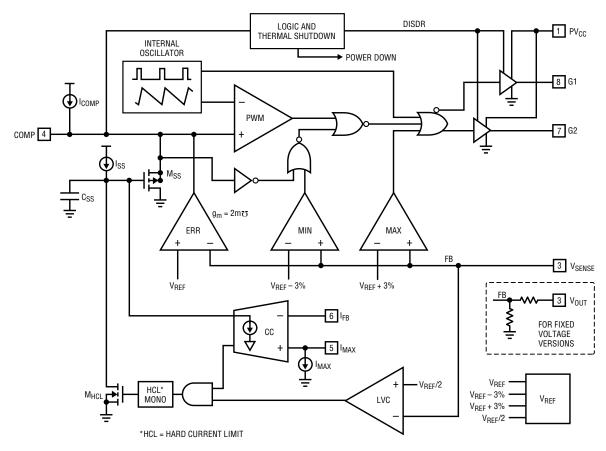
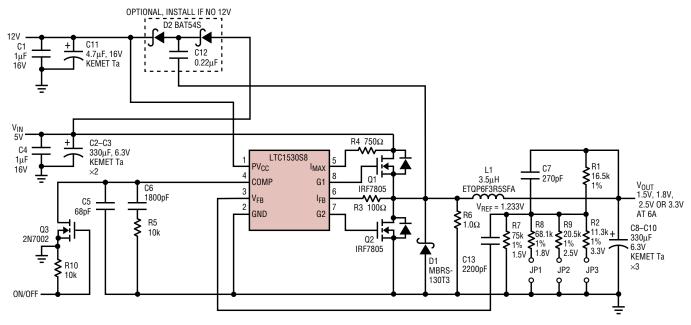

Figure 1. LTC1530 block diagram

Figure 2. 6A buck regulator; output voltage is jumper selectable for 1.5V, 1.8V, 2.5V or 3.3V.

the regulator into shutdown for a period of time, typically a few milliseconds. After the time delay, the supply attempts to restart. If the overload still exists, the hiccup mode operation will continue. Once the short is removed, the regulator will start normally.

Unlike its predecessor, the LTC1530's soft-start capacitor is internal. The start-up rise time was chosen to satisfy the vast majority of application requirements. Turn on is clean, well controlled and monotonic.

Since dynamic performance is of extreme importance in many of today's systems, the LTC1530 incorporates several features to provide improved response times to load transients. First are the min/max comparators.
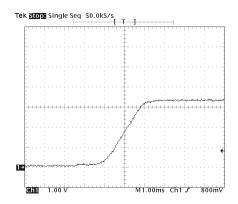

Figure 3. Output voltage at turn-on for Figure 2's circuit

These are a pair of comparators that continuously monitor the output voltage. If the output is more than 3% on either side of nominal, the appropriate comparator forces the duty factor to maximum or zero in an attempt to restore the output to the correct level as quickly as possible. Eventually, the error amplifier and main feedback loop will catch up and force the output to settle nicely. The error amplifier is also an improvement over earlier designs. The transconductance and output impedance have both been increased substantially from the LTC1430 values. This has the effect of raising the DC open-loop gain of the amplifier, resulting in better line and load regulation. Transconductance is also trimmed to ensure accuracy. The result is more predictable and repeatable loop response. The amplifier g_m is temperature compensated so loop gain stays nearly constant over temperature extremes.

The LTC1530 also has a low power shutdown mode. If the Comp pin is pulled to ground with an open collector or open drain transistor, the LTC1530's quiescent current will drop to approximately 45µA.

Virtually all integrated circuits have some quirks that will get you in trouble if you don't pay attention. The LTC1530 is no exception. Care must

be taken in choosing the power MOSFETs used in circuits that depend on a charge pump to supply gate-drive power. It is essential to select a FET for the upper device that will be almost fully enhanced before the PV_{CC} supply voltage reaches 8V with whatever main input voltage happens to be available. Failure to heed this requirement can lead to a circuit that may not start up properly at all times. Standard logic-level FETs work fine. Be sure V_{TH} is less than 2V in the worst case.

The cause of this start-up phenomenon is related to the way the current limit circuit behaves. Below a PV_{CC} level of 8V, current limit is disabled. Assume for the sake of this discussion that the main input supply is derived from 5V. At turn on, as the charge pump gradually pushes the PV_{CC} supply upward, the current-limit circuit wakes up at 8V on PV_{CC}. If the 5V supply is exactly 5V, the gate drive available for the FET is only 3V (8V – 5V). If the FET's $R_{DS(ON)}$ is very high relative to its nominal value at this point, the current-limit circuit may activate in a misguided attempt to maintain control of the output current. If, at the same time, the output voltage has come up to less than one-half of its final value, the LTC1530 will respond by discharging the soft-
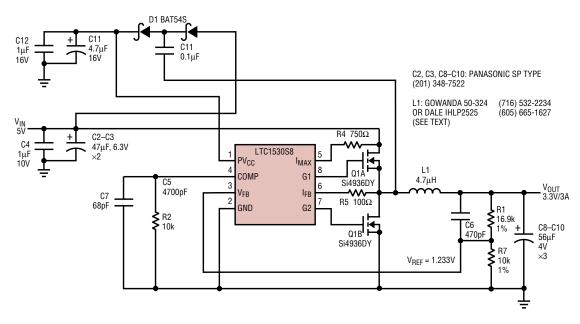
Figure 4. 3.3V/3A regulator

start capacitor and trying to initiate a restart.

As long as the output voltage has reached a level of greater than one-half of its final value before the PV_{CC} voltage reaches 8V, the output will continue to rise in current limit. If the output is below this level, start-up is not ensured. If the PV_{CC} supply is derived from a 12V source instead of charge pumped from the 5V supply, this problem cannot occur.

A Few Circuit Examples

The LTC1530 turns out to be a rather versatile device. Although intended as a buck regulator, the part has been successfully used in boost and buck-boost designs. Figure 2 is a classic buck topology. The circuit was designed to handle approximately 6A while maintaining a low profile. Input and output capacitors are tantalum devices. The inductor is a very low DC resistance design for high efficiency. The input is 5V, while the output voltage can be jumper selected for 3.3V, 2.5V, 1.8V or 1.5V. The photo in Figure 3 shows the output voltage rise at turn on. A clean, monotonic rise is evident.

Figure 4 is a 3A design that has a total height of less than 2.4mm. The inductor is a Gowanda part #50-324,

which mounts through a hole in the PCB for a total height above the board of approximately 1.5mm. Output ripple voltage is approximately $10mV_{P-P}$ at a 3A load with the specified Panasonic SP series output capacitors. There are several options for the main inductor. The overall smallest size available is an IHLP-2525 by Dale Electronics. It's 3mm tall but only 6.4mm on a side. Output ripple is about 50% higher with this inductor.

Figure 5 is an example of a synchronous boost regulator. The input is 3.3V and the output is 5V. The circuit is rated for a maximum output current of 6A. Since the output cur-
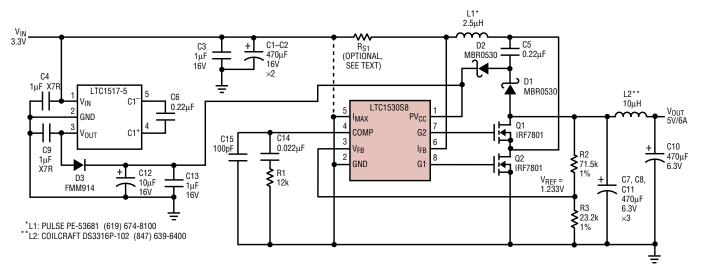

Figure 5. 5V/6A synchronous boost regulator

rent waveform is discontinuous, the output ripple is inherently large in any boost regulator. The second stage LC filter is added to clean things up a bit. The feedback divider connects to the output before the LC filter for a reason. If the divider is connected after the LC filter, the extra 180° of phase shift above the LC corner frequency will make the regulator's feedback loop unstable. The DC resistance of the inductor is small, so the effect on load regulation is minimal.

The LTC1517 charge pump is used to generate a sufficiently high voltage for the LTC1530 to function correctly and also to ensure adequate gate drive for the power MOSFETs. It runs from the 3.3V input and delivers a regulated 5V output. Once the main output comes into regulation, charge pump power is derived through D2. This causes the LTC1517's regulated output voltage set-point to be exceeded and D3 back biases, shutting the LTC1517 down. Note that current limit is disabled in this design by grounding I_{MAX} and connecting I_{FB} to V_{IN}. Since in the boost topology there is a direct DC path from input to

output, there is no point in using the current limit feature except to protect against inductor saturation. It is also worth mentioning that the FET $R_{DS(ON)}$ cannot be used as the current sense resistor in this application because FET Q2's drain is not common to V_{IN}. If inductor saturation protection is desirable, it is possible to install a small value current sense resistor between C2 and L1. Install an appropriate value resistor (R_{S1}) between C2 and L1; connect the I_{MAX} pin to the C2 side of R_{S1} (instead of ground) and connect I_{FB} directly to the input side of L1. Just don't expect the circuit to limit current in the event of a short circuit.

Figure 6 is a positive input to negative 5V output design. Since the LTC1530 needs to be referenced to the –5V output, the design requires external gate-drive circuitry for both the main and synchronous FETs. The absolute maximum voltage rating of the LTC1530's gate drive would be exceeded if the high-side gate were driven directly. Q3 and the associated parts at the input to the LTC1693 gate driver provide the required level-shift function. The synchronous FET

is driven by the other half of the LTC1693. The driver is only required at this location to match the propagation delay of the high-side drive. Failure to pay attention to these details will result in severely degraded efficiency. Output currents of up to 4A can be obtained from this circuit. Like the boost regulator, the output currents are discontinuous, so ripple on the output is somewhat high. A small, second-stage LC filter can easily remedy this if desired.

Conclusion

The LTC1530 is a small, versatile controller that is usable in numerous topologies and over a wide range of power levels. In the basic buck applications for which it was designed, the LTC1530 permits the designer to realize very simple, low parts count designs that require minimal real estate. The part provides clean turn-on and current-limit characteristics. With a little ingenuity, it is possible to develop circuits different than those that the part's designers intended, but which give excellent performance nonetheless. *LT*
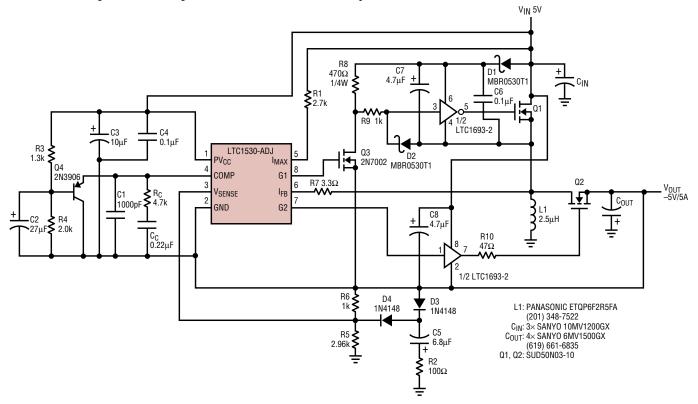

Figure 6. 5V to –5V/4A synchronous switching, inverting polarity converter

16-Bit Parallel DAC Has 1LSB Linearity, Ultralow Glitch and Accurate 4-Quadrant Resistors

by Patrick Copley

Today's fast paced marketplace has developed a major appetite for high resolution, high accuracy, fast digital-to-analog converters. System requirements in instrumentation, automatic test equipment, communications, waveform generation, data acquisition and feedback control systems, among many other applications, have fueled the need for 16-bit digital-to-analog converters. Not only does the converter need to meet the stringent speed and accuracy requirements of the system, it needs to do so in both unipolar (0V to 10V) and bipolar (±10V) modes of operation without degradation. To meet and exceed these requirements, Linear Technology introduces its LTC1597 16-bit parallel, current output, low glitch, multiplying DAC with 4-quadrant resistors. Key features of the new DAC include:

❏ ±1LSB maximum INL and DNL over the industrial temperature range

❏ On-chip 4-quadrant resistors allow precise 0V to 10V, 0V to –10V or ±10V outputs

❏ Ultralow, < 1nV-s midscale glitch impulse

❏ Small 28-pin SSOP package

❏ Low supply power consumption: 10µW typical

❏ Pin-compatible with the LTC1591 14-bit parallel, current output, low glitch, multiplying DAC with 4-quadrant resistors.

Unique Features of the LTC1597

The LTC1597 operates from a single 5V supply and provides both unipolar 0V to –10V or 0V to 10V and bipolar ±10V output ranges from a 10V or –10V reference input using a single or dual external op amp. The device achieves bipolar operation using three additional on-chip precision resistors. The DAC consists of a precision thin-film R/2R ladder for the thirteen LSBs. The three MSBs are decoded into seven segments of resistor value R, as shown in Figure 1. R is nominally 48k. Each of these segments and the R/2R ladder carry an equally weighted current of one-eight of full-scale. The feedback resistor, R_{FB}, and 4-quadrant resistor, R_{OFS}, have a value of R/4. 4-quadrant resistors R1 and R2 have a magnitude of R/4.

The reference pin presents a constant input impedance of R/8 in unipolar mode and R/12 in bipolar mode. The output impedance of the current output pin, I_{OUT1}, varies with DAC code.
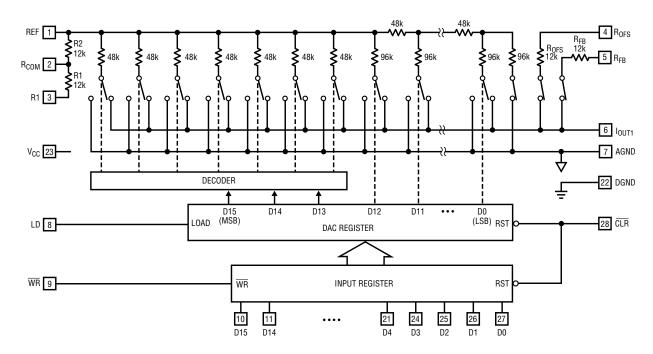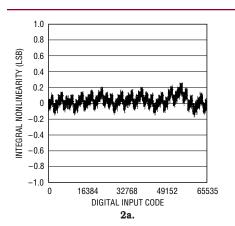

Figure 1. The LTC1597 16-bit CMOS DAC uses a precision thin-film modified R/2R architecture to provide unsurpassed accuracy and stability. Accurate 4-quadrant multiplication applications are now possible with on-chip resistors R1, R2 and R_{OFS}. A built-in deglitcher reduces glitch impulse to 1nV-s.
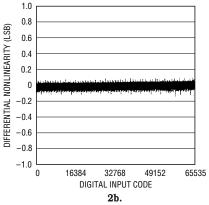
2a.

2b.

Figure 2. The outstanding INL and DNL (typically less than 0.25LSB) and very low linearity drift allow a maximum 1LSB spec to be guaranteed over the industrial temperature range.

An added feature of the LTC1597 is a proprietary deglitcher that reduces the glitch energy to below 1nV-s over the DAC's output voltage range.

The LTC1597 has a 16-bit parallel input data bus and is double buffered with two 16-bit registers. The double buffered feature permits the updating of several DACs simultaneously. The $\overline{WR}$ signal updates the input register and the LD signal loads the DAC register. The deglitcher is activated on the rising edge of the LD signal.

The versatility of the interface also allows the use of the input and DAC registers in a master/slave or edge-triggered configuration. This mode of operation occurs when $\overline{WR}$ and LD are tied together to act as a clock signal.

The asynchronous clear pin ($\overline{CLR}$) resets the LTC1597 to zero scale and the LTC1597-1 to midscale. CLR resets both the input and DAC registers. The LTC1597 also features a power-on reset.

16-Bit Accuracy Over Temperature

The LTC1597 has ultralow linearity drift of well below ±0.2LSB from –45°C to 85°C. This allows the LTC1597 to hold its accuracy of 1LSB integral nonlinearity (INL) and differential nonlinearity (DNL) over time and temperature. In the past, the only DACs that approached this accuracy over temperature were of the autocalibrated type. These DACs were very large, very expensive and therefore not very practical for most applications.

Figures 2a and 2b show the typical INL and DNL curves of the LTC1597. The outstanding 0.25LSB INL, 0.15 LSB DNL (typical) and very low drift allow a maximum 1LSB specification over the extended industrial temperature range. For optimum performance, the REF pin of the LTC1597 should be driven by a source impedance of less than 1kΩ. However, the DAC has been designed to minimize source impedance effects. An 8kΩ source impedance degrades both INL and DNL by a mere 0.2LSB.

Figure 4. When used with the LT1468 and a 20pF feedback capacitor (see Figure 3), the LTC1597 can settle in an amazing 1.7µs to within 0.0015%. The top trace shows the LD pulse; the bottom trace shows the gated settling waveform settling to 1LSB in 1.7µs.

Fast Settling: Less than 2µs to within 0.0015% of Full-Scale

Now system designers no longer have to make tough decisions in the trade-off between accuracy and speed. The solution is here. The combination of the LTC1597 DAC and the LT1468 op amp provides an industry first: superb 16-bit settling of less than 2µs for a 10V step while maintaining 1LSB DC accuracy.

Figure 3 shows the application circuit for unipolar mode. Figure 4 shows the resulting full-scale 10V step settling time of the LTC1597/LT1468 combination. With a 20pF feedback capacitor, the optimized settling time to 0.0015% is an amazing ≈1.7µs. A

Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB			LSB	
1111	1111	1111	1111	$-V_{REF}$ (65,535/65,536)
1000	0000	0000	0000	$-V_{REF}$ (32,768/65,536) = $-V_{REF}/2$
0000	0000	0000	0001	$-V_{REF}$ (1/65,536)
0000	0000	0000	0000	0V

Figure 3. With a single external op amp, the LTC1597 performs 2-quadrant multiplication with ±10V input and 0V to $-V_{REF}$ output. With a fixed –10V reference, it provides a precision 0V to 10V unipolar output.

6a. Unipolar-mode full-scale: the noise and distortion (N + D) is less than –96dB for signal frequencies up to 30kHz. Out to 100kHz, the N + D is less than –78dB.

6b. Bipolar-mode zero-scale: the N + D is less than –96dB for signal frequencies up to 30kHz. Out to 100kHz, the N + D is less than –82dB.

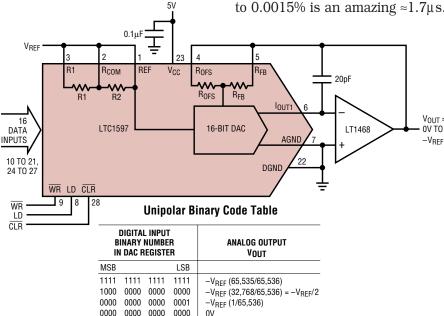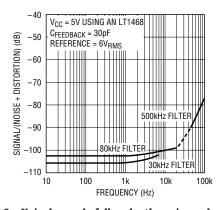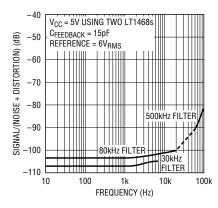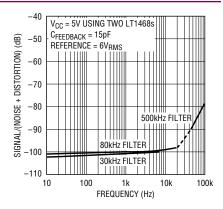6c. Bipolar-mode full-scale: the (N + D) is less than –96dB for signal frequencies up to 30kHz. Out to 100kHz, the N + D is less than –79dB.

Figure 6. LTC1597 multiplying-mode signal-to-noise vs frequency

detailed discussion of 16-bit settling time can be found in Linear Technology Application Note 74, "Component and Measurement Advances Ensure 16-Bit DAC Settling Time."

The ability to minimize settling time is limited by the need to null the DAC output capacitance, which varies from 70pF to 115pF, depending on code. This capacitance at the amplifier input combines with the feedback resistor to form a zero in the closed-loop frequency response in the vicinity of 200kHz–400kHz. Without a feedback capacitor, the circuit will oscillate. The choice of 20pF stabilizes the circuit by adding a pole at 1.3MHz to limit the frequency peaking and also optimizes settling time. The settling time to 16-bit accuracy is theoretically bounded by 11.1 time constants set by the feedback resistance and capacitance.

Figure 5. The proprietary deglitcher reduces the output glitch to less than 1nV-s, which is ten times less than any other 16-bit, voltage-output DAC. Further, the deglitcher makes the glitch uniform, independent of code.

Ultralow 1nV-s Glitch

Glitches in a DAC's output when it updates can be a big problem in precision applications. Usually, the worst-case glitch occurs when the DAC output crosses midscale. The LTC1597's new proprietary deglitcher reduces the output glitch impulse to 1nV-s, which is at least ten times lower than any of the competition's 16-bit voltage output DACs. In addition, the deglitcher makes the glitch impulse uniform for any code. Figure

5 shows the output glitch for a midscale transition with a 0V to 10V output range.

Unipolar 0V to 10V Outputs with a Single Op Amp

Figure 3 shows the circuit for a 0V to 10V output range. The DAC uses an external reference and a single op amp in this configuration. This circuit can also perform 2-quadrant multiplication where the REF pin is driven by a ±10V AC input signal and V_{OUT} swings from 0V to $-V_{REF}$.

Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB			LSB	
1111	1111	1111	1111	V_{REF} (32,767/32,768)
1000	0000	0000	0001	V_{REF} (1/32,768)
1000	0000	0000	0000	0V
0111	1111	1111	1111	$-V_{REF}$ (1/32,768)
0000	0000	0000	0000	$-V_{REF}$

Figure 7. With a dual op amp, the LTC1597 performs 4-quadrant multiplication. With a fixed 10V reference, it provides a ±10V bipolar output. For fast bipolar settling applications, an LT1468 can be used for the output amplifier.

Bipolar ±10V Output with Two Op Amps

The LTC1597 contains all the 4-quadrant resistors necessary for bipolar operation. For a fixed 10V reference, the circuit shown in Figure 7 gives a precision –10V to 10V output swing, with 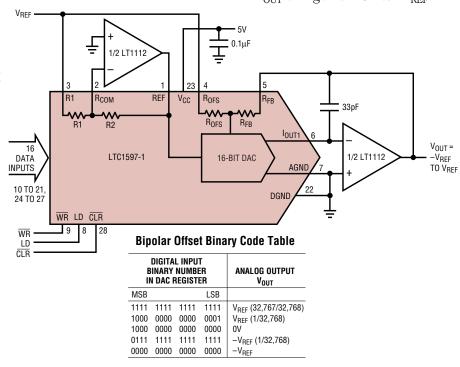a minimum of external components: a feedback capacitor and a dual op amp. The bipolar zero error is 8LSB maximum over temperature. If two LT1468 op amps are used instead of the LT1112, the circuit can perform wider bandwidth 4-quadrant multiplication, where the reference input is driven by a ±10V AC input signal and V_{OUT} swings ±10V .

Figure 6 shows a graph of the multiplying mode total harmonic distortion and noise of the LTC1597/LT1468 combination in both unipolar and bipolar modes of operation. For AC signals less than 40kHz, the THD+noise is superb (better than 90dB) and is still very good out to 100kHz (78dB). Filtering at the output of the LT1468 is necessary to reduce the noise bandwidth to acceptable levels. The wider the bandwidth, the higher the noise floor.

17-Bit Sign Magnitude DAC Gives Perfect Bipolar Zero

Figure 8 shows a novel application of the LTC1597, a 17-bit sign magnitude DAC, and the resulting output coding. This circuit has an extremely accurate bipolar zero error, which is the offset voltage of the current-to-voltage op amp plus the bias current times the DAC feedback resistor. For the LT1468, this corresponds to a maximum bipolar zero error of 0.92LSB (140µV) at 17 bits for room temperature. The circuit uses the LTC1597 in its unipolar mode with the reference input inverted (–V_{REF}, by means of R1 and R2 and an external op amp) for the output voltage range 0V to V_{REF}. When the sign bit changes, the analog switch changes the reference input polarity to noninverting (V_{REF}) for the output range 0V to –V_{REF}.

94dB SFDR Digital Sine Wave Generator

Figure 9 shows the circuit diagram for a variable frequency digital waveform generator. The circuit shows the bipolar configuration for the LTC1597 but the unipolar configuration will work just as well. For a sampling frequency of 50kHz and an output sine wave frequency of 1kHz, the second harmonic distortion is –94dB and the third harmonic is –101dB. The on-chip deglitcher circuit minimizes the code-dependent glitch (which

Bipolar Sign Magnitude Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER					ANALOG OUTPUT V_{OUT}
SIGN	MSB			LSB	
1	1111	1111	1111	1111	V_{REF} (65,535/65,536)
1	0000	0000	0000	0001	V_{REF} (1/65,536)
1	0000	0000	0000	0000	0V
0	0000	0000	0000	0000	0V
0	0000	0000	0000	0001	–V_{REF} (1/65,536)
0	1111	1111	1111	1111	–V_{REF} (65,535/65,536)

Figure 8. This 17-bit sign-magnitude DAC uses the LTC1597 in its unipolar mode with the reference bit inverted (–V_{REF}) for the output range 0V to V_{REF}. When the sign bit changes, the analog switch changes the reference input polarity to noninverting (V_{REF}) for the output range 0V to –V_{REF}. The resulting circuit produces an impressive bipolar zero error of 140µV (0.92LSB) max at room temperature—less than 1LSB at 17 bits.

Figure 9. This digital waveform generator produces a 1kHz sine wave with a second harmonic distortion of –94dB. The sampling frequency is 50kHz.

$$f_0 = \frac{M \cdot f_C}{2^n}$$

Figure 10. The effect of op amp offset on the LTC1597 gain and offset errors in unipolar mode (left) and bipolar mode (right); op amp offset has virtually no effect on DAC linearity; it merely shifts the end points.

	Amplifier Specifications						
Amplifier	V_{OS} μV	I_B nA	A_{OL} V/mV	Voltage Noise nV/√Hz	Current Noise pA/√Hz	Slew Rate V/μs	Gain Bandwidth Product MHz	Power Dissipation mW
LT1001	25	2	800	10	0.12	0.25	0.8	46
LT1097	50	0.35	1000	14	0.008	0.2	0.7	11
LT1112 (dual)	60	0.25	1500	14	0.008	0.16	0.75	10.5/op amp
LT1124 (dual)	70	20	4000	2.7	0.3	4.5	12.5	69/op amp
LT1468	75	10	5000	5	0.6	22	90	117

Table 1. Amplifiers recommended for use with the LTC1597, with relevant specifications

Op Amp Selection Considerations

A significant advantage of the LTC1597 is the ability to choose the I-to-V output op amp to optimize system accuracy, speed, power and cost. Table 1 shows a sampling of op amps and their relevant specifications for this application.

The LTC1597 is designed to minimize the sensitivity of INL and DNL to op amp offset; this sensitivity has been greatly reduced compared to that of competing multiplying DACs. Figure 10 summarizes the effects of op amp offset for both modes of operation. Note that the bipolar LSB size is twice its unipolar counterpart. As Figure 10 shows, op amp offset has a minimal effect on DAC linearity; it merely shifts the end points.

The amplifier's input bias current, which flows through the feedback resistor, adds to the output offset voltage. The amplifier's finite DC open-loop gain also degrades accuracy. The DAC gain error is inversely proportional to the open-loop gain and feedback factor of the op amp. In unipolar mode at full-scale the feedback factor is 0.5; for a 0.2LSB of gain error (REF = 10V) at 16 bits, the open-loop amplifier gain should be greater than 650,000.

The op amp's input voltage and current noise also limit DC accuracy. Noise effects accuracy similarly to voltage and current offsets and adds in an RMS fashion. As with any precision application, and with wide bandwidth amplifiers in particular, the noise bandwidth should be minimized with a filter on the output of the op amp to maximize resolution.

Referring to Table 1, the LT1001 provides excellent DC precision, low noise and low power dissipation. The LT1468 provides the optimum solution for applications requiring DC precision, low noise and fast 16-bit settling.

Conclusion:

Wherever system requirements demand true 16-bit accuracy over temperature, the LTC1597 provides the best solution. The LTC1597 has outstanding 1LSB linearity over temperature, ultralow glitch impulse, on-chip 4-quadrant resistors, low power consumption, asynchronous clear and a versatile parallel interface. Combined with the LT1468 op amp, the LTC1597 provides the best in its class, 1.7µs settling time to 0.0015%, while maintaining superb DC linearity specifications. �
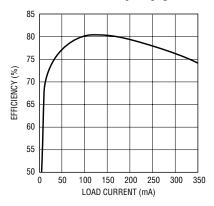

Figure 15. 12V supply at L1A increases efficiency to 81% and output current to 350mA.

Figure 17. 4-cell to –10V converter efficiency

Figure 16. 4-Cell to –10V inverting converter delivers 75mA from a 4V input.

LT1611 4-Cell to –10V Inverting Converter

A –10V low noise output can be generated in a similar manner as the –5V circuit described above. Figure 16's circuit can deliver –10V at up to 60mA from a 3.6V input. Efficiency, graphed in Figure 17, reaches a high of 78%.

Conclusion

The flexibility of individually controlled outputs in multiple-supply applications can make several LT1611/ LT1613 converters attractive compared to a multiple-output flyback design with one large switching regulator and a custom transformer. Changing an output voltage on a multiple output flyback requires changing the transformer turns ratio, hardly a simple task. Conversely, individual control of each output, using the multiple LT1611/LT1613 approach, provides for complete control of each output voltage as well as supply sequencing. The LT1611 and LT1613 SOT-23 switchers provide small, low noise solutions to power generation needs in tight spaces. ⎷LT

Fast Rate Li-Ion Battery Charger

by Goran Perica

Introduction

The recent trend in notebook computers has been toward increasing battery operating time and faster processor speeds. These two requirements, in conjunction with a need for faster battery recharging (1–2 hours) have placed a strain on battery charging circuits and wall adapters. A typical notebook computer system configuration is shown in Figure 1.

Wall adapters are typically AC/DC converters with a 20V output at 3A–4A of load current. When a notebook computer is running, all of the available current from the wall adapter may be consumed by the system, with no power left for charging the battery. However, as soon as the system's power requirements drop below the wall adapter's current limit, the battery charging can resume. In order to recharge the battery in the shortest time possible, the recharging should start as soon as there is any current left over from the system. The ideal situation is when the sum of battery charging current and the system current is just below the wall adapter's current limit:

$$I_{IN\_MAX} > I_{SYS} + I_{CHARGER}$$

where I_{IN_MAX} is the wall adapter current limit, I_{SYS} is the system load current and $I_{CHARGER}$ is the battery charger current.

To achieve this objective, it is necessary to adjust the battery charger current so that the sum of the two currents is just below the maximum available input current, I_{IN_MAX}. The LT1505 incorporates a patented battery charger input current limiting function along with other functions necessary to provide a complete, single-chip battery charging circuit solution.

LT1505 Features

The LT1505 is a constant-current (CC), constant-voltage (CV) current mode switching battery charger circuit with the following features:
- ❏ 0.5% voltage reference
- ❏ 5% output current regulation
- ❏ Output voltage is preset for 3 or 4 Li-Ion cells (12.3V, 12.6V, 16.4V and 16.8V)
- ❏ Output voltage is programmable from 1V to 21V
- ❏ Low V_{IN}-to-V_{OUT} operation (dropout <0.5V)
- ❏ Programmable AC wall adapter current limiting
- ❏ Programmable peak battery charging current
- ❏ Battery drain <10µA in shutdown
- ❏ 94% efficiency

Circuit Description

The LT1505 is a synchronous buck converter using N-channel MOSFETs. The LT1505 operates at 200kHz and can be synchronized to an external clock with a frequency higher than 240kHz. The LT1505 IC has an undervoltage lockout circuit that detects the presence of an input power source and enables the battery charging. Once the undervoltage lockout has been exceeded, the PWM will start running and the input MOSFET M3 is turned ON, thus reducing the voltage drop across its internal body diode D_{BODY} (see Figure 2).

The LT1505 monitors the current from the wall adapter and controls the battery charger current. For example, if a 3A, 20V wall adapter is used along with a 12.6V Li-Ion battery pack, the peak battery charging current, when the system is off, can be set to:

$$I_{BATT\ MAX} = \eta \times I_{IN\_MAX} \times V_{IN}/V_{BATT}$$

where $I_{BATT\ MAX}$ is the maximum battery charging current when the system is idle, η is the efficiency of battery charger, V_{IN} is the wall adapter output voltage and V_{BATT} is the battery charging voltage.

Assuming an efficiency of 90%, the above example could provide battery charging current in excess of 4A. The LT1505 will reduce the battery charging current as soon as the system current exceeds $(I_{IN\_MAX} - I_{CHARGER})$. For example, if a 20V, 3A wall adapter is used and the system draws 2A from the adapter, the available current for charging the battery will be $I_{CHARGER} = 1A$. The resulting battery charging current I_{BATT} will be:

$$I_{BATT} = \eta \times I_{CHARGER} \times V_{IN}/V_{BATT}$$
or
$$I_{BATT} = 0.9 \times 1A \times 20V/12.6V = 1.428A$$

The input current from the wall adapter passes through a current sense resistor, R_{S4}. One part of the input current goes to the system load and the remaining part goes to the LT1505 battery charger. The voltage drop across R_{S4} is monitored by a current comparator with a 90mV threshold. Once the threshold of 90mV is reached, the LT1505 will reduce the programmed battery charging current so that the peak input current does not exceed the preset limit. Thus, the maximum input current (I_{IN_MAX}) will be:
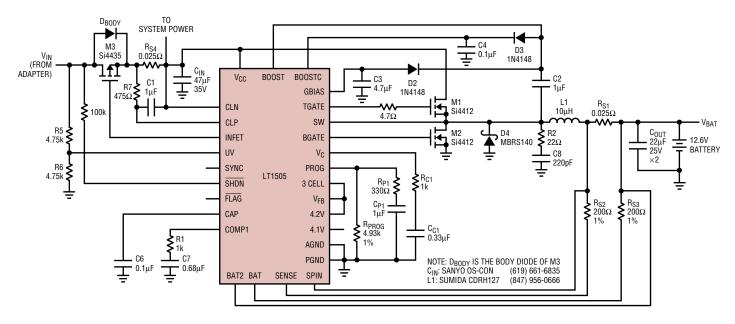
$$I_{IN\_MAX} = I_{SYSTEM} + I_{CHARGER} = 0.090V/R_{S4}$$

Figure 1. Typical notebook computer power supply

Figure 2. 4A Li-Ion battery charger

where I_{SYSTEM} is the system load current, $I_{CHARGER}$ is the LT1505 battery charger current and R_{S4} is the current sense resistor. With the resistor value of 0.025Ω in Figure 2, the input current limit I_{IN_MAX} will be set to 3.6A.

The battery charging current limit is set by R_{PROG}, R_{S1} and R_{S2} and is:

$$I_{BAT\_MAX} = (V_{PROG}/R_{PROG}) \times (R_{S2}/R_{S1})$$

where V_{PROG} is the reference voltage of 2.465V. The values in Figure 2 have been selected for a current limit (I_{BAT_MAX}) of 4A. Changing R_{S1} to 0.050Ω will set the I_{BAT_MAX} to 2A.

Also, the peak battery charging current (I_{BAT_MAX}) can be programmed by the host computer. The I_{BAT_MAX} can be set in increments of 0.25A if R_{PROG} is replaced by a network of resistors, as shown in Figure 3.

The battery charger in Figure 2 achieves high efficiency thanks to synchronous operation and input power FET. The efficiency is as high as 94%, as can be seen in Figure 4.

PCB Layout

When laying out the PCB, a multilayer layout with one of the inner layers as a solid ground plane is recommended. The LT1505 and low power components associated with it should be kept as close together as possible. Additionally, all power components should be kept together and next to LT1505 control circuitry. The goal is to keep all high power switching currents as localized as possible. Components that connect to the ground plane should have vias placed as close as possible to the pins connected to the ground plane. Also, power components should have larger or multiple vias connecting to

Figure 4. Efficiency of 4A, 12.6V battery charger at 20V input

the ground plane. Avoid placing the power components in such a way that input and output currents flow by the LT1505 IC. Also, to keep the component temperature rise low, use as much copper as possible. The use of polygon planes for high power nets such as the ones connecting to V_{IN}, V_{CC}, *continued on page 35*

Figure 3. Programming of battery-charge current

Figure 5. Typical telecom application

No R$_{SENSE}$ Controller Delivers 12V and 100W at 97% Efficiency

by Christopher B. Umminger

Heat removal presents a thorny problem in many of today's compact systems. This is especially the case when power converters deliver high output voltages with several amperes of current and are processing tens to hundreds of watts. In this regime, a converter with only moderate efficiency will have a significant amount of waste heat and may require heat sinks and additional air flow. A very high efficiency converter can reduce the wasted power, which saves space and lowers costs.

The circuit shown in Figure 1 is a power converter that produces a 12V output at up to 8.5A from an input that can range between 12V 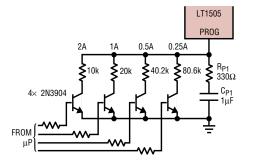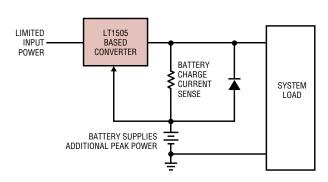and 28V. The 100W of output power is converted at 97% efficiency with only 3W dissipated on the board. No special heat sinks were used other than a widened V$_{IN}$ trace connected to the drain of M1. This point reached a
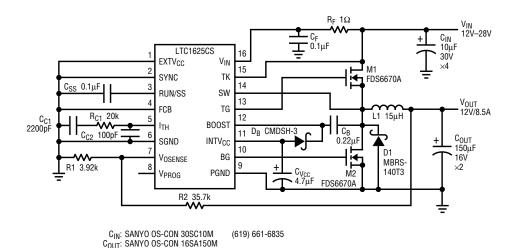
maximum temperature of 75°C in a 25°C environment. L1 is a custom-wound inductor using fourteen turns of 15 gauge wire on a Magnetics, Inc. Kool Mµ[®] 77206-A7 core. The entire converter takes up a volume of only 0.65in^3 and processes an impressive 150W per cubic inch.

The circuit uses the LTC1625 No R$_{SENSE}$[TM] controller to deliver the high output voltage with excellent efficiency. This controller provides true current mode control without using a sense resistor by monitoring the voltage drop across the power MOSFET switches. Eliminating the sense resistor saves board space and improves efficiency. In this application, a 0.01Ω sense resistor would dissipate about 0.7W at full load.

Many current mode controllers use a sense resistor in series with the inductor. Unfortunately, they must restrict the maximum output voltage

due to limits on the input range of the current comparator. However, the LTC1625 has no such constraint. The circuit in Figure 1 uses the LTC1625 in its adjustable mode, with the V$_{PROG}$ pin left open. The internal error amplifier compares the voltage at the V$_{OSENSE}$ pin to a 1.19V reference and an external resistive divider sets the output voltage.

Figure 2 shows that 97% efficiency is achieved over a wide range of load current. The application uses the FCB pin to disable Burst Mode operation and force continuous, synchronous operation down to no load. Enabling Burst Mode would keep the efficiency above 90% down to a load of only 50mA. The current mode control of the LTC1625 incorporates foldback current limiting that reduces the output current to 6A when the output is shorted. ![LT]

Kool Mµ is a registered trademark of Magnetics, Inc.

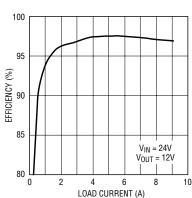

Figure 1. 100W, 12V, 8.5A supply

Figure 2. Efficiency vs load current for Figure 1's circuit

Generating Low Cost, Low Noise, Dual-Voltage Supplies

by Ajmal Godil

Some sensitive electronic applications, such as telecommunication and data acquisition, require both 5V and –5V low noise supplies, which may have to be generated from a single high voltage positive supply. The circuit in Figure 1 shows a cost-effective way to generate 5V and –5V from a single 10V–28V supply by using the low noise LT1777 and a few off-the-shelf components.

The LT1777 is a step-down regulator specially designed for low noise applications. In order to achieve low noise, the LT1777 is equipped with dI/dt limiting circuitry, which is programmed via a small external inductor in the power path. It also contains internal circuitry to limit the dV/dt turn-on and turn-off ramp rates. Figure 2 shows the V_{SW} node voltage and the V_{SW} node current for the low noise LT1777. Figure 3 shows the V_{SW} node voltage and V_{SW} node current for the high voltage LT1676 buck regulator under the same test conditions. It can be seen from Figures 2 and 3 that the

Table 1. Allowable load current on the –5V supply vs input voltage and 5V load current

5V I_{LOAD} (mA)	Maximum allowed current on the –5V supply (mA)
V_{IN} = 10V	
50	40
100	70
200	110
300	130
350	140
V_{IN} = 18V	
50	90
100	150
200	200
300	230
350	200
V_{IN} = 28V	
50	130
100	180
200	260
300	270
350	230

L1A/B: COILTRONICS CTX200-4
        (561) 241-7876
L_{SENSE}: GOWANDA SML32-470K
        (716) 532-2234
C3, C7: AVX TPSD107M010R0065
        (803) 946-0362
C6: 63CV1D0BS
C2: AVX 1206YG475

* SEE TABLE 1 FOR RELATIONSHIP BETWEEN LOAD
  ON +V_{OUT} AND MAXIMUM CURRENT ON –V_{OUT}.
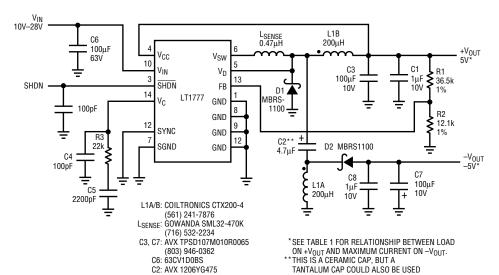** THIS IS A CERAMIC CAP, BUT A
   TANTALUM CAP COULD ALSO BE USED

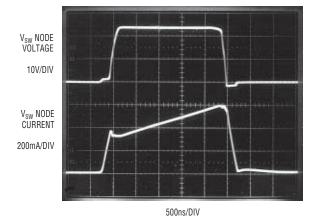**Figure 1. This cost-effective supply generates ±5V from a 10V–28V input.**

Figure 2. V_{SW} node voltage and node current for the LT1777
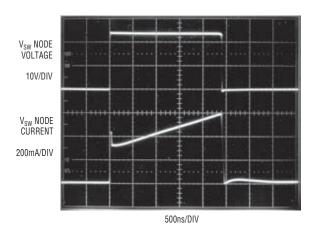

Figure 3. V_{SW} node voltage and node current for the LT1676

Switched Capacitor Voltage Regulator Provides Current Gain

by Jeff Witt

A switched capacitor voltage inverter is normally used to generate a negative supply voltage from a positive input supply. The negative supply current is equal in magnitude to the current drawn from the input. This design idea describes two circuits that use an inverter to double the current between the input and output, increasing efficiency and eliminating heat dissipation problems.

More Efficient than a Linear

If the roles of the ground and output pins are swapped (Figure 1), an inverter will divide the input voltage by two. This circuit can be used in place of a linear regulator when the input voltage is more than twice the desired output, for example, regulation of 12V to 5V or 3.3V.

The circuit's operation is illustrated in Figure 2. An internal oscillator alternately closes and opens four switches. In the first half cycle, switches 1 and 2 are closed and current flows from the input to the output, charging C1. In the second half cycle, switches 3 and 4 are closed, dis-
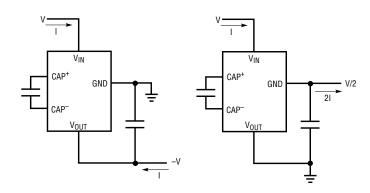

Figure 1. Rewiring a switched capacitor inverter for step-down regulation results in a current gain of 2.

charging C1 into the output. The current delivered to the output is continuous and equal to twice the average input current. Because the output current is continuous, the output voltage ripple is low. Note that C1 and C_{OUT} do not need to be matched, as their voltages are equalized on each cycle.

Figure 3 shows the actual circuit. Instead of halving the input voltage, the LT1054 modulates the input current (through switch 1 of Figure 2) to regulate the output voltage. This cir-

cuit can deliver 200mA at 5V from an input of 11.2V to 13V. Typical efficiency is 74%, compared to 42% for a linear regulator. More importantly, dissipation is decreased from 1.4W for the linear regulator to 0.35W, easily managed by the LT1054's 8-pin surface mount package. For a 3.3V/200mA output, the circuit is 49% efficient, compared to a linear regulator's 27%, with power dissipation reduced from 1.8W to 0.7W. A 6.2Ω resistor in series with C1 shares the dissipated power with the LT1054; no heat sink is needed.

Three Diodes Improve the Inverter

The same advantages can be realized while generating a negative output. However, a switched capacitor inverter does not have the right compliment of switches. By adding three diodes (see Figure 4), the inverter can charge two capacitors in series and then discharge them in parallel to an output capacitor. The absolute value of the output voltage will equal half of the input voltage, minus some loss due to the switches and diodes.

Figure 5 shows a practical circuit, which converts 12V to –4V. The LT1054's servo loop keeps the output regulated to –4V over an input range of 11V to 15V and a load current up to
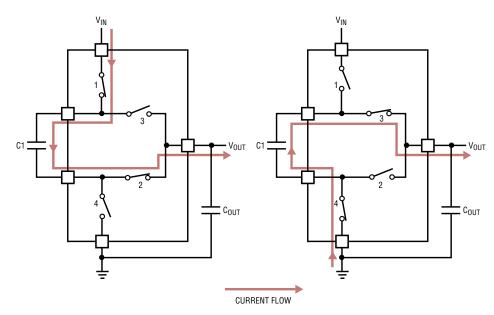

Figure 2. The LT1054's internal switches alternately charge and discharge C1, delivering a continuous current to the output.

Figure 3. This switched capacitor regulator doubles the current between the input and the output, increasing efficiency and eliminating the need for a heat sink.

C1, C2, C3: AVX TAJB336M010R
C4: AVX TAJB685M025R
D1, D2, D3: MOTOROLA MBR0520LT1
Q1: IR IRLML2402

Figure 5. This circuit converts 12V to –4V. Only 63mA of input current is required for 100mA of output current.

100mA. (Unfortunately, there is too much voltage loss to regulate to –5V from a 12V source.) Note that many negative supplies will power loads that can pull the output above ground (op amp circuits in particular); Q1 prevents such a load from pulling U1's V_{OUT} pin above its ground pin.

Because most of U1's operating current flows out of its ground pin, the input current to this circuit is a bit more than one-half of the output current. While delivering 100mA, the input from 12V was measured at 64mA, resulting in 53% efficiency.

One alternative, a switched capacitor inverter followed by a linear regulator, would be 33% efficient at best and power dissipation would be 0.8W. This circuit dissipates only 0.35W, allowing this all–surface mount circuit to run cool. *LT*

CURRENT FLOW

Figure 4. Adding three diodes to a switched capacitor inverter doubles the current between the input and the output.

switch node voltage and current waveforms for the LT1777 are more controlled and rise and fall more slowly than those of the LT1676 regulator. By slowing down the sharp edges during turn-on and turn-off for the power switch, conducted and radiated EMI are reduced.

The circuit in Figure 1 shows three inductors: L1A, L1B and L$_{SENSE}$. L1A and L1B are two windings on a single core to generate ±5V. C2 has been added to minimize coupling mismatches between the two windings (L1A and L1B); this forces the winding potentials to be equal and improves cross-regulation. This creates the dual SEPIC (single-ended primary inductance converter) topology. L$_{SENSE}$ is a user-selectable sense inductor to pro-

gram the dI/dt ramp rate (see the LT1777 Data Sheet for more information). Table 1 summarizes the allowable load current on the –5V supply as a function of input supply voltage and the load current on the 5V supply. Note that 5V and –5V supplies are allowed to droop by 0.25V, which corresponds to 5% load regulation. *LT*

High Current Step-Down Conversion from Low Input Voltages

by Dave Dwelley

Many modern logic systems run with 3.3V as the sole power source. At the same time, some modern microprocessors and ASICs require supply voltages of 2.5V or less. Traditional step-down switching regulators can have difficulty running from the 3.3V supply, because affordable power MOSFETs generally require 5V gate drive to work efficiently. Two attractive solutions to generating 2.5V or less from a 3.3V supply are possible using the LTC1649 and the LTC1430A.

The LTC1649 is a switching regulator controller designed to use 5V MOSFETs while running from an input supply as low as 2.7V. No 5V supply is required. The LTC1649 includes an onboard charge pump to generate the 5V gate drive that the external power MOSFETs require. It also features an architecture designed to use all N-channel external MOSFETs and a high performance voltage mode feedback loop to ensure excellent transient response for use with high speed microprocessors and logic.

Figure 1. 3.3V to 2.5V/15A converter using the LTC1649

Figure 2. Efficiency of Figure 1's circuit

A typical circuit is shown in Figure 1. The 3.3V supply voltage at V_{IN} is converted to a regulated 5V output at CP_{OUT}. This 5V supply powers the PV_{CC2} and V_{CC} pins to provide gate drive to Q3. Q1 and Q2 require an additional charge-pump stage to drive their gates above the V_{IN} supply voltage. D1 and C2 provide this boosted supply at PV_{CC1}. The voltage feedback loop is closed through R1 and R2, with loop compensation provided by an RC network at the COMP pin. Soft-start time is programmed by the value of C_{SS}. Maximum output current is set by R_{IMAX} at the I_{MAX} pin and is sensed across the $R_{DS(ON)}$ of the Q1/Q2 pair, eliminating the need for a high current external resistor to monitor current. The circuit boasts efficiency approaching 95% at 5A (Figure 2).

Some applications have a small 5V supply available, but need to draw the load current from the 3.3V supply. Such an application can use the circuit shown in Figure 3, with the

Figure 3. 3.3V to 2.5V/15A converter using a 5V auxiliary supply and the LTC1430A

How to Design High Order Filters with Stopband Notches Using the LTC1562 Operational Filter (Part 2)

by Nello Sevastopoulos

This is the second in a series of articles describing applications of the LTC1562 connected as a lowpass, highpass or bandpass filter with added stopband notches to increase selectivity. Part 1 (*Linear Technology* VIII:2, May 1998, pp. 28–31) described one method of coupling the four Operational Filter™ building blocks of the LTC1562 to design an 8th order lowpass filter with two stopband notches. Part 2 expands the technique of Part 1 to design an 8th order bandpass filter with two stopband notches.

Throughout this series of articles, notches will be generated by first summing the input signal with a 180 degree out-of-phase signal appearing at the output(s) of the LTC1562 Operational Filter and second, by adjusting the summation gains to yield a zero sum.

Part 1 showed one proprietary method of creating notches in the stopband of a lowpass filter. The essence of this method is briefly revisited in Figure 1, where two of four Operational Filter sections are coupled to form a 4th order lowpass filter with one stopband notch. The notch is obtained by summing the input signal, V_{IN}, with the output, V1A, into the inverting node of the next section of the IC. The two signals, V_{IN} and V1A, will tend to cancel each other at a frequency where they are 180 degrees out of phase. The cancellation will be complete if the amplitudes of V_{IN} and V_{IA} yield equal (and opposite) currents at the summing junction of the op amp of Figure 1, that is if:

$$R_{IN2} = R_{FF2} \bullet (R_{Q1}/R_{IN1}) \qquad (1)$$

In Figure 1, the lead capacitor C_{IN1} raises the frequency where a 180 degree phase shift occurs above the center frequency of the 2nd order section (f_O). The resulting notch frequency is then higher than the cutoff frequency of the 4th order filter.

Figure 1 can be easily modified to make the frequency of the notch *lower* than the center frequency of the 2nd

order section from which it is derived. This is useful in bandpass filters where an unwanted frequency lower than the center frequency of the filter must be rejected. This is shown in Figure 2, where the input signal is summed with output V2A instead of output V1A. The frequency of the resulting notch is:

$$f_{N2} = f_{O1} \bullet \sqrt{1 - \frac{R1}{R_{Q1}} \bullet \frac{C}{C_{IN1}} \bullet \frac{R21}{R_{IN1}}} \qquad (2)$$

(R1 = 10k; C = 159.15pF)

and the gain conditions dictating Equation 1 now translate to:

$$R_{IN2} = R_{FF2} \bullet \left(\frac{R_{Q1}}{R1} \bullet \frac{C_{IN1}}{C} \right) \qquad (3)$$

The circuit of Figure 2 can be used to build a 4th order bandpass filter with one notch below its center frequency. Such a filter can simultaneously detect a tone and reject an unwanted frequency located in the vicinity of the passband.
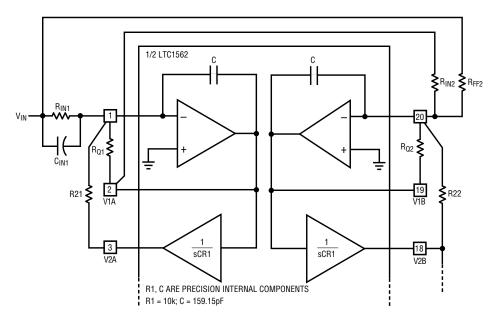

Figure 1. Two out of four Operational Filter sections are coupled to form a 4th order lowpass filter with one stopband notch.
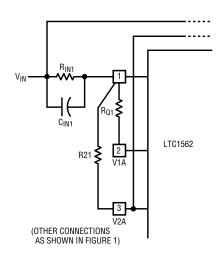

Figure 2. Figure 1's circuit modified to make the frequency of the notch *lower* than the center frequency of the 2nd order section from which it is derived.
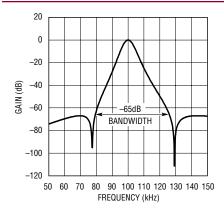
Figure 3. Theoretical amplitude response of 8th order, 100kHz bandpass filter

The notch techniques of Figures 1 and 2 will be referred as "feedforward." This is necessary to separate these techniques from others to be shown later, in Part 3 of this series of articles.

The feedforward notch technique of Figure 2 can be advantageously combined with Figure 1 to realize sharp bandpass filters with two stopband notches: one notch below and one above the center frequency. Filters of this type can be very selective, although they are quite cumbersome to design. A step-by-step design procedure is illustrated below.

A Practical Example

An 8th order 100kHz bandpass filter is realized, through FilterCAD™ for Windows® (available at no charge from Linear Technology—see the "Design Tools" page in this issue), by cascading four 2nd order sections of equal Q. The –3dB band-edges are arithmetically symmetric with respect to the filter's 100kHz center frequency and signals below 80kHz and above 125kHz are attenuated by 60dB or more. Figure 3 shows the theoretical amplitude response and Table 1 shows the desired filter parameters, namely, the center frequencies, Qs and notch frequencies. The filter of Figure 3/Table 1 can be realized by decomposing the 8th order realization into two independent 4th order filter sections and then cascading these two 4th order sections, which is an easier task than designing an 8th order elliptic bandpass filter all at once. FilterCAD, in custom mode,

should be used to perform this operation. Figure 4 and Table 2 show the filter decomposition and the cascading sequence; note the left and right notches. Figure 5 uses the LTC1562 Operational Filter to realize the filter of Figure 3 as decomposed in Figure 4. The design is split into two 4th order sections. The algorithm to calculate the external passive components is outlined below.

In order to obtain a practical realization that closely approximates the theoretical one, the Q of each 2nd order section will be lowered by 15%. (Please consult the LTC1562 final data sheet.)

In order to follow the long and tedious algorithm below, consider the intuitive outline: We need to calculate the following set of passive components for the first 4th order section: R_{IN1}, C_{IN1}, R21, R_{Q1}, and R_{IN2}, R_{FF2}, R22 and R_{Q2}. The resistors R21, R_{Q1},

R22 and R_{Q2} are easily calculated via the expression for the center frequency, f_{Oi}, and Q_i for the 2nd order section "i." The expression for the notch, equation (2), involves the product of $R_{IN1} \bullet C_{IN1}$, so neither component can be calculated separately. Instead, R_{IN1} is calculated by considering the maximum gain (which occurs around the center frequency f_{O1}) at either node V1A or V2A. This controls premature internal clipping. Once R_{IN1} is set, C_{IN1} is easily calculated via equation (2) for the lower band notch. Similarly, equation (3) defines the ratio of R_{IN2} to R_{FF2}, so neither of these components can be calculated independently of the other. R_{FF2} is calculated by considering the gain factor ("GAIN") of the 4th order filter section at the V1B output (Figure 1/Table 2)). Once R_{FF2} is set, R_{IN2} is calculated via equation (3).

Table 1. Parameters of the four sections of an 8th order, 100kHz bandpass filter

f_0	Q	f_N	Q_N	Type
99.9687e3	10.0000	——	——	BP
96.9964e3	10.0000	129.2814e3	——	LPN
103.0322e3	10.0000	77.3023e3	——	HPN
100.0000e3	10.0000	——	——	BP

Figure 4. Cascading two 4th order bandpass sections to realize the filter of Figure 3.

Table 2. Filter decomposition and cascading sequence

f_{01} = 96.9964k Q1 = 10	f_{03} = 100k Q3 = 10
f_{02} = 99.9687k Q2 = 10 f_{N2} = 77.3k	f_{04} = 103.0322k Q4 = 10 f_{N2} = 129.2814k
H(s) = GAIN • N(s)/D(s)	H(s) = GAIN • N(s)/D(s)
GAIN = 0.2823	GAIN = 0.1788
N(s) = A1s(s^2 + 235 • 9072 • 10^9)	N(s) = A1s(s^2 + 659 • 83 • 10^9)
A1 = 62.8122 • 10^3	A1 = 62.8319 • 10^3

The same design method is later repeated to derive the passive components for the second 4th order section:

I. Calculate the passive components of the of the first 4th order section
(f_{O1} = 96.9964kHz, Q = 8.5, f_{O2} = 99.9687kHz, Q = 8.5, f_{n2} = 77.3kHz)

1. Calculate the center frequency-setting resistor, R21:
(For details, please refer to the LTC1562 data sheet.)
$R21 = (100kHz/f_{O1})^2 \cdot 10k$ = 10.629k
(choose the closest 1% value, R21 = 10.7k (1%))

2. Calculate the Q-setting resistor, R_{Q1}:
(For details, please refer to the LTC1562 data sheet)
$R_{Q1} = Q1 \sqrt{R21 \cdot 10k}$ = 87.925k
(choose the closest 1% value, R_{Q1} = 86.6k (1%))

3. Calculate the input resistor R_{IN1} from the following expression(s):
3a. if $f_{O1} \leq 100kHz$ (for LTC1562)

$$R_{IN1} = Q1 \cdot R21 \cdot \sqrt{1 + \frac{1}{Q1^2 \cdot \left(1 - \frac{f_{N2}^2}{f_{O1}^2}\right)^2}} \quad (4)$$

R_{IN1} = 95.56k

Although not applicable for this example, thoroughness dictates mentioning the case below:
3b. if $f_{O1} \geq 100kHz$ (for LTC1562)

$$R_{IN1} = R_{Q1} \cdot \sqrt{1 + \frac{1}{Q1^2 \cdot \left(1 - \frac{f_{N2}^2}{f_{O1}^2}\right)^2}} \quad (5)$$

Make sure, in either case 3a or 3b, that R_{IN1} is greater than R21, that is, the DC gain at pin 3 in Figure 5 is less than unity; if not set R_{IN1} = R21 and proceed to step 4a.

The expression for R_{IN1} sets the gain at f_{O1} equal to unity at the node of maximum swing (V1A or V2A). Note that, for high Qs, the gain at f_{O1} is the maximum gain. If you know the spectrum of the signals that will be applied to the filter input and if internal gains higher than unity will be allowed, the value of R_{IN1} can be reduced to improve the input signal-to-noise ratio.

4a. Use the value of R_{IN1}, calculated above, and calculate the value for the input capacitor C_{IN1} from the notch equation (2).

$$C_{IN1} = \frac{R1}{R_{Q1}} \cdot \frac{R21}{R_{IN1}} \cdot C \left[\frac{1}{1 - \left(\frac{f_{N2}^2}{f_{O1}^2}\right)}\right] \quad (6)$$

($f_{N1} < f_{O1}$; C = 159.15pF)

C_{IN1} = 5.639pF.

Use the commercially available NPO type 0402 surface mount capacitor with the value nearest the ideal value of C_{IN1} calculated above. For instance, for C_{IN1}, choose an off-the-shelf 5.6pF capacitor.

Figure 6. Measured amplitude response of Figure 5's filter

4b. Recalculate the value of R_{IN1} after C_{IN1} is chosen.
$R_{IN1} = (C_{IN1(ideal)} R_{IN1(ideal)})/ C_{IN1(NPO,0402)}$ = 96.22k
Choose the closest 1% value:
R_{IN1} = 95.3k (1%)

5. Calculate the frequency- and Q-setting resistors R22, R_{Q2}, as done in steps 1 and 2, above. Choose the closest 1% standard resistor values.
R22 = 10k (1%);
R_{Q1} = 84.5k(1%)

6. Calculate the feedforward resistor, R_{FF2}:
$1/(R_{FF2} C)$ = Gain • A1;
C = 159.15pF

The values for parameter (Gain • A1) are provided by FilterCAD; they relate to the coefficients of the numerator of the transfer function (V1B/V_{IN} in Figure 1); a passband AC gain of unity is assumed (see Table 2). Please note that, for a lowpass case, as in Part 1 of this article series, the value of (Gain • A1) is the DC gain of the filter and its value can be easily set without software assistance.

Equating the numerator of the filter transfer function with the values provided by FilterCAD:

$$\frac{V_{1B}}{V_{IN}} = \frac{s(s^2 + \omega_{N2}^2)}{(R_{FF2} \cdot C) \cdot D(s)} = \frac{GAIN (A1s)(s^2 + A2)}{D(s)} \quad (7)$$

GAIN = 0.2823
A1 = 62.8122 • 10^3
A2 = $(2\pi f_{N2})^2$ = 235.9 • 10^9

$R_{FF2} = 1/((Gain A1) C)$ = 354.35k;
C = 159.15pF
R_{FF2} = 357k(1%)

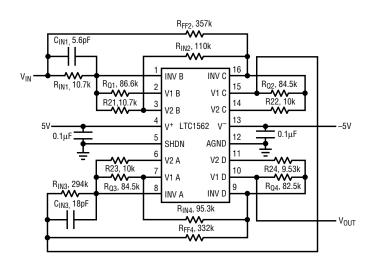

Figure 5. Hardware realization of the filter in Figure 3, using all four sections of an LTC1562

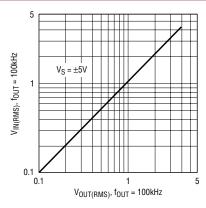**Figure 7. Gain linearity of Figure 5's filter, measured at the 100kHz theoretical center frequency**

7. Solve for R_{IN2} by using Equation (3), which dictates the gain condition for the occurrence of the notch:

R_{IN2} = $(R_{FF2}\ R_{Q1}\ C_{IN1})/(R1\ C)$ = 108.785k; $(R1,C)$ = (10k, 159.15pF)
R_{IN2} = 110k (1%)

II. Calculate the passive components of the second 4th order section
(f_{O3} = 100kHz, Q3 = 8.5, f_{O4} = 103.0322kHz, Q4 = 8.5, f_{n4} = 129.2814kHz)
Except for the bandpass gain calculations, the algorithm will be the same as the lowpass design of Part 1 of this article.

1. R23 = $(100kHz/f_{O3})^2 \bullet$ 10k = 10k (1%)
2. R_{Q3} = Q3 $\sqrt{R23 \bullet 10k}$ = 85k, R_{Q3} = 84.5k (1%)
3. Calculate the input resistor R_{IN3} from the following expression(s):
3a. if $f_{O3} \leq$ 100kHz (for LTC1562)

$$R_{IN3} = Q3 \bullet R23 \bullet \sqrt{1 + \left(1 - \frac{f_{O3}^2}{f_{N4}^2}\right)^2 \bullet Q3^2} \quad (8)$$

R_{IN3} = 302.41k

3b. if $f_{O3} \geq$ 100kHz (for LTC1562)

$$R_{IN3} = R_{Q3} \bullet \sqrt{1 + \left(1 - \frac{f_{O3}^2}{f_{N4}^2}\right)^2 \bullet Q3^2} \quad (9)$$

For f_{O3} = 100kHz, as in the example above, either expression can be used. Note that the expression for R_{IN3} in 3b, above, is the same as expression for R_{IN1} shown in Part 1 of this article.

4a. Use the theoretical value for R_{IN3}, calculated above, and calculate the value of the input capacitor C_{IN3} from the notch equation (2) of part 1 of this article; for convenience this is repeated below:

$$C_{IN3} = C \bullet \frac{R_{Q3}}{R_{IN3}} \bullet \left(1 - \frac{f_{O3}^2}{f_{N4}^2}\right) \quad (10)$$

C_{IN3} = 17.86pF;

Use a commercially available NPO-type 0402 surface mount capacitor with the value nearest the ideal value of C_{IN3} calculated above. For instance, C_{IN3} = 18pF.

4b. Recalculate the value for R_{IN3} calculated in step 3a after C_{IN3} is chosen.

R_{IN3} = $(C_{IN3(ideal)}\ R_{IN3(ideal)})/C_{IN3(NPO,0402)}$ = 300.058k
R_{IN3} = 294k (1%)

5. Calculate the frequency- and Q-setting resistors, R24 and R_{Q4}, as done in steps 1 and 2, above. Choose the nearest 1% standard value.

R24 = 9.42k; R24 = 9.53k (1%)
R_{Q4} = 82.97k; R_{Q4} = 82.5k (1%)

6. Calculate the feedforward resistor, RFF4. First equate the numerator of the 4th order filter transfer function with the values provided by FilterCAD (see Table 2):

$$\frac{V_{OUT}}{V_{1B}} = \frac{s}{R_{FF4} \bullet C} \bullet \frac{\omega_{O3}^2}{\omega_{O4}^2} \bullet \frac{s^2 + \omega_{N4}^2}{D(s)} = \quad (11)$$

$$\frac{GAIN \bullet A1s \bullet (s^2 + \omega_{N4}^2)}{D(s)}$$

$$THEN\ R_{FF4} = \frac{1}{GAIN \bullet A1} \bullet \frac{1}{C} \bullet \frac{\omega_{O3}^2}{\omega_{N4}^2}$$

GAIN = 0.1788
A1 = 62.8319 • 10^3

R_{FF4} = 334.64k, choose R_{FF4} = 332k (1%).

7. Solve for R_{IN4} by using equation (1) of Part 1 of this article, which dictates the gain condition for the occurrence of a notch. For convenience, this gain condition is repeated below.

$$R_{IN4} = R_{FF4} \bullet \frac{R_{Q3}}{R_{IN3}} \quad (12)$$

R_{IN4} = 95.422k; R_{IN4} = 95.3k(1%)

Experimental Results

Figure 6 shows the measured amplitude response of the filter of Figure 5. The values of the passive component are as calculated above and as shown in Figure 5. The measured amplitude response closely approximates the ideal response as synthesized by FilterCAD. The peak frequency with standard 1% resistor values and 5% capacitor values is 100.65kHz (0.65% off). The higher frequency notch, although it shows a respectable depth of 70dB, is not as well defined as the notch below the filter's center frequency, yet the –65dB bandwidth is as predicted by FilterCAD. The 10dB lack of the upper band notch depth is due to the finite speed of the internal op amps; they cause the practical 180 degree phase shift frequency and the gain at V1A's output to depart slightly from the theoretical calculations.

For the sake of perfection, the notch depth can be easily restored by tweaking the value of R_{Q3}; the new R_{Q3} will be 75k. This is shown with dashed lines in Figure 6. This, however, lowers the passband gain by the ratio of the new to the old R_{Q3} value, that is, by about –1.0dB (you cannot fool mother nature). Depending on the application, the 10dB of additional notch depth for 1.5dB of passband gain loss may be a reasonable trade. The passband gain can also be corrected by lowering the values of either pair, (R_{FF2}, R_{IN2}) or (R_{FF4}, R_{IN4}), by the same amount (1.5dB). In Figure 6, the gain was restored to 0dB by changing the values of R_{IN2}, R_{FF2} to 93.1k and 300.1k respectively.

The total integrated noise was an impressively low 69μV_{RMS}, allowing a signal-to-noise ratio well in excess of 80dB. The input signal-to-noise ratio can be further increased if the pass-

band gain can be higher than 0dB or if internal nodes are allowed to have gains higher than 0dB. Please contact the LTC Filter Design and Applications Group for further details.

The low noise behavior of the filter makes it useful in applications where the input signal has a wide voltage range. This is true provided the filter magnitude response does not change with varying input signal levels, that is, the filter gain is linear. The gain linearity measured at the 100kHz theoretical center frequency of the filter is shown in Figure 7. The gain is perfectly linear for input amplitudes up to $1.25V_{RMS}$ ($3.5V_{P-P}$) so an 84dB dynamic range can be claimed. The input signal, however, can reach amplitudes up to $3V_{RMS}$ ($8.4V_{P-P}$, 92dB SNR) with some reduction in gain linearity. ⎏

Conclusion

The LTC1735 and LTC1736 are the latest members of Linear Technology's family of constant frequency, N-channel high efficiency controllers. With new protection features, improved circuit operation and strong MOSFET drivers, the LTC1735 is an ideal upgrade to the LTC1435/LTC1435A for higher current applications. With the integrated VID control, the LTC1736 is ideal for CPU power applications. The high performance of these controllers with wide input range, 1% reference and tight load regulation makes them ideal for next generation designs. ⎏

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level is $44\mu V_{RMS}$ over a bandwidth of 800kHz or 98dB below the maximum unclipped output.

Acknowledgments

Philip Karantzalis and Nello Sevastopoulos of LTC's Monolithic Filter Design and Applications Group contributed to the application examples.

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2. Sevastopoulos, Nello. "How to Design High Order Filters with Stopband Notches Using the LTC1562 Quad Operational Filter, Part 1." *Linear Technology* VIII:2 (May 1998), pp. 28-31.
3. Sevastopoulos, Nello. "How to Design High Order Filters with Stopband Notches Using the LTC1562 Quad Operational Filter, Part 2." in the Design Ideas section of this issue of *Linear Technology.*
4. LTC1562 Final Data Sheet.
5. For example: Schwartz, Mischa. *Information Transmission, Modulation, and Noise*, fourth edition, pp. 180–192. McGraw-Hill 1990. ⎏

SW, V_{BAT} and GND in Figure 2 will help in spreading the heat and will reduce the power dissipation in conductors and MOSFETs.

Other Applications

The LT1505 can also be used in other system topologies, such as the telecom application shown in Figure 5. The circuit in Figure 5 uses the battery to supply peak power demands. By doing so, the required peak power from the wall adapter can be much lower than the peak power required by the load. The wall adapter has to supply the average power only.

Conclusion

The LT1505 is a complete, single-chip battery charger solution for today's demanding charging requirements in high performance laptop applications. The device requires a small number of external components and provides all necessary functions for battery charging and power management. High efficiency and small size allow for easy integration with the laptop circuits. Also, by adding a simple external circuit, charging can be easily controlled by the host computer, allowing for more sophisticated charging schemes. ⎏

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lower cost LTC1430A replacing the LTC1649. The LTC1430A does not include the 3.3V to 5V charge pump and requires a 5V supply to drive the external MOSFET gates. The current drawn from the 5V supply depends on the gate charge of the external MOSFETs but is typically below 50mA, regardless of the load current on the 2.5V output. The drains of the Q1/Q2 pair draw the main load current from the 3.3V supply. The remaining circuitry works in the same manner as in Figure 1. Efficiency and performance are virtually the same as the LTC1649 solution, but parts count and system cost are lower.

In a 3.3V to 2.5V application, the steady-state, no-load duty cycle is 76%. If the input supply drops to 3.135V (3.3V – 5%), the duty cycle requirement rises to 80% at no load, and even higher under heavy or transient load conditions. Both the LTC1649 and the LTC1430A guarantee a maximum duty cycle of greater than 90% to provide acceptable load regulation and transient response. The standard LTC1430 (not the LTC1430A) can max out as low as 83%—not high enough for 3.3V to 2.5V circuits. Applications with larger step-down ratios, such as 3.3V to 2.0V, can use the circuit in Figure 3 successfully with a standard LTC1430. ⎏

The LTC1658 and LTC1655: Smallest Rail-to-Rail 14-Bit and 16-Bit DACs

by Hassan Malik

Expanding the rail-to-rail, voltage output DAC family, Linear Technology introduces two new voltage output DACs that break the size/bits barrier. The LTC1658 is a 14-bit rail-to-rail voltage output DAC in a tiny MSOP-8 package and the LTC1655 is a 16-bit voltage output DAC in an SO-8 package. Both of these DACs also provide a convenient upgrade path for users of LTC's 12-bit voltage output DAC family. The LTC1658 draws only 270μA from a 3V or 5V supply and is 14-bit monotonic over temperature. The LTC1655 draws 600μA from a 5V supply and is 16-bit monotonic over temperature.

These DACs have a flexible 3-wire serial interface that is SPI/QSPI and MICROWIRE compatible.

Figures 1 demonstrates the ease of using the LTC1658. The output swings from 0V to V_{REF} at full-scale. V_{REF} should be less than or equal to V_{CC} to prevent the loss of codes and degradation of PSRR near full-scale. The input serial data is loaded as one 16-bit word with two dummy bits. The digital inputs are TTL/CMOS level compatible and the CLK input has an internal Schmitt trigger for noise immunity. This allows direct optocoupler interfacing to the part. Figure 2 plots the part's 0.25LSB typical DNL.

A typical application for the LTC1655 is shown in Figure 3. The LTC1655 has the same interface as the LTC1658 and is also capable of being daisy chained. There is an onboard 2.048V bandgap reference connected internally to the 16-bit DAC. The rail-to-rail output nominally swings from 0V to 4.096V, since there is a gain of two in the output amplifier. The reference pin can be overdriven to a value higher than 2.048V if a larger output swing is desired. Since there is a gain of 2 from the reference pin to the output at full-scale, the voltage on the REF pin must always be less than $V_{CC}/2$. Figure 4 plots the typical DNL of the LTC1655. *LT*
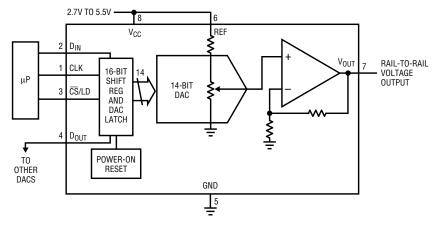

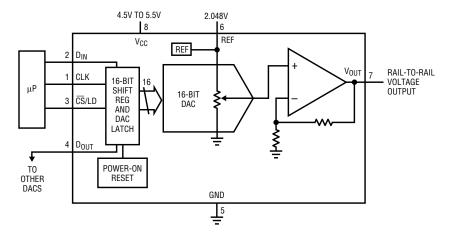
Figure 1. LTC1658 block diagram

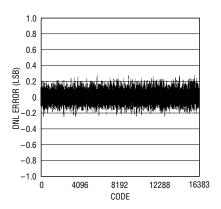Figure 2. The LTC1658 14-bit rail-to-rail DAC in MSOP has 0.25LSB typical DNL.

Figure 3. LTC1655 block diagram
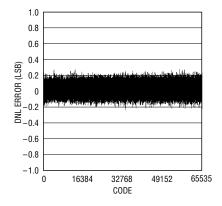

Figure 4. LTC1655 typical DNL plot

New Device Cameos

LTC1502-3.3
Single Cell to 3.3V
Inductorless DC/DC Converter

The LTC1502-3.3 is LTC's latest offering in the regulated charge pump arena. This new charge pump is the only inductorless single-cell boost converter in the industry. The part employs a quadrupler switched capacitor architecture to generate a regulated 3.3V supply from a single NiCd or alkaline cell. Start-up enhancement circuitry enables the LTC1502-3.3 to power up with V_{IN} as low as 0.8V. Only five small ceramic capacitors are required to make a complete 3.3V single-cell power supply with 10mA of output load capability.

The part also has a shutdown feature that disconnects the load from V_{IN} and reduces quiescent current to only 5µA. The LTC1502-3.3 is short-circuit protected and can survive an indefinite V_{OUT} short to GND. Small size (8-pin MSOP package) and low quiescent current (40µA typical) make the LTC1502-3.3 ideal for space conscious, low power applications such as pagers and PDAs. Since the V_{OUT} pin is high impedance during shutdown, the part is also well suited for single-cell battery backup applications.

LTC1661 Micropower Dual 10-Bit DAC with Sleep Mode Available in MS-8

The LTC1661 is a micropower, dual, 10-bit voltage-output DAC that is available in a tiny 8-pin MSOP package. Required board area is only 0.01in^2 per DAC.

Operating on a single 2.7–5.5V supply, the LTC1661 draws just 60µA per DAC (120µA total for the part) for true micropower performance. Sleep mode further reduces total supply-plus-reference current to just 1µA.

The LTC1661 is guaranteed monotonic over temperature—differential nonlinearity error is typically ±0.2LSB (±0.75LSB Max). Each DAC has a

gain of 1 from reference to output; the Reference pin can be tied to V_{CC} for full rail-to-rail operation. The output amplifiers are stable driving capacitive loads of up to 1000pF and can source or sink up to 5mA. The outputs swing to within a few millivolts of either supply rail when unloaded and have an equivalent output resistance of 85Ω when driving a load to the rails.

The 3-wire serial interface uses a 16-bit input word comprising 4 control bits, 10 input-code bits, and 2 don't-care bits. Power-on reset is also provided. The input logic is double buffered for additional flexibility in interfacing with the microprocessor and for more effective control of multiple chips that share clock and data lines.

Low supply current, power-saving Sleep mode and extremely compact size make the LTC1661 ideal for battery-powered applications, while its straightforward usability, high performance and wide supply range make it an excellent choice as a general-purpose converter.

LTC1841/LTC1842/LTC1843 Dual Micropower Comparator with Built-In Reference

The LTC1841/LTC1842/LTC1843 are dual micropower comparators with built-in references (LTC1842/LTC1843). These parts feature less than 5.7µA supply current over temperature, a 1.182V ±1% reference (LTC1842/LTC1843), programmable hysteresis (LTC1842/LTC1843) and open-drain output comparators that can sink greater than 20mA. The reference output can drive a bypass capacitor of up to 0.01µF without oscillation.

The comparators operate from single 2V to 11V supplies or ±1V to ±5.5V supplies (LTC1841). Comparator hysteresis is easily programmed using two resistors and the HYST pin. The comparator's input operates from the negative supply to within 1.3V of

the positive supply. The comparator output stage can typically sink greater than 20mA. By eliminating the cross-conduction current that normally occurs when the comparator changes logic states, power supply glitches are eliminated.

The LTC1841/LTC1842/LTC1843 are available in 8-pin SO packages.

LTC1605-1/-2: 100ksps 16-Bit ADC Now Available with 0V to 4V and ±4V Analog Input Ranges

The LTC1605-1 and LTC1605-2 are the newest members of Linear Technology's family of 16-bit ADCs. The two new ADCs offer the user a choice of analog input ranges to help make full use of the wide dynamic range offered by these converters. These 100ksps sampling ADCs feature 16-bit resolution with no missing codes and ±2LSB INL. They operate from a single 5V supply with typical power dissipation of only 55mW. They are offered in both 28-pin PDIP and SSOP packages.

The LTC1605-1 has an analog input range of 0V to 4V with ±20V overvoltage protection. This 16-bit ADC is ideally suited for single-supply systems. It is a complete data acquisition system containing a differential, successive-approximation A/D that uses switched capacitor technology to perform a 16-bit conversion. The analog front end consists of a resistor divider network followed by a sample-and-hold that allows fast moving signals to be digitized. The LTC1605-1 also has a trimmed bandgap reference that can be overdriven with an external reference if greater accuracy is needed. It also features a simple parallel I/O where the digital output word can be read as a 16-bit word or as two 8-bit bytes. The digital output word format for the LTC1605-1 is straight binary.

The LTC1605-2 has a bipolar analog input range of ±4V with ±20V overvoltage protection (±15V overdrive recoverable) operating on a single 5V supply. It is also a complete data acquisition system with the same features and parallel I/O as the

LTC1605-1. The LTC1605-2 digital output word format is two's complement.

LTC1754-5 Regulated Charge Pump Delivers 50mA in an SOT-23 Package

The LTC1754-5 is the newest addition to Linear Technology's industry leading family of switched capacitor regulated charge pumps. Combining the best features of its predecessors, it delivers a full 50mA from a tiny SOT-23 package while stepping up from 3V to a regulated 5V. The 6-pin package provides additional functionality by including shutdown capability. Finally, it has built-in thermal shutdown circuitry that allows it to survive a continuous short circuit to ground at its output.

The quiescent supply current of the LTC1754-5 is only 13µA. This low supply current means very low power consumption in light load applications. Furthermore, because it uses Burst Mode operation, its efficiency is typically 82.7% when delivering moderate to high load current. This efficiency is very close to the ideal 83.3% for a 3V to 5V regulating charge pump. In shutdown, the supply current is guaranteed to be less than 1µA.

With no inductors and only three small capacitors, the LTC1754-5 regulated charge pump delivers significant power from a small amount of real estate.

LTC1569-7: Unique 10th Order, Linear-Phase, DC Accurate Lowpass Filter is Tunable by a Single Resistor

The LTC1569-7 is a self-contained 10th order linear-phase filter featuring cutoff frequencies up to 256kHz while operating on supplies from 3.3V (3V minimum) up to ±5V. Cutoff frequencies up to 128kHz can also be obtained with a 3V (2.7V minimum) supply. Unlike other monolithic filters, the LTC1569-7's precision on-chip oscillator allows the cutoff frequency to be set accurately (within 2%) by a single resistor. Alternatively, for swept cutoff frequency applications, an external clock can be used.

The amplitude response of the LTC1569-7 approximates a root raised cosine, with an alpha of 0.5, for phase linearity with excellent attenuation. The attenuation of the LTC1569-7 at 1.5 times the cutoff frequency is 55dB, whereas attenuation is in excess of 60dB at 2.1 times the cutoff frequency.

The DC offset of the LTC1569-7 is typically 2mV. Its DC gain linearity and SINAD are suitable for 12-bit systems. The input of the filter can be configured as single ended or differential.

When operated at full bandwidth, the LTC1569-7 consumes 20mA on a single 5V supply but, when slower sampling rates are required (that is, at lower cutoff frequencies), the device automatically switches to a reduced supply current, which can be as low as 5mA. The LTC1569-7 is available in an 8-pin SO package. *LT*

for the latest information on LTC products, visit www.linear-tech.com

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For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

DESIGN TOOLS

Applications on Disk

FilterCAD™ 2.0 CD-ROM — This CD is a powerful filter design tool that supports all of Linear Technology's high performance switched capacitor filters. Included is FilterView™, a document navigator that allows you to quickly find Linear Technology monolithic filter data sheets, the FilterCAD manual, application notes, design notes and *Linear Technology* magazine articles. It *does not* have to be installed to run FilterCAD. It is not necessary to use FilterView to view the documents, as they are standard .PDF files, readable with any version of Adobe Acrobat™. FilterCAD runs on Windows® 3.1 or Windows 95. FilterView requires Windows 95. The FilterCAD program itself is also available on the web and will be included on the new LinearView™ CD.
Available at no charge.

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp. Available at no charge

SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim. Available at no charge

SwitcherCAD™ — The SwitcherCAD program is a powerful PC software tool that aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. 144 page manual included. $20.00

SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

Micropower SwitcherCAD™ — The MicropowerSCAD program is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components which surround the DC/DC converter. In the case of a battery supply, MicropowerSCAD can perform a battery life simulation. 44 page manual included. $20.00

MicropowerSCAD supports the following LTC micropower DC/DC converters: LT1073, LT1107, LT1108, LT1109, LT1109A, LT1110, LT1111, LT1173, LTC1174, LT1300, LT1301 and LT1303.

Technical Books

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook, Vol II — This 1248 page supplement to the 1990 Linear Databook is a collection of all products introduced in 1991 and 1992. The catalog contains full data sheets for over 140 devices. The 1992 Linear Databook, Vol II is a companion to the 1990 Linear Databook, which should not be discarded. $10.00

1994 Linear Databook, Vol III—This 1826 page supplement to the 1990 and 1992 Linear Databooks is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The 1994 Linear Databook Vol III is a companion to the 1990 and 1992 Linear Databooks, which should not be discarded. $10.00

1995 Linear Databook, Vol IV—This 1152 page supplement to the 1990, 1992 and 1994 Linear Databooks is a collection of all products introduced since 1994. A total of 80 product data sheets are included with updated selection guides. The 1995 Linear Databook Vol IV is a companion to the 1990, 1992 and 1994 Linear Databooks, which should not be discarded. $10.00

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1990 Linear Applications Handbook, Volume I — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook, Volume II — Continues the stream of "real world" linear circuitry initiated by the 1990 Handbook. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. References and articles from non-LTC publications that we have found useful are also included. $20.00

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Notes 55 through 69 and Design Notes 70 through 144. Subjects include switching regulators, measurement and control circuits, filters, video designs, interface, data converters, power products, battery chargers and CCFL inverters. An extensive subject index references circuits in LTC data sheets, design notes, application notes and *Linear Technology* magazines. $20.00

1998 Data Converter Handbook — This impressive 1360 page handbook includes all of the data sheets, application notes and design notes for Linear Technology's family of high performance data converter products. Products include A/D converters (ADCs), D/A converters (DACs) and multiplexers—including the fastest monolithic 16-bit ADC, the 3Msps, 12-bit ADC with the best dynamic performance and the first dual 12-bit DAC in an SO-8 package. Also included are selection guides for references, op amps and filters and a glossary of data converter terms. $10.00

Interface Product Handbook — This 424 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422, V.35 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, mixed RS232 and RS485 devices, 10kV ESD protection of RS232 devices and surface mount packages.
Available at no charge

Power Solutions Brochure — This collection of circuits contains real-life solutions for common power supply design problems. There are over 70 circuits, including descriptions, graphs and performance specifications. Topics covered include battery chargers, power supplies for desktop and portable computers, supplies for portable electronics, telecommunications supplies, offline supplies and various other power management techniques, including Hot Swap™ circuits.
Available at no charge

Data Conversion Solutions Brochure — This 64 page collection of data conversion circuits, products and selection guides serves as excellent reference for the data acquisition system designer. Over 60 products are showcased, solving problems in low power, small size and high performance data conversion applications—with performance graphs and specifications. Topics covered include ADCs, DACs, voltage references and analog multiplexers. A complete glossary defines data conversion specifications; a list of selected application and design notes is also included.
Available at no charge

Telecommunications Solutions Brochure — This collection of circuits, new products and selection guides covers a wide variety of products targeted for the telecommunications industry. Circuits solving real life problems are shown for central office switching, cellular phone, base station and other telecom applications. New products introduced include high speed amplifiers, A/D converters, power products, interface transceivers and filters. Reference material includes a telecommunications glossary, serial interface standards, protocol information and a complete list of key application notes and design notes. Available at no charge

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