LINEAR TECHNOLOGY

FEBRUARY 2000 VOLUME X NUMBER 1

IN THIS ISSUE...

1- and 2-Channel, No Latency ΔΣ, 24-Bit ADCs Easily Digitize a Variety of Sensors

by Michael K. Mayes and Derek Redmayne

Introduction

Since its introduction, the LTC2400's performance and ease-of-use have transformed the method of designing analog-to-digital converters into a variety of systems. Some key features that separate the LTC2400 from conventional high-resolution ADCs and enable direct digitization of many sensors include:

- ❑ Ultralow offset (1ppm), offset drift (0.01ppm/°C), full-scale error (4ppm) and full-scale drift error (0.02ppm/°C) without user calibration
- ❑ Absolute accuracy typically less than 10ppm total (linearity + offset + full-scale + noise) over the full operating temperature range
- ❑ Ease-of-use (eight pins, no configuration registers, internal oscillator and latency-free conversion)
- ❑ Low noise and wide dynamic range (0.3ppm$_{RMS}$ with V_{REF} = V_{CC} = 5V—21.6 effective bits of resolution)

This article introduces two new products based on the technology used in the LTC2400. Both parts come in tiny 10-pin MSOP packages. They include full-scale and zero-scale set inputs for removing systematic offset/full-scale error. The LTC2401 is a single-ended 1-channel device. The LTC2402 is a 2-channel device with automatic ping-pong channel selection.

The absolute accuracy and near zero drift of these devices enable many novel applications, of which four are presented here. The first application uses the full-scale and zero-scale set inputs of the 1-channel device (LTC2401) to digitize a half-bridge sensor. The second is a thermocouple digitizer with a digital cold-junction compensation scheme using the automatic ping-pong channel selection of the LTC2402 for simplified optocoupled isolation. The third combines the LTC2402's ping-pong channel selection, absolute accuracy and excellent rejection into a pseudo-differential bridge digitizer. The final application uses the LTC2402 to digitize an RTD temperature sensor and remove voltage drop errors due to long leads using the second channel and underrange capabilities.

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Issue Highlights

Happy Y2K and welcome to the tenth year of *Linear Technology* magazine. Did any of your analog circuits shut down at 12:01 on January first?

Our cover article for this issue introduces two new No Latency ΔΣ ADCs, the LTC2401 and the LTC2402, based on the technology of the LTC2400 (see *Linear Technology* VIII:4, November 1998). Both come in 10-pin MSOP packages and include full-scale and zero-scale set inputs for removing offset/full-scale error. The LTC2401 is a single-ended 1-channel device. The LTC2402 is a 2-channel device with automatic ping-pong channel selection. Both feature ultra-low offset, offset drift, full-scale error and full-scale drift; absolute accuracy typically less than 10ppm; low noise and wide dynamic range.

This issue also debuts another new ADC: the LTC1402 12-bit serial ADC has a full conversion speed of 2.2Msps and a very compact 3-wire interface for connecting to DSPs and microprocessors without glue logic. Its minuscule 16-pin narrow SSOP package and compact serial interface fit close to sensors for optimum analog signal integrity. The LTC1402 captures fast steps from an external analog input multiplexer for high speed data acquisition and digitizes high frequency signals very accurately, with a 72dB S/(N+D) at 1.1MHz, for communications or signal processing systems.

Also revealed in these pages are three new power devices: the LTC1701, the LTC1708-PG and the LTC1771. LTC1701 is a 5-lead SOT-23, step-down, current mode, DC/DC converter for low- to medium-power applications. It operates from a 2.5V to 5.5V input voltage and switches at 1MHz. The high switching frequency allows the use of tiny, low cost capacitors and inductors. Combined with the tiny SOT-23, the area consumed by the complete DC/DC converter can be less than $0.3in^2$.

The LTC1708-PG is LTC's newest PolyPhase™ DC/DC controller. It includes a dual, synchronous, current mode controller, VID voltage programming and a power-good function, for a compact CPU power supply solution. The turn-on timing of the top MOSFETs is interleaved for the two controllers, reducing the input RMS current and hence the input capacitance requirement. OPTI-LOOP™ compensation and Burst Mode™ operation reduce the output capacitance requirement.

The LTC1771 is a step-down controller that drives an external P-channel MOSFET for output loads up to 5A. Its low quiescent current and flexible operation with a wide range of output loads allow it to maintain high efficiency for over four decades of operating current. Wide supply range and 100% duty cycle for low dropout allow maximum energy to be extracted from the battery, while current mode operation gives excellent transient response and start-up behavior. The LTC1771 also features short-circuit protection, micropower shutdown to 2μA and a Burst Mode disable pin for low noise applications.

In the signal condition arena, we introduce a new family of amplifiers: the LT1395, LT1396 and LT1397 are 400MHz current feedback amplifiers with a high slew rate and a –3dB bandwidth that remains relatively constant over a wide range of open-loop gains. The current feedback topology of the these parts can provide improved performance in many designs that have historically used voltage feedback op amps. Because of their current feedback topology, they have a slew rate of 800V/μs on a supply current of only 4.6mA per amplifier, resulting in a much higher full-power bandwidth than comparable voltage feedback op amps.

This issue features three design ideas: a Hot Swap circuit that selects between 3.3V and 5V inputs and provides a regulated 3.3V/3A supply; a discussion of the "active voltage positioning" technique, which reduces the need for output capacitors when used in conjunction with selected LTC switching controllers; and part one of a 2-part series on ADSL driver/receiver design. Our Design Information section includes data on three new parts: the LTC1565-31 7th order, linear phase lowpass filter, the LTC1546 multiprotocol serial transceiver and the LTC2050 zero-drift operational amplifier. The issue concludes with eight new device cameos.

LTC in the News...

On January 18, Linear Technology announced its financial results for the second quarter of fiscal year 2000. Robert H. Swanson, Chairman and CEO, stated, "This was a very strong quarter for us as we achieved record levels of bookings, sales and profits, with sales increasing 10% and profits 11% sequentially from the September quarter. Demand from our customers escalated throughout the quarter and increased in all major geographical areas and all major end markets. Given this positive business climate, we expect the upcoming March quarter to have continuing sequential sales and profit growth." The Company reported sales of $162,294,000 and net income of $64,951,000 compared with $45,904,000 a year ago. Net sales were up 35% over last year.

Also, LTC announced a two-for-one stock split for shareholders of record on March 6, 2000. Certificates will be distributed on March 27, 2000. The split will increase the number of shares of common stock outstanding from approximately 160,000,000 to 320,000,000. According to Robert H. Swanson, Chairman and CEO, "the Board of Directors authorized the stock split with the intention of benefiting the shareholders by obtaining wider distribution and improving the marketability of the common stock."

The Company was featured by *Investor's Business Daily* in an article entitled "Linear Carves Out Unique Niche In Analog Semiconductor Field." Reporter Alan Elliott states, "Give some guys a niche and they'll take a mile." The article points out, "When Linear Technology took its first steps, analog was almost a nasty word. Digital chips were the wave of the future and analog seemed set to go the way of the buggy whip."

LTC2401/LTC2402, continued from page 1

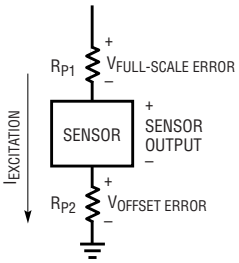

Figure 1. Errors due to excitation currents

Single-Ended Half-Bridge Digitizer with Reference and Ground Sensing

Sensors convert real world phenomena (temperature, pressure, gas levels and others) into voltages. Typically, the voltage is generated by passing an excitation current through the sensor. This excitation current also flows through wiring parasitics R_{P1} and R_{P2} (see Figure 1). The voltage drop across these parasitic resistances leads to systematic offset and full-scale errors.

In order to eliminate the errors associated with these parasitic resistances, the LTC2401/LTC2402 include a full-scale set input (FS_{SET}) and a zero-scale set input (ZS_{SET}). As shown in Figure 2, the FS_{SET} pin acts as a full-scale sense input. Errors due to parasitic resistance R_{P1} in series with the half-bridge sensor are removed by the FS_{SET} input to the ADC. The absolute full-scale output of the ADC (data out = $FFFFFF_{HEX}$) will occur at $V_{IN} = V_B = FS_{SET}$ (see Figure 3). Similarly, the offset errors due to R_{P2} are removed by the ground sense input, ZS_{SET}. The absolute zero output of the ADC (data out = 000000_{HEX}) occurs at $V_{IN} = V_A = ZS_{SET}$. Parasitic resistances R_{P3}–R_{P5} have negligible errors due to the 1nA (typ) leakage current at pins FS_{SET}, ZS_{SET} and V_{IN}. The wide dynamic input range (–300mV to 5.3V) and low noise ($0.6ppm_{RMS}$) enable the LTC2401 to directly digitize the output of a bridge sensor.

Digital Cold-Junction Compensation

In order to measure absolute temperature with a thermocouple, cold-junction compensation must be performed. The LTC2402 enables simple digital cold-junction compensation. One channel measures the output of the thermocouple while the other measures the output of the cold-junction sensor—diode, thermistor or the like (see Figure 4).

The selection between CH0 (the thermocouple) and CH1 (the cold junction) is automatic. The LTC2402 alternates conversions between the two input channels and outputs a bit corresponding to the selected channel in the data output word. This simplifies the user interface by eliminating a channel-select input pin. As a result, the LTC2402 is ideal for systems that perform isolated measurements; it only requires two optoisolators (one for serial data out and one for the serial data output clock).

Alternating conversions between two input channels is difficult with conventional ΔΣ ADCs. These devices require 3–5 conversion cycle settling every time the input channel is switched. On the other hand, the LTC24xx family uses a completely different architecture than other ΔΣ converters. This results in latency-free, single-cycle settling. The LTC2402 enables continuous conversion between two alternating channels without the added complexity associated with conventional ΔΣ converters.

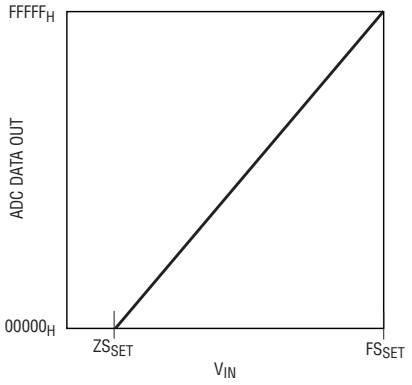

Figure 3. Transfer curve with zero-scale and full-scale set

Pseudodifferential Applications

Generally, system designers choose fully differential topologies for several reasons. First, the interface to a 4- or 6-wire bridge is simple (it has a differential output). Second, good rejection of line frequency noise is required. Third, the output of the sensor is typically a small differential signal sitting on a large common mode voltage; as a result, accurate measurements of the differential signal independent of the common mode input voltage is needed. Many applications currently using fully differential analog-to-digital converters for any of the above reasons can migrate to a pseudodifferential conversion using the LTC2402.

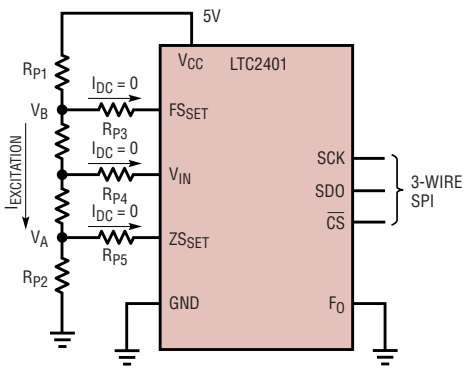

Figure 2. Half-bridge digitizer with zero-scale and full-scale sense

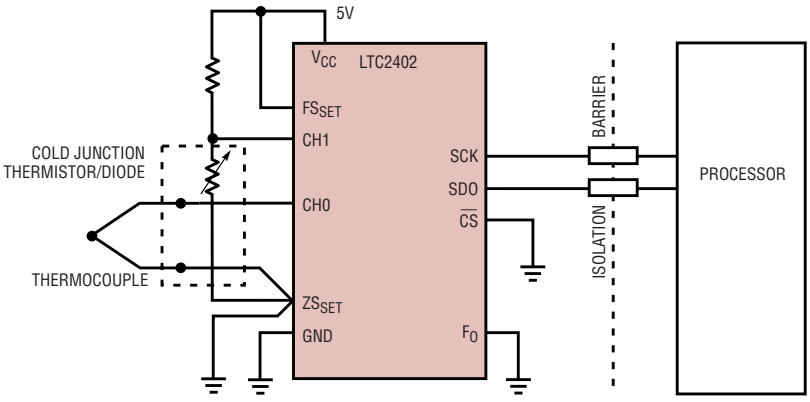

Figure 4. Digital cold-junction compensation

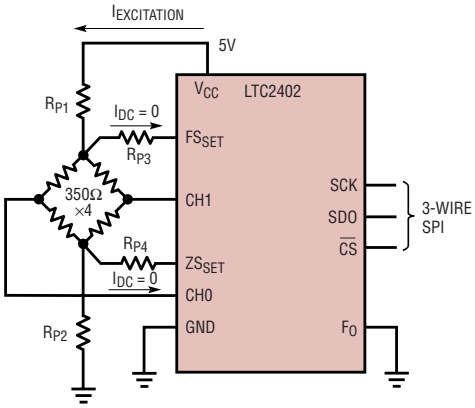

Figure 5. Pseudodifferential strain gauge application

Direct Connection to a Full Bridge

The LTC2402 interfaces directly to a 4- or 6-wire bridge (see Figure 5). Like the LTC2401, the LTC2402 includes FS_{SET} and ZS_{SET} pins for sensing the excitation voltage directly across the bridge. This eliminates errors due to excitation currents flowing through parasitic resistances (R_{P1}–R_{P4}). The LTC2402 also includes two single-ended input channels that can be tied directly to the differential output of the bridge. The two conversion results can be digitally subtracted, yielding the differential result.

Noise Rejection

The LTC2402's single-ended rejection of line frequencies (50Hz/60Hz ±2%) and their harmonics is better than 110dB. Since the device performs two independent single-ended conversions, each with >110dB rejection, the overall common mode and differential rejection is much better than the 80dB rejection typically found in other differential ΔΣ converters.

In addition to excellent rejection of line frequency interference, the LTC2402 also exhibits excellent single-ended noise rejection of a wide range of frequencies due to its 4th order sinc filter (see Figure 6). Each single-ended conversion independently rejects high frequency noise (>60Hz). Care must be taken to ensure that noise at frequencies below 15Hz and at multiples of the ADC sample rate (15.6kHz) are not present. For this application, it is recommended that the LTC2402 be placed in close proximity to the bridge sensor in order to reduce the noise applied to the ADC input. By performing three successive conversions (CH0–CH1–CH0) the drift and low frequency noise can be measured and compensated digitally.

Small Differential Signals Sitting on Large Common Mode Voltages

The absolute accuracy (<10ppm total error) of the LTC2402 enables extremely accurate measurement of small signals sitting on large voltages. Each of the two pseudodifferential measurements performed by the LTC2402 is absolutely accurate independent of the common mode voltage output from the bridge. The pseudodifferential result obtained from digitally subtracting the two single-ended conversion results is accurate to within the noise level of the device times the square root of 2 ($3\mu V_{RMS} \bullet \sqrt{2}$), independent of the common mode input voltage.

Typically, bridge sensors output 2mV/V full scale. With a 5V excitation this translates to a full-scale output of 10mV. Divided by the RMS noise of the LTC2402, this circuit yields 2357 counts with no averaging or amplification. If more counts are required, several conversions may be averaged. The number of effective counts is increased by $\sqrt{2}$ for each doubling of averages. For example, to achieve 10,000 counts sixteen readings should be averaged.

In order to achieve more counts, an LT1126 low noise dual op amp can be placed in front of the LTC2402, see Figure 7. The noise performance of this device is $2.6nV/\sqrt{Hz}$. With a gain of 100, the input-referred noise contribution of the LTC2402 is less than $50nV_{RMS}$.

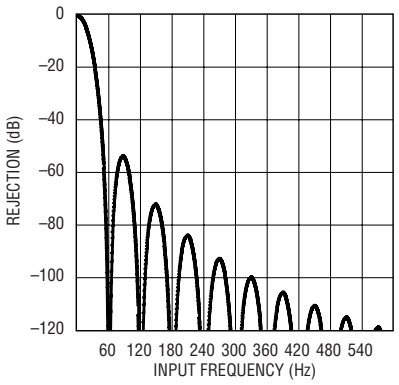

Figure 6. Single-ended LTC2401/LTC2402 input rejection

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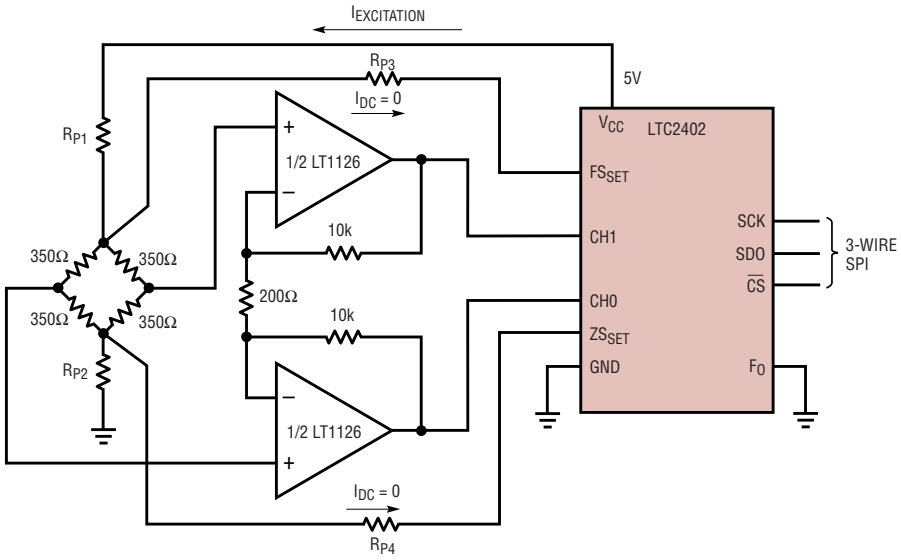


Figure 7. 100,000 count pseudodifferential strain gauge application

Tiny SOT-23 Step-Down Regulator Switches at 1MHz for Space-Critical Applications

by Damon Lee

Introduction

As portable devices continue to shrink, the need for progressively smaller components increases. To use smaller capacitors and inductors, switching regulators need to run at ever higher frequencies in ever smaller packages. To help meet this growing demand, Linear Technology introduces the LTC1701 5-lead SOT-23, step-down, current mode, DC/DC converter. Intended for low- to medium-power applications, it operates from a 2.5V to 5.5V input voltage and switches at 1MHz. The high switching frequency allows the use of tiny, low cost capacitors and inductors, which can be 2mm in height or less. Combined with the tiny SOT-23, the area consumed by the complete DC/DC converter can be less than 0.3in^2, as shown in Figure 1.

The output voltage is adjustable from 1.25V to 5V. The LTC1701 can also be used as a zeta converter for battery-powered applications. A built-in 0.28Ω switch allows up to 500mA of output current at high efficiency. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

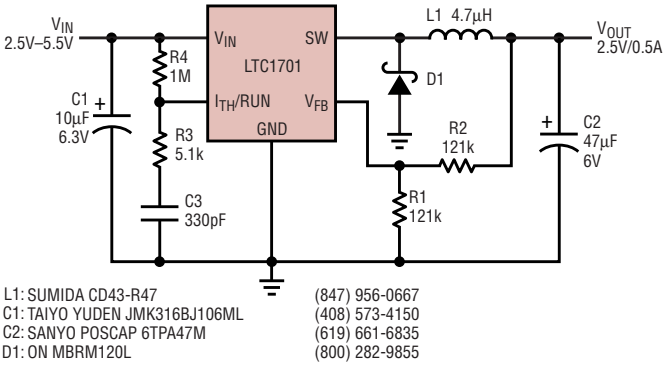


Figure 2. High efficiency 2.5V/500mA step-down regulator

The LTC1701 incorporates a current mode, constant-off-time architecture and includes automatic, power saving Burst Mode operation to reduce gate charge losses at low load currents. With no load, the converter draws only 135µA; in shutdown, it draws less than 1µA, making it ideal for battery-powered applications. In dropout, the internal P-channel MOSFET switch is turned on continuously, maximizing the usable battery life.

High Efficiency 2.5V Step-Down DC/DC Converter

A typical application for the LTC1701 is a 2.5V step-down converter, as shown in Figure 2. This circuit converts a 2.5V to 5.5V input supply to a regulated 2.5V output supply at up to 500mA. The efficiency peaks at 94% with a 3.3V input supply, as shown in Figure 3. The graphs show an improvement in efficiency above 100mA, where Burst Mode operation is disabled. Burst Mode operation provides better efficiency at lower currents by producing a single pulse or a group of pulses that are repeated

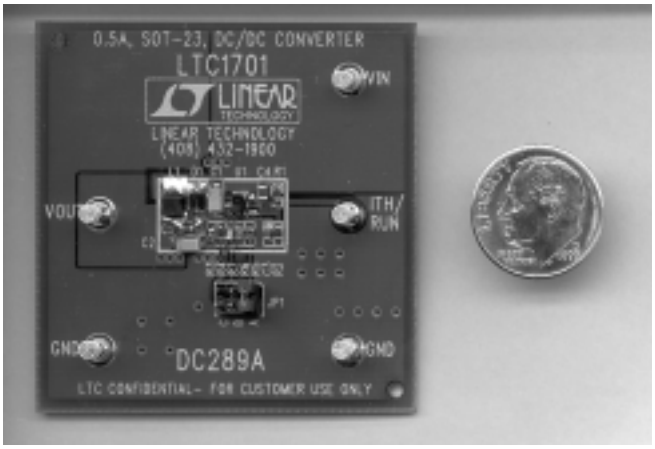


Figure 1. LTC1701 evaluation circuit

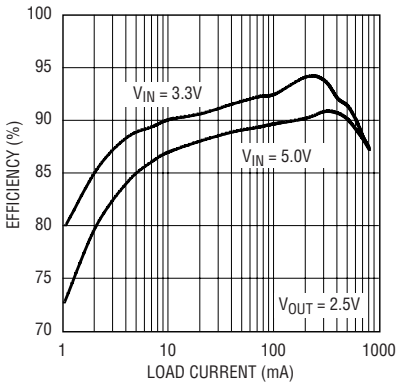


Figure 3. Efficiency of Figure 2's circuit

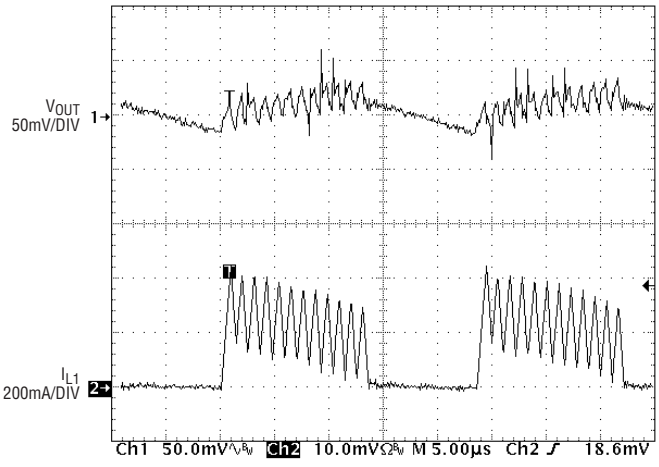


Figure 4. Example of Burst Mode operation

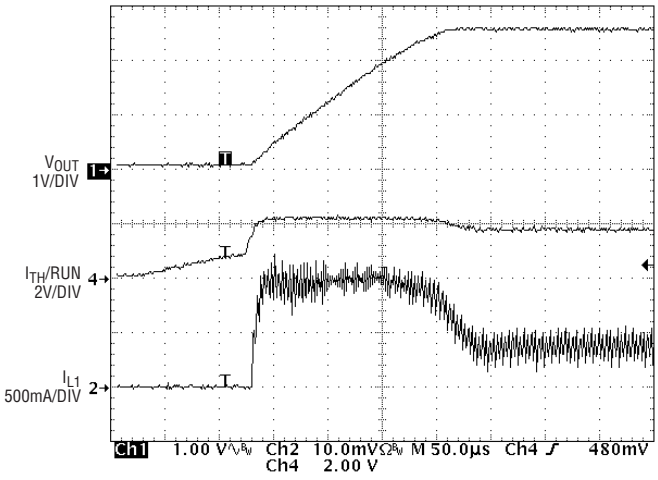


Figure 5. Start-up with 3.3V input into a 6Ω load

periodically, as shown in Figure 4. By switching intermittently, the switching losses, which are dominated by the gate-charge losses of the power MOSFET, are minimized.

Start-up waveforms from a 3.3V input into a 6Ω load are pictured in Figure 5. The converter reaches regulation in approximately 200µs, depending on the load. Soft-start can be implemented by ramping the voltage on the I_{TH}/RUN pin, which requires only an RC delay with a small Schottky diode, as shown in Figure 6.

Single-Cell Li-Ion to 3.3V Zeta Converter

Some designs need the ability to maintain a regulated output voltage while the input voltage may be either above or below the desired output. When the input is above the output, the circuit must behave like a buck regulator; when the input is below the output, it must behave like a boost regulator. The circuit configuration known as a zeta converter is a very simple design that can meet this requirement.

A single lithium-ion battery is a popular choice for many portable applications due to its light weight and high energy density, but it has a cell voltage that ranges from 4.2V to 2.5V. Thus, a simple buck or boost topology cannot be used to provide a 3.3V output voltage.

In Figure 7, the LTC1701 is used in a zeta configuration to supply a constant 3.3V with over 200mA of load current. The circuit uses a single, dual-winding inductor (a 1:1 transformer) for better performance, although two separate inductors can also be used with somewhat lower efficiency. The components shown in the schematic result in a 3mm high converter, suitable for portable applications.

As can be seen in Figure 8, the overall efficiency does not vary much with supply voltage variations, except at high currents (over 100mA). This

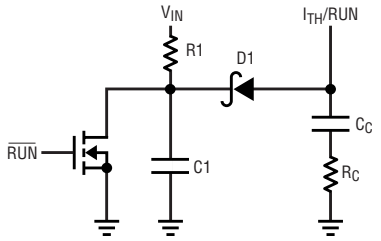


Figure 6. Soft-start hookup

can be attributed to the dominance of switching losses across most of the current range. Since Li-Ion batteries spend most of their lives with a cell voltage in the 3.6V–4.0V range, the typical efficiency is about 81%.

2mm High, 1.5V Converter

In many applications, the height constraint can be more of a concern than the area constraint. Small, low profile inductors and capacitors can be used with the LTC1701, due to the high switching frequency of 1MHz. In Figure 9, a circuit is shown that uses low profile components to produce a 2mm

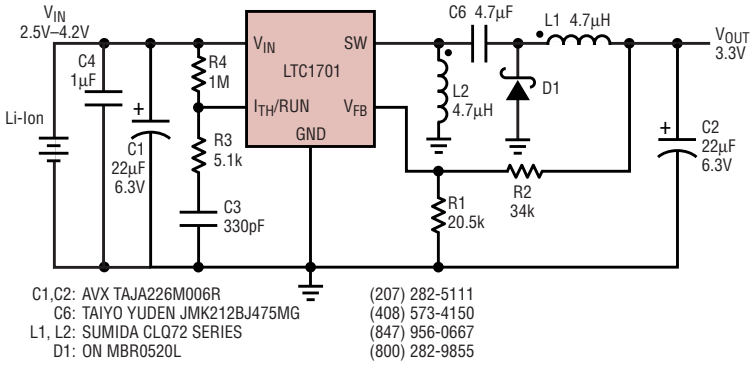


Figure 7. Single-cell Li-Ion to 3.3V zeta converter

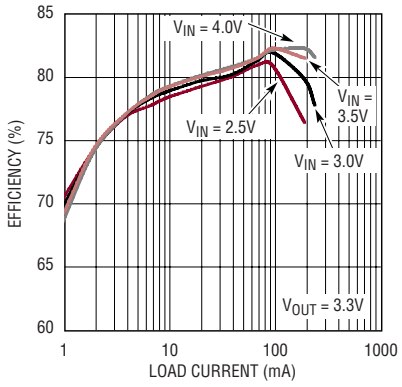
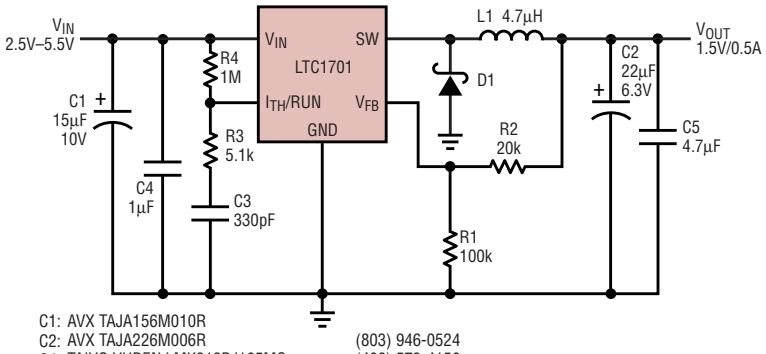


Figure 8. Efficiency of Figure 7's circuit



C1: AVX TAJA156M010R
C2: AVX TAJA226M006R (803) 946-0524
C4: TAIYO YUDEN LMK212BJ105MG (408) 573-4150
C5: TAIYO YUDEN JMK212BJ475MG
L1: MURATA LQH3C4R7M24 (814) 237-1431
D1: ON MBRM120L (800) 282-9855

Figure 9. 2mm high 1.5V converter

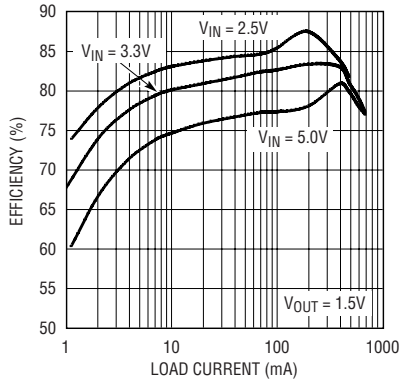


Figure 10. Efficiency of Figure 9's circuit

high (nominal), 1.5V step-down converter that occupies less than 0.3in^2. The photograph in Figure 1 shows an example of a layout with these components. The efficiency, shown in Figure 10, peaks at 88%. As can be seen, the overall efficiency tends to degrade with a larger V_{IN}-to-V_{OUT} ratio, which is typical for step-down regulators.

2.5V Converter with All Ceramic Capacitors

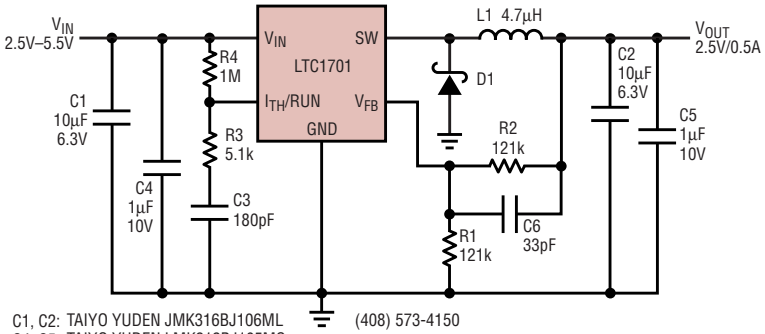
The low cost and low ESR of ceramic capacitors make them a very attractive choice for use in switching regulators. Unfortunately, the ESR is so low that loop stability problems may result. Solid tantalum capacitor ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in providing acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR damping becomes effective. Also, ceramic caps are prone to temperature effects, which require the designer to check loop stability over the full operating temperature range.

For these reasons, great care must be taken when using only ceramic input and output capacitors. The OPTI-LOOP compensation components can be adjusted when ceramic capacitors are used. For a detailed explanation of optimizing the compensation components, refer to LTC Application Note 76. Figure 11 shows one example of an all-ceramic-capacitor circuit; its efficiency graph is shown in Figure 12. The efficiency in this case has a very flat peak at 93% due to the relatively low output capacitance and the low ESR of the ceramic capacitors.

Conclusion

The LTC1701 is a small, monolithic, step-down regulator that switches at high frequencies, allowing the use of tiny, low cost capacitors and inductors for a cost- and space-saving DC/DC converter. Although the LTC1701 was designed for basic buck applications, the architecture is versatile enough to produce an effective zeta converter, due in part to its power saving Burst Mode operation and its optimized OPTI-LOOP compensation.

By combining a high switching frequency and an onboard P-channel MOSFET in a tiny SOT-23 package, the LTC1701 is ideal for space-critical portable applications.



C1, C2: TAIYO YUDEN JMK316BJ106ML (408) 573-4150
C4, C5: TAIYO YUDEN LMK212BJ105MG
L1: MURATA LQH3C4R7M24 (814) 237-1431
D1: ON MBRM120L (800) 282-9855

Figure 11. All-ceramic-capacitor converter delivers 2.5V at 500mA.

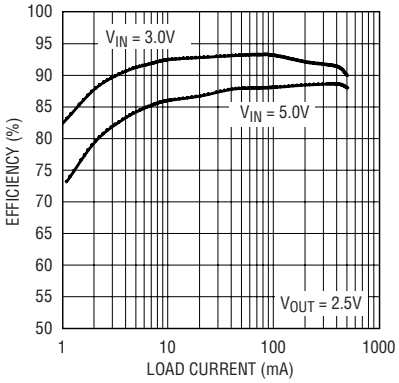


Figure 12. Efficiency of Figure 11's circuit

10µA Quiescent Current Step-Down Regulator Extends Standby Time in Handheld Electronics

by Greg Dittmer

Introduction

Many handheld products on the market today are used only occasionally but must be kept alive and ready all the time. When not being used, the circuitry is powered down to save battery energy, with a minimum amount of circuitry remaining on. Although the supply current is significantly reduced in this low power standby mode, the battery energy will still be slowly depleted to power the keep-alive circuitry and the regulator. If the device spends most of its time in this standby mode, the quiescent current of the regulator can have a significant effect on the life of the battery (see Figure 1). To maximize the life of the battery in these types of products, Linear Technology has extended its family of low quiescent current step-down converters. The LTC1474/LTC1475 series broke new ground a few years ago by providing a monolithic step-down regulator that requires only 10µA of supply current to regulate its output voltage at no load while maintaining high efficiency at loads up to 300mA. Now, two new products provide solutions for applications requiring higher output currents or constant-frequency operation at a higher switching frequency while still operating on the ultralow 10µA no-load supply current. The new LTC1771 is a constant off-time controller for up to 5A of output current with the addition of an appropriately sized external P-channel FET. A second product, soon to be released, is a monolithic regulator that provides constant frequency (550kHz) plus synchronous operation at up to 500mA of output current.

LTC1771 Controller for Output Loads to 5A

The LTC1771 is a step-down controller that drives an external P-channel MOSFET for output loads up to 5A. Its low quiescent current and flexible operation with a wide range of output loads allow the LTC1771 to maintain high efficiency for over four decades of operating current. Wide supply range (2.8V–18V) and 100% duty cycle for low dropout allow maximum energy to be extracted from the battery, while current mode operation gives excellent transient response and start-up behavior. LTC1771 also features short-circuit protection (the maximum current is programmable with an external sense resistor), micropower shutdown to 2µA and a Burst Mode disable pin for low noise applications.

The LTC1771 uses a constant off-time, current mode architecture to regulate its output voltage. During normal operation, the P-channel MOSFET is turned on at the beginning of each cycle, causing current to ramp up in the inductor and sense resistor. When the sensed current reaches the current comparator threshold, the current comparator trips and triggers a 1-shot timer that turns off the MOSFET for 3.5µs. At the end of this period, the MOSFET is turned back on and the cycle is repeated. The peak inductor current at which the current comparator trips is controlled by the voltage on pin 2 (I_{TH}), the output of the error amplifier. An external resistor divider allows the error amplifier to receive an output feedback voltage. When the load current increases, it causes a slight decrease in the feedback voltage, which, in turn, causes the average inductor current to increase until it matches the new load current.

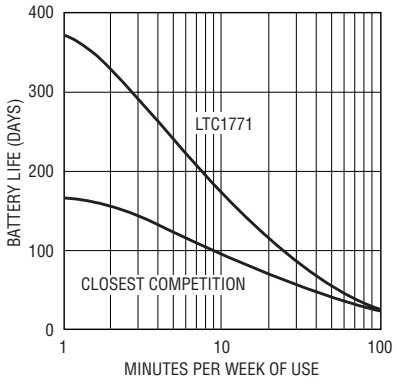


Figure 1. 9V battery-life comparison for load requiring 100mA normal and 100µA standby current at 3.3V

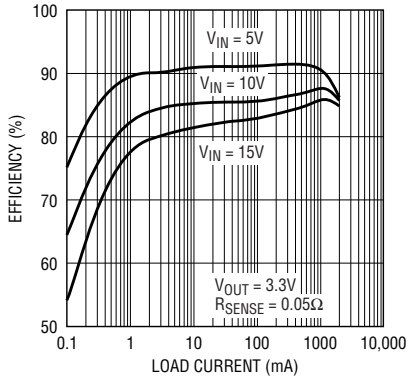


Figure 2. LTC1771 efficiency vs load current for Figure 5's circuit

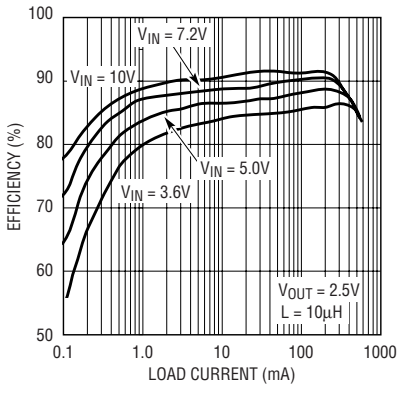


Figure 3. Efficiency vs load current for a new constant frequency monolithic regulator

Burst Mode for Outstanding Low Current Efficiency

The LTC1771 is able to maintain an ultralow no-load supply current and high efficiency at extremely light loads by using Burst Mode operation. Burst Mode operation commences when the load, detected by a comparator monitoring the I_{TH} voltage, falls below about 20%–30% of the maximum load. During Burst Mode operation, short burst cycles of normal switching to charge the output capacitor alternate with longer sleep periods when the switch is turned off and the load current is supplied by the output capacitor. During this sleep period, only the minimum required circuitry—the reference voltage and the error amplifier—are left on. Supply current is further reduced with innovative new circuitry that allows the error amplifier to run on 10% of its normal operating current during sleep mode with no degradation in the transient response, reducing the total supply current to less than 10µA. At light loads, the regulator spends most of the time in this low quiescent current sleep mode, minimizing supply current and maximizing efficiency.

Burst Mode operation can be disabled by pulling the Mode pin to ground. Disabling Burst Mode operation allows the loads to decrease another decade, to about 1%–2% of maximum load, before the regulator must skip cycles to maintain regulation. Although less efficient, disabling Burst Mode operation is useful because it reduces both audio and RF interference by reducing voltage and current ripple and by keeping operating frequency constant at lower output currents.

Component Considerations for Minimizing Supply Current

No-load supply current for the LTC1771 consists of the 10µA quiescent current of the IC plus a small additional current to power the low frequency burst cycles needed to recharge the output capacitor. Even at no load, the output capacitor is slowly discharged due to leakage currents from the feedback resistors and the Schottky diode. This leakage current, though small, can be significant when the total supply current is only 10µA. The feedback resistor leakage can be minimized by using resistors in the megohm range. Care must be used in selecting the Schottky diode to minimize no-load supply current without sacrificing efficiency at higher loads. Low leakage is critical for minimizing no-load supply current; however, forward voltage drop is critical for higher current efficiency because loss is proportional to the forward voltage drop. Unfortunately, these are conflicting parameters (see Figure 4) and the user will need to weight the importance of each spec in choosing the best diode for the application.

3.3V/2A Step-Down Regulator

A typical application circuit using the LTC1771 is shown in Figure 5, with the associated efficiency curves in Figure 2. This circuit supplies a 2A load at 3.3V with an input supply range of 4.5V to 18V. The 0.05Ω sense resistor sets the maximum output current to just above 2A. The 15µH inductor sets the inductor ripple current at about 1A, and with the 0.05Ω ESR of the output capacitor, results in 50mV of output voltage ripple. Since the LTC1771 gate drive pin swings rail-to-rail, a MOSFET must be chosen that can handle the full supply voltage. The Si6447 P-Channel MOSFET is a good compromise between low gate charge and $R_{DS(ON)}$. Gate charge affects efficiency at lighter loads, whereas $R_{DS(ON)}$ affects the efficiency at heavier loads. The 4.5V minimum supply voltage is due to minimum gate voltage required for the Si6447. If the input supply is limited to 12V or less, a 2.5V MOSFET, such as the Si3443, could be used allowing the regulator to operate to lower supply voltages. The Microsemi Powermite UPS5817 Schottky diode (617-926-0404) provides a good compromise between reverse leakage and forward drop for the 1A–2A range. The diode leakage and the feedback resistors increase the no-load supply current to about 12µA.

Conclusion

With Linear Technology's growing family of high performance 10µA parts, the designers of handheld electronics now have a myriad of solutions to optimize their designs without compromising the main goals of extending

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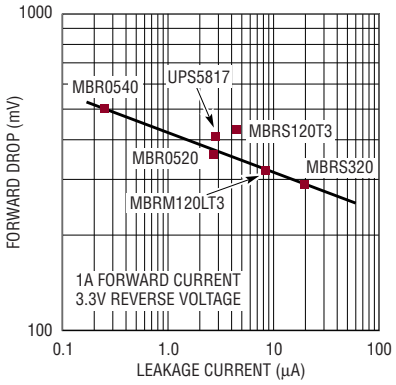


Figure 4. Schottky diode parameter trade-off

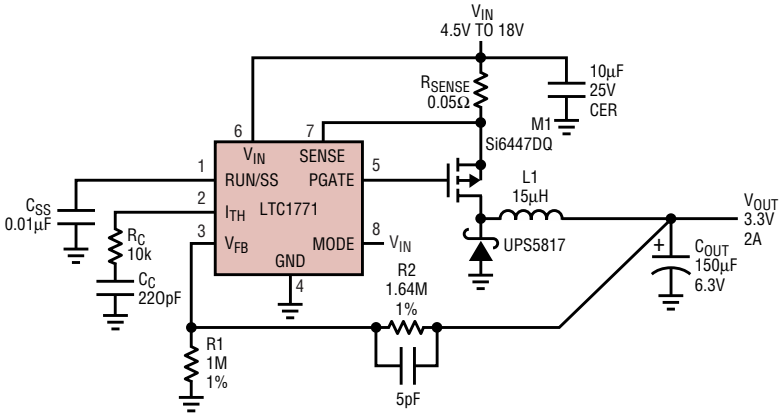


Figure 5. LTC1771 3.2V/2A regulator

Beware: Worst-Case Specifications Can Be a Reality

by Steve Hobrecht

Introduction

The design of portable electronic devices always involves trade-offs among cost, weight, size, speed, runtime, features and reliability. It is necessary to design the power supply for worst-case conditions because the software, which may or may not have been written yet, may, in some situations, exercise the hardware to its fullest potential. If typical operating conditions are used to define the power supply design requirements, hardware reliability may depend upon the particular software being used, either in normal operation or when the software is "acting up."

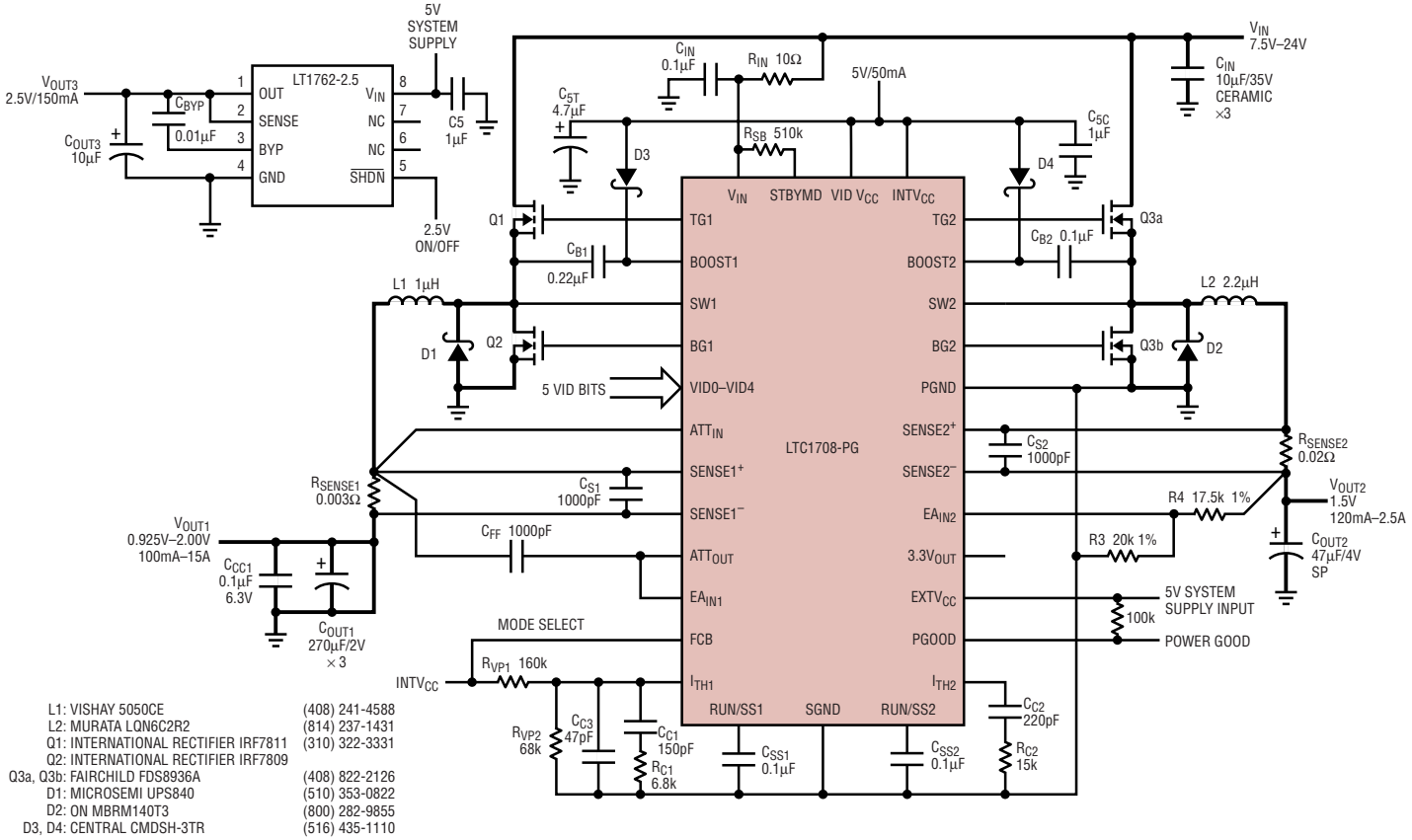
In the case of a typical notebook computer, the nominal 120mA I/O current can rise to 2.5A for an indeterminate amount of time. The software being executed is the determining factor. If a linear regulator is used that is only capable of a lower continuous current due to power dissipation or maximum current limit, a system crash or a hardware failure may result when higher current is required. Hidden costs for warranty repair may result from running seemingly innocuous code, posing a long-term risk for the manufacturer. A high efficiency, dual, current mode controller can be substituted for the single controller plus linear regulator normally used in this application, to provide a small, reliable, efficient solution. This will prevent the inevitable thermal problems associated with the use of a linear regulator.

The application presented here provides a VID-controlled, 0.9V–2.0V, 15A CPU supply, 1.5V/2.5A I/O supply and 2.5V ±5%/150mA clock supply. The power supply components chosen meet the maximum current specifications over the operating temperature and input voltage range.

The LTC1708-PG is the newest member of Linear Technology's third generation of PolyPhase DC/DC controllers. This controller is similar to the LTC1628 controller (see "A Third Generation Dual, Opposing-Phase Switching Regulator Controller," *Linear Technology* IX:2 [June, 1999], pp. 16–20) but with the addition of 5-bit VID output voltage control and a power-good indicator.

Application Benefits

The LTC1708-PG includes a dual, synchronous, current mode controller, VID output voltage programming and a power-good function in a 28-pin SSOP package, providing a compact



L1: VISHAY 5050CE (408) 241-4588
L2: MURATA LQN6C2R2 (814) 237-1431
Q1: INTERNATIONAL RECTIFIER IRF7811 (310) 322-3331
Q2: INTERNATIONAL RECTIFIER IRF7809
Q3a, Q3b: FAIRCHILD FDS8936A (408) 822-2126
D1: MICROSEMI UPS840 (510) 353-0822
D2: ON MBRM140T3 (800) 282-9855
D3, D4: CENTRAL CMDSH-3TR (516) 435-1110

Figure 1. LTC1708 microprocessor core, I/O and clock supply: 0.9V–2V/15A, 1.5V/120mA–2.5A and 2.5V/150mA with active voltage positioning

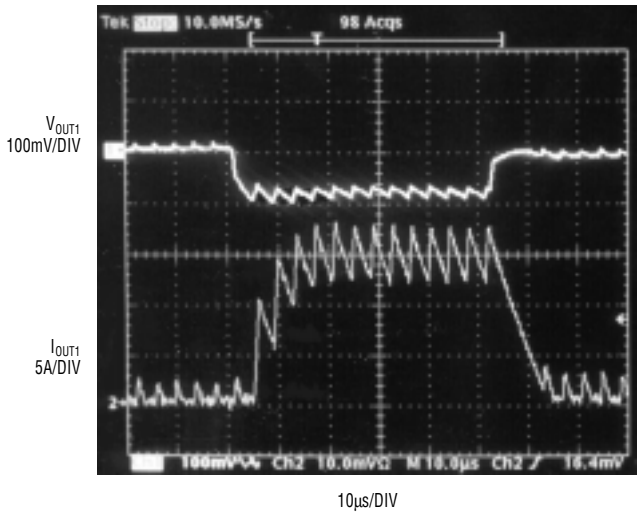


Figure 2. Output voltage response to a 100mA–15A load step

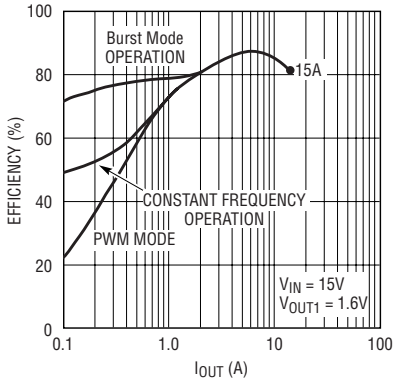


Figure 3. Efficiency vs output current of Figure 1's circuit for three operating modes

CPU power supply solution. Internal timing control interleaves the turn-on timing of the top MOSFETs for the two controllers, reducing the input RMS current and hence the input capacitance requirement. OPTI-LOOP compensation and low current Burst Mode operation reduce the output capacitance requirement.

The 1%, 0.8V reference voltage provides output voltage accuracy along with compatibility for future, lower voltage microprocessor and ASIC requirements. Load regulation is typically 0.1% and is compatible with active voltage positioning techniques (see "Active Voltage Positioning Saves Output Capacitors in Portable Computer Applications" on page 23 in this issue). The device incorporates an overvoltage "soft-latch" that protects the load if power supply problems develop but does not interfere or latch off when extreme transient conditions end. Internal foldback current limiting eliminates the need to overdesign the power components to protect against short circuits; an overcurrent shutdown can be enabled if desired. These protection features combine to make a very robust solution for long term reliability. The operating modes provide a choice of Burst Mode operation, constant-frequency operation and PWM modes (in order of decreasing efficiency) to satisfy almost any application. The constant frequency mode offers a low noise solution that has high efficiency due to discontinuous operation, offering a solution for applications requiring bursts of high current at an audible rate. This technique reduces or eliminates the audible noise emanating from the gapped inductor that is typically used. The fast response time of the internal controller circuits allows the controller to maintain its operating frequency even with very high input-to-output voltage ratios. A 5V and a 3.3V linear regulator are provided to power ancillary functions.

2-Phase Operation

The LTC1708 dual, high efficiency DC/DC controller brings the considerable benefits of 2-phase operation to portable applications. Notebook computers, PDAs, handheld terminals and automotive electronics will all benefit from the lower input filtering requirement, reduced electromagnetic interference (EMI) and increased efficiency associated with 2-phase operation.

Application Circuit

Figure 1 shows a VID-controlled 0.9V to 2.0V, 15A CPU supply, a 1.5V/2.5A I/O supply and 2.5V ±5%/150mA clock supply. The controller's V_{IN} and $EXTV_{CC}$ pins should be connected to a supply of at least 4.5V, as specified by the MOSFET manufacturer, but the topside switching MOSFET drains can be connected independently to a 3.3V, 5V or 10V–15V battery supply, or even a 24V wall adapter if desired. The schematic illustrates components selected for a 7.5V to 24V input.

Transient Performance

The oscilloscope photo (Figure 2) shows the switching power supply's high current output voltage response to a load current step of 100mA to 15A in the constant frequency mode. Figure 3 illustrates the overall efficiency for the three different operating modes: Burst Mode operation, constant-frequency operation and forced continuous (PWM) mode for 100mA to 15A.

Conclusion

A practical solution has been presented that exceeds the mobile CPU core, I/O and CLK specifications. The circuit performs reliably under the most adverse stimulus. The high overall efficiency minimizes cooling requirements as well.

The LTC1708 is just one member of Linear Technology's third generation family of constant frequency, N-channel high efficiency controllers. With PolyPhase timing control, VID programming, overvoltage and overcurrent protection features, OPTI-LOOP compensation and strong MOSFET drivers, the LTC1708 is a very safe choice for CPU core and I/O power applications.

400MHz Current Feedback Amps Offer High Slew Rate without the Gain Bandwidth Product Limitations of Voltage Feedback Amps

by Brian Hamilton

Introduction

The LT1395, LT1396 and LT1397 are 400MHz current feedback amplifiers with a high slew rate and a –3dB bandwidth that remains relatively constant over a wide range of closed-loop gains. The current feedback topology of the LT1395/LT1396/LT1397 family can provide improved performance in many new and existing designs that have historically used voltage feedback op amps. Because of its current feedback topology, the LT1395/LT1396/LT1397 family boasts a slew rate of 800V/µs on a supply current of only 4.6mA per amplifier, resulting in a much higher full-power bandwidth than comparable voltage feedback op amps. The current feedback topology of the LT1395/LT1396/LT1397 also results in additional design flexibility because the –3dB bandwidth remains relatively constant regardless of closed-loop gain. In contrast, the –3dB bandwidth of voltage feedback op amps decreases in proportion to the closed-loop gain that has been chosen. For example, a voltage feedback op amp with a 400MHz gain bandwidth product (GBW) will only have a 100MHz bandwidth at a closed-loop gain of four. At the same gain, the LT1395/LT1396/LT1397 have a gain bandwidth of about 240MHz. The parts have industry-standard single, dual and quad pinouts, allowing easy upgrades of existing applications.

The LT1395/LT1396/LT1397 Family

In addition to a 400MHz –3dB bandwidth and an 800V/µs slew rate, the LT1395/LT1396/LT1397 family has exceptionally flat frequency response. Applications that require gain accuracy across a broad frequency range will benefit from the family's ±0.1dB bandwidth, which exceeds 100MHz. For increased design flexibility, the LT1395/LT1396/LT1397 also boast a very flexible output stage. They have over 80mA of output current drive and, on ±5V supplies, they can swing up to ±3.6V with a 150Ω load.

The LT1395/LT1396/LT1397 family's wide supply voltage range and versatile packaging options also increase design flexibility. Supplies can range from a single 4V to ±6V. All devices and package types are compatible with standard op amp pinouts. In addition to standard SO packages, the LT1396 and LT1397 are also available in smaller form factors. The LT1396 is available in an 8-lead MSOP package. The LT1397 is available in a 16-lead SSOP package that takes the same amount of board space as an SO-8. The LT1395 will be available in SOT-23 soon.

A simplified schematic of a single amplifier from the LT1395/LT1396/LT1397 family can be seen in Figure 1. Transistors Q1–Q7, J1 and R1 generate the necessary internal bias currents, with Q6 and Q7 acting as current sources for the input stage. Transistors Q8–Q11 form the amplifier's input stage. Currents coming from Q10 and Q11 are mirrored on top and bottom by transistors Q12–Q17. The collectors of transistors Q13 and Q15 drive the high impedance node of the amplifier. Transistors Q16 and Q17 act as current sources for the output stage. Transistors Q18–Q21 and resistors R2 and R3 form the output stage.

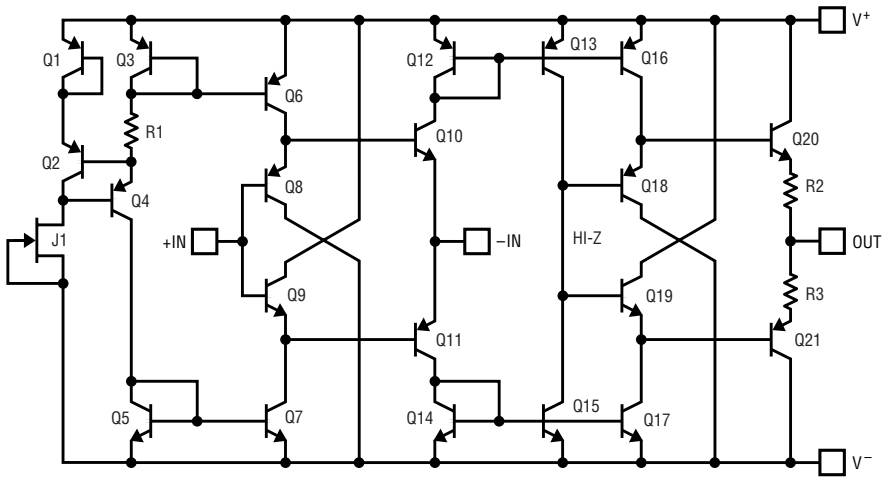


Figure 1. LT1395/LT1396/LT1397 simplified schematic (one amplifier)

It's the Input Stage

The advantages of a current feedback amplifier (CFA) can be better understood by examining the internal circuit topology in greater detail. The LT1395/LT1396/LT1397 input stage reveals that the noninverting input drives the bases of Q8 and Q9, resulting in a high impedance input. On the other hand, the inverting input drives the emitters of Q10 and Q11 and results in a low impedance input; any differential voltage imposed across

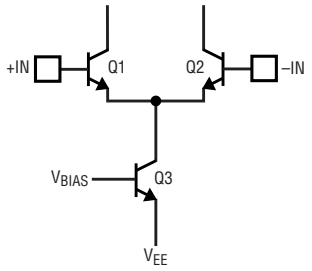


Figure 2. Voltage feedback input stage

the inputs creates a current that flows into or out of the inverting input. This current modulates the collector currents of Q10 and Q11, is mirrored on top and on the bottom, and produces a voltage swing at the high-impedance node (and output) of the amplifier. Since the output voltage swing is based upon the current flowing through the inverting input, the gain of a current feedback amplifier is expressed as the ratio of output voltage change (dV) divided by inverting input current change (dI_{B-}) and is referred to as the amplifier's transimpedance (Z_0).

A conventional voltage feedback input stage (Figure 2) is dramatically different than the current feedback input stage described above. The inverting input of the voltage feedback input stage is a high impedance input; thus, any feedback to this node is in the form of a voltage. Since the currents flowing into or out of the inverting input are small, the maximum slew current at the high-impedance node is derived from internal currents only and has an upper limit equal to the collector current of Q3. In contrast, the slew current in a CFA is not limited to internal currents; it is provided externally via the inverting input and

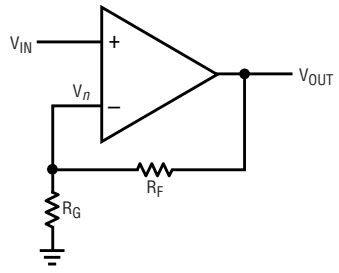


Figure 3. Noninverting gain topology

results in much higher slew rates than those of conventional voltage feedback op amps.

A CFA's constant bandwidth over closed-loop gain can be easily explained if we derive equations for closed-loop gain and closed-loop bandwidth; we can then compare them with the equations for a voltage feedback op amp. Let's start by comparing open-loop transfer functions and open-loop gain:

A conventional voltage feedback op amp has an open-loop gain A_{JF} that defines the transfer function of the amplifier as follows:

$$V_{OUT} = A_{JF} \bullet d(V_{IN}) \quad (1)$$

where $d(V_{IN})$ is the difference voltage between the noninverting input and the inverting input. Over frequency, A_{JF} has a value at DC (A_0) and a dominant pole frequency (f_a). The open-loop response can be expressed as:

$$A_{JF} = A_0/(1 + j(f/f_a)) \quad (2)$$

A current feedback amplifier has an open-loop transimpedance Z_{JF} that defines the transfer function of the amplifier as follows:

$$V_{OUT} = Z_{JF} \bullet I_{B-} \quad (3)$$

where I_{B-} is the current flowing out of the inverting input. Over frequency, Z_{JF} has a value at DC (Z_0) and a dominant pole frequency (f_a). The open-loop response can be expressed as:

$$Z_{JF} = Z_0 / (1 + j(f/f_a)) \quad (4)$$

If we take an amplifier (either CFA or voltage feedback) that has been connected in a noninverting gain topology (Figure 3), we can now determine the closed-loop transfer function as follows:

For a voltage feedback amplifier, we can see from inspection of Figure 3 that

$$d(V_{IN}) = V_{IN} - V_{OUT} \bullet (R_G/(R_F + R_G)) \quad (5)$$

Combining equations 5, 1 and 2 (and assuming $(1+ R_F/R_G)/A_0 << 1$), we get the closed-loop transfer function:

$$V_{OUT}/V_{IN} = (1 + R_F/R_G)/(1 + j(f/f_A)) \quad (6)$$

where

$$f_A = (A_0 \bullet f_a)/(1 + R_F/R_G) \quad (7)$$

is the closed-loop bandwidth.

For a current feedback amplifier, we know that the topology of the input stage ensures that $V_n = V_{IN}$. With this in mind, we can see from inspection of Figure 3 that

$$I_{B-} = (V_{IN}/R_G) + ((V_{IN} - V_{OUT})/ R_F) \quad (8)$$

Combining equations 8, 3 and 4 (and assuming $R_F/Z_0 << 1$) we get the closed-loop transfer function:

$$V_{OUT}/V_{IN} = (1 + R_F/R_G)/(1 + j(f/f_A)) \quad (9)$$

where

$$f_A = (Z_0 \bullet f_a)/R_F \quad (10)$$

is the closed-loop bandwidth.

Looking at equations 6 and 9, we can see that the closed-loop gain equations are identical for a voltage feedback amplifier and a CFA. However, the closed-loop bandwidths (equations 7 and 10) are quite different. As expected, the voltage feedback amplifier (equation 7) has a closed-loop bandwidth that decreases with increased closed-loop gain such that their product is a constant.

The CFA has a closed-loop bandwidth (equation 10) with some interesting consequences. To be properly compensated, the CFA *requires* a specific value of feedback resistor (R_F) between the inverting input and the output. The value of R_F can be increased to improve stability (or lower closed-loop bandwidth) in a variety of applications, such as driving capacitive loads. The requirement of a resistor in the feedback path can preclude CFAs from being drop-in replacements for voltage feedback op amps in some classes of circuits. Active filters and integrators are good examples of this class of circuit; their implementation usually has capacitors in the feedback network. Circuits where the value of the feedback resistance may change can also be problematic for a CFA. There are often alternative circuit topologies that allow CFAs to be used in these applications. Many of these topologies are

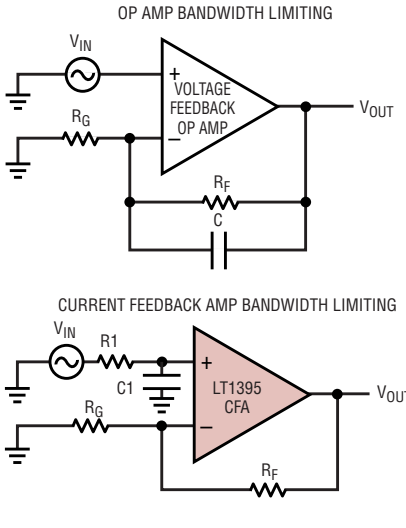


Figure 4. Bandwidth limiting

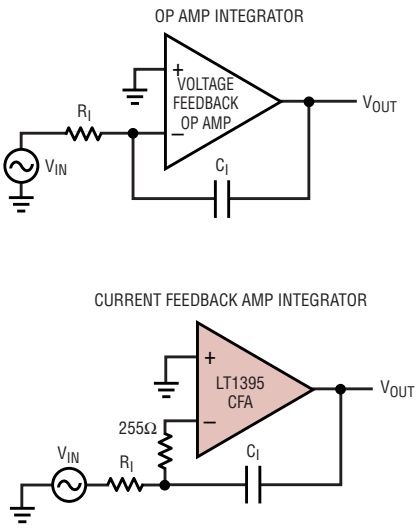


Figure 5. Integrators

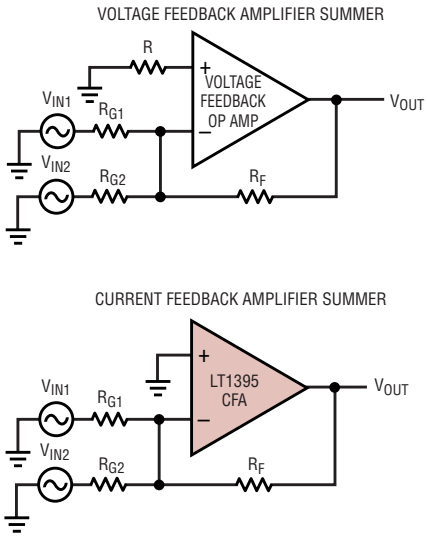


Figure 6. DC-accurate summing

discussed in the applications section that follows.

The bandwidth (and compensation) of a CFA is totally independent of R_G.[1] As seen in equation 9, R_G is only used to set the closed-loop gain.

Application Circuits: Comparing Voltage Feedback and Current Feedback

As seen in Figure 4, it is very common to limit the bandwidth of a conventional voltage feedback amplifier by putting a small capacitor in parallel with the feedback resistor, R_F. This technique does not work with current feedback amplifiers because the capacitor lowers the impedance seen by the inverting input at high frequencies. This results in reduced phase margin, which eventually leads to oscillation. To reduce the bandwidth of an application circuit using one of the LT1395/LT1396/LT1397 CFAs, simply increase the value of the feedback resistor from the nominal 255Ω; this will lower the bandwidth and increase stability. If the capacitor was added to compensate for parasitic capacitance at the inverting input, then increasing the feedback resistor may not help. In this case, a lowpass RC filter can be placed at the noninverting input.

As seen in Figure 5, an integrator is one of the easiest application circuits to make with a conventional op amp. The LT1395/LT1396/LT1397 CFAs require a slight change to the conventional topology to make sure that the inverting input always sees a resistance; simply add a resistor between the inverting input and the other passive elements.

The summing amplifier seen in Figure 6 has almost the same topology for voltage feedback op amps and for the LT1395/LT1396/LT1397 CFAs. The voltage feedback op amp has a series resistor added to the noninverting input to cancel the effects of bias current at the inverting and noninverting inputs. The CFA design eliminates the resistor at the noninverting input because the inverting bias current is uncorrelated with the noninverting bias current. The additional resistor would not improve DC accuracy.

Conclusion

With the introduction of the LT1395/LT1396/LT1397 family of 400MHz current feedback amplifiers, Linear Technology offers design solutions that are often superior to those using conventional voltage feedback op amps. High slew rate, consistent closed-loop gain and a flexible output stage all merge in a family of amplifiers that are useful in a broad range of applications.

Note:

[1]The actual –3dB bandwidth of a CFA falls off slightly with increased closed-loop gain. This bandwidth reduction is caused by the nonzero input impedance of the inverting input.

LTC1771, continued from page 9

standby time and maximizing battery live. With these parts, the designer has a choice of high or low input voltage and monolithic or controller configurations. The LTC1771 provides a wide supply range up to 18V and output currents up to 5A, whereas an upcoming product gives you constant frequency operation and loads of up to 500mA without the need for an external MOSFET and Schottky diode. With both available in the MS8 package and requiring only 10µA of supply current at no load, these products are perfect solutions for handheld electronics.

Tiny 12-Bit ADC Delivers 2.2Msps Through 3-Wire Serial Interface

by Joe Sousa

Introduction

Serial interfaces occupy little routing space, but usually limit the speed of an ADC. The LTC1402 has a full conversion speed of 2.2Msps and a very compact 3-wire interface for connecting to DSPs and microprocessors without glue logic. It comes in a 16-pin narrow SSOP package. This minuscule package (200mil × 230mil footprint) and compact serial interface are easy to fit close to sensors to best preserve analog signal integrity.

Other serial 12-bit ADCs have sample rates limited to hundreds of kilosamples-per-second, which limits their utility in high speed data acquisition systems. This slow sample rate, combined with poor distortion characteristics, makes them unsuitable for tracking high frequency signals. The LTC1402 will capture, in less than 60ns, the fast steps from an external analog input multiplexer for high speed data acquisition and it will digitize high frequency signals very accurately, with a 72dB S/(N+D) (signal-to-noise plus distortion ratio) at 1.1MHz, for communications or signal processing systems.

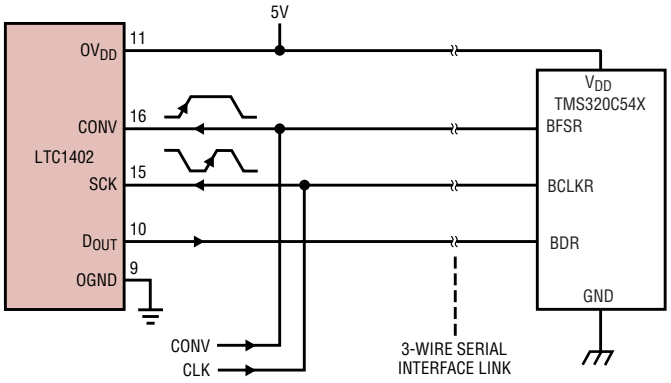


Figure 1a. DSP serial interface to the TMS320C54X

3-Wire Serial Interface for DSPs, Cables and Optocouplers

Figure 1a shows an example of interfacing the LTC1402 to the TMS320C54x DSP. No glue logic is needed to interface the LTC1402 to DSPs. The buffered serial port of the TMS320C54x talks directly to a dedicated 2kB segment of internal buffer memory. The ADC's serial data is collected in the 2k buffer, in two alternating 1kB segments, in real time, at the full 2.2Msps conversion rate of the LTC1402. Consult the LTC1402 data sheet for the TMS320C54x assembly code for this application.

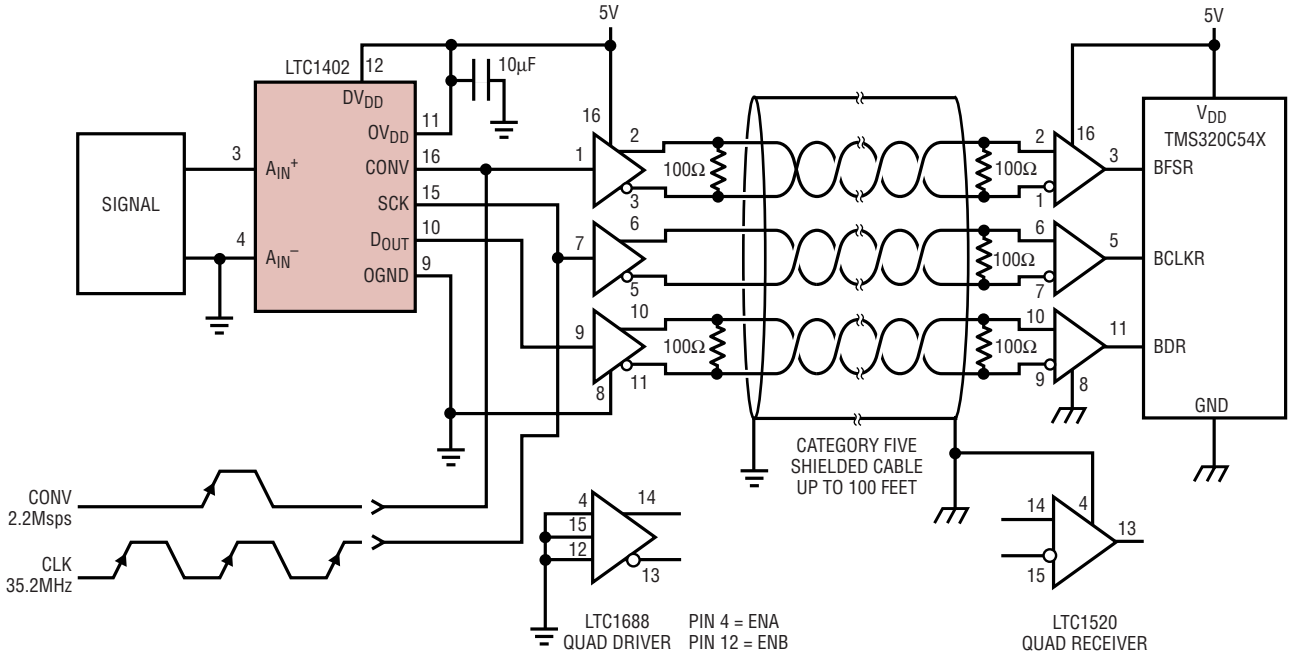


Figure 1b. The LTC1402 3-wire serial port sends data over 100 feet of category 5 twisted pair with the LTC1688/LTC1519 quad driver/receiver pairs

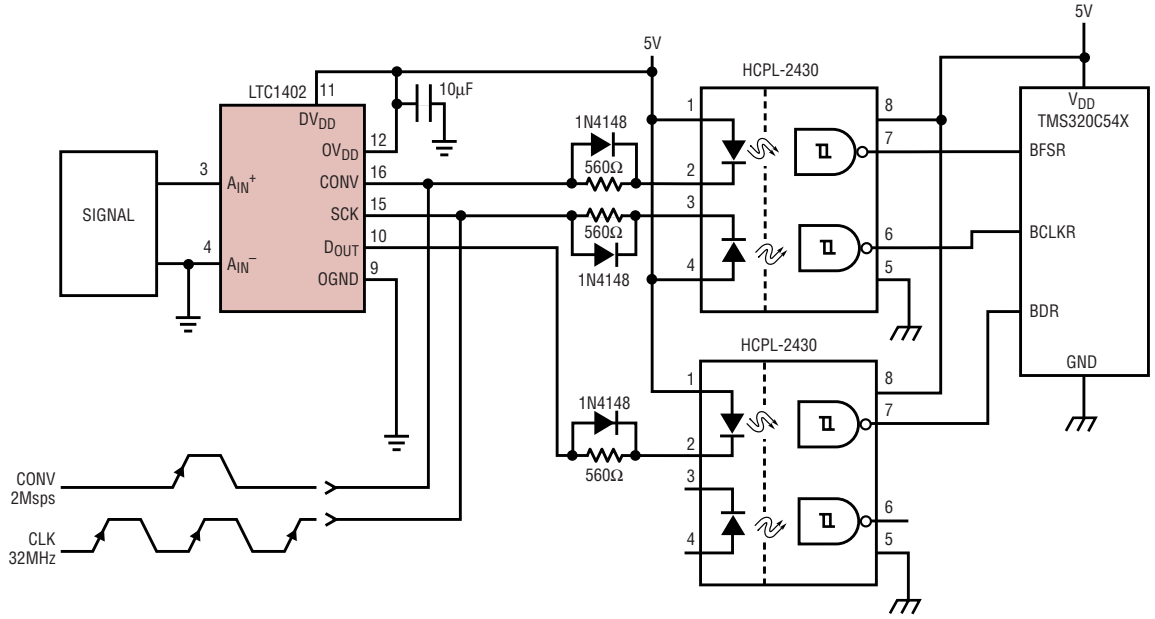


Figure 1c. The LTC1402 is easily isolated with high speed optocouplers

The minuscule 16-pin narrow SSOP package of the LTC1402 saves space in compact systems or systems that require a large number of ADCs. It can be located near the signal conditioning circuitry and send serial output data over a PC board trace of up to one foot in length to the DSP, as shown in Figure 1a.

Figure 1b shows the LTC1688/LTC1520 quad cable driver/receiver interfacing the LTC1402 to the DSP port to send the serial data over longer distances. The category-5 quad twisted pair shielded cable can extend up to 100 feet without data corruption. Because the SCK, CONV and D_{OUT} signals originate at the LTC1402, they arrive at the serial port with similar delays and remain synchronized. When the data is received at the serial port of a DSP or other processor, the port must be programmed to respond to the appropriate SCK and CONV edges. It is also necessary to check where the 12-bit output DATA sits in the 16-bit data frame. The TMS320C54x serial port READ instructions can shift the 12-bit data to the preferred position within the 16-bit data frame.

The serial interface lends itself to galvanic isolation with external optocouplers. Figure 1c shows how to isolate the LTC1402 with the HPCL-2430 dual optocoupler. The 40ns propagation delays through the dual optocouplers cancel to maintain a good timing match between the D_{OUT}, SCK and CONV signals. The LTC1402, running at a 2Msps conversion rate, sends 16-bit data frames through the HPCL-2430 optocouplers at 32MB/s.

3V or 5V Serial Interface without Spurious Noise

Figure 2 shows the block diagram of the LTC1402. The internal architecture has been optimized to send out data serially during conversion, without degradation of conversion accuracy due to digital noise. The 35MHz clock input at the SCK pin (15) and the external 2.2Msps conversion start input at the CONV pin (16) do not inject noise into the internal analog signal path of the ADC. As a result, the analog accuracy of the LTC1402 is insensitive to the phase, duty cycle or amplitude (3V or 5V) of the external digital inputs. The D_{OUT} pin (10) swings from the voltage at the OGND pin (9) to the voltage at the OV_{DD} pin (11) to allow direct interfacing to 5V or 3V DSPs and microprocessors. The LTC1402 is ideal in multiple-ground systems, where the differential input is connected to one ground, the supplies and grounds of the LTC1402 connect to a second, local ground and the output ground connects to a third, digital ground.

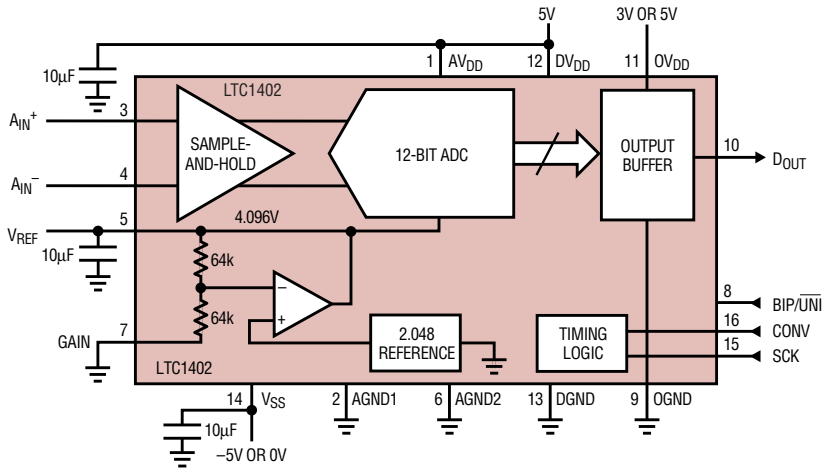


Figure 2. LTC1402 block diagram

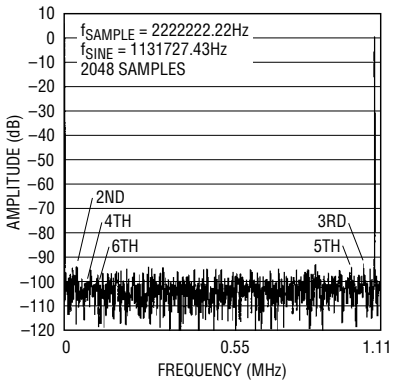


Figure 3. Sine wave spectrum plot (bipolar ±2V) with ±5V supplies

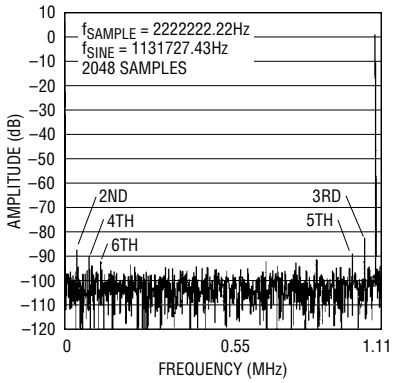


Figure 4. Sine wave spectrum plot (unipolar 0V–4V) with single 5V supply

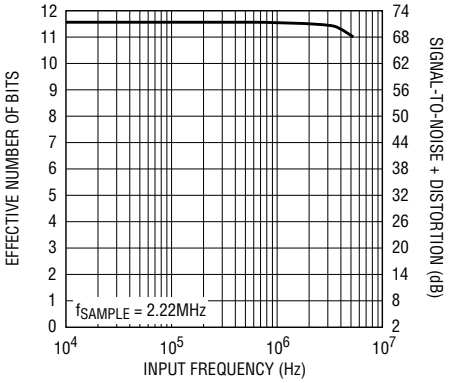


Figure 5a. ENOBs and SINAD vs input frequency (bipolar ±2V) with ±5V supplies

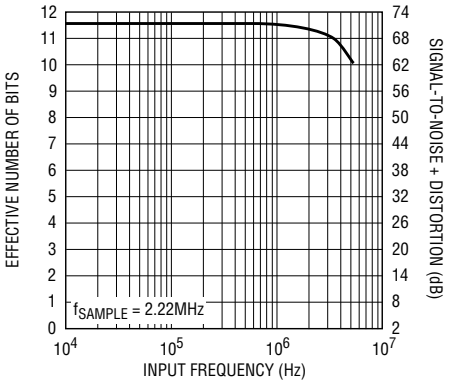


Figure 5b. ENOBs and SINAD vs input frequency (unipolar 0V–4V) with single 5V supply

Very High SFDR in Single 5V Supply Applications

A proprietary sampling front end circuit achieves exceptional dynamic performance at the 1.1MHz Nyquist frequency: –89dB THD with ±5V supplies and –82dB THD with a single 5V supply. Figures 3 and 4 show the spectra from a 1.1MHz Nyquist frequency sine wave with ±5V supplies and a single 5V supply, respectively. With this very clean spectrum, the LTC1402 minimizes crosstalk and interference in communications applications where the spectrum is divided into many frequency slots.

The LTC1402 maintains 72dB S/(N+D) with a 1.1MHz input sine wave, with either a single 5V or ±5V supplies. Positive signals can be applied with single or dual supplies and bipolar signals are easily accommodated with dual-supply operation.

The full power bandwidth of the LTC1402 is 80MHz; the full linear bandwidths (SINAD > 68dB) of 5MHz with ±5V supplies and 3.5MHz with a single 5V supply round out the exceptional dynamic performance of the LTC1402. The wideband signal conversion purity shown in Figures 5a and 5b makes the LTC1402 well suited for digitizing sine wave signals well above the 1.1MHz Nyquist frequency. Figures 6 and 7 show that transfer function purity, represented by the differential and integral linearity plots, is maintained at the full 2.2Msps conversion rate.

True Differential Inputs Cancel Wideband Common Mode Noise

The front-end sampling circuit acquires the input signal differentially from the A_{IN}^+ and A_{IN}^- analog inputs. Except for the sign inversion, these two inputs are identical. The wide common mode rejection bandwidth of the LTC1402 (–60dB at 10MHz input) affords excellent ground noise rejection in complex, noisy systems. Figure 8a shows the CMRR performance vs input frequency.

The differential inputs are very easy to interface to a wide range of signal sources. Grounding the A_{IN}^- input near the signal source reduces common mode ground noise. Setting the BIP/$\overline{UNI}$ pin (8) to a logic high selects the bipolar ±2.048V range; setting it to a logic low selects the unipolar 0V to 4.096V range.

The 0V to 4.096V unipolar range is ideal for single 5V supply applications where the A_{IN}^- input is grounded and the signal is applied to the A_{IN}^+ input. The ±2.048V bipolar range centered around midsupply can also be used in single 5V supply applications, with the A_{IN}^- input tied to a 2.5VDC source. Alternately, the full ±2.048V bipolar range can be driven with a pair of complementary ±1.024V signals into A_{IN}^+ and A_{IN}^-. This limits the swing of external single 5V supply amplifiers to their most linear region, from 1.5V to 3.5V. Figure 8b shows half of the LT1813 dual op amp driving the LTC1402 in this fully differential configuration with a single 5V supply.

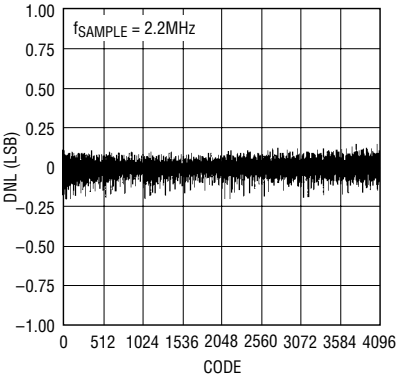


Figure 6. Differential nonlinearity vs output code (unipolar 0V–4V)

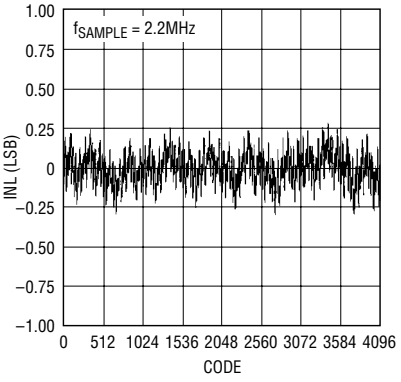


Figure 7. Integral nonlinearity vs output code (unipolar 0V–4V)

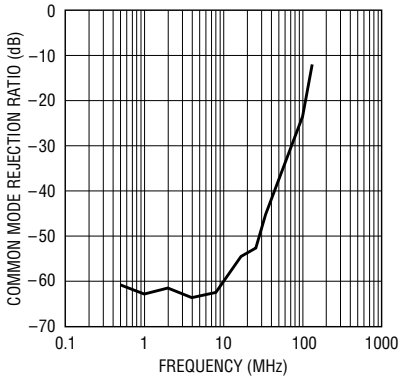


Figure 8a. CMRR vs input frequency

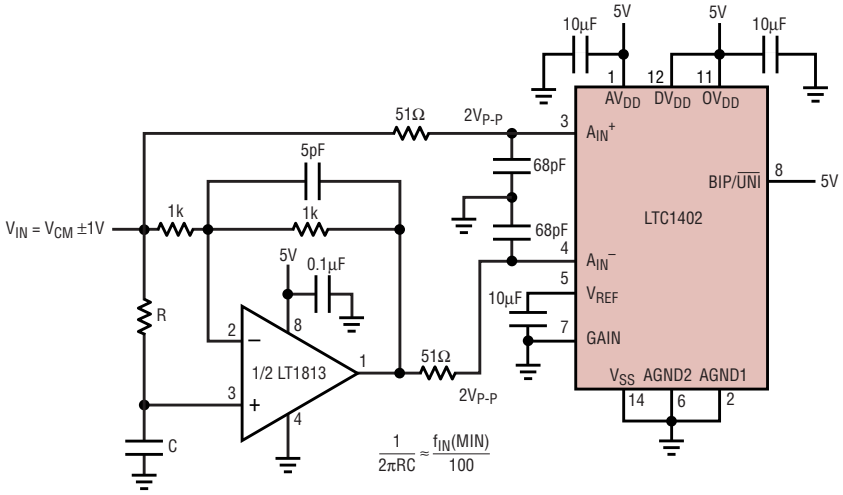


Figure 8b. True differential inputs accept $4V_{P-P}$ bipolar differential signal with $2V_{P-P}$ swings on each input and an effective gain of 2 from the LT1813 inputs. SINAD = 70.7dB with a 1MHz input.

Internal or External Reference

The internal 2.048V reference (multiplied by 2 at the V_{REF} output) sets the bipolar and unipolar ranges to ±2.048V and 0V to 4.096V, respectively. Tying the Gain pin (7) to the V_{REF} pin (5) cuts the reference voltage at the V_{REF} pin and analog input spans in half, to 2.048V. The internal reference can also be disabled by tying the Gain pin to V_{CC} and tying an external reference with an output between 2V and 5V directly to V_{REF}.

The single-ended unipolar input range of Figure 9a's circuit depends on the DAC's output voltage, which acts as an infinite sample-and-hold for signals such as a CCD sensor dark current or similar applications, as determined by software procedures. The LTC1446 12-bit serial DAC applies a voltage to the GAIN and A_{IN}^- pins of the ADC, in this case subtracting the A_{IN}^- voltage from the V_{REF} voltage, thus maintaining a positive full scale of 4.096V while varying zero scale over the range of 0V to 2V. This adjustment of the low end of the scale preserves the full 12-bit dynamic range of the ADC to digitize the input video signal between the dark-current value and 4.096V. The dark-current value must be a slow-moving DC value so that the DAC and the reference buffer amplifier can drive their respective 10µF capacitors. The LTC1446 DAC is stable with a 10µF load; care must be taken when substituting capacitors.

Figure 9b shows alternative connections to emulate the functional range of a flash converter in an image scanner application. The top and bottom of the conversion ranges are set independently by the LTC1446 DAC, just like the top and bottom voltages of the internal resistor ladder in a flash converter. The bottom of the

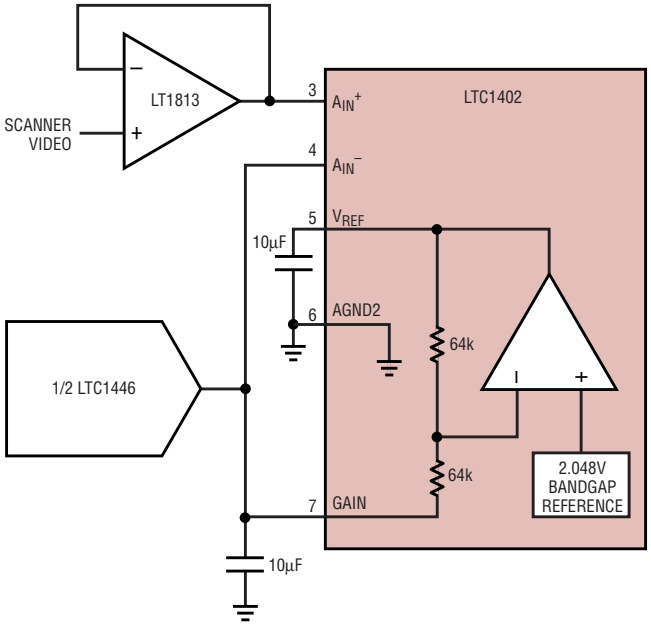


Figure 9a. The use of a DAC allows software adjustment of the lower end of the ADC range for applications such as dark-current cancellation.

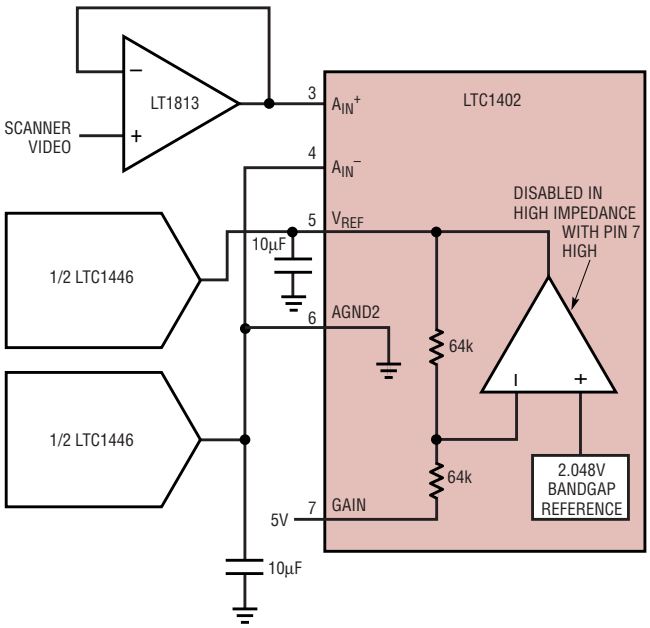


Figure 9b. A dual DAC allows software adjustment of both the full-scale and zero-scale voltages of the ADC, emulating the behavior of a flash converter.

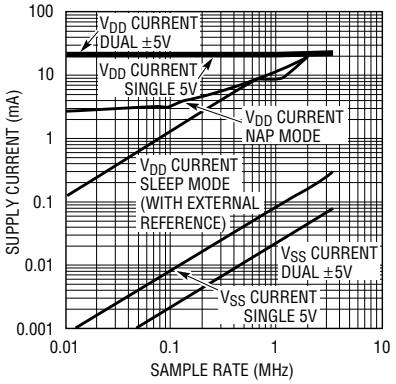


Figure 10. Current consumption vs sample rates for various operating modes and supply configurations

conversion range starts at the dark-current value and the top of the range is set externally to match the maximum possible output from the image scanner. The voltage at AGND (pin 6) may vary from 0V to 1V; that at VREF (pin 5) may vary from 2V to 5V. The LT1813 input buffer amplifiers may not be necessary if the image sensor has a low input impedance (<100Ω).

Reducing Power at Low Sample Rates

The LTC1402 consumes 90mW in normal operation, on either single 5V or ±5V supplies. NAP and SLEEP modes cut back power drain to 15mW and 10mW, respectively. NAP mode leaves the reference on and takes only 300ns to wake up, making it ideal for saving power between conversions in lower-sample-rate applications. SLEEP mode also shuts down the reference and takes 10ms to wake up. The REFREADY bit in the output data stream indicates when the reference has settled to full accuracy. NAP and SLEEP modes are easily set with two or four pulses at the CONV pin (16) input, respectively. One or more pulses at the SCK pin (15) input wakes up the LTC1402 for conversion.

Figure 10 shows the reduced power consumption while the sample rate is reduced and the NAP or SLEEP modes is used between conversions. For example, an undersampling application with NAP mode between conversions at a 455ksps sample rate draws only 40mW.

Conclusion

The LTC1402 has all the speed and AC and DC performance of fast 12-bit ADCs with parallel data interfaces, but it offers a much smaller, glueless serial interface that saves space in the 16-pin narrow SSOP package. The tiny LTC1402 can be placed right at the sensor for optimum analog signal capture and the compact 3-wire serial interface can be routed through a system board, through a cable or through an isolation barrier, to serial ports on DSPs and other processors.

LTC2401/LTC2402, continued from page 4

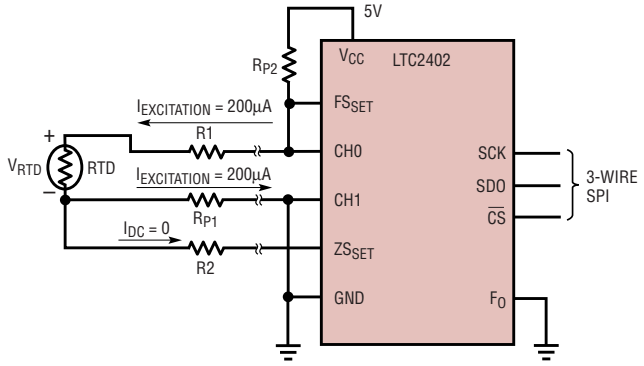


Figure 8. RTD remote temperature measurement

RTD Temperature Digitizer

RTDs used in remote temperature measurements often have long leads between the ADC and RTD sensor. These long leads result in parasitic voltage drops due to excitation current in the interconnect to the RTD. This voltage drop can be measured and digitally removed using the LTC2402, as illustrated in Figure 8.

The excitation current (typically 200µA) flows from the ADC reference through a long lead to the remote temperature sensor (RTD). This current is applied to the RTD, whose resistance changes as a function of temperature (100Ω–400Ω for 0°C to 800°C). The same excitation current flows back to the ADC ground and generates another voltage drop across the return leads. In order to get an accurate measurement of the temperature, these voltage drops must be measured and removed from the conversion result. Assuming that the resistance is approximately the same for the forward and return paths (R1 = R2), the second channel (CH1) on the LTC2402 can measure this drop. These errors are then removed with simple digital correction.

The result of the first conversion on CH0 corresponds to an input voltage of V_{RTD} + R1 • $I_{EXCITATION}$. The result of the second conversion (CH1) is –R1 • $I_{EXCITATION}$. Note that the LTC2402's input range is not limited to the supply rails; it has underrange as well as overrange capabilities. The device's input range is –300mV to FS_{SET} + 300mV (D_{OUT} includes a sign bit indicating a negative input). Adding the two conversion results, the voltage drop across the RTD's leads is cancelled and the final result is V_{RTD}.

Conclusion

Linear Technology has introduced two new converters to its 24-bit No Latency ΔΣ™ converter family. The family consists of the LTC2400 (1-channel, 8-pin SO), LTC2408 (8-channel, 24-bit ADC) and the LTC2401/LTC2402 shown here. Each device features excellent absolute accuracy, ease-of-use and near zero drift. The LTC2401/LTC2402 also include full-scale set (FS_{SET}) and zero-scale set (ZS_{SET}) inputs for removing errors due to systematic voltage drops. The performance, features and ease-of-use of these devices warrant that designers reconsider the accuracy capabilities of their future system designs.

LTC1645/LTC1735 Circuit Solves PCI Power Problem

by Ajmal Godil

In some applications, it is necessary to select and hot swap the higher of two supplies and generate a regulated output voltage from the selected supply. If only one input supply is present, the circuit should select it and generate the same output voltage. The term "hot swapping" refers to plugging a circuit board into or removing it from a live backplane. When this is done, the supply bypass capacitors on the board can draw huge transient currents from the backplane power bus as they charge. The transient currents can cause permanent damage to the connector pins and cause glitches on the system supply, causing other boards in the system to reset. A circuit based on an appropriate LTC Hot Swap™ controller can eliminate these problems.

The circuit in Figure 1 selects between and hot swaps a 3.3V and a 5V input supply and generates a

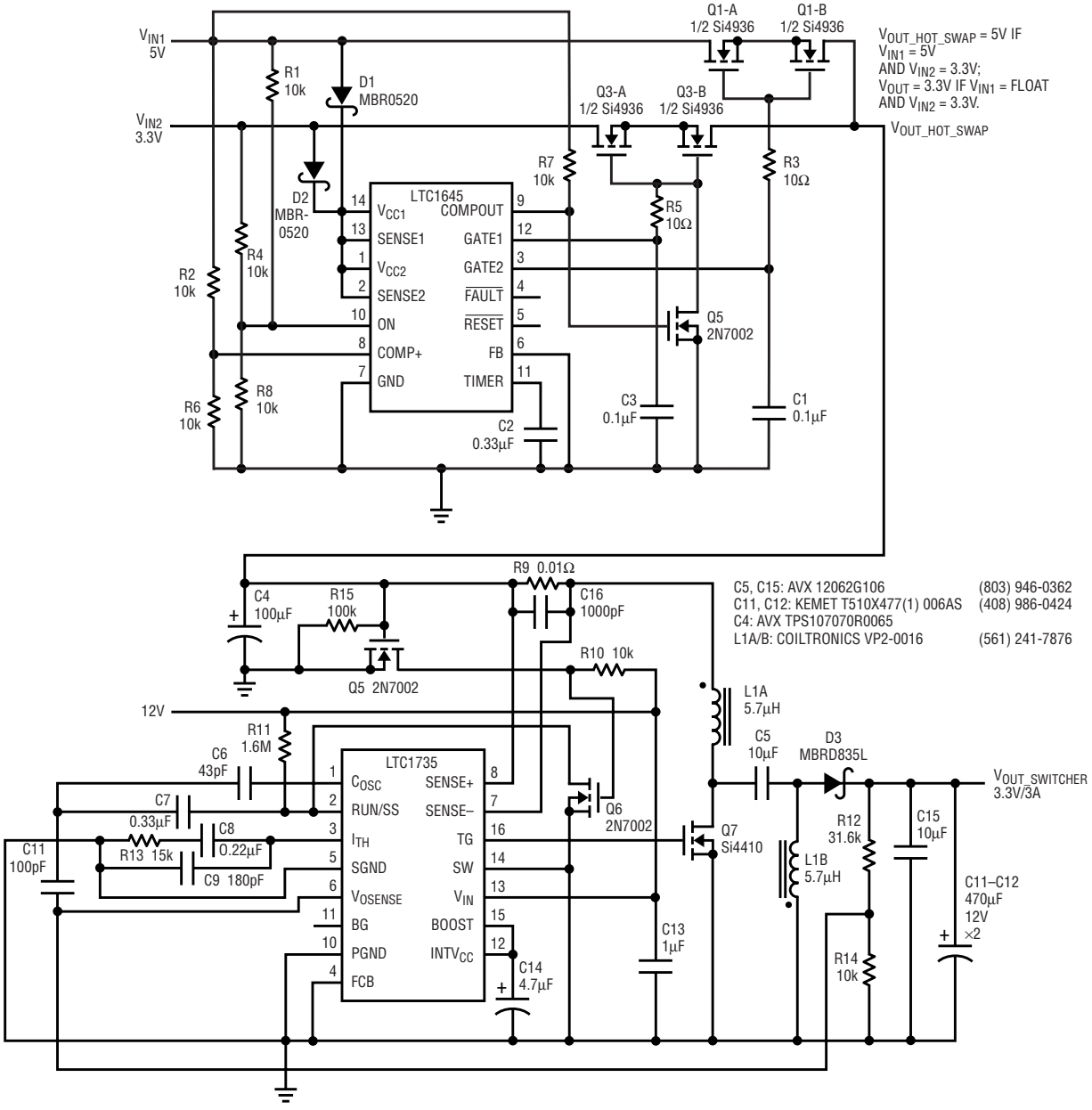


Figure 1. LTC1645 3.3V/5V Hot Swap circuit plus LTC1735 SEPIC converter

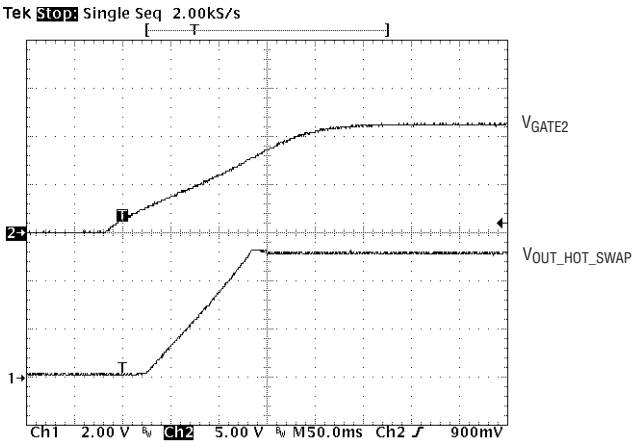


Figure 2. V_{GATE2} and $V_{OUT\_HOT\_SWAP}$ increasing to 12V and 5V, respectively

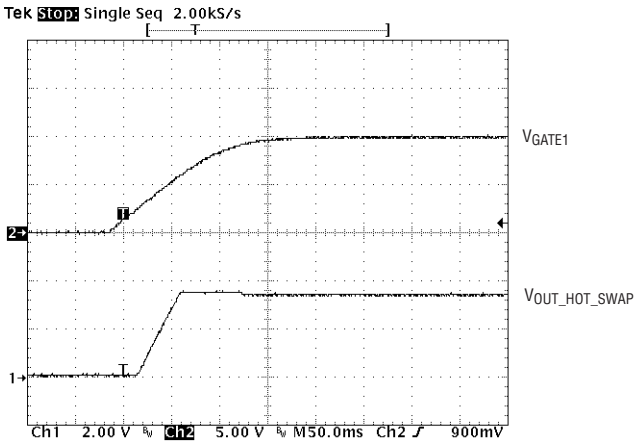


Figure 3. V_{GATE1} and $V_{OUT\_HOT\_SWAP}$ increasing to 10V and 3.3V, respectively

constant 3.3V output supply using the LTC1645 and the LTC1735. The LTC1645 is a 2-channel Hot Swap controller and the LTC1735 is a synchronous step-down switching regulator. The two voltage supplies, V_{IN1} and V_{IN2}, are fed into the LTC1645 Hot Swap circuit, where the higher of the two supplies is selected ($V_{OUT\_HOT\_SWAP}$) and then fed into the LTC1735 DC/DC converter. The LTC1735 circuit generates a constant 3.3V output voltage, regardless of whether its input is 3.3V or 5V. To simplify the circuit description, the operation of the LTC1645 and the LTC1735 will be discussed separately.

LTC1645 Hot Swap Operation

Back-to-back MOSFETs Q1 and Q2 are connected to the V_{IN1} (5V) supply and Q3 and Q4 are connected to the V_{IN2} (3.3V) supply. The reason for using back-to-back MOSFETs is to keep the internal body diodes from shorting the 5V and 3.3V supplies together. The LTC1645's Gate1 pin controls Q3 and Q4 and its Gate2 pin controls Q1 and Q2. The ON pin has a 0.8V turn-on threshold for Gate1 and a 2.0V turn-on threshold for Gate2. The V_{CC1} and V_{CC2} pins have 2.3V and 1.2V undervoltage lockout thresholds, respectively. Since the circuit in Figure 1 selects between two supplies, the following two cases are possible:

Case One: 5V and 3V Supplies Present

When the 5V and 3.3 supplies are present on V_{IN1} and V_{IN2}, respectively, V_{CC1}, V_{CC2}, Sense2 and Sense1 are pulled up to approximately 4.7V by D1, which clears the undervoltage lockout thresholds of V_{CC1} and V_{CC2}. The $COMP^+$ pin is pulled up to 2.5V by the voltage divider formed by R2 and R6. Since the voltage on the $COMP^+$ pin (noninverting terminal of the onboard comparator) is greater than a 1.24V threshold, the COMPOUT pin (open drain output of the comparator) is pulled up to 5V by R7. This turns on Q5 and pulls the gates of Q3 and Q4 to ground. The ON pin is pulled up to approximately 2.74V through R1, R4 and R8. After one timing cycle (t = C2 • 1.24V/2µA), an internal 10µA current source from the charge pump is connected to the Gate1 and Gate2 pins. The Gate1 pin is pulled to ground by Q5 and the voltage on the Gate2 pin starts to rise, with a slope given by dV/dt = 10µA/C1. The internal charge pump guarantees that the Gate2 voltage will rise to approximately 12V. As

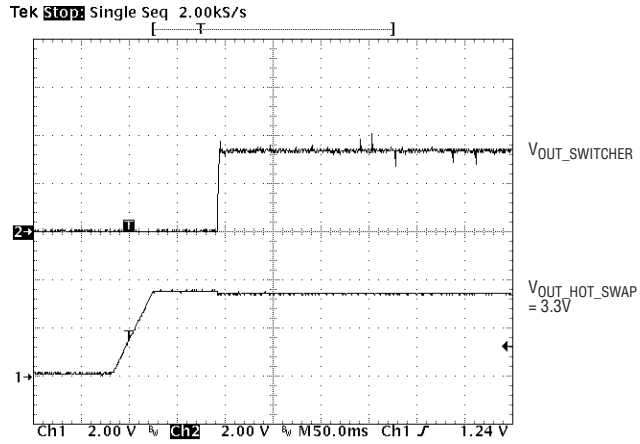


Figure 4. LTC1735 SEPIC voltage-rise waveforms; $V_{OUT\_HOT\_SWAP}$ and $V_{OUT\_SWITCHER}$ = 3.3V

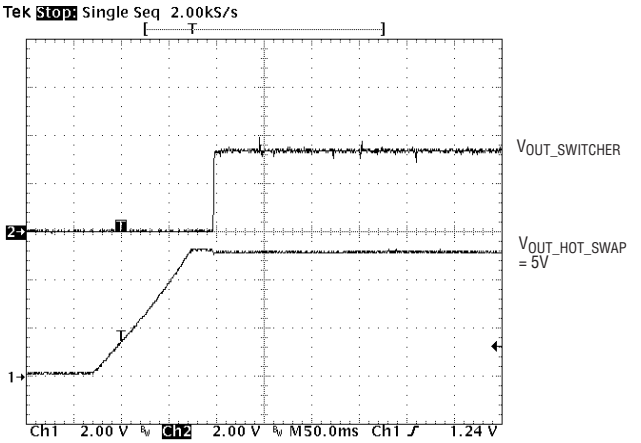


Figure 5. LTC1735 SEPIC voltage-rise waveforms; $V_{OUT\_HOT\_SWAP}$ = 5V and $V_{OUT\_SWITCHER}$ = 3.3V

the Gate2 voltage rises to about 1V, Q1 and Q2 start conducting and $V_{OUT\_HOT\_SWAP}$ starts rising. The output voltage will eventually rise to the input supply, which is 5V. Figure 2 shows the Gate2 pin and $V_{OUT\_HOT\_SWAP}$ voltages rising to 12V and 5V, respectively.

Case Two: Only 3.3V Supply Present

V_{CC1}, V_{CC2}, Sense1 and Sense2 are pulled up to 3.0V by D2, which clears the undervoltage lockout thresholds of V_{CC1} and V_{CC2}. Since the 5V supply is not present, the ON pin is only pulled up to 1.65V by R4 and R8. After one timing cycle, an internal 10µA current source from the charge pump is connected to the Gate1 pin. The voltage on the Gate1 pin starts to rise with a slope given by dV/dt = 10µA/C3. The internal charge pump guarantees that the Gate1 voltage will rise to approximately 10V. Since the ON pin is below 2V (the ON pin turn-on threshold for Gate2), a 40µA current source pulls the Gate2 pin toward ground. As the Gate1 pin voltage rises to about 1V, Q3 and Q4 start conducting and $V_{OUT\_HOT\_SWAP}$ starts rising. The output voltage will eventually rise to the input supply voltage, which is 3.3V. Figure 3 shows the Gate1 and $V_{OUT\_HOT\_SWAP}$ voltages rising to 10V and 3.3V, respectively.

LTC1735 Operation

The LTC1735 is connected in a SEPIC (single-ended, primary inductance converter) configuration to produce a constant 3.3V output at 3A. Since the minimum input voltage for the LTC1735 is 3.5V, the V_{IN} pin on the chip is connected to a 12V supply that can provide a few milliamps. The main load current is supplied by either V_{IN1} (5V) or V_{IN2} (3.3V). Q5, Q6 and R11 in Figure 1 allow the LTC1735 to produce to an output voltage after the input supply ($V_{OUT\_HOT\_SWAP}$) has finished rising. Figures 4 and 5 show the LTC1735 producing a 3.3V output from a 3.3V or a 5V $V_{OUT\_HOT\_SWAP}$ supply input. Figure 6 shows the typical efficiency curves for a $V_{OUT\_HOT\_SWAP}$ supply of 3.3V or 5V at an output voltage of 3.3V. Figure 7 shows the output voltage ripple with a steady-state load of 3A and Figure 8 show the transient response for a 0.5A–3A load step. Note that all the components used in the circuit of Figure 1 are surface mountable and fit in an area of less than 1.5in^2.

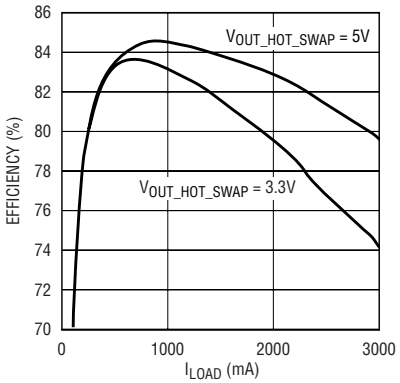


Figure 6. LTC1735 efficiency vs load current ($V_{OUT\_SWITCHER}$ = 3.3V)

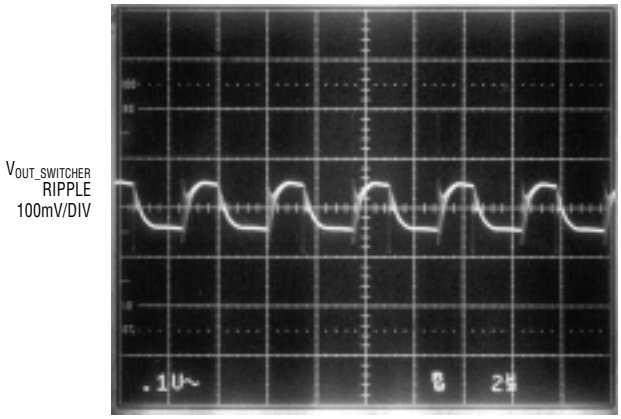


Figure 7. LTC1735 output voltage ripple: output voltage = 3.3V, load current = 3A

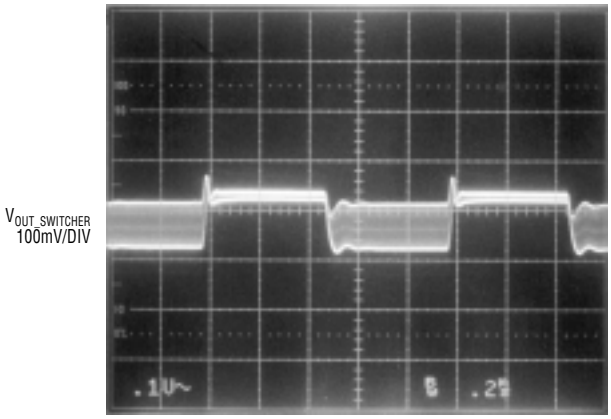


Figure 8. LTC1735 transient response: load step = 0.5A–3.3A

For more information on parts featured in this issue, see http://www.linear-tech.com/go/ltmag

Active Voltage Positioning Saves Output Capacitors in Portable Computer Applications

by John Seago
and Ajmal Godil

Introduction

Active voltage positioning is a technique that can be used to save cost and space by reducing the number of output capacitors required to meet a microprocessor's power supply requirements. Total system cost and required PCB space are important aspects of today's portable equipment designs, so decreasing the number of large, expensive output capacitors is worth some effort. Both the LTC1735/LTC1736 current mode switching regulator controllers (*Linear Technology* IX:1, February 1999, pp. 1, 3–5, 35) and the LTC1702/LTC1703 voltage mode controllers (*Linear Technology* IX:3, September 1999, pp. 16–20) can take advantage of active voltage positioning.

Microprocessor Load Steps

Microprocessors frequently change their load current requirement from almost no load to maximum load current and back again very quickly. The rising and trailing edges of these load current steps exceed the bandwidth of the switching regulator control loop. Currently, a typical load step is either 0.2A to 12A in 100ns or 12A to 0.2A in 100ns. The core voltage of the microprocessor must be held to about ±0.1V of nominal in spite of these load steps.

Since the switching regulator control loop cannot respond in 100ns, the output capacitors must temporarily supply the load current when the output current increases rapidly. Also, the output capacitors must absorb the energy stored in the inductor when the output current decreases rapidly. Capacitor ESR and ESL primarily determine the amount of droop and overshoot in the output voltage caused by a load current step. Normally, several capacitors in parallel are required to meet the microprocessor load transient requirements.

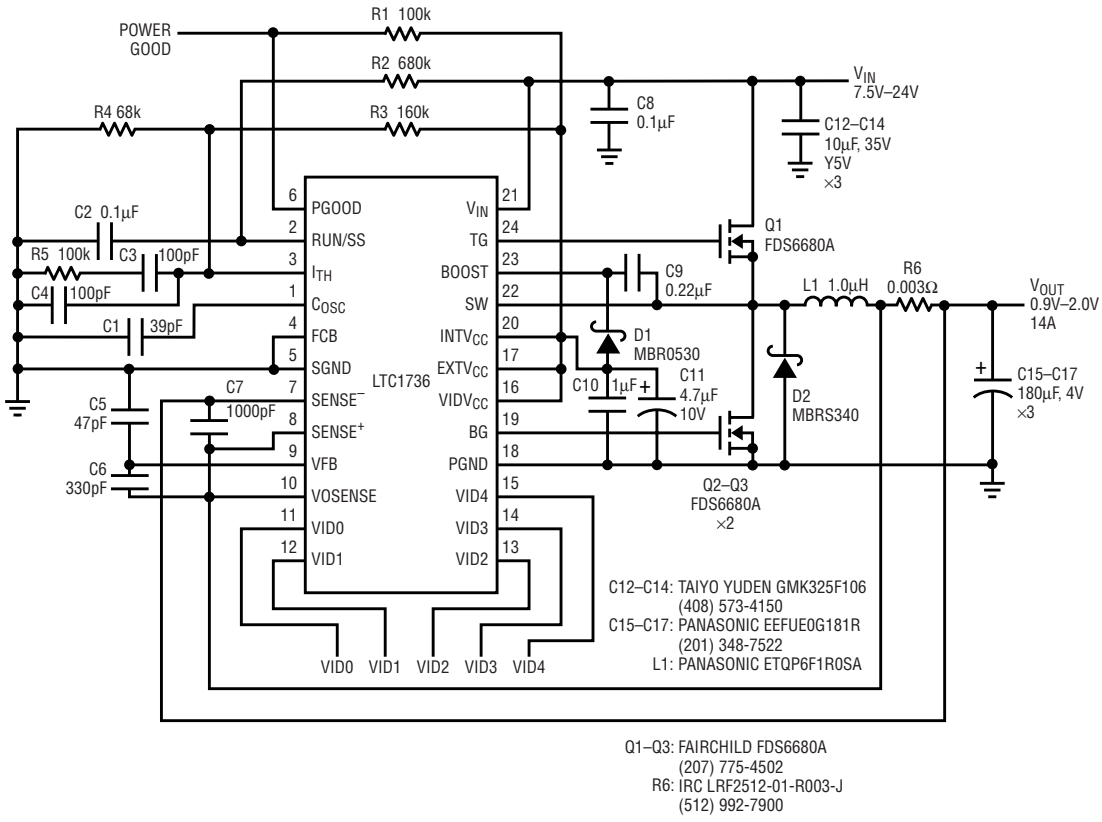


Figure 1. LTC1736-based core-voltage regulator with active voltage positioning

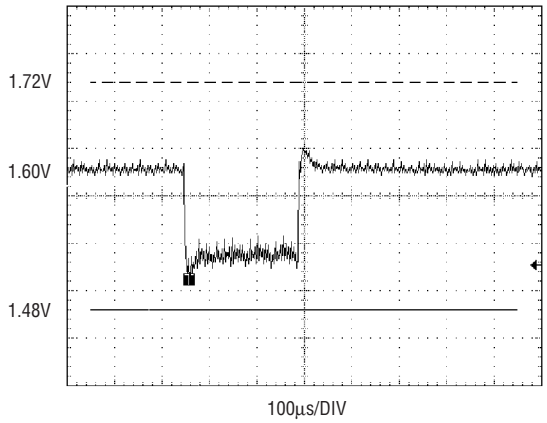


Figure 2. Transient response for a 12A load-current step

How Active Voltage Positioning Works

Active voltage positioning is a form of deregulation. It sets the output voltage high for light loads and low for heavy loads. In the low-current-to-high-current transition, the output voltage starts at a voltage higher than nominal so the output voltage can sag more and still meet the minimum output voltage specification. By setting the output voltage lower than nominal for heavy load conditions, more output voltage variation is possible when the load current suddenly decreases to almost zero. Less output capacitance is required because more output voltage variation is allowed on the output capacitors.

The implementation of active voltage positioning depends on the type of OPTI-LOOP error amplifier used in the switching regulator. With the LTC1736, connecting two resistors to the I_{TH} pin adjusts the output voltage in inverse proportion to the amount of load current. This technique will only work with a current mode control regulator. Different techniques are available for the LTC1703; these can also be used on the LTC1736 and will be discussed later.

LTC1736 Circuit with Active Voltage Positioning

Reducing output capacitance with active voltage positioning requires connecting two resistors to the I_{TH} pin and readjusting the loop compensation component values. Figure 1 shows a core voltage regulator circuit designed to operate from a 7.5V to 24V input and provide ±7.5% accuracy to VID controlled output voltages from 0.9V to 2.0V with load current steps from 0.2A to 12A. Although 7.5% output voltage accuracy does not sound very impressive, 7.5% of 1.4V is only 105mV, including setpoint accuracy and load and line regulation, as well as margin for transient response to the 12A load step.

The circuit in Figure 1 is a current mode, synchronous buck regulator with a switching frequency of 300kHz. The nominal output voltage is selected by the standard Intel mobile VID code. The actual output voltage varies as a function of the load current. The no-load output voltage from this circuit is higher than nominal because the current sourced by R3 creates a positive offset at the input of the transconductance error amplifier. The error amplifier current sourced into

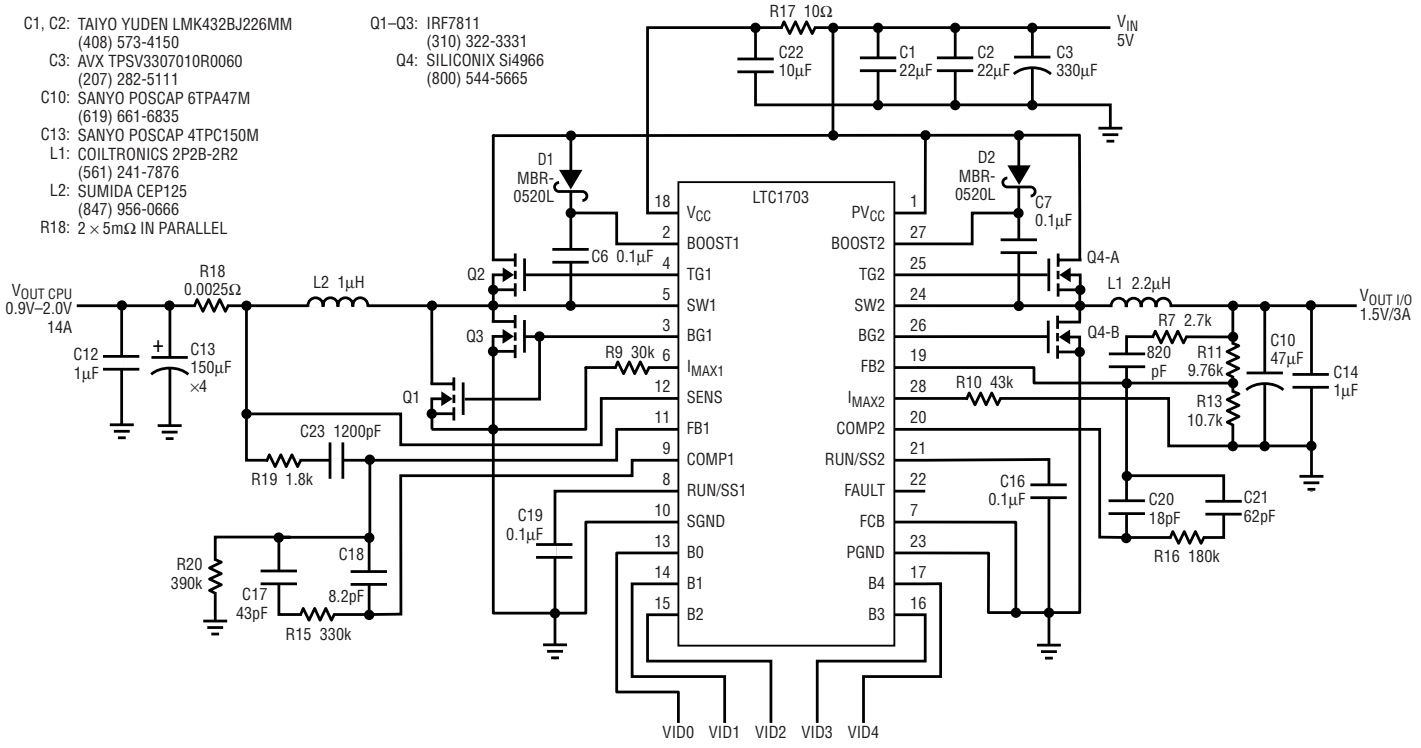


Figure 3. LTC1703-based regulator with active voltage positioning implemented with a sense resistor

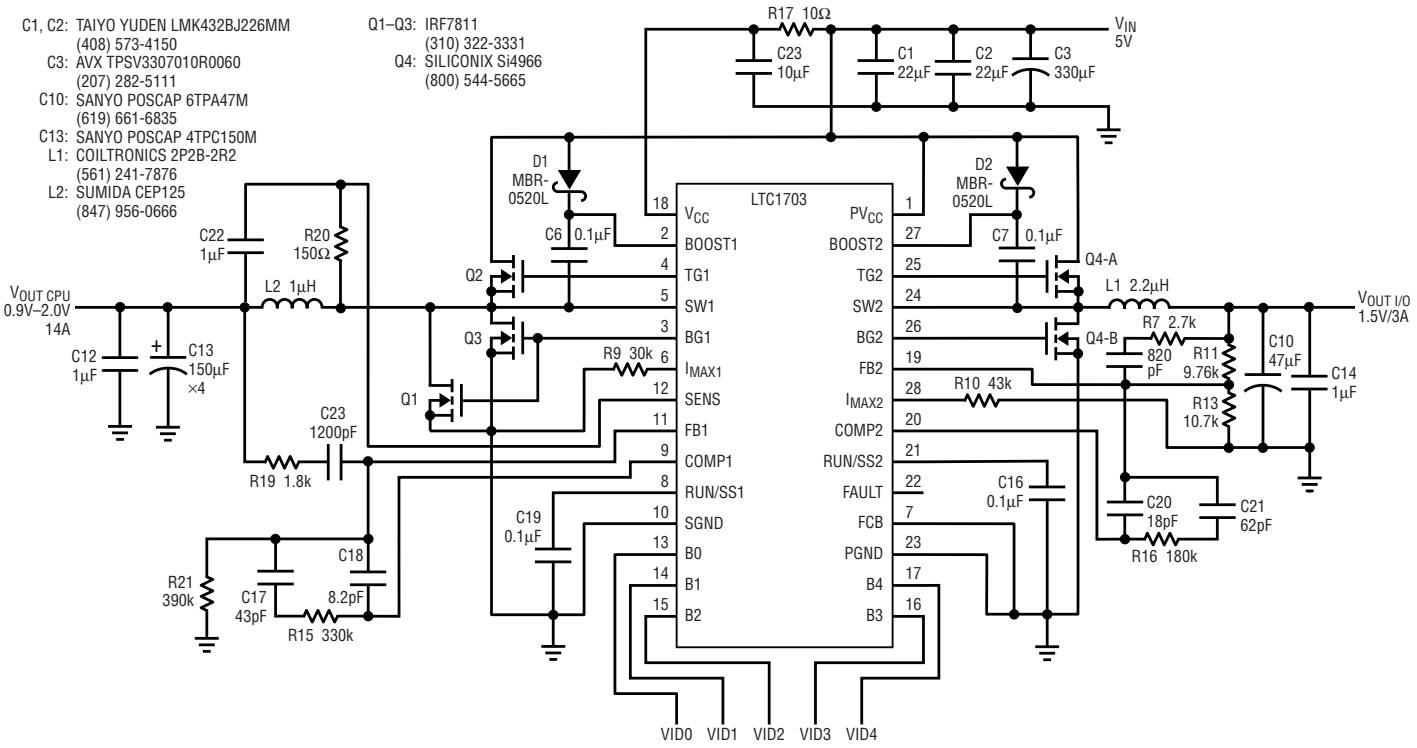


Figure 4. LTC1703-based regulator with active voltage positioning implemented using the DC resistance of the inductor

R4 develops a negative input offset voltage. This negative offset causes the output voltage to be less than nominal under full load conditions.

Forced offsets at the input of the error amplifier should be limited to ±30mV. If a lower output voltage is required at full load, the voltage drop across the current sense resistor can be subtracted from the regulated output voltage by connecting the V_{OSENSE} pin to the inductor side of the sense resistor, as shown in Figure 1. Figure 2 shows a transient waveform of 50mV and –100mV from a 12V input and 1.6V output of Figure 1's circuit. The output voltage tolerance of 7.5% allows a ±120mV variation.

LTC1703 Circuit with Active Voltage Positioning

Figures 3 and 4 show two methods of implementing active voltage positioning on an LTC1703 circuit. In Figure 3, the voltage deregulation is set by adding a 2.5mΩ resistor (R18) in the power path. At full load, the output voltage will be less than nominal by $I_{FULL\ LOAD}$ • 0.0025. In order to program the output voltage higher than nominal at zero load, a 390k resistor, R20, is added between the FB1 pin and ground. The DC value by which the output voltage increases over nominal can be calculated by the following formula:

$$V_{HIGHER} = (0.8/390k) \bullet 10k \approx 20mV$$

In Figure 4, the voltage deregulation is set by the DC resistance of the power inductor, which is approximately 2.5mΩ. The SENSE pin on the LTC1703 is connected between R20 (150Ω) and C24 (1µF). R20 and C24, which are connected across the inductor L2, act as a lowpass filter with a time constant of 150µs. Likewise, a 390k resistor, R21, is added between the FB1 pin and ground. Figure 5 shows the transient response of the LTC1703 circuit in Figures 3 and 4 for a 0A–14A transient load step with four 150µF Poscap capacitors.

Conclusion

Active voltage positioning allows more output voltage change during a load transient so fewer output capacitors are required. Fewer capacitors result in a smaller, less expensive regulator.

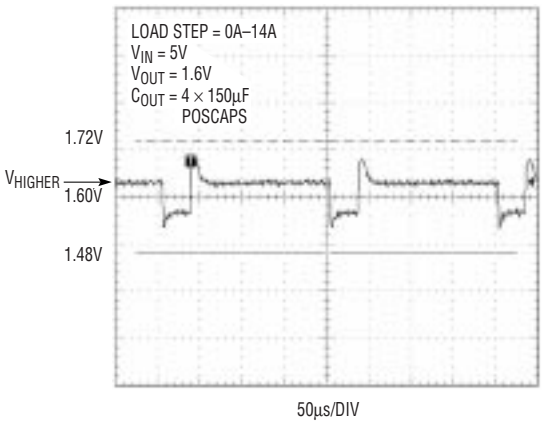


Figure 5. LTC1703 $V_{OUT\ CPU}$ transient response with active voltage positioning

ADSL Line Driver/Receiver Design Guide, Part 1

by Tim Regan

Introduction

Consumer desire for faster Internet access is driving the demand for very high data rate modems. A digital subscriber line (DSL) implementation speeds data to and from remote servers with data rates of 512Kbps to 8Mbps, much faster than current 56Kbps modem alternatives. This speed of data communication is providing the Internet with the capability to transfer information in new formats such as full-motion video, while greatly improving the timeliness of conventional information access.

One very important feature of DSL technology is that the connection is handled through a normal telephone line; therefore, no special high speed cables or fiber optic links are required and every home and office is most likely DSL ready. Another feature is that the data interface can operate simultaneously with normal voice communication over the same telephone line. This allows the modem to be connected at all times and not interfere with the use of the same line for normal incoming and outgoing phone calls or faxes.

The real "magic" of DSL technology stems from the application of digital signal processing (DSP) algorithms and data coding schemes. The implementations have built-in intelligence to accommodate the wide variations of data transmission signal conditions

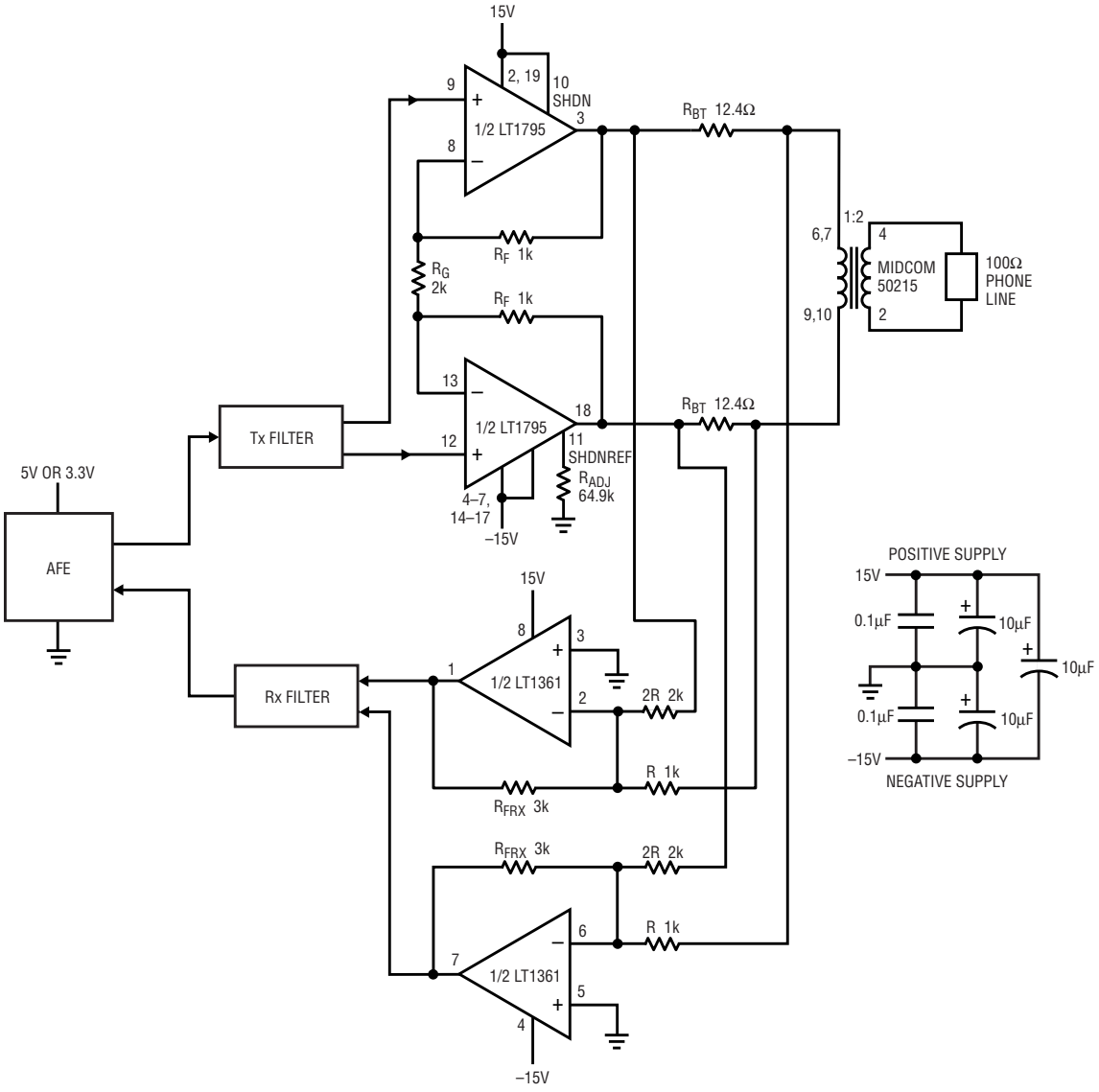
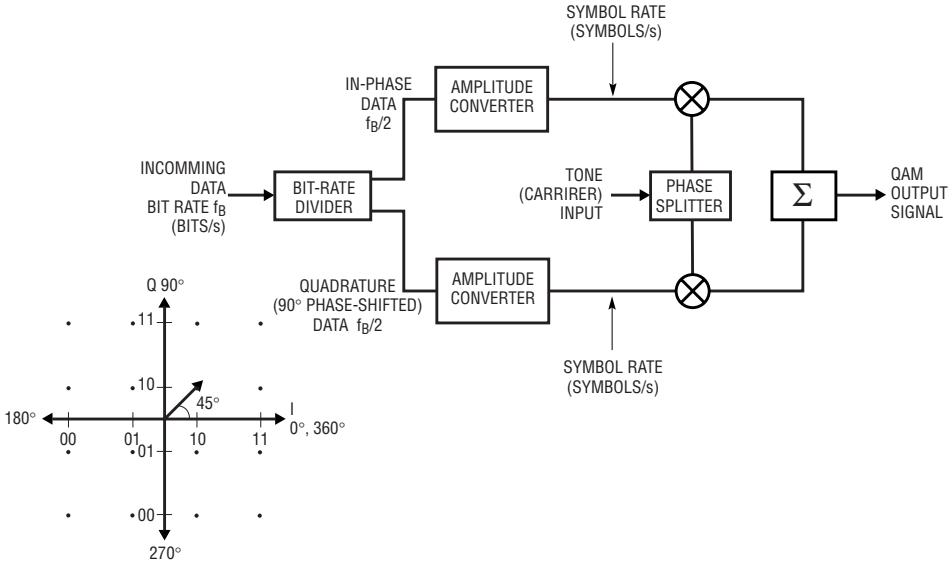


Figure 1. Central-office ADSL transceiver



CODE		LEVELS		VECTOR	
I	Q	I (2MSB)	Q (2LSB)	MAG	ANGLE (°)
00	00	–3	–3	4.2	225
00	01	–3	–1	3.2	198
00	10	–3	1	3.2	162
00	11	–3	3	4.2	135
01	00	–1	–3	3.2	252
01	01	–1	–1	1.4	225
01	10	–1	1	1.4	135
01	11	–1	3	3.2	108
10	00	1	–3	3.2	288
10	01	1	–1	1.4	315
10	10	1	1	1.4	45
10	11	1	3	3.2	72
11	00	3	–3	4.2	315
11	01	3	–1	3.2	342
11	10	3	1	3.2	18
11	11	3	3	4.2	45

Figure 2. Quadrature amplitude modulation

encountered with each connection through the telephone switching network. Sophisticated ASICs have been developed to provide small modems for PCs and handheld devices and the ability to compact many DSL lines on a single PCB card for telephone central-office deployment.

However, as is the case with almost any system, DSL still requires fundamental operational amplifier functions to put the signal on to the phone line and to pick off the small signals received at the other end. Although many system designers are competent and comfortable with DSP and all things digital, they often find their understanding of analog issues to be a bit rusty when it comes to implementing the physical connection to and from the telephone line. This series of articles will provide an overview of the requirements placed on the amplifiers and provide guidelines to component selection and the implications on distortion performance and power consumption and dissipation, the most important system issues related to the analog components.

Figure 1 shows a complete central office DSL line driver/receiver. This is the basic circuit topology that provides differential transmit signal drive to the line and detection of the differential received signal. The full requirements of DSL are easily met by using devices from Linear Technology's broad line of high speed power amplifiers for the driver and high speed, low noise dual amplifiers for the receiver. Using either current feedback or voltage feedback topologies, the family of drivers consists of amplifiers with bandwidths from 35MHz to 75MHz, slew rates in excess of 200V/µs with output current capability from 125mA to over 1 amp. The receiver family combines similar high speed performance with low noise, less than 10nV/$\sqrt{Hz}$, and low quiescent operating current, less than 10mA. The devices shown in Figure 1 are the LT1795 500mA output current, 50MHz bandwidth dual op amp and the LT1361 50MHz dual amplifier with input noise voltage of 9nV/$\sqrt{Hz}$ and total supply current of only 10mA.

Although there are several variations of DSL technology (SDSL, HDSL, HDSL2, VDSL and ADSL, to name a few) the requirements placed on the amplifiers for these different standards are very similar. The major difference between the approaches, as they affect the line driver, is the amount of power actually put on to the phone line by the line-driver amplifier. For simplicity, these articles will focus on the most recently approved standard, ADSL (asymmetric DSL), but the concepts discussed apply equally to any of the other standards.

This first installment will provide an overview of the requirements of ADSL and how it is done, as well as a discussion of the circuit topology and the requirements for the components used for implementation.

The Requirements for ADSL

The full specifications for ADSL are contained in two ITU (International Telecommunications Union) documents called G.992.1, for systems often referred to as Full-Rate ADSL or G.dmt, and G.992.2, a lower data rate approach often called G.Lite. Both systems use a technique called discrete multitone, or DMT, for transmitting data. With DMT, a frequency band up to 1.2MHz is split up into 256 separate tones (also call subcarriers) each spaced 4.3125kHz apart. With each tone carrying separate data, the technique operates as if 256 separate modems were running in parallel. To further increase the data transmission rate, each individual tone is quadrature amplitude modulated (QAM). As shown in Figure 2, the data to be transmitted is used to create a unique amplitude and phase-shift characteristic for each carrier tone, through the combination of I and Q data, called a symbol. The symbols represented by each tone are updated at a 4kHz rate or 4000 symbols per second. Full Rate ADSL uses up to 15 bits of data to create

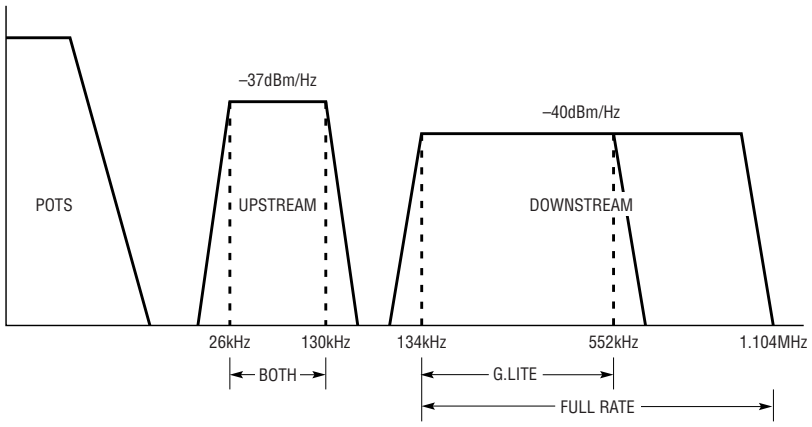


Figure 3. DMT channel allocation

each symbol. This results in a theoretical maximum of 60Kb/s for each tone. If all 256 tones are used in parallel, the total theoretical data rate can be as fast as 15.36Mb/s. For G.Lite, only 8 bits are used per symbol with only half of the carrier tones used for a theoretical maximum data rate of 4.096Mb/s.

In an actual DSL application, the tones are allocated for use depending on the direction of communication, as shown in Figure 3. Most of the tones are used for communication from the central office (CO) to an end user's PC modem (often referred to as the CPE or customer premises equipment). This direction of communication is called "downstream." The direction of communication from a PC modem to the central office (and, ultimately, to an Internet server) is called "upstream." The use of more tones for the downstream direction makes sense from an Internet-access point of view, because most users download more information than they upload. Most upstream communication with a server is simply to request information to be sent quickly downstream. This difference in data rates up- and downstream is the reason ADSL is called asymmetric DSL.

Also indicated in Figure 3 is the power spectral density (PSD) of all of the tones used. This determines the amount of signal power that needs to be put on to the phone line. The power levels are restricted to minimize crosstalk and interference into other phone lines contained in wire bundles *en route* to and from the central office. The total power required can be determined from the following equation:

$$\text{LINE POWER (dBm)} = \text{PSD (dBm/Hz)} + 10 \bullet \text{Log}(F_{MAX} - F_{MIN})$$

The downstream power requirements are much higher than the upstream requirements because of the wider bandwidth used for the transmission. For this reason, Full Rate ADSL requires more line power than G.Lite for downstream transmissions. Upstream power is the same for both Full Rate and G.Lite

Table 1. ADSL requirements

Parameter		Full Rate ADSL Downstream	ADSL G.Lite Downstream	Full Rate ADSL or G.Lite Upstream
Characteristics	Channels Used	31 to 256	31 to 128	6 to 30
	Frequency Band (kHz)	133.7 to 1104	133.7 to 552	25.8 to 129.4
	Bandwidth (kHz)	970.3	418.3	103.5
	Power Spectral Density, PSD (dBm/Hz)	–40	–40	–37
	Line Power (dBm)	20	16.3	13
Electrical Requirements	RMS Line Power (mW)	100	43	20
	Line Impedance (Ω)	100	100	100
	RMS Line Voltage (V)	3.1	2	1.4
	RMS Line Current (mA)	31	21	15
	Peak-to-Average Ratio, PAR	5.3	5.3	5.3
	Peak Line Voltage (V)	16.5	11	7.6
	Peak-to-Peak Line Voltage (V)	33	22	15.2
	Peak Line Current (mA)	170	110	76
	Peak Line Power (mW)	2725	1175	580
Theoretical Data Rates	Bits/Symbol	15	8	15 (Full) 8 (G.Lite)
	Bits/Channel (KBits/s)	60	32	60 (Full) 32 (G.Lite)
	Max Data Rate for Channels Used	13.5Mb/s	3.1Mb/s	1.4Mb/s (Full) 768Kb/s (G.Lite)

implementations. As will be seen, the line power requirement is the most significant factor in designing a line driver for a particular application.

Table 1 is a summary of the characteristics, electrical requirements and maximum data rates for ADSL modems.

The following are important items to note:

The phone line characteristic impedance for ADSL is 100Ω. This is used to determine the voltage and current required to provide the proper line-power level.

The term PAR stands for peak-to-average ratio. This term is similar to the more common term of crest factor. This determines the peak value of the voltage put on the line over time with respect to the RMS voltage level:

$$V_{PEAK} = PAR \bullet V_{RMS}$$

The DMT signal placed on the line looks basically like white noise, because many different frequencies of rapidly changing amplitude and phase are combined simultaneously. The changes of each tone are considered random as they result from an arbitrary sequence of data bits comprising the transmitted information. Over time, the signals can align and stack up to create a large peak signal. If this large peak is not processed cleanly (for example, if the line-driver amplifier clips) data errors can occur, which must be detected and resent. Transmission errors, particularly over a noisy environment such as phone lines, are inevitable. These errors are identified by a term called the bit-error rate (BER); an acceptable level to maintain fast and accurate data transmission is one error per every 10^7 symbols. The PAR is determined by the probability of the random line signal reaching a certain peak voltage during the time interval required for 10^7 symbols. For the DMT signal, this peak value is 5.3 times the RMS signal level. This factor is very important in determining both the minimum supply voltage required to prevent clipping of the signal and also the peak output current capability of the line driver.

Although the data rates shown in Table 1 are impressively fast, they are, indeed, theoretical. In an actual connection over the phone line, all manner of interference sources will alter the frequency response over the 1.2MHz band. These interference sources can contaminate or attenuate many of the carrier tones to render them completely unusable, or useful but with less than the maximum possible number of data bits encoded. Additionally, higher frequency tones are attenuated more than the lower ones, particularly over longer lengths of phone line used to make the connection.

Another issue that can render particular tones unusable or create transmission errors is distortion from the amplifier driving the line. Distortion products, whether harmonic, intermodulation or from signal clipping, from any of the carrier tones, create signal energy in the frequency spaces used by other tones. This energy also contaminates the data content of the tones and can result in fewer tones being used for data transmission. If many tones are unusable or their data handling capability is reduced, the actual data rate for any given connection can be significantly less than the theoretical maximum.

One of the best features of a DSL modem is the intelligence built in to obtain the fastest data rate for any set of line conditions. When a connection between a modem and the telephone central office is initiated, the first action to occur is called "training-up." During this interval, both ends transmit maximum power in each channel in an effort to determine which channels are best suited for use. The DSP algorithms will automatically pack the most data into the best transmission channels to maximize the data rate for a particular connection. Figure 4 illustrates a typical line spectrum during a training-up interval in a G.Lite example, as measured at the central office end.

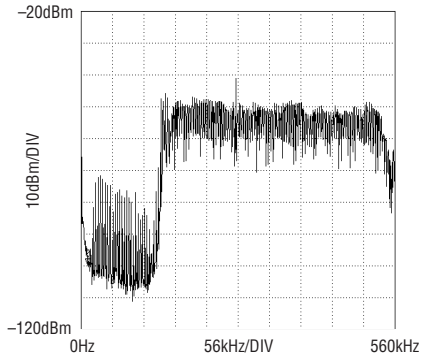


Figure 4. G.Lite training-up spectrum

A Typical ADSL Line Driver/ Receiver Circuit

Referring to Figure 1, the components shown will implement a Full Rate ADSL central office (downstream) port. A discussion of the circuit topology and aspects important for component selection follow.

Transformer Coupling

A transformer is used to connect the transceiver to the phone line, mainly to provide isolation from the line. The turns ratio of the transformer can be used to provide gain to the transmitted signal. This turns ratio has a major effect on the power supply voltages for the line-driver amplifiers. By stepping up the signal from the driver to the line via the transformer, the amount of voltage swing needed by the amplifiers is reduced. As an ideal transformer has equal power in the primary and secondary, while the voltage is stepped up, the current is stepped down. The consequences of using a step-up transformer are beneficial in that lower, more conventional supply voltages can be used, but the amplifiers must have higher current driving capability.

The limit on the turns ratio is primarily a function of the sensitivity of the receive circuitry. Step-up transformers will, unfortunately, step-down the signal received from the phone line. Further attenuation of the received signal by the transformer in addition to the inherent transmission line attenuation can cause the receiver to stop functioning. If this occurs, the modem will disconnect from the line.

A transformer should be selected for a flat, distortion-free frequency response from 20kHz to 2MHz to cover the full frequency spectrum for an

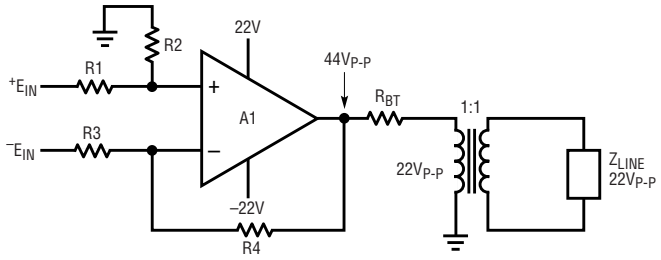


Figure 5a. A single-ended driver requires a high supply voltage to produce the desired peak-to-peak swing of the DMT signal on the phone line.

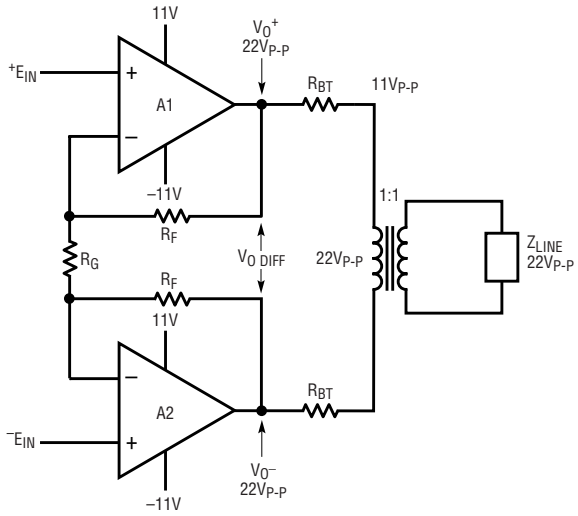


Figure 5b. A differential driver achieves the same swing with half the supply voltage of the single-ended driver.

ADSL transmission. Minimal insertion loss in the transformer over the same frequency range is also desirable. Insertion loss, usually specified in dBm, is power lost in the transformer. The driver amplifier must provide this additional power in order to maintain the required signal power level on the phone line.

Transformer Termination Resistors

The two resistors (called back-termination resistors) shown between the amplifier outputs and the primary of the transformer are inserted for two reasons: to provide a means for detecting the received signal and to make the impedance of the modem match the impedance of the phone line. The receiver circuit is two difference amplifiers that provide gain to the small signals that appear across the termination resistors. The connection and scaling of the input resistors to the receiver amplifiers are purposely set to provide a first-order cancellation of the simultaneously occurring transmit signal. This technique is called "echo cancellation" and the circuit topology is called a "2-wire to 4-wire hybrid" (the 2-wire phone line interfaces with four wires, the two differential driver lines and the two receive signal lines). The cancellation of the transmitted signal from the received signal path is not perfect. Due to signal phase shifts and resistor mismatching, a factor of 6dB to 20dB of attenuation is typical, with higher frequencies being cancelled less. The amount of transmitted signal that remains is cancelled digitally by DSP echo-canceling algorithms.

The value of the termination resistors is a function of the line impedance and the transformer turns ratio. The turns ratio, n, is defined by the number of turns of the winding connected to the phone line (the secondary) divided by the number of turns of the driver side winding (the primary). To make the modem impedance match the line impedance, the total impedance across the primary winding is determined by the following relationship:

$$R_{PRIMARY} = \frac{Z_{LINE}}{n^2}$$

To provide balanced drive to the primary of the transformer, so that each power amplifier shares the work load evenly, each termination resistor is set to a value of one-half of $R_{PRIMARY}$.

This value of termination resistance on the primary is also optimal for receiving maximum power from the line. The received signal on the phone line, e_{RX}, driving the secondary through the line impedance, Z_{LINE} (nominally 100Ω) will develop signal power in the primary per the following relationship:

$$\text{RECEIVED PRIMARY POWER} = \frac{e_{RX}^2}{\frac{Z_{LINE}^2}{n^2 \bullet R_{PRIMARY}} + 2 \bullet Z_{LINE} + n^2 \bullet R_{PRIMARY}}$$

which is also at a maximum when

$$R_{PRIMARY} = \frac{Z_{LINE}}{n^2}$$

While the termination resistors serve an important purpose, they also create significant signal and power loss. With the resistors set to their proper value, one-half of the power delivered by the amplifiers is dissipated in these resistors. To deliver 100mW of signal power to the phone line, for example, requires the driver amplifiers to output at least 200mW of power.

Why Differential Drive?

Two amplifiers configured as a differential gain stage are typically used to provide signal drive to the primary of the transformer. There are two reasons for this configuration: it reduces the supply voltage to the amplifiers by a factor of two and also cancels any even harmonic distortion nonlinearity contributed by the amplifiers.

With single-ended drive of the primary, the supply voltage for the amplifier must be large enough to provide the full peak-to-peak signal swing of the DMT signal placed on to the phone line. With differential drive, each amplifier contributes just one-half of the peak signal amplitude; therefore, the total supply voltage is only one half the peak-to-peak voltage level placed on the line. This is shown conceptually in Figure 5. This reduction in supply voltage allows the use of the standard power supply voltages available in computers for the high speed DSL modem card.

A differential amplifier will ideally cancel all even harmonic distortion products. This is due to the application of a signal that is the difference between two signals, one signal being

an inverted version of the other, to the primary of the transformer. This can be shown mathematically by representing the linear output signals of the amplifiers as a power series:

Each output is a linear function of the input signal:

$$V_O = f(E_{IN})$$

which, represented as a power series, is

$$V_O = a_1E_{IN} + a_2E_{IN}^2 + a_3E_{IN}^3 + a_4E_{IN}^4 + a_5E_{IN}^5 \ldots$$

The inputs to the differential amplifier are E_{IN}^+ and E_{IN}^-; therefore:

$$V_O(+) = a_1E_{IN} + a_2E_{IN}^2 + a_3E_{IN}^3 + a_4E_{IN}^4 + a_5E_{IN}^5 \ldots$$

and

$$V_O(-) = -a_1E_{IN} + a_2E_{IN}^2 - a_3E_{IN}^3 + a_4E_{IN}^4 - a_5E_{IN}^5 \ldots$$

The differential output of the amplifier stage is

$$V_{ODIFF} = V_O(+) - V_O(-)$$

therefore:

$$V_{ODIFF} = 2a_1E_{IN} + 2a_3E_{IN}^3 + 2a_5E_{IN}^5 + \ldots$$

which does not contain any even harmonic products. The complete cancellation of even harmonics depends on the gain and phase-shift matching of the amplifiers and the signal paths over the frequency range of concern.

Bandwidth, Slew Rate and Noise Requirements of the Amplifiers

High speed amplifiers with bandwidths much wider than the transmitted signal bandwidth should be used to maintain flat gain and constant phase shift of the DMT signals. The amount of gain required in the transmit power amplifiers is dependant on the signal levels provided by the analog front end (AFE), which is a circuit block that provides the interface between the line transceiver and the DSP processor. The gain must be sufficient to put the proper amount of power on the phone line for the DSL standard being implemented (refer to Table 1). The maximum frequency to be processed by the amplifiers is also a function of the standard being applied; this, in turn, sets the minimum bandwidth required. As a rule of thumb, the gain bandwidth product specification of the amplifiers used should be at least five times the required value to maintain linear accuracy over the transmitted signal spectrum. This specification provides an indication of the distortion-free, high speed signal processing capability of the amplifier. For example, a Full Rate ADSL downstream transmitter with a gain of four and a maximum frequency of 1.1MHz requires a gain-bandwidth of 4.4MHz; therefore, amplifiers should be chosen that have a gain-bandwidth specification of at least 22MHz. Parts with higher bandwidths are even better for preserving excellent gain and phase shift matching over the 1.1MHz band of operation.

The slew rate of the amplifiers used is not so critical, because the signal spectrum is typically band-limited by filter networks. The step response of these filters slows down the rise and fall times of the signals presented to the amplifiers. A slew rate of at least 10V/µs is usually adequate. However, very fast slew rates are essentially free in wideband amplifier designs. Internal biasing currents charging and discharging internal compensation capacitors and individual node capacitances of the circuit determine the slew rate of an amplifier. To produce a high frequency amplifier, circuit-biasing currents are increased to minimize impedances at critical circuit nodes and small geometry transistor structures are used to minimize stray capacitance. This results in very fast slew rates for the amplifier as an inherent byproduct of a high gain-bandwidth product characteristic. Faster slew rates ensure very fast dynamic response and reduced signal distortion.

Low noise characteristics, together with a wide gain bandwidth capability are most important for the amplifiers used in the receive circuitry. On a typical connection, a phone line will have a noise floor

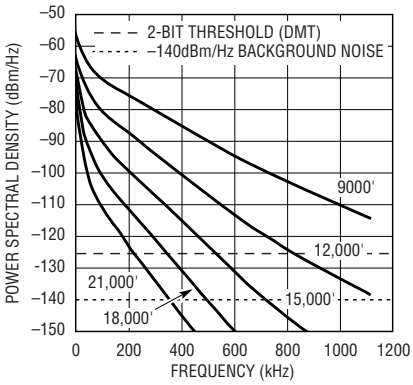


Figure 6. Typical received signal power spectral density, AWG26 loops

power spectral density of –140dBm/Hz. This is equivalent to a noise voltage of 31nV/√Hz. The receiver amplifier should have a noise spectral density in the band between 20kHz and 1MHz lower than this level. Linear Technology provides several fast amplifiers with noise voltage spectra of less than 10nV/√Hz. Lower noise is required in inverse proportion to the turns ratio of the transformer used to address the attendant reduction in both the noise floor and the received signal.

The amount of signal received is a function of the length of phone line used to make the connection, as shown in Figure 6. This is referred to as the loop length. Very long loop lengths can severely attenuate the transmitted signal, particularly at the higher channel frequencies. The greater the attenuation of a channel, the fewer data bits can be transmitted in that channel, which affects the overall communication data rate. As a rule of thumb, a received signal-to-noise ratio of 18dB allows two data bits to be used in a channel. With each 3dB of additional signal above the noise floor, an extra bit of data can be used. With 45dB to 50dB signal-to-noise ratio, a full 12 bits of data can be exchanged in one channel frequency.

The next installment in this series will provide the design calculations to determine the minimum requirements for supply voltage, current drive capability and resultant power consumption and dissipation. In addition, heat management issues will be discussed.

New Continuous-Time Lowpass Filters Feature Differential I/O, Linear Phase and Wide Dynamic Range

by Michael Kultgen and Nello Sevastopoulos

The new LTC1565-XX family of monolithic, continuous-time lowpass filters is tailored for data communication systems requiring band-limiting in their *differential* signal paths.

Because it eliminates the need for external components, The LTC1565-XX offers a compact solution to high frequency, differential filter requirements. Each LTC1565-XX is optimized for a single cutoff frequency. The first member of the LTC1565-XX family, the LTC1565-31, is a 7th order, linear-phase lowpass filter with a 650kHz cutoff frequency. It is tailored primarily for CDMA cellular base stations or any other application requiring linear-phase lowpass filtering with a cutoff frequency in the vicinity of 650kHz.

Figure 1 shows the extremely simple hookup of the LTC1565-31. The filter is packaged in an SO-8 and it operates on a single 5V supply. Aside from power supply and analog ground bypass capacitors, no other external components are required. The device is designed to be driven differentially, yet, for single-ended applications, either input can be shorted to the analog ground (pin 3). Differential signals with a common mode range of 1.3V to 2.7V and up to $2V_{P-P}$ amplitude can be DC coupled into the input pins of the filter without any significant performance degradation. The maximum dynamic range (THD plus S/N ratio) is 78dB. This is obtained with a $2.5V_{P-P}$ differential signal biased at a 2VDC common mode voltage.

The filter output should be taken differentially, as indicated in Figure 1. The common mode voltage of the differential output is the voltage of pin 3, which is one-half of the power supply of the filter. Figure 2 shows the frequency response of the filter, which features an almost flat group delay in the filter's passband. The amplitude response has a –3dB gain at 650kHz, –20dB at 1MHz and in excess of –70dB at 2MHz.

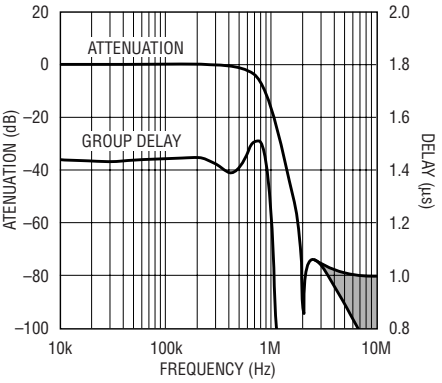


Figure 2. LTC1565-31 frequency response

The out-of-band rejection of the filter is quite impressive. Depending on the input signal amplitude, the stopband attenuation above 3MHz is between 80dB and 100dB (see Figure 2). The LTC1565-31 achieves these attenuation levels without prefiltering. This is highly desirable in applications where strong interfering signals are present at the inputs of the filter.

Other responses and configurations will be available in the near future. Contact LTC marketing for details regarding other cutoff frequencies.

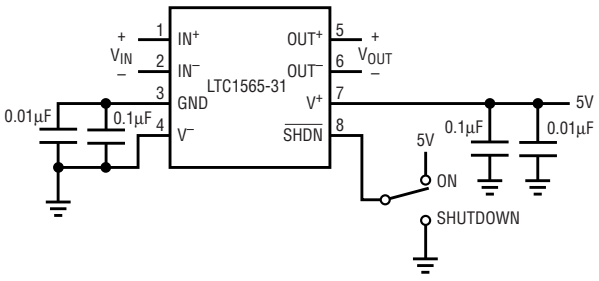


Figure 1. The LTC1565-31 is extremely simple to hook up.

LTC1546 Multiprotocol Chip Simplifies NET1-, NET2- and TBR2-Compliant Serial Interfaces

by Dan Eddleman

The LTC1546 multiprotocol transceiver simplifies network interface design and frees up valuable PC board real estate. Operating from a single 5V supply, the LTC1546 and LTC1544 form a complete, software-selectable DTE or DCE interface port that supports the V.28 (RS232), V.35, V.36, X.21, RS449, EIA530 and EIA530-A protocols, including all of the necessary cable termination. With these two chips, the physical layer of a NET1-, NET2- and TBR2-compliant interface can be implemented in less than 3cm^2.

In a typical application (see Figure 1), the 3-driver/3-receiver LTC1546 multiprotocol serial transceiver/cable terminator handles the clock and data signals, and the 4-driver/4-receiver LTC1544 multiprotocol transceiver handles the control signals. The mode pins, M0, M1 and M2, select the active protocol and termination (see Table 1) and the DCE/$\overline{\text{DTE}}$ pin selects DTE or DCE mode. PC board layout consists of routing the pins of an LTC1546 and an LTC1544 to the connector and placing bypass and charge pump capacitors (see Figure 1). The LTC1546/LTC1544 chipset is appropriate for most multiprotocol applications. Systems that additionally require LL (local loop-back), RL (remote loop-back), TM (test mode) or RI (ring indicate) signals should use the 5-driver/5-receiver LTC1545 multiprotocol transceiver in place of the LTC1544.

The LTC1546 is pin compatible with the popular LTC1543 multiprotocol transceiver and has the added feature of on-chip cable termination. Most previous applications used an LTC1543 for the clock and data transceivers and an LTC1344A for the necessary cable termination. With the

continued on page 35

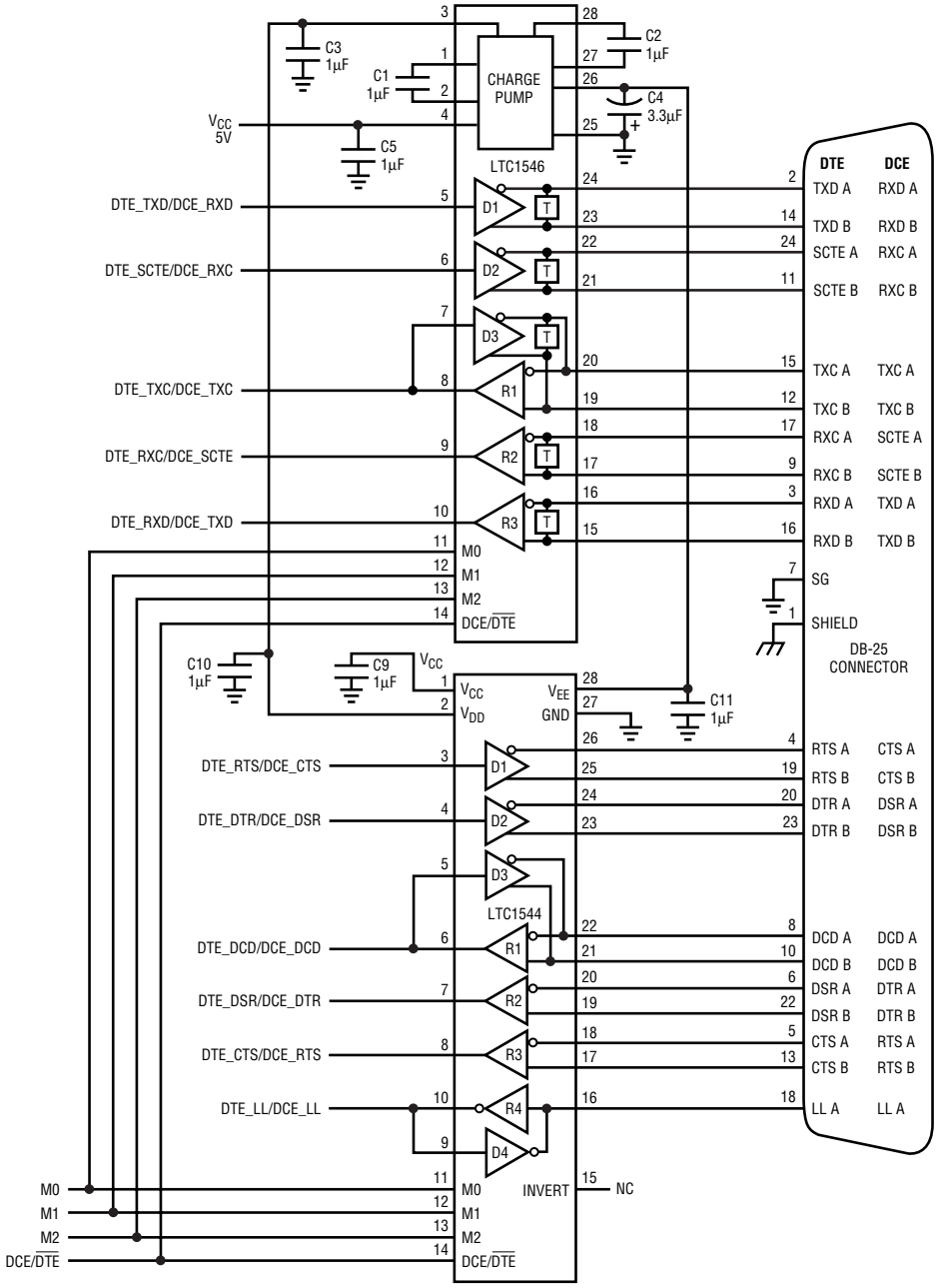


Figure 1. LTC1544/LTC1546 software-selectable multiprotocol DCE/DTE port

Table 1. Mode-pin functions

LTC1546/LTC1545 Mode Name	M2	M1	M0
Not Used	0	0	0
EIA-530A	0	0	1
EIA-530	0	1	0
X.21	0	1	1
V.35	1	0	0
RS449/V.36	1	0	1
RS232/V.28	1	1	0
No Cable	1	1	1

LTC2050, Zero-Drift Operational Amplifier in SOT-23 Package Minimizes Board Area without Compromising Specs

by David Hutchinson

Introduction

The LTC2050 is a zero-drift operational amplifier available in the 5- or 6-lead SOT-23 and SO-8 packages. It minimizes board area while providing uncompromising DC performance, including 3µV (max) DC offset and 30nV/°C (max) DC offset drift. It operates from a 2.7V supply while still supporting 5V applications. The power consumption is 800µA and the versions in the 6-lead SOT-23 and SO-8 packages offer power shutdown.

Other key features of this new device include:

- ❏ Small 5- or 6-lead SOT-23 package
- ❏ 2.7V operation
- ❏ 3µV maximum offset voltage
- ❏ 30nV/°C maximum offset voltage drift
- ❏ 1.5µV_{P-P} typical noise (0.1Hz to 10Hz)
- ❏ More than 130dB of DC PSRR, CMRR and gain (typical)
- ❏ Output swings rail-to-rail with 1kΩ loads
- ❏ Extended common mode input range
- ❏ Power shutdown below 10µA (available in 6-lead SOT-23 and SO-8)

Extended Input Common Mode Range with Uncompromising CMRR

At room temperature, with the input common mode level at mid-supplies, the LTC2050 typically has 0.5µV of input-referred offset (input-referred offset is guaranteed to be less than ±3µV). To ensure this DC accuracy over the common mode input range, the LTC2050 has exceptionally high CMRR over a wide common mode range from the negative supply typically to within 0.9V of the positive rail, as shown in Figure 1. For example, as the input is varied over the entire common mode range, the input referred offset changes typically by less than 0.4µV at 5V and less than 0.3µV at 3V. Figure 2 shows the CMRR over frequency, illustrating more then 80dB at 1kHz.

Similar levels of PSRR (typically less then 0.1µV of offset per volt of supply change) and the near-zero temperature drift ensure that the offset does not exceed 5µV over the entire supply and commercial temperature range.

Rail-to-Rail Output Drive with a 1k Load

The LTC2050 maintains its DC characteristics while driving resistive loads requiring source or sink current as high as 5mA with a 3V or 5V supply. Figure 3 shows the op amp rail-to-rail swing versus output resistance loading. With a 1k or 5k load, the output typically swings to within 100mV or 30mV, respectively, of the rails.

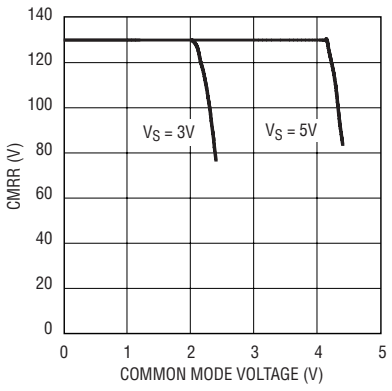


Figure 1. LTC2050 DC common mode rejection ratio vs common mode input voltage

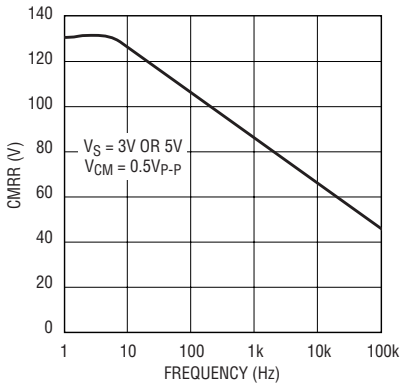


Figure 2. LTC2050 common mode rejection ratio vs frequency

Clock Feedthrough Virtually Eliminated

The LTC2050 uses autozeroing circuitry to achieve its zero-drift offset and other DC specifications. In the LTC2050, the clock used for autozeroing is typically 7.5kHz. The term clock feedthrough is used to indicate visibility of this clock in the op amp output spectrum. There are typically two types of clock feedthrough in autozeroed op amps such as the LTC2050.

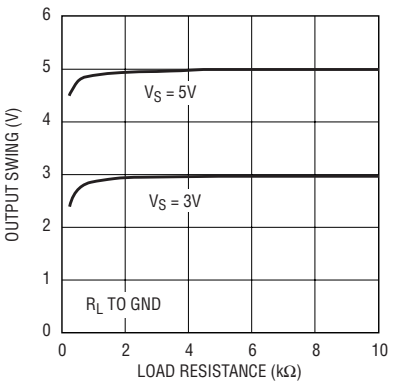


Figure 3. LTC2050 output voltage swing vs load resistance

The first source is caused by the settling of the internal sampling capacitor and is input referred; that is, it is multiplied by the closed loop gain of the op amp. *This form of clock feedthrough is independent of input source resistance or gain setting resistors.* Figure 4 shows the spectrum of the LTC2050 with a closed loop gain of –100 with R2 = 100k, and R1 = R_S = 1k. There is a residue clock feedthrough of less than $1\mu V_{RMS}$ (input-referred) at 7.5kHz. This very low clock feedthough is achieved in the LTC2050 by internal circuitry that improves settling of the internal autozero storage capacitors. Also in Figure 4, the clock feedthrough of the LTC2050 is compared with that of the very popular LTC1050.

The second form of clock feedthrough appears when the input has a large source resistance or the gain-setting resistors are large. In this case, the charge injection caused by the internal MOS switches creates input-referred clock feedthrough currents that are multiplied by the impedance seen at the input terminals of the op amp. This form of clock feedthrough is not significant in the LTC2050 when R_S and R1 in Figure 4 are below approximately 10k. Placing a capacitor across R2 reduces either form of clock feedthrough by lowering the bandwidth of the closed-loop response.

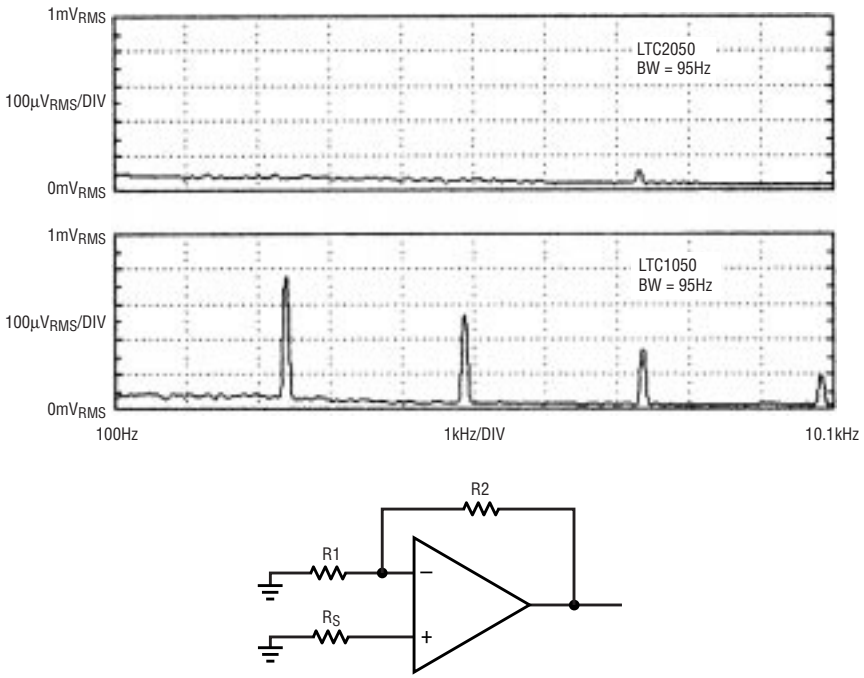


Figure 4. Output spectrum with a gain of 100; R2 = 100k; R1 = R_S = 1k

Conclusion

The LTC2050 is the latest member of Linear Technology's family of zero-drift operational amplifiers. It provides small packaging while still maintaining precision DC specifications. In addition, it operates at supplies as low as 2.7V and includes a power shutdown in the 6-lead SOT-23 package.

For more information on parts featured in this issue, see http://www.linear-tech.com/go/ltmag

LTC1546/LTC1545, continued from page 33

introduction of the LTC1546, the LTC1344A is no longer required. In fact, in most existing designs, the LTC1543 can be replaced by an LTC1546, and the LTC1344A can be removed without any changes to the PC board. In new designs, the LTC1546 will simplify PC board layout and reduce the required footprint compared to the LTC1543/LTC1544 solution.

The LTC1546/LTC1544 chipset has been tested by TUV Telecom Services, Inc. and has been found to be compliant with the NET1, NET2 and TBR2 requirements. Test reports are available from LTC or TUV upon request (NET1 and NET2 report NET2/091301/99; TBR2 report CTR2/091301/99).

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New Device Cameos

LTC1706-81 5-Bit Desktop VID Voltage Controller Achieves ±0.25% Accuracy for 1.3V to 3.5V Microprocessor Supplies

Intel's Pentium® microprocessors are breaking through speed barriers, thanks, in part, to a tightly regulated power supply that's capable of producing hundreds of amps of current at various VID levels. The Pentium processors' supply voltage requirements change with the various clock speed options. The LTC1706-81, a 5-bit desktop VID voltage programmer, meets this need by adjusting the outputs of a whole family of LTC DC/DC converters to provide precise supply voltages to these Pentium processors. Depending on the state of the five VID inputs, a ±0.25% accurate output voltage from 1.3V to 2.05V or from 2.1V to 3.5 V can be programmed in 50mV or 100mV steps, respectively. This is fully compliant with the Intel Pentium Processor Desktop VID Specification (VRM 8.4).

The LTC1706-81 comes in the small 10-lead MSOP package. It consumes practically zero current (only device leakage) when all five inputs are high; each grounded VID input adds only 68µA of input current in a 3.3V system. For extremely high current applications, such as servers and supercomputers, just one LTC1706-81 can program up to six LTC1629 PolyPhase, high efficiency, step-down DC/DC controllers to complete an extremely compact, powerful, programmable power supply that uses only surface mount components.

In addition to the LTC1629, the LTC1706-81 also works equally well with the LTC1735, the LTC1702, the LTC1628 and other LTC DC/DC converters with onboard 0.8V references.

Pentium is a registered trademark of Intel Corp.

Authors can be contacted at (408) 432-1900

LTC1664: Quad Micropower 10-Bit Voltage Output DAC Saves Power and Space

The LTC1664 is a quad, micropower, 10-bit, rail-to-rail voltage output DAC with Sleep mode. Operating on a single 2.7V–5.5V supply rail, the LTC1664 has the lowest power consumption of any available quad 10-bit voltage output DAC. Each buffered DAC draws just 59µA of supply current at 5V (43µA at 3V), yet it is capable of supplying DC output currents in excess of 5mA. Sleep mode operation further reduces total supply-plus-reference current to just 1µA.

The LTC1664 is available in LTC's tiny 16-lead Narrow SSOP package, delivering outstanding board-space efficiency with four DAC channels in the space of an SO-8; required board area is just 0.012in^2 per DAC. Each of the four output amplifiers is stable driving capacitive loads up to 1000pF, so designers need not worry about the capacitance of long board traces. The LTC1664 is guaranteed monotonic; differential nonlinearity (DNL) is typically ±0.2LSB (±0.75LSB maximum) over the full industrial temperature range.

The 3-wire serial interface uses a 16-bit input word comprising four control bits, ten input-code bits and two don't-care bits. Asynchronous $\overline{CLR}$, power-on reset and daisy-chain capability are also provided. It is possible to keep one or more chips in a daisy chain in continuous Sleep mode by giving the Sleep instruction to these chips each time the active chips in the chain are updated. The LTC1664 is also available in a fully software- and pin-compatible octal version, the LTC1660.

The LTC1664 has a reference-to-output gain of one and the Reference pin can be tied to V_{CC} for ratiometric, 0V-to-V_{CC} output. Other voltage output DACs either use a gain of two, thus requiring a separate reference, or cannot reach the upper rail when using a gain of one. Moreover, the Reference input has constant impedance over all codes (70k minimum), unlike many units that have input impedance that varies greatly with code. This constant reference impedance causes the linearity of the LTC1664 to be insensitive to the source impedance of the external voltage reference, eliminating the need for low impedance buffer amplifiers.

Ultralow supply current, power-saving Sleep mode and extremely compact size make the LTC1664 ideal for battery-powered devices, while its ease of use, high performance and wide supply range make it an excellent choice for general-purpose voltage adjustment and trimmer potentiometer applications.

LTC1657: Micropower, 16-Bit, Parallel, Voltage Output DAC in 28-Pin SSOP Package Saves Power and Board Space

Linear Technology introduces its first buffered 16-bit, parallel, voltage output DAC. The LTC1657 includes a deglitched rail-to-rail output amplifier, an internal 2.048V reference and a double-buffered parallel digital interface for standalone performance. The LTC1657's architecture guarantees ±1LSB maximum differential nonlinearity (DNL) over temperature to provide true 16-bit performance. The INL, full-scale and offset are all laser trimmed to maintain accuracy over the full operating temperature range. The device operates on a single supply of 4.5V to 5.5V and the typical power supply current is 650µA. The LTC1657 is similar to Linear Technology's LTC1450 12-bit voltage-output DAC family, allowing an easy upgrade path.

The LTC1657's output amplifier provides a voltage output settling time of 20µs to within 0.0015% for a full-scale step. The rail-to-rail voltage output can sink or source 5mA over the entire operating temperature range, to within 500mV of the positive supply voltage or ground. The output stage is equipped with a deglitcher

that results in a midscale glitch impulse of 8nV-s. The full-scale output can be one or two times the reference voltage, depending on how the X1/X2 pin is connected. The LTC1657 is available in 28-pin SSOP and PDIP packages.

LT1767: Monolithic 1.25MHz, 1.5A Buck Converter in MS8 Operates Over a 2.7V to 25V Input Range

The LT1767 is LTC's latest high speed, high efficiency, monolithic buck converter in a very space efficient MS8 package. The LT1767 adds features not found on previous-generation monolithic regulators. Its monolithic approach results in few external components and a straightforward board layout. The high 1.25MHz switching frequency reduces the values of input/output filtering components and allows the use of low value chip inductors, reducing overall system cost. Using the Sync pin, the operating frequency can be increased to as high as 2MHz, further easing system noise filtering requirements.

Operating from 2.7V to 25V, the LT1767 can utilize inputs ranging from 24V wall adapters, to preregulated 12V, 5V or 3.3V supplies, to batteries. Undervoltage lockout can be implemented using the accurate 1.3V threshold of the Shutdown pin. Additionally, an internal 2.6V undervoltage lockout ensures predictable operation near minimum input voltages. Both fixed and adjustable output voltage versions will be available. The adjustable version has a feedback reference voltage of 1.2V, simplifying low output voltage supply design.

High efficiency is the result of the 1.5A, 200mΩ internal switch and low 900µA quiescent current. The LT1767's efficiency permits a relatively high 1.5A switch current to be used in a small MS8 package. Efficiency is high even at lower output loading because of the LT1767's low quiescent current. With the S/D pin pulled to ground, supply current falls to only 6µA.

LTC1694-1 SMBus/I²C Accelerator Eliminates Data Integrity Problems

The LTC1694-1 is an active pull-up for SMBus and I²C™ systems. It is designed to eliminate data integrity problems and enhance transmission speed under all specified loading conditions. The LTC1694-1 allows multiple device connections or a longer, more capacitive interconnect, without compromising rise times or bus performance, by supplying a high pull-up current of 2.2mA to slew the SMBus or I²C lines during positive bus transitions. During negative bus transitions or steady DC levels, the LTC1694-1 sources zero current. External resistors, one on each bus line, trigger the LTC1694-1 during positive bus transitions and set the pull-down current level. These resistors determine the logic low DC level, set the fall time for negative bus transitions and permit fine tuning of rise time vs fall time.

The SMBus and I²C communication protocols employ open-drain drives with resistive or current-source pull-ups. These protocols allow multiple devices to drive and monitor the bus without bus contention. The simplicity of resistive or fixed-current-source pull-ups is offset by the resultant slow rise times if bus capacitance is high. Rise times are improved by using lower value pull-up resistors or higher value current sources, but the additional current increases the low state bus voltage, decreasing noise margins. Slow rise times seriously affect data reliability, enforcing a maximum practical bus speed well below the established maximum transmission speed of 100kHz.

Faster transition times can be obtained or higher capacitance driven by simply paralleling LTC1694-1 devices. Paralleling multiple LTC1694-1s has no effect on the logic low DC level or the fall time. The LTC1694-1 is available in a 5-lead SOT-23 package, which occupies the same area as two surface mount resistors. The LTC1694 is a companion part to the LTC1694-1 that integrates the DC pull-up current for simplicity. The LTC1694 and the LTC1694-1 effectively eliminate SMBus and I²C data integrity problems and increase the maximum system transmission speed.

I²C is a trademark of Philips Electronics N.V.

On-Chip Power-Good Indicator in LTC1628PG and LTC1629PG Saves Board Space and Lowers Total Cost

The power-good indicator in the new LTC1628PG and LTC1629PG eliminates the necessity of adding comparators, biasing resistors, decoupling capacitors and a voltage reference to circuits using these third generation DC/DC controllers. These parts have a PGOOD pin that outputs a logic low when the output voltage exceeds ±7.5% of the setpoint. Both outputs are monitored by the LTC1628PG, so the PGOOD pin indicates a fault when either output voltage is outside the ±7.5% window.

The new PG parts are exactly like the original LTC1628 and LTC1629 except that the PGOOD pin replaces the FLTCPL pin on the LTC1628 and the AMPMD pin on the LTC1629. The FLTCPL function in the LTC1628PG is programmed so that the FCB pin controls both outputs and an overcurrent fault on either output will latch-off both outputs. Overcurrent latch-off can be defeated on the LTC1628PG in the same manner as on the LTC1628. The AMPMD function in the LTC1629PG is programmed so that the differential amplifier is configured as a precision instrumentation amplifier to provide true remote sensing of the voltage across the load.

Other than preprogramming the FLTCPL and AMPMD functions, all of the features of the LTC1628 and LTC1629 are available in the new PG parts. The high efficiency, PolyPhase switching of both LTC1628PG and LTC1629PG reduces the number of input capacitors and allows the LTC1629PG to control 30A to 45A without a heat sink, using smaller inductors and less output capacitance than competing circuits.

LTC1643L-1 Hot Swaps PCI-Bus without the –12V Supply

The LTC1643 Hot Swap controller allows a board to be safely inserted into and removed from a live PCI-Bus slot containing 5V, 3.3V and ±12V supplies. A new version, the LTC1643L-1, loosens the tolerances on the +12V and –12V supplies. In systems where the –12V supply has been eliminated, the $-V_{EE}$ input pin may simply be grounded without affecting the operation of the Hot Swap controller.

All other familiar LTC1643 Hot Swap features are retained, including the narrow 16-pin SSOP package and pinout, programmable foldback current limit with circuit breaker, fault and power-good outputs and programmable supply ramp rates, allowing insertion into a live backplane without disturbing the supply bus. A new data sheet combining the specifications for the LTC1643L, LTC1643H, and LTC1643L-1 has been printed and is available for downloading from the LTC web site.

LTC1707 Monolithic Synchronous Stepdown Regulator Works with One or Two Li-Ion Batteries

The LTC1707 is a new addition to a growing family of monolithic stepdown regulators optimized for use with Li-Ion batteries. New features include a ±1%, 1.19V reference output, capable of sourcing 100µA, and selectable low load current operating modes (Burst Mode operation or pulse skipping mode). Pulse skipping allows the LTC1707 to maintain a constant operating frequency down to low output currents, reducing noise and RF interference, but without the quiescent current penalty of forced continuous operation.

The LTC1707, like its predecessor the LTC1627, is a monolithic, current mode, synchronous step-down regulator using a fixed frequency architecture. The current mode architecture gives the LTC1707 excellent load and line regulation, and Burst Mode operation provides high efficiency at low load currents. 100% duty cycle provides low dropout operation, which extends operating time in battery-operated systems. The operating frequency is internally set at 350kHz and can be externally synchronized at frequencies up to 550kHz. Burst Mode operation is inhibited during external clock synchronization or when the SYNC/MODE pin is pulled low. The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode, saving components and board space. The LTC1707 is available in an 8-lead SO package.

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Authors can be contacted at (408) 432-1900

DESIGN TOOLS

Technical Books

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

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